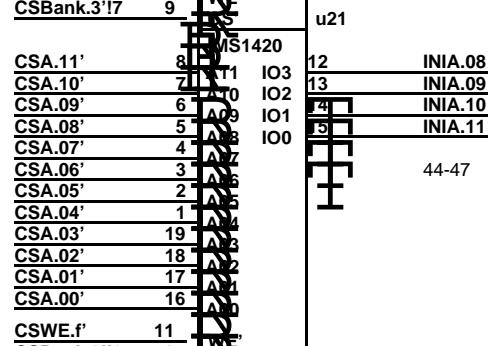
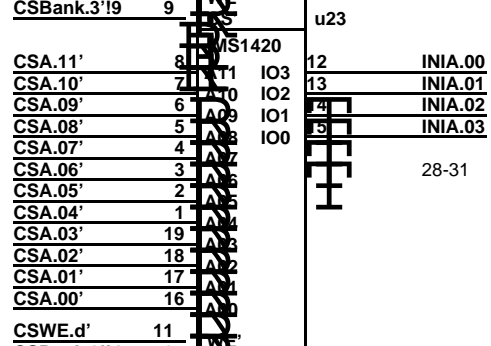
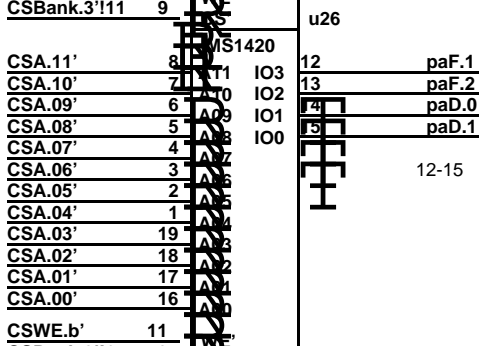
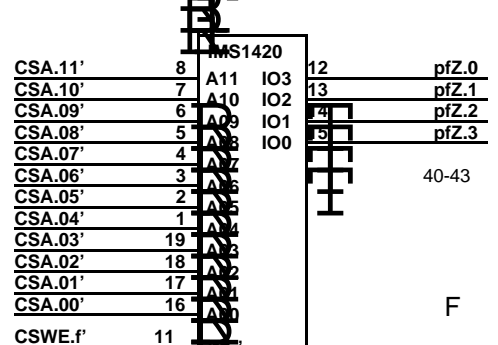
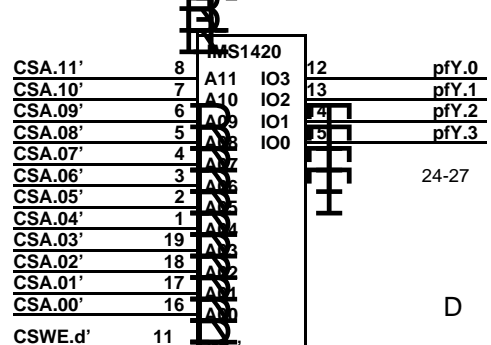
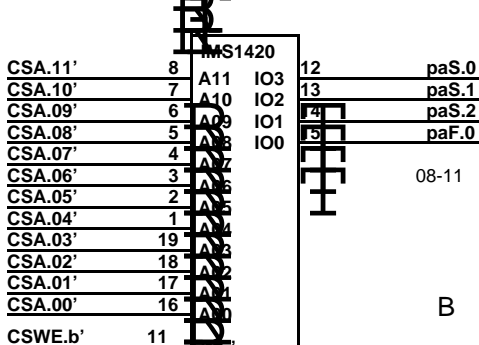
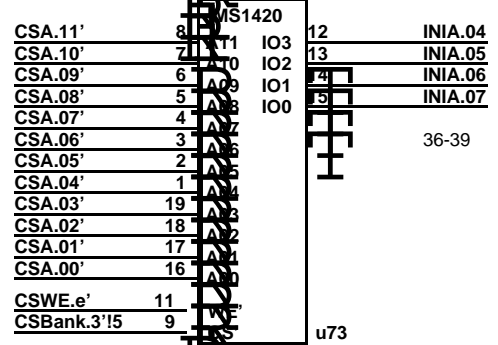
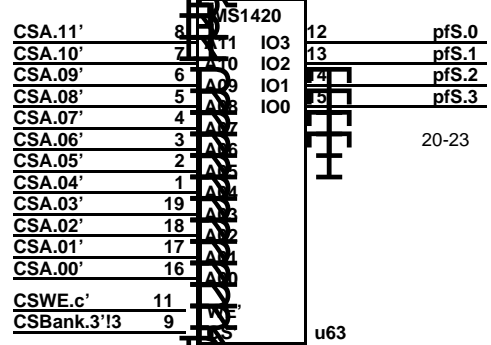
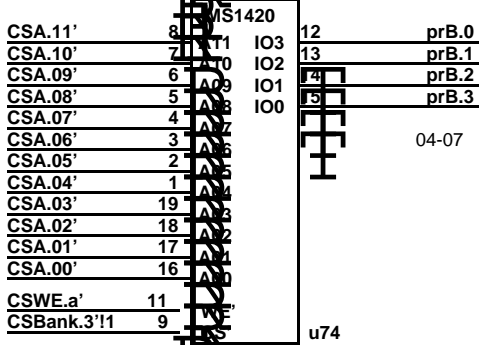
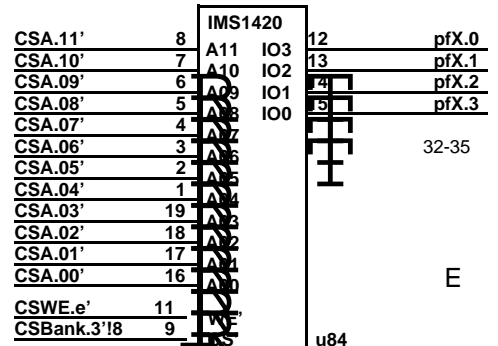
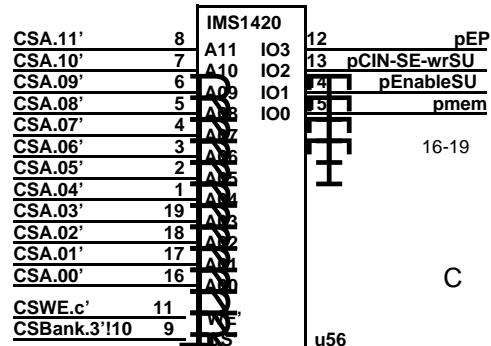
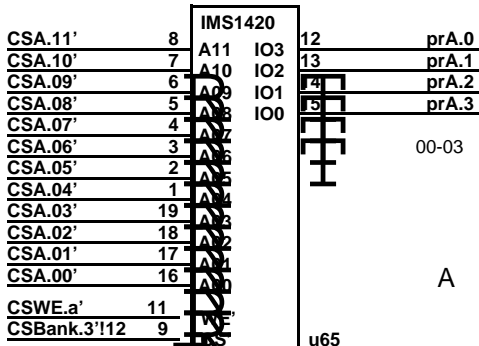
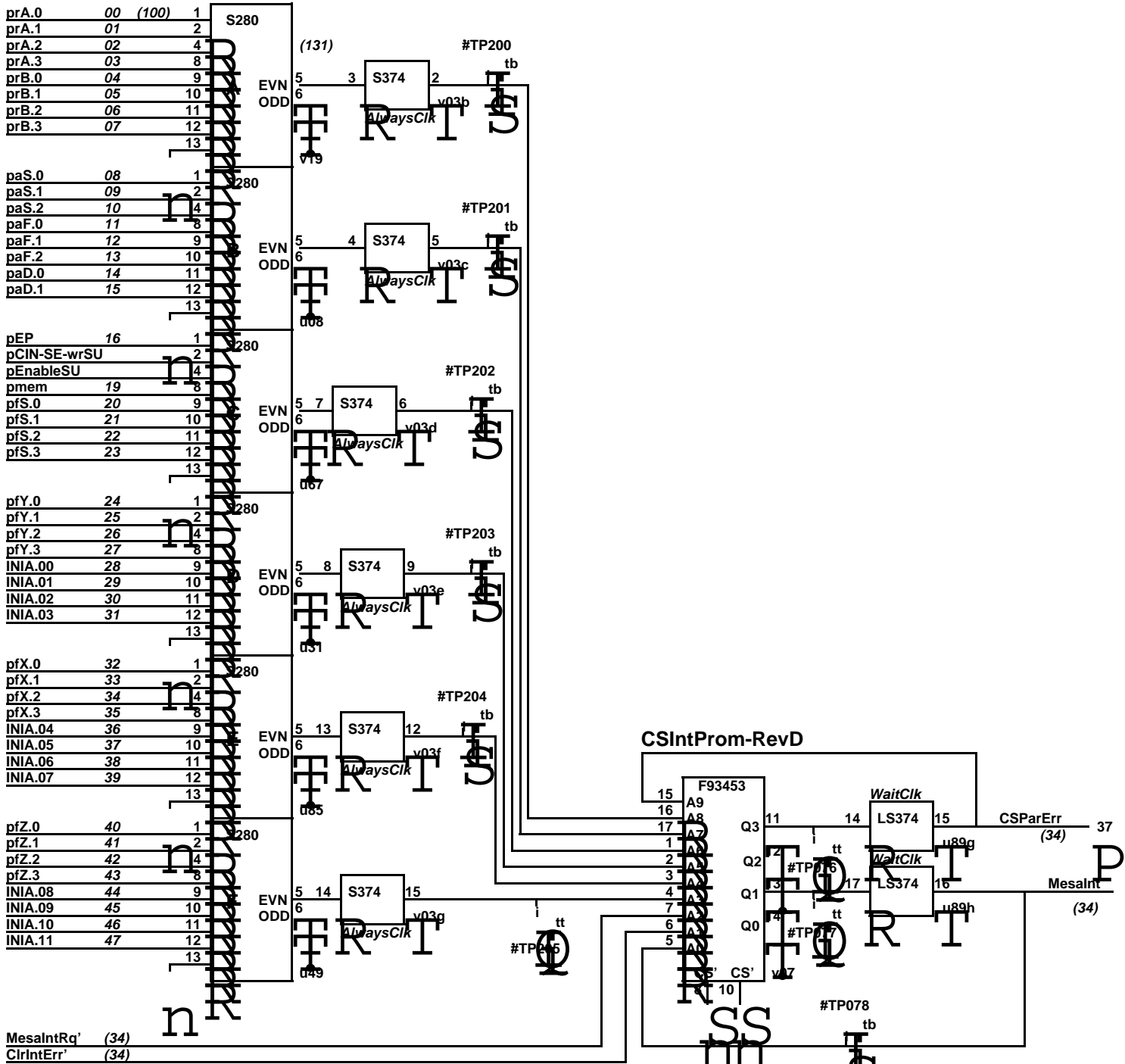


Warning: This drawing contains font 4 macros!

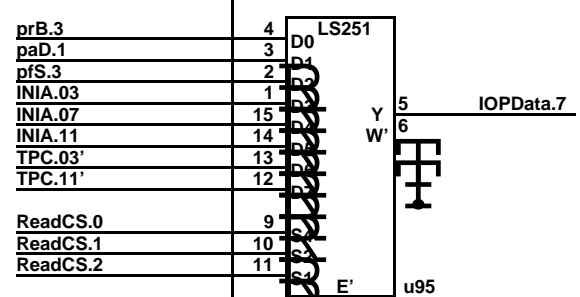
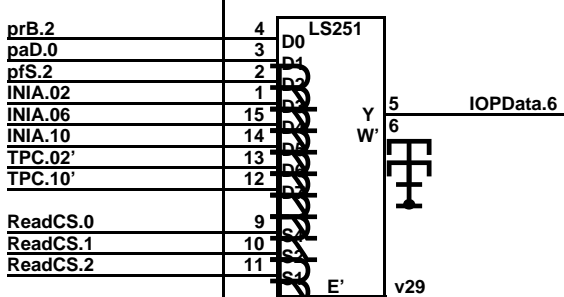
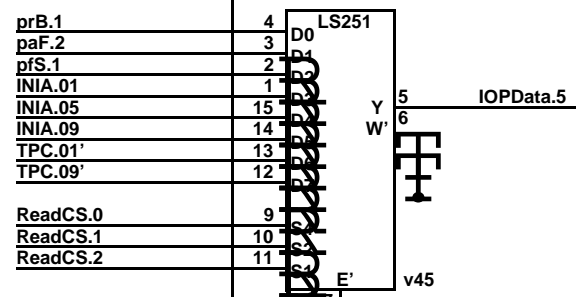
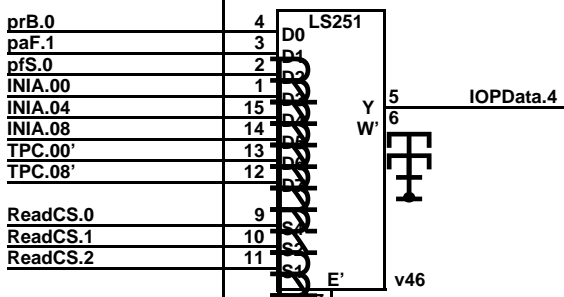
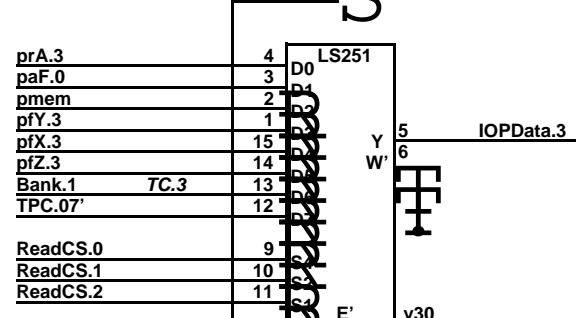
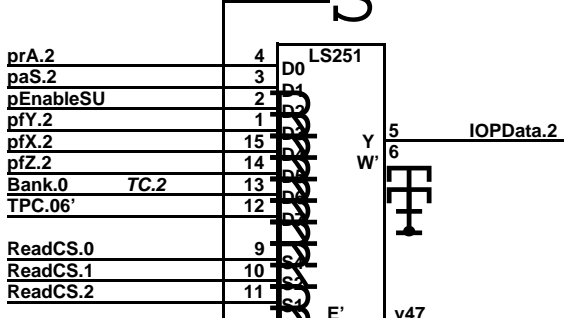
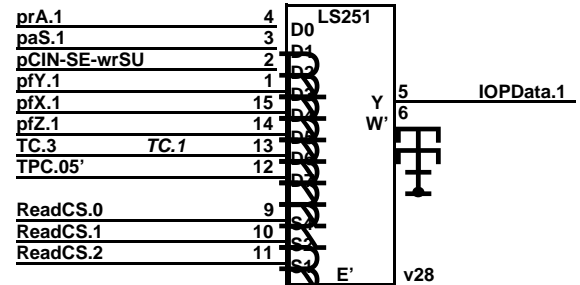
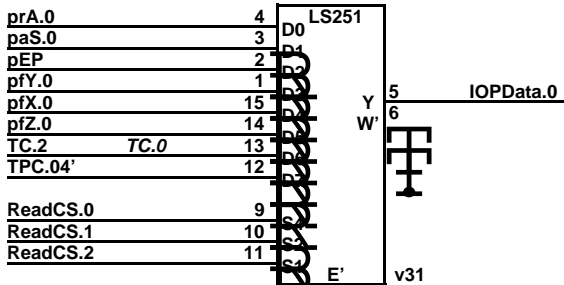


Warning: This drawing contains font 4 macros!



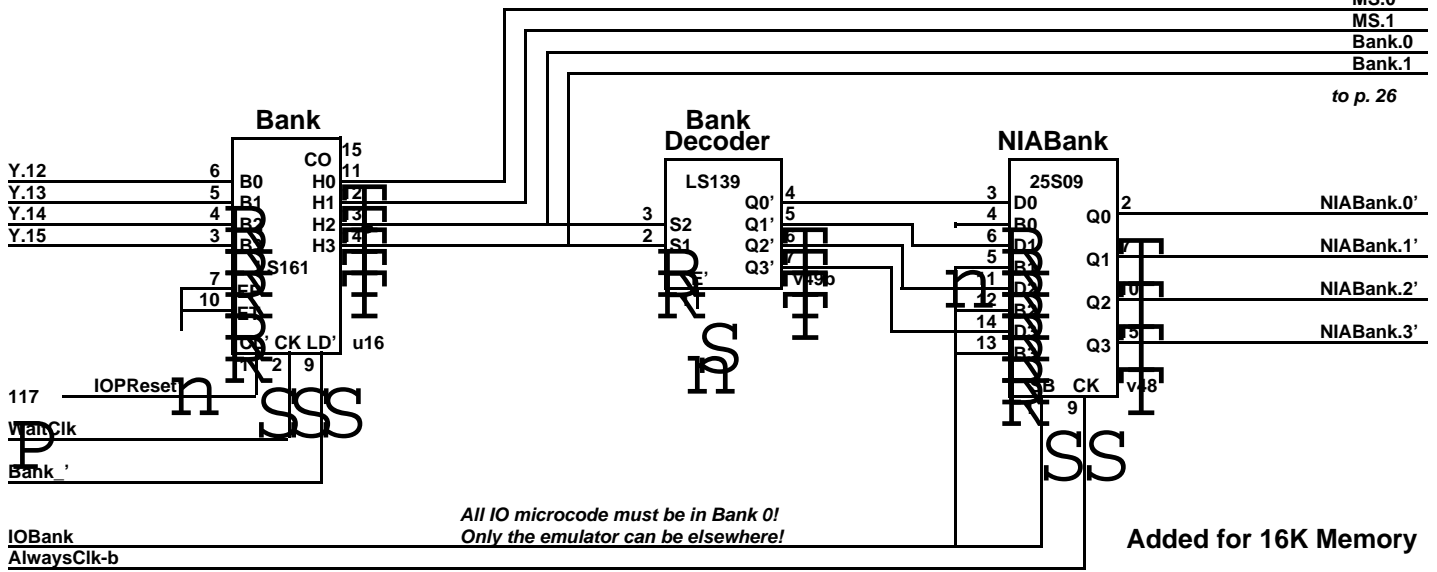
$CSParErr = XOR(CSPar[0..5])$

NB: TC[0-3] have been replaced by Bank[0-3].



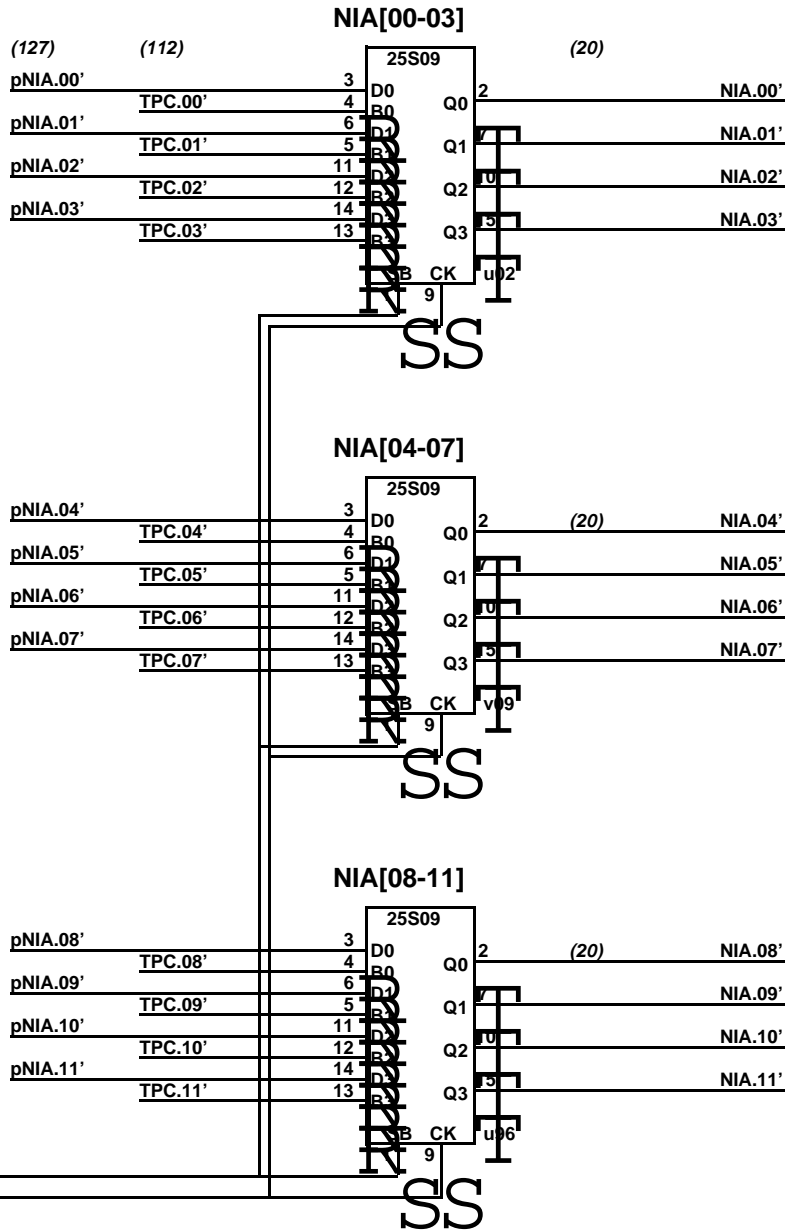
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P



Added for 16K Memory

This section is standard



**NOTE on Control Store Addresses**

The next instruction address for the control store comes from one of two basic places:

1. TPC registers if switching tasks
2. From the INIA field of the previous microinstruction

In the case of (1), task 6's TPC registers are used by the IOP to provide the address when the IOP wants to read or write data into the control store.

In the case of (2), the INIA field is suitably modified by the trap and conditional branch logic on page 16

Swc2 (122)  
AlwaysClk-b