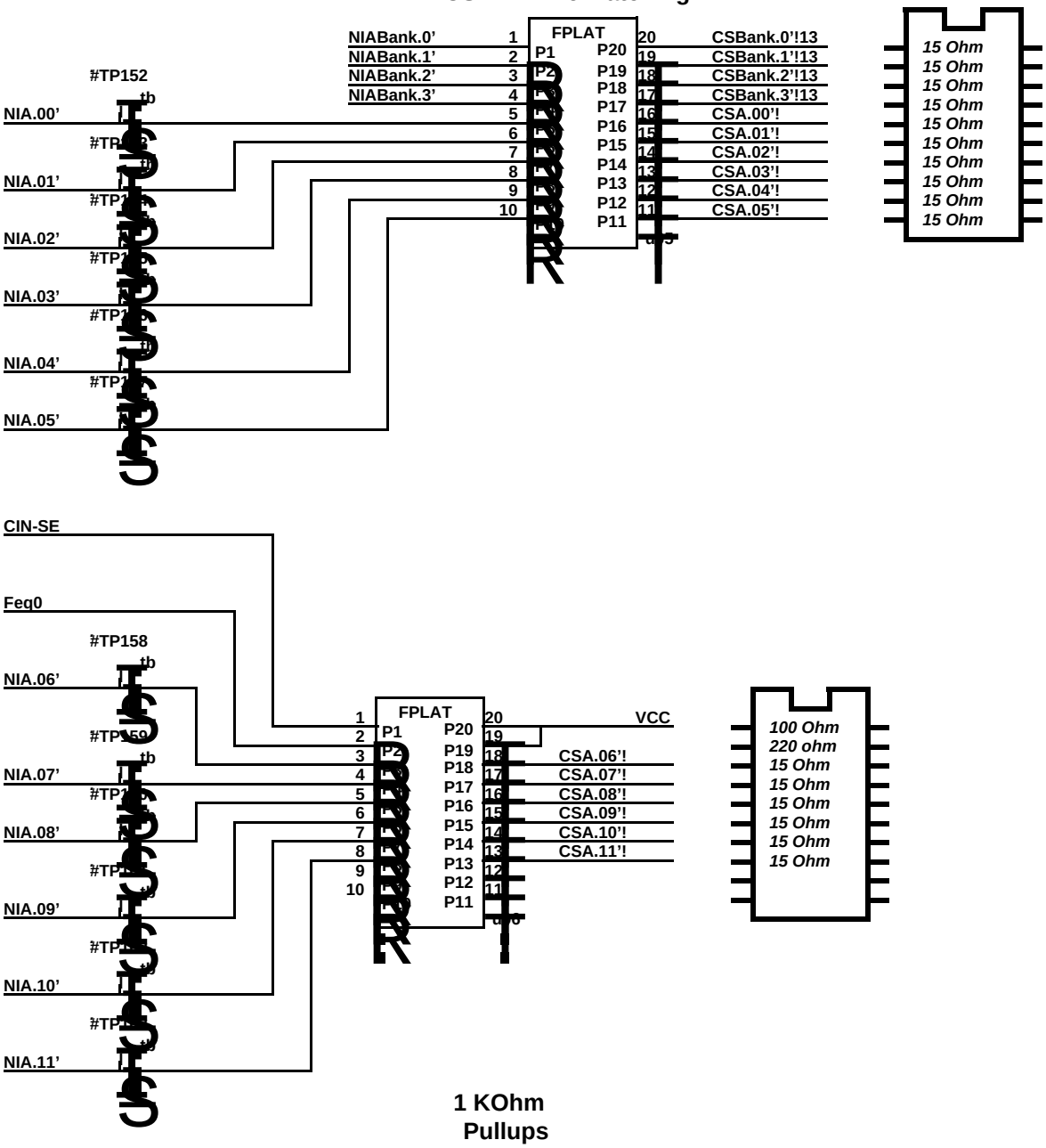
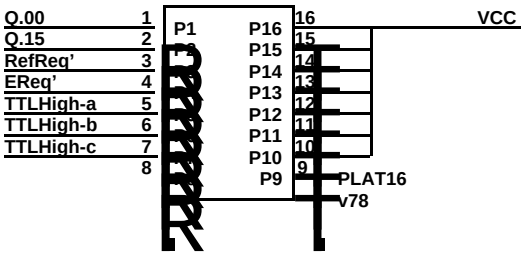
CS NIA Line Matching



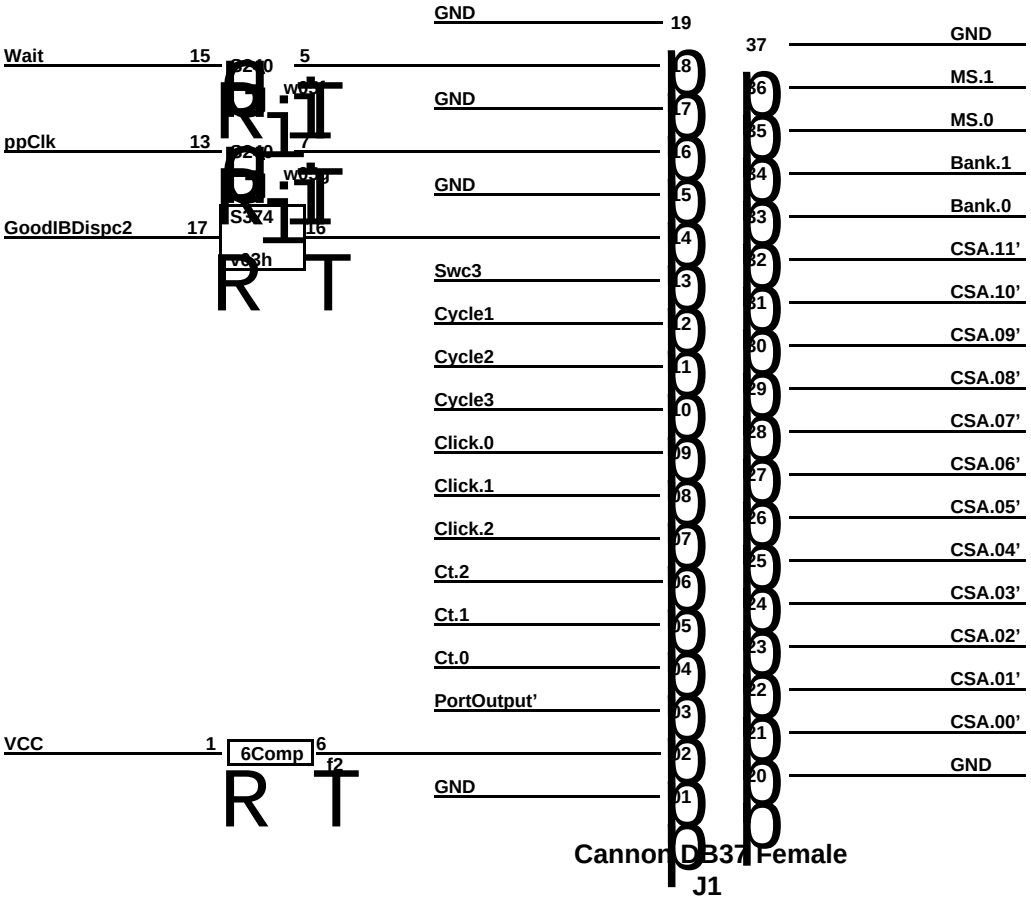
1 KOhm Pullups



Beckman Resnet DIP

898-1-1K

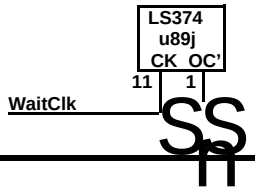
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Resistors	CPE26.sil	Tony West	Ba	5/30/83	27



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Debugger Box Connector	CPE27.sil	David Boggs	Ba	5/30/83	28

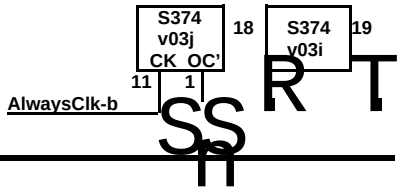
LS374 *u89*

b IBPtr.0
c IBPtr.1
d EmuMemErr
e StackErr
f pc16'
g CSParErr
h MesaInt
i SFLG'



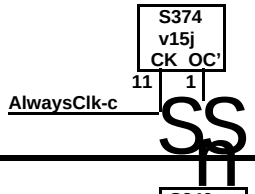
S374 *v03*

b CSPar.0
c CSPar.1
d CSPar.2
e CSPar.3
f CSPar.4
g CSPar.5
h GoodIBDispc3
i



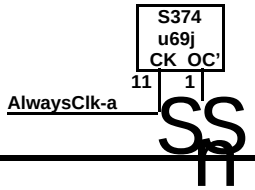
S374 *v15*

b MAR_'
*c AllowMDR_*
d TC.0
e TC.1
f TC.2
g TC.3
h KernReq'
i TCWaitc1'



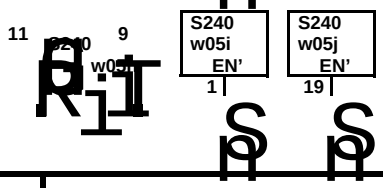
S374 *u69*

b Swc3
c Swc3'
d EKTrapc2'
e EKTrapc2
f EKErr.0'
g EKErr.1'
h Waitc2'
i Waitc3'



S240 *w05*

a Cycle1
b Cycle2
c Cycle3
d Cycle3'
e DRef
f WaitPin'
g Click.2Pin'



S04 *v43*

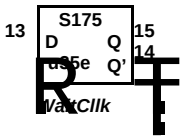
a aD.0'
*b MAR_*
c IBEmptyErr'
d Des_YBus
e XBus_SU
*f Port_*

S04 *v39*

a AlwaysClk-a
b AlwaysClk-b
c AlwaysClk-c
d WaitClk
*e RH_*
f Fne0

S175 *u35*

b MAS'
c MDS'
d SDS'
e
*f *anon**



S00 *v42*

a XBus_SU'
b pMAR_'
c MarPgCross'
d CIN_pc16

S00 *v85*

a Pop
b Nibble'
c Byte'
d Xhigh_0

S00 *u36*

*a *anon**
b WPort
*c *anon**
d DesClkDisable

S00 *v93*

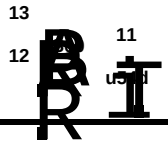
a WriteSU'
b WriteLink'
c WriteRH'
d WrIBFront

S00 *u33*

a pTC.0
b pTC.1
c WriteTC'
d C2Clk

S00 *u54*

a DRef'
b Mode4'
c
d



S02 *v08*

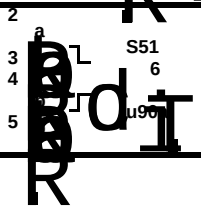
a pAlwaysCLK'
b pWaitCLK'
c WriteIB
d Nt_Pt

S08 *v32*

a paSh.0
*b pAllowMDR_*
c pME
*d *anon**

S51 *u90*

a
b WrTPC



S10 *v79*

a sh
b Push
c XByte'

S10 *v23*

a pTC.2
b pTC.3
c Wait

S20

a XBus_IB'
b EnLRotn'

LS32 *v98*

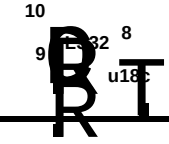
a DispBr'
b EnDispBr.3A'
c EnDispBr2-3B'
d EnDispBr0-1'

LS32 *v20*

a Link.0'
b Link.1'
c Link.2'
d Link.3'

LS32 *u18*

a pRet'
*b *anon**
c
d M01



S38 *v58*

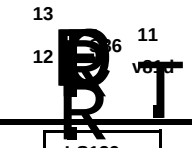
a Q.00
b Q.15
c CarryIn
d CarryIn

S51 *u90*

a Waitc1'
b WriteTPC'

S86 *v81*

a PageCross
b MapRef
c Refresh
d

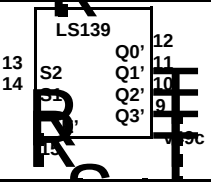


S260 *w04*

a IBEmptyErr
*b *anon**

LS139 *v49*

a
b bank decode

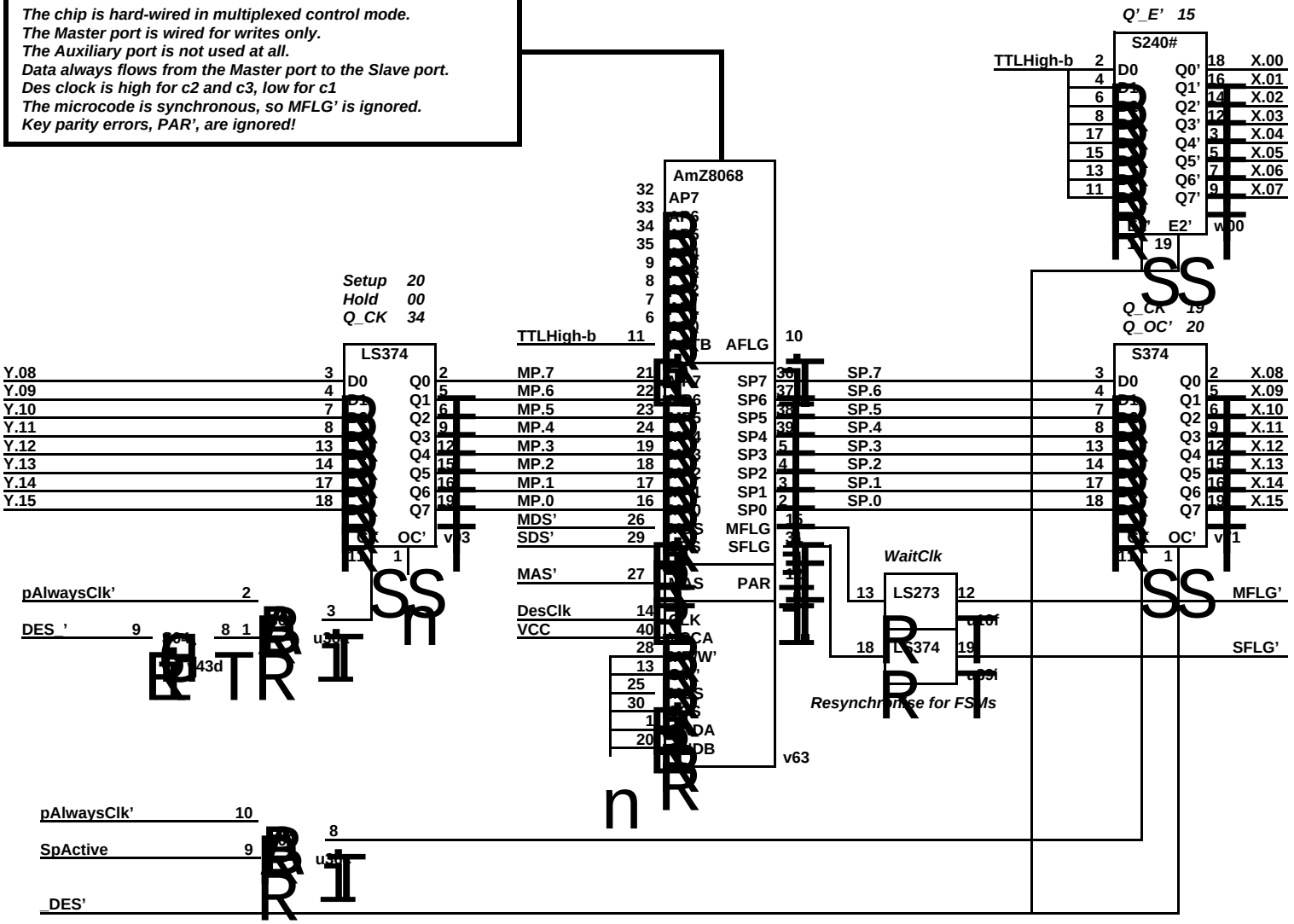


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Part Allocation & Spares	CPE28.sil	Tony West	Ba	5/30/83	29

DES Hardware Configuration Information

The chip is hard-wired in multiplexed control mode.
The Master port is wired for writes only.
The Auxiliary port is not used at all.
Data always flows from the Master port to the Slave port.
Des clock is high for c2 and c3, low for c1
The microcode is synchronous, so MFLG' is ignored.
Key parity errors, PAR', are ignored!

Zero out the high X bus when reading DES



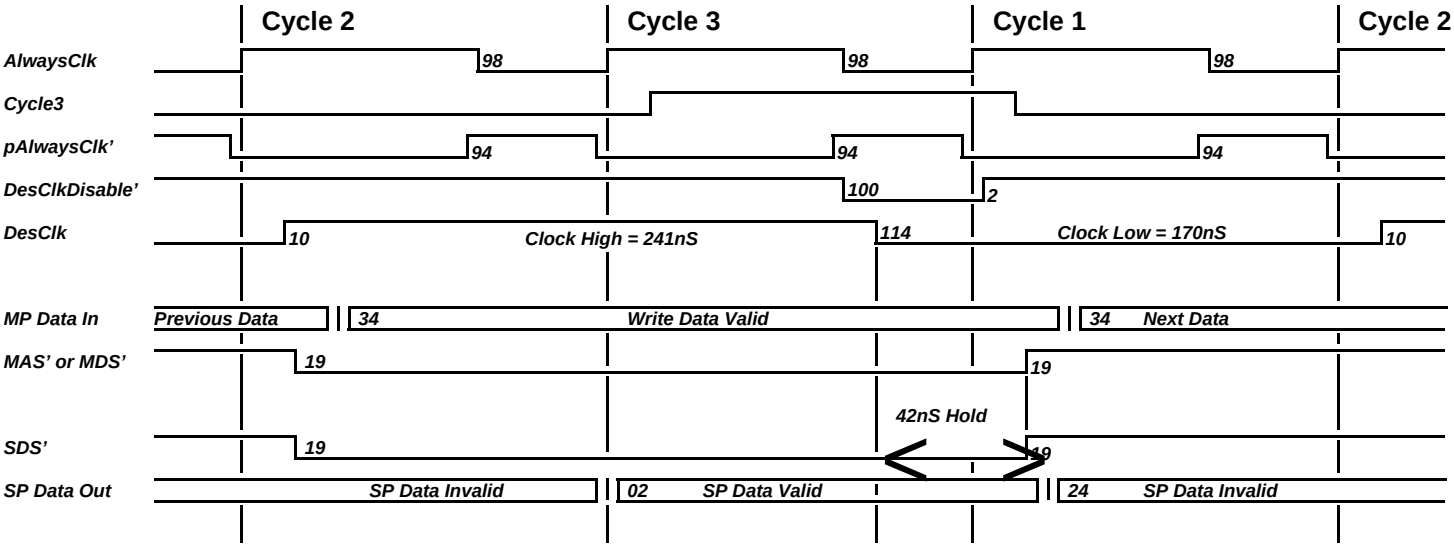
Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	DES Encryption Hardware	CPE29.sil	Tony West	Ba	5/30/83	30

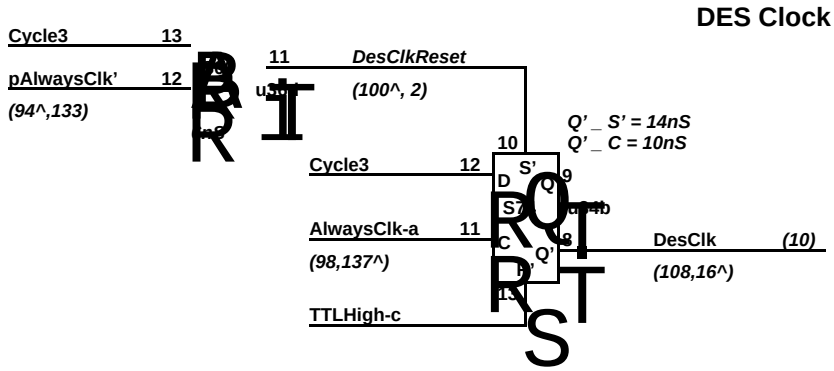
		AMD #	min.	max.	actual used	Notes
Clock & Reset						
Clock width HIGH		*1*	*115*		*241*	
Clock width LOW		*2*	*115*		*170*	
Clock Cycle		*3*	*250*		*411*	
Clock High to MAS'&MDS' High	*Reset Hold*	*6*	*0*	*50*	*19*	
MP and SP Strobe Times						
MAS' falling to MAS' rising (address)	*MAS width Low*	*32*	*80*		*274*	
MDS' falling to MDS' rising (data)	*MDS width Low*	*44a*	*125*	*1000*	*274*	*Can't exceed 1000, so have to watch out for WaitClk*
MDS' rising to MDS' falling	*MDS Recovery*	*46*	*125*		*137*	
SDS' falling to SDS' rising (data read)	*SDS width Low*	*44a*	*125*	*1000*	*274*	*Can't exceed 1000, so have to watch out for WaitClk*
SDS' rising to SDS' falling	*SDS Recovery*	*46*	*125*		*137*	
Clk falling to MDS' rising	*MDS Hold*	*45*	*20*	*70*	*42*	*This is the difficult bit! See circuitry below.*
Clk falling to SDS' rising	*SDS Hold*	*46*	*20*	*70*	*42*	*This is the difficult bit! See circuitry below.*
MAS Write into Master Port						
Data Valid to MAS' rising	*Address Setup*	*36*	*55*		*268*	
Data Hold after MAS' rising	*Address Hold*	*37*	*60*		*243*	
MDS Write into Master Port						
Data Valid to MDS' rising	*Data Setup*	*47b*	*125*		*268*	
Data Hold after MDS' rising	*Data Hold*	*48*	*80*		*243*	
SDS Read from Slave Port						
SDS falling to Data Valid	*SP Access*	*49b*		*120*		
SDS rising to Data Invalid	*SP Data Hold*	*50*	*5*			
SDS falling to SFLG rising	*SP Flag*	*51*		*125*		*for last byte read*

DES Clock Generator Timing

Note: *Because of the requirement to hold MDS' and SDS' for 20 to 70 nanoseconds after DesClk falling, we bring DesClk down early in Cycle 3. MAS', MDS' and SDS' follow at the end of Cycle 3.*



DES Clock Generator



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	DES Timing & Clock Generator	CPE30.sil	Tony West	Ba	5/30/83	31