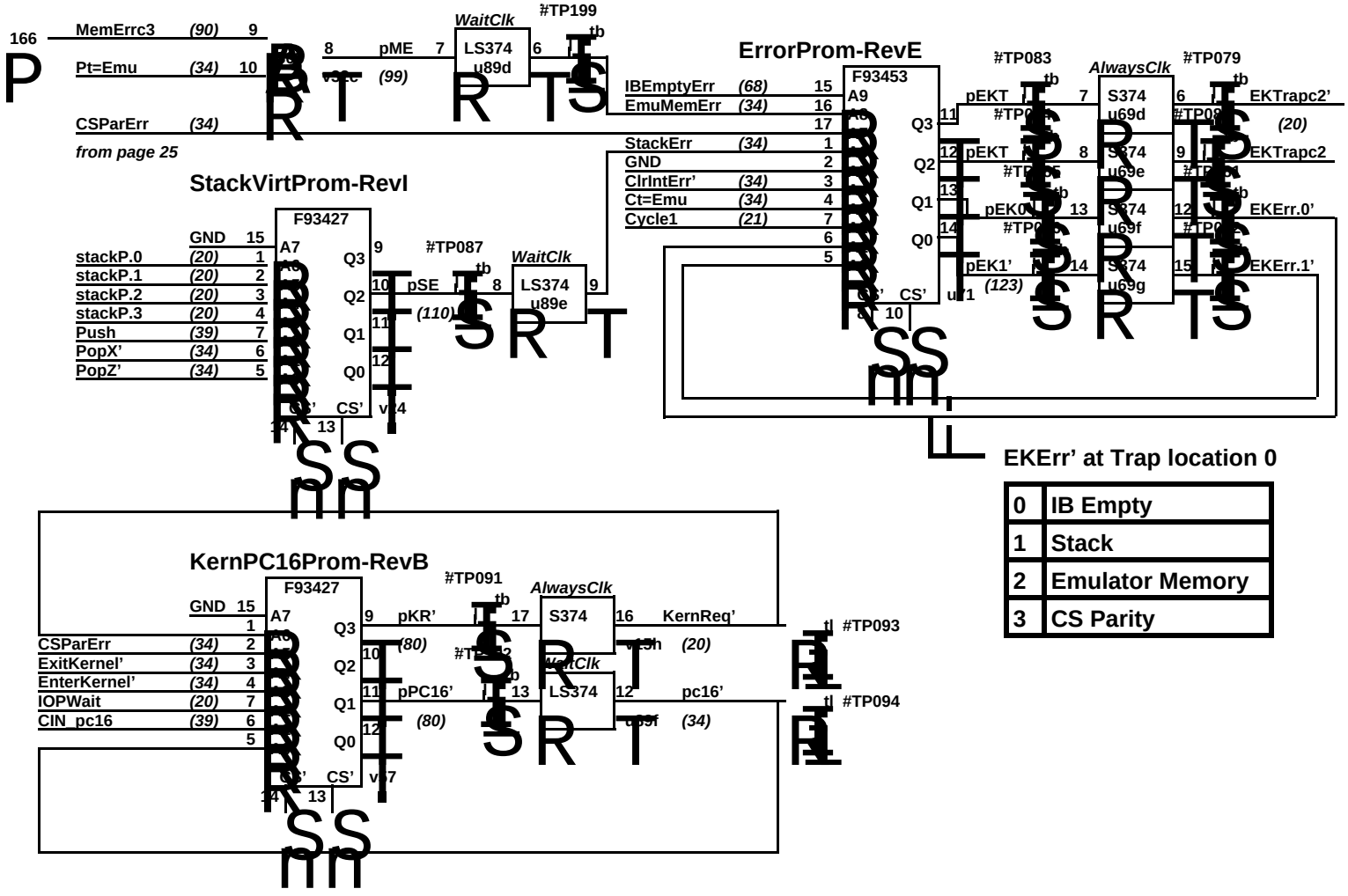
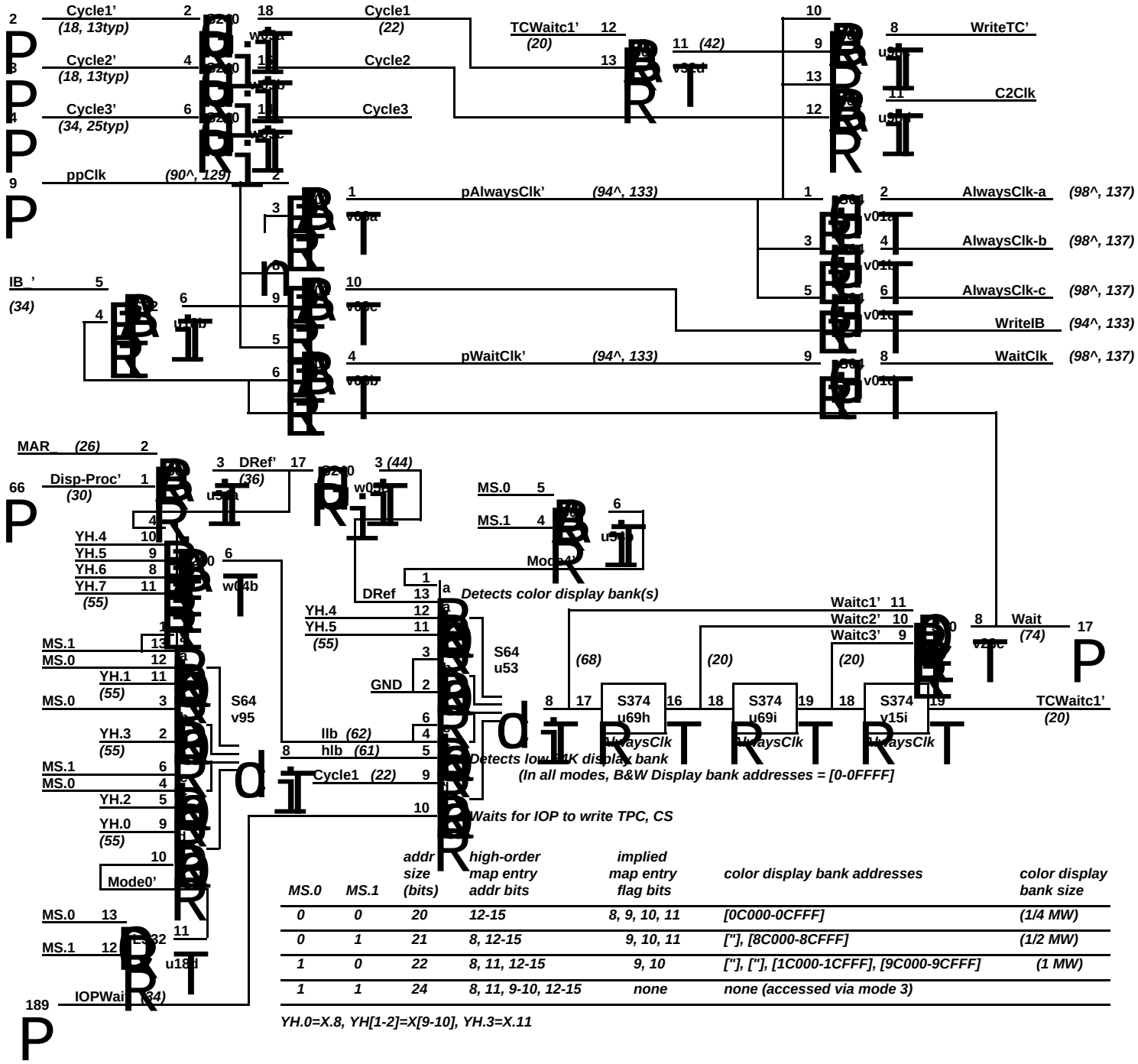
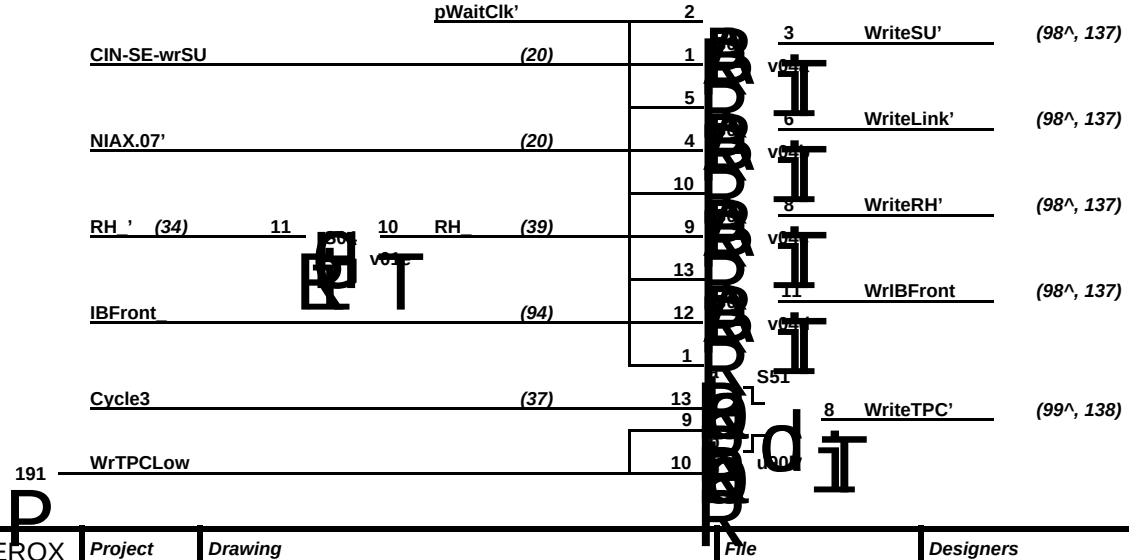


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Error, Emulator, & Kernel Proms	CPE16.sil	Bob Garner	Ba	5/30/83	17

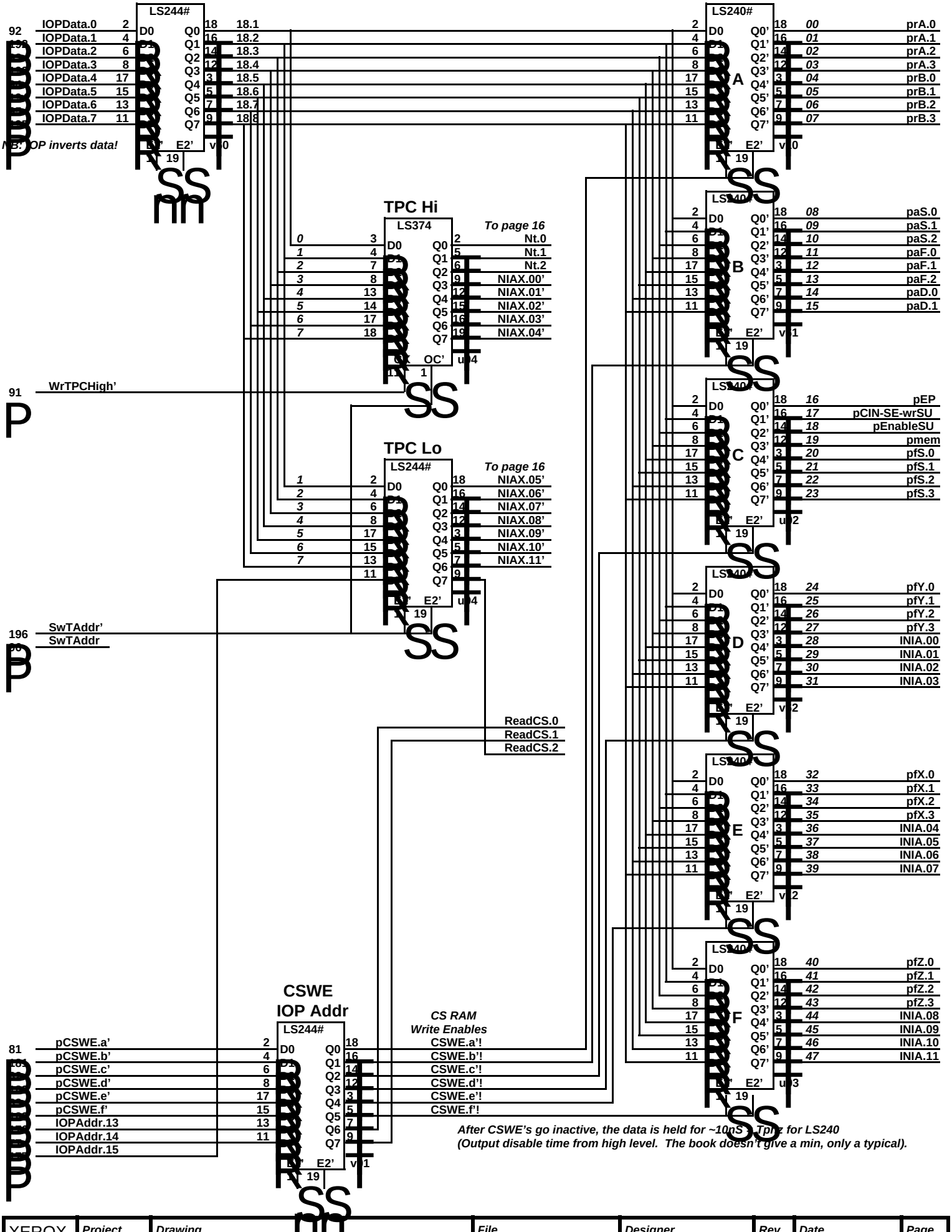


MS.0	MS.1	addr size (bits)	high-order map entry addr bits	implied map entry flag bits	color display bank addresses	color display bank size
0	0	20	12-15	8, 9, 10, 11	[0C000-0CFFF]	(1/4 MW)
0	1	21	8, 12-15	9, 10, 11	["], [8C000-8CFFF]	(1/2 MW)
1	0	22	8, 11, 12-15	9, 10	["], ["], [1C000-1CFFF], [9C000-9CFFF]	(1 MW)
1	1	24	8, 11, 9-10, 12-15	none	none (accessed via mode 3)	

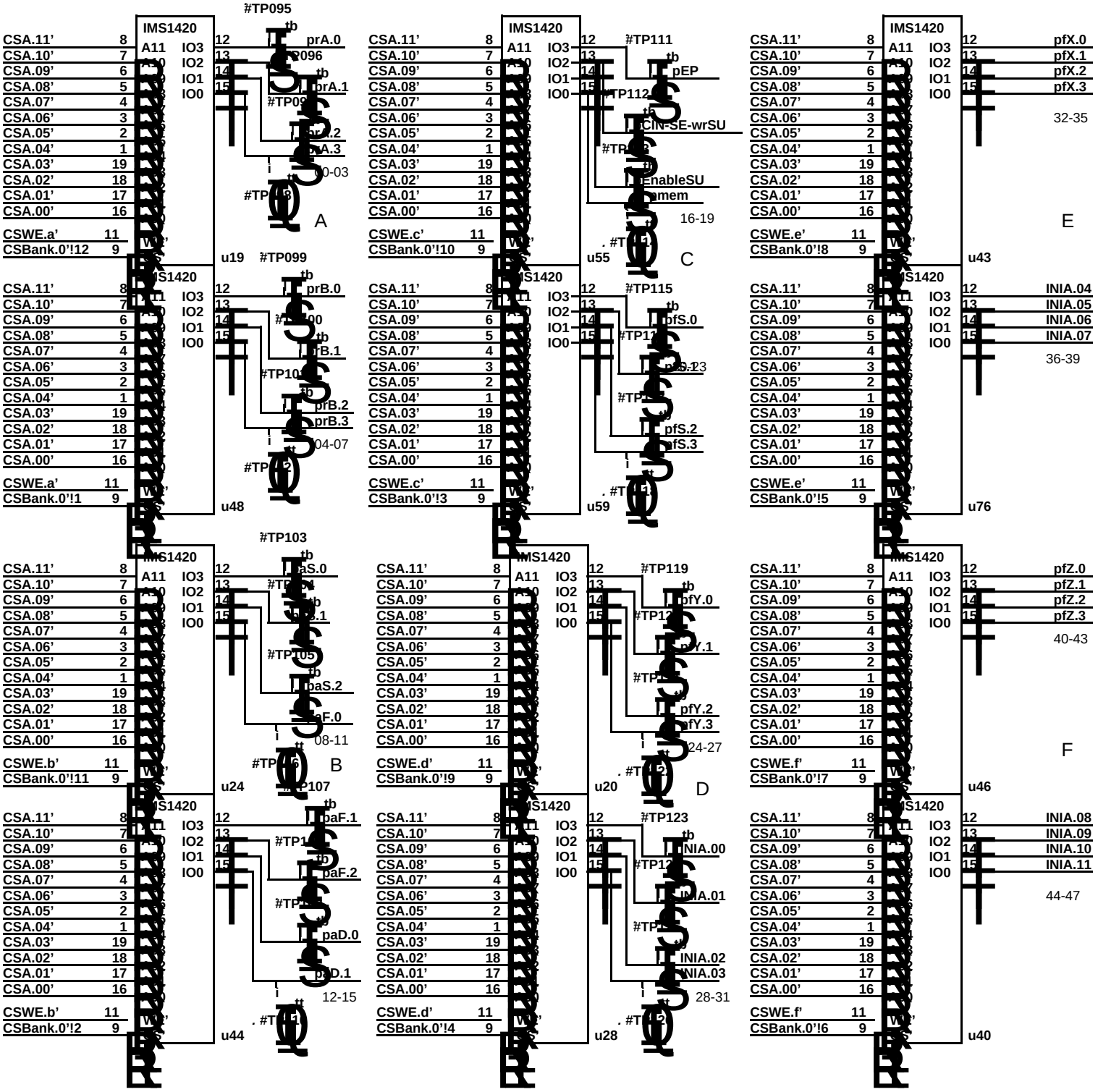
YH.0=X.8, YH[1-2]=X[9-10], YH.3=X.11



XEROX PARC	Project	Drawing	File	Designers	Rev	Date	Page
	CPE	Clocks, Wait	CPE17.sil	Garner, Purcell	Ba	5/30/83	18



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	IOP Data In, CS Write	CPE18.sil	Tony West	Ba	5/30/83	19

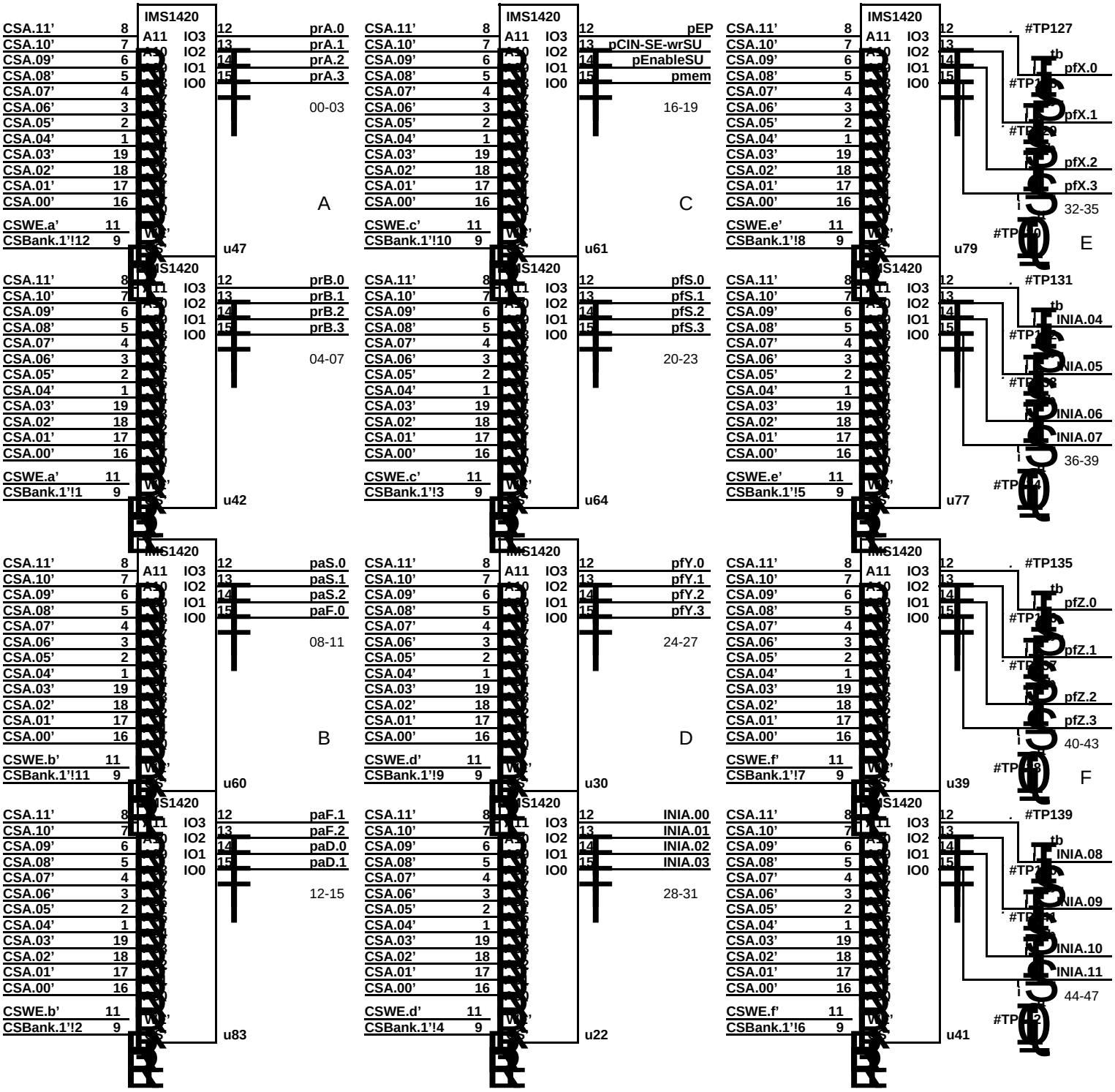


READ		WRITE - Data Hold	
Clock to CSA' valid	*17*	*tPLH for LS240*	*12*
Transmission Delay	*13*	*tPZ for LS244*	*10*
tAA for IMS 1420-55	*50*		*22*
CS Data valid at	*80*		

This suggests that IMS 1420-70 would also work without any trouble.

Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Control Store Bank 0: 0000-0FFF	CPE19.sil	Tony West	Ba	5/30/83	20



Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Control Store Bank 1: 1000-1FFF	CPE20.sil	Tony West	Ba	5/30/83	21