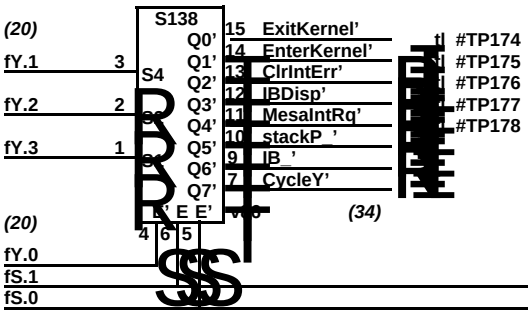
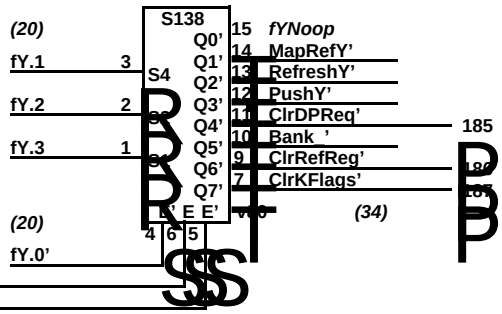
fYNorm - Low

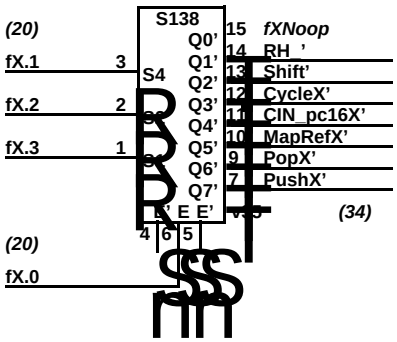


fYNorm - High



Bank_' replaces ClrIOPReq', which was connected to 184 on backplane

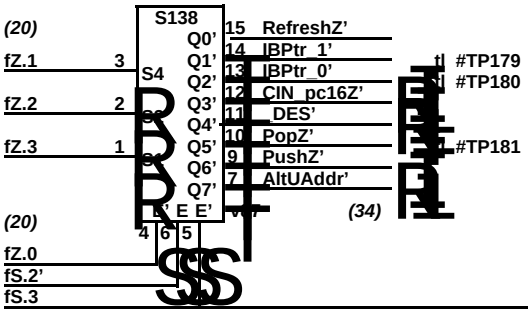
fX - High



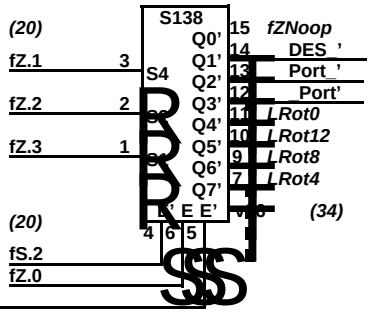
fX - Low is pCall/pRet

ADDED for CPE

fZNorm - Low



fZNorm - High



There are 2 spare fZ decodes available for future expansion

Notes on 16K CP additions:

Note that Bank_' is fY=D, not fZ=4, as stated in the Dandelion Hardware Manual!

Bank_' replaces ClrIOPReq', which is now obsolete. ClrIOPReq' was also connected to backplane pin 184.

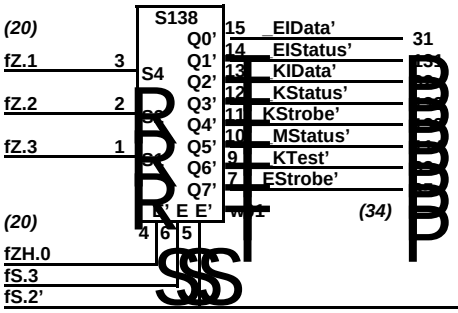
The meaning of Des_YBus' depends on which cycle it is activated in:

Des_YBus' in C2 means Write Des Address
Des_YBus' in C1 or C3 means Write Des Data

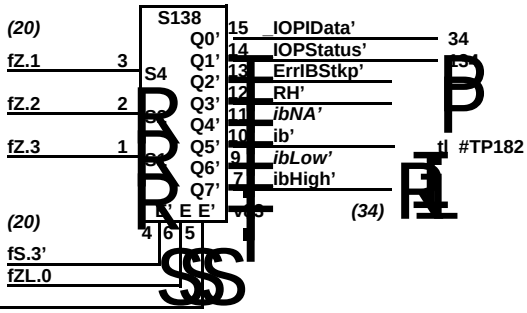
XBus_Des' can be activated in any cycle
See page sCPE31 for details of DES logic

The fZNorm-High decoder has been added in the 16K CP to derive the DES decodes.

IOXIn - Low



IOXIn - High



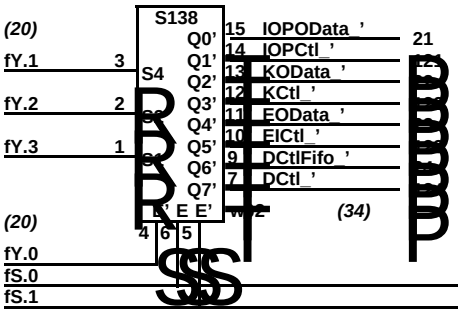
S138 Timing:

Propagation delays

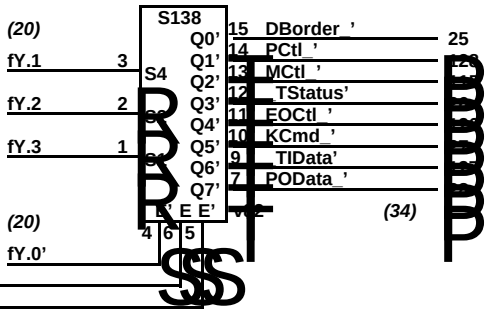
from Selects to Q'	***14nS***
from Enables to Q'	***13nS***

These timings are very conservative!

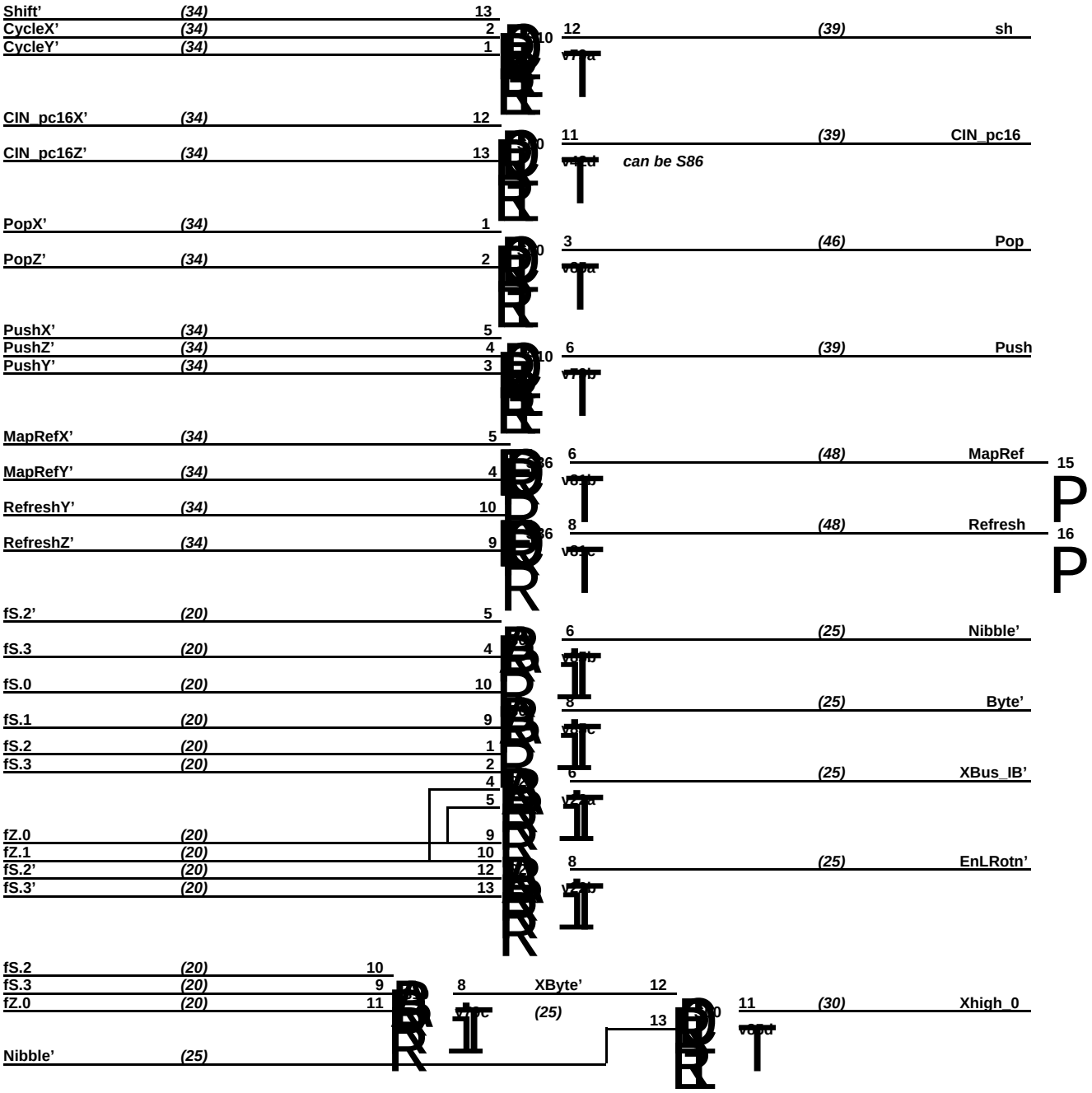
IOOut - Low



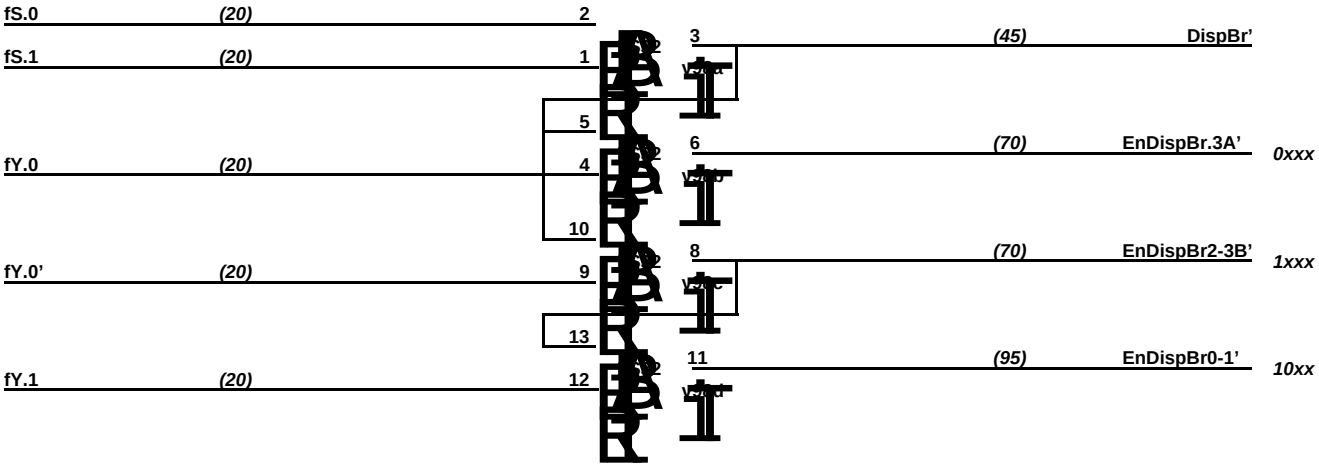
IOOut - High



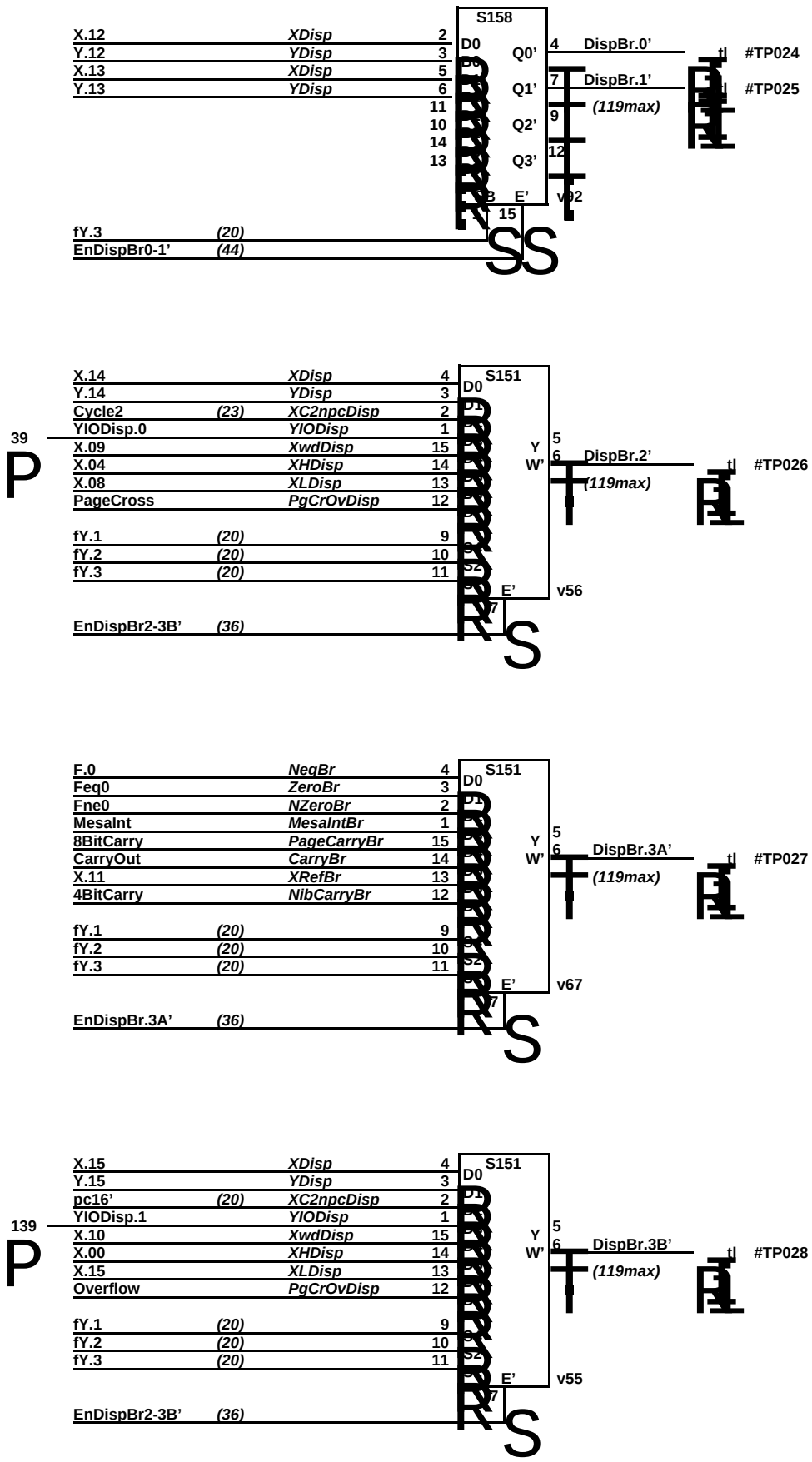
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Microinstruction Decoding I	CPE10.sil	Bob Garner	Ba	5/30/83	11



EnDispBr



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Microinstruction Decoding II	CPE11.sil	Bob Garner	Ba	5/30/83	12



DispBr[0-1] = max(c+32,69,133)

20 ^ to fY
24[3] S151 select to DispBr
18 DispBr' setup

64[3]=69

95 ^ to EnDispBr0-1'
18[2] S151 E' to DispBr
18 DispBr' setup

131[2] = 133 nS

c condition source
12[2] S151 data to DispBr
18 DispBr' setup

c+30[2]= c+32

DispBr Setup

5 S00 in to pTC
6[1] S64 in to pNIA
5[1] 25S09/S374 setup

18 nS

DispBr[2-3]=max(c+26,55,103)

20 ^ to fY
15[2] S151 select to DispBr
18 DispBr' setup

51[4]=55 nS

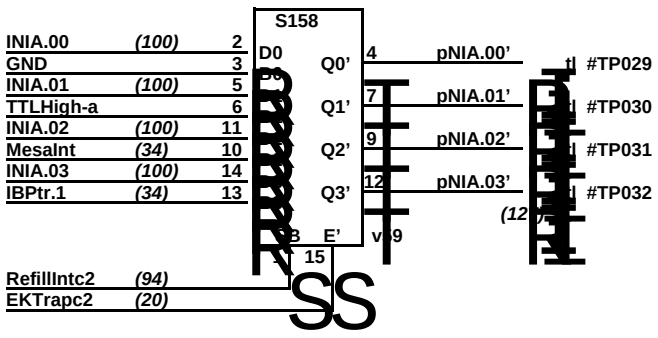
70 ^ to EnDispBr.3A'
13[2] S151 E' to DispBr
18 DispBr' setup

101[2] = 103 nS

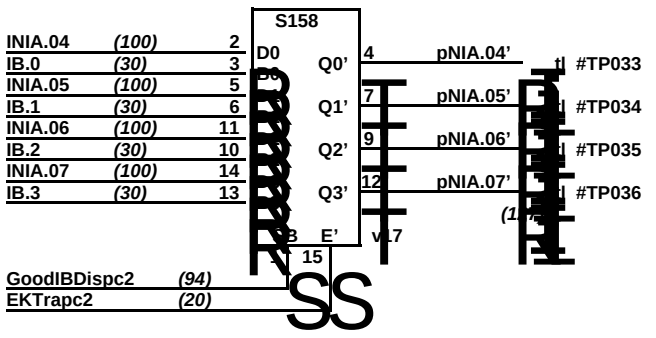
c condition source
7[1] S151 data to DispBr
18 DispBr' setup

c+23[3]=c+26 nS

pNIA[0-3]



pNIA[4-7]

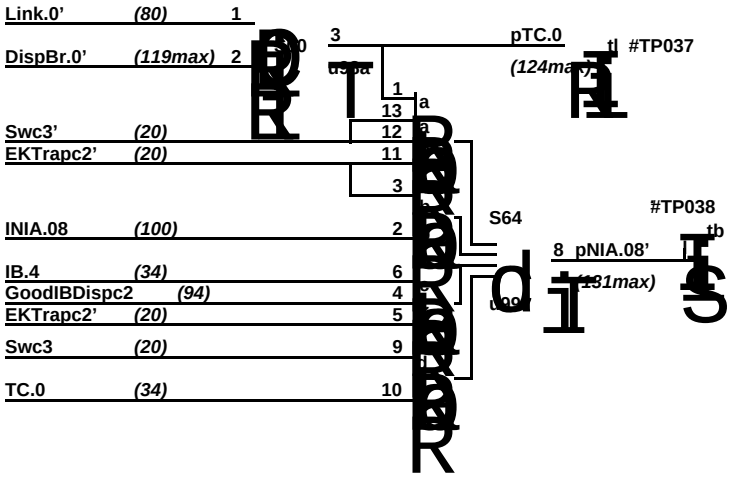


pNIA[0-7]=max(127, 120, 46) nS

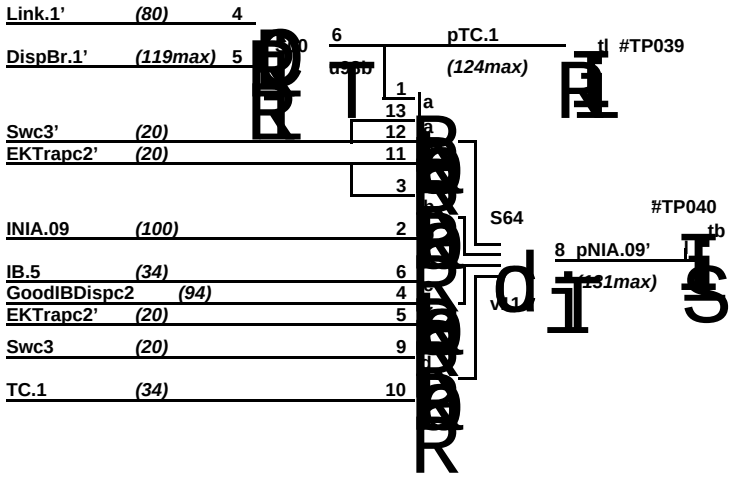
94	*^ to RefillIntc2*		*100*	*^ to INIA*		*20*	*^ to EKErrc2*	
24[3]	*LS158 SB to pNIA'*		*12[2]*	*LS158 data to pNIA'*		*18[2]*	*LS158 E' to pNIA'*	
5[1]	*25S09/S374 setup*		*5[1]*	*25S09/S374 setup*		*5[1]*	*25S09/S374 setup*	
123[4]=127 nS			*117[3]=120 nS*			*43[3]=46nS*		

(See page 11 for pNIA[8-11] timing)

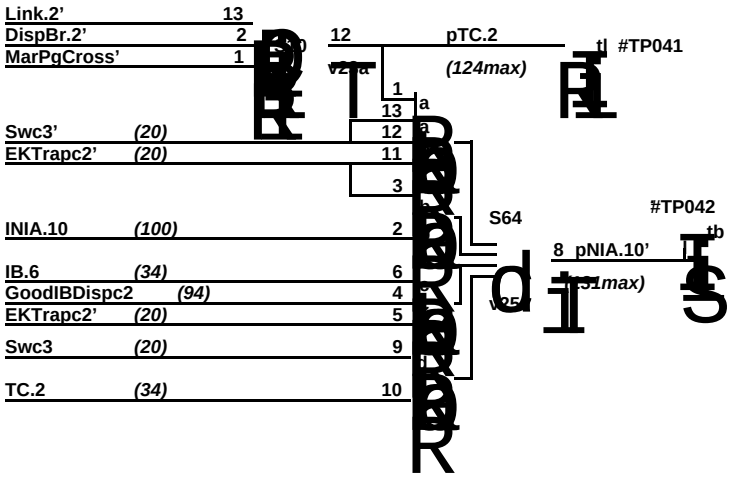
pNIA.8



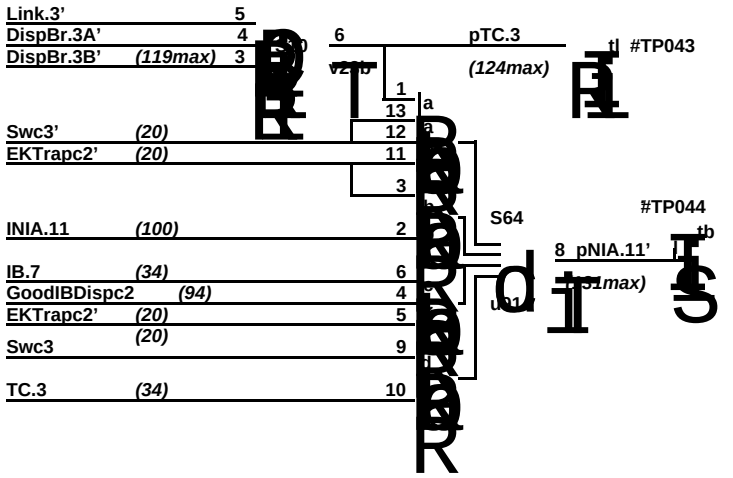
pNIA.9



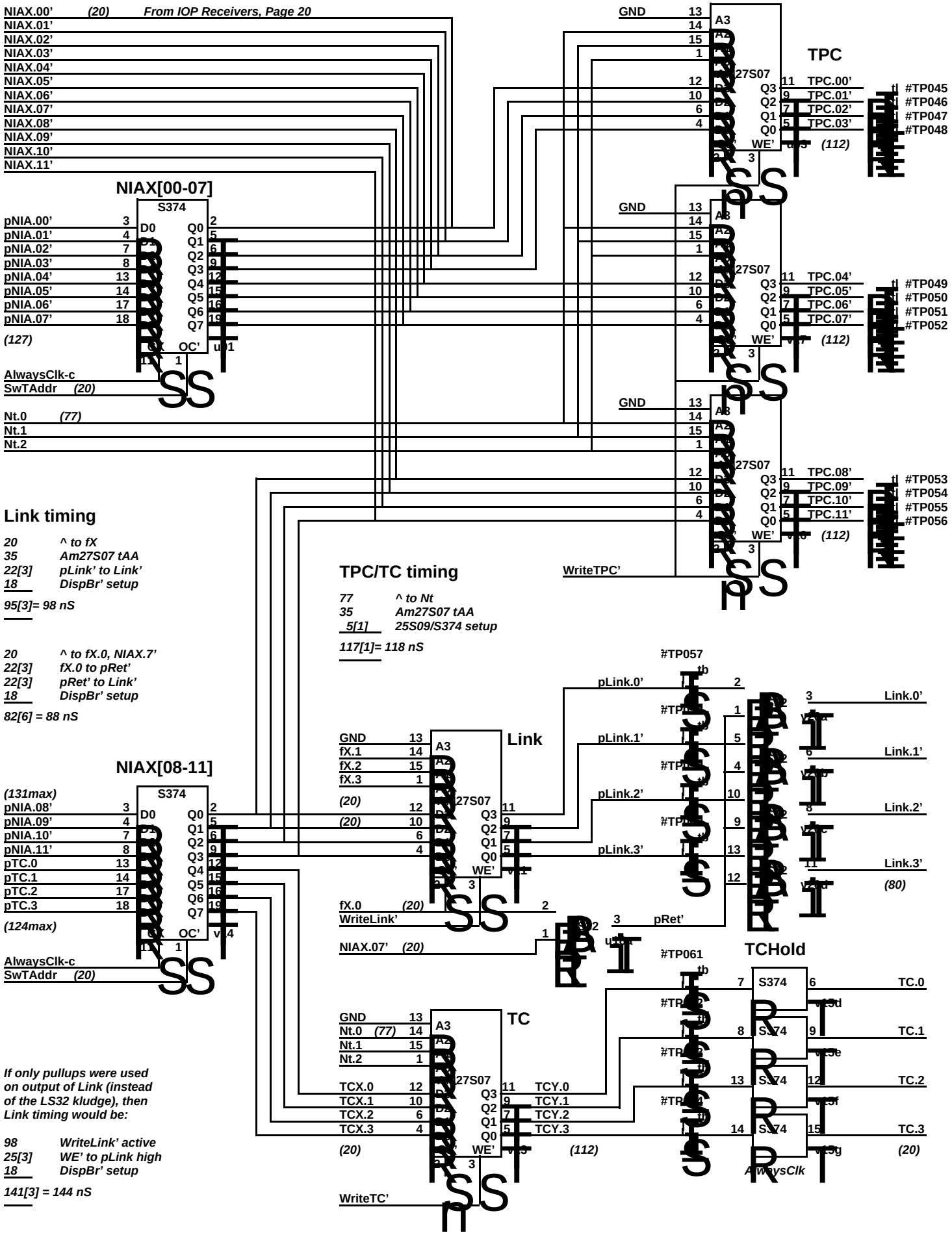
pNIA.10



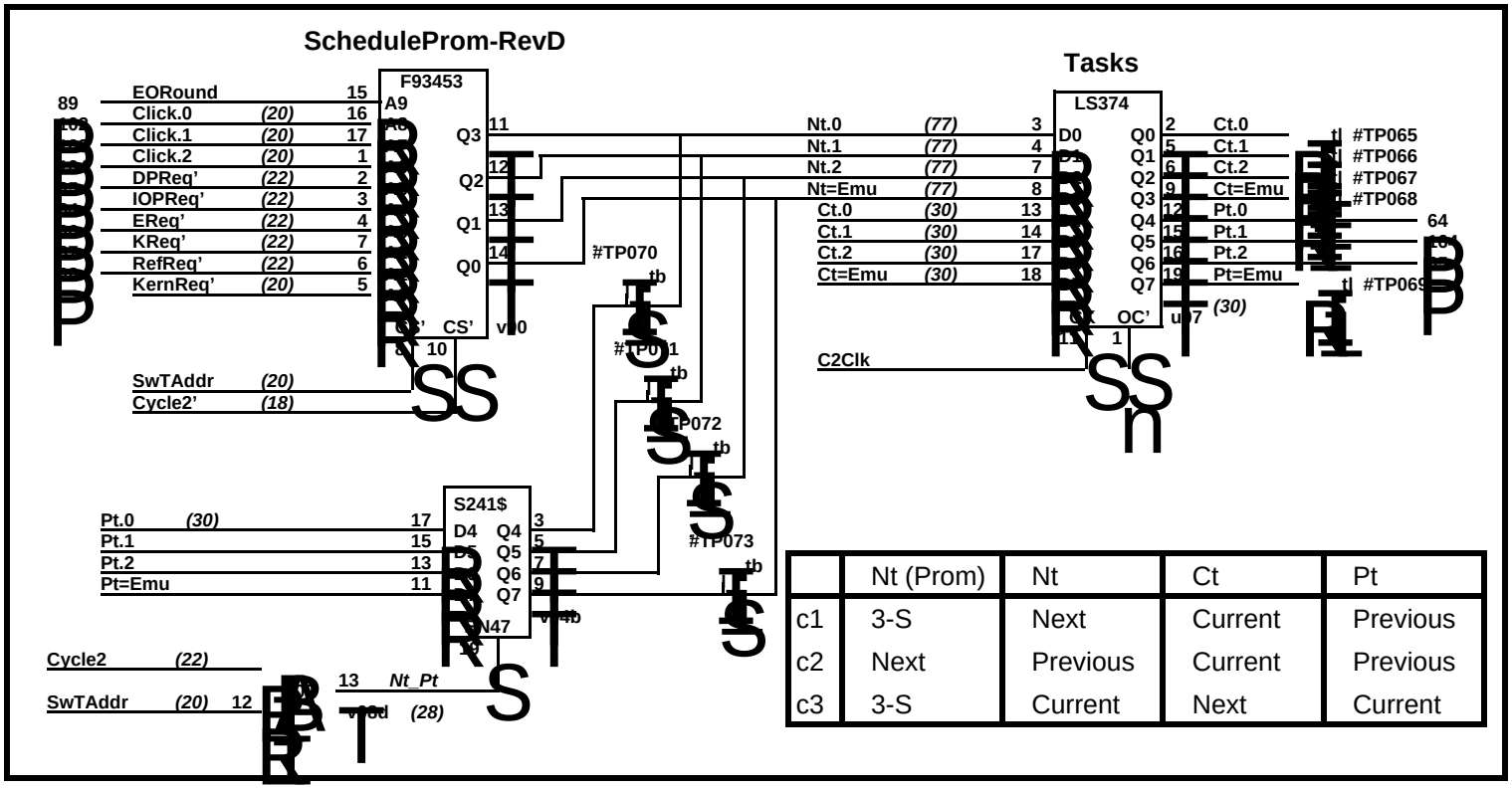
pNIA.11



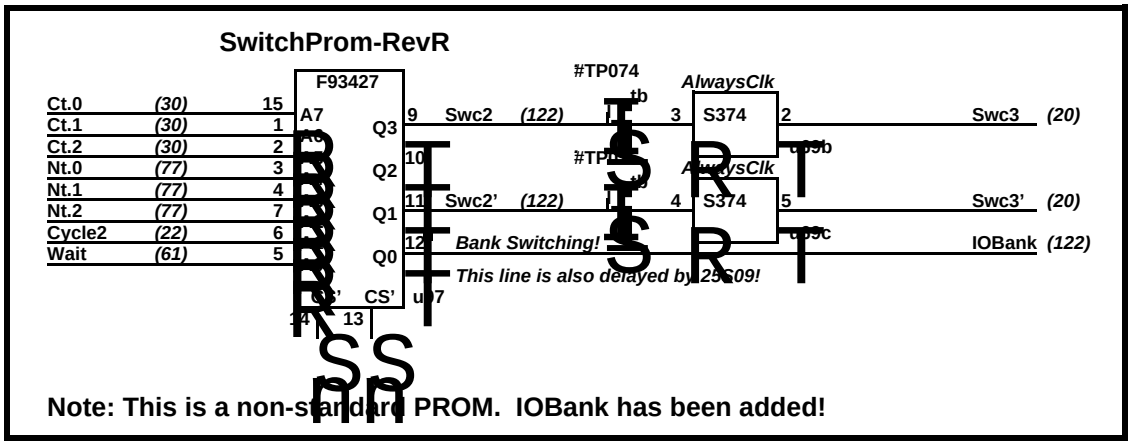
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	pNIA, pTC (Branching)	CPE13.sil	Bob Garner	Ba	5/30/83	14



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	TPC, TC, & Link	CPE14.sil	Bob Garner	Ba	5/30/83	15



	Nt (Prom)	Nt	Ct	Pt
c1	3-S	Next	Current	Previous
c2	Next	Previous	Current	Previous
c3	3-S	Current	Next	Current



Note: This is a non-standard PROM. IOBank has been added!

Task Numbers

0	Emulator
1	Display/LSEP
2	Ethernet
3	Refresh
4	Disk
5	IOP
6	Control Store R/W
7	Kernel

Swc2 timing=max(133,101,101)

22	*^ to Kreq'*	*20*	*^ to SwTAddr*	*28*	*^ to Nt_Pt*
55	*F93453 addr to Nt*	*25*	*F93453 CS' to Nt*	*15[2]*	*S241 EN to Nt*
45	*F93427 addr to Swc2*	*45*	*F93427 addr to Swc2*	*45*	*F93427 addr to Swc2*
10[1]	*25S09 SB setup*	*10[1]*	*25S09 SB setup*	*10[1]*	*25S09 SB setup*
132[1]=133 nS		*100[1]=101 nS*		*98[3]=101 nS*	

Click Assignment

0	Ethernet
1	Disk
2	IOP
3	Ethernet/Disk
4	Display/LSEP/Rfrsh

Notes:

When Disk = SA4000, Click 3 is Ethernet only.
When Disk = Trident, Click 3 is Ethernet on even rounds, Trident on Odd rounds (ie, 10-click round)

The Display & LSEP-refresh tasks never both use Click 4

Warning: This drawing contains font 4 macros!

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	CPE	Schedule, Switch, & Tasks	CPE15.sil	Bob Garner	Ba	5/30/83	16