A1

Connector

COMPONENT SIDE

ADGJ

BEHK

CFIL

A1 | B1 | C1 |

01-23

ODD

VEE -5.2

VDD +12

VTT -2

02-24

EVEN

VCC +5

01-23

ODD

VEE -5.2

VDD +12

VTT -2

02-24

EVEN

VCC +5

The pattern, shown twice above, repeats
12 times vertically
4 times horizontally

= GND

8
0.3"

18
0.3"

16
0.3"

14
0.3"

20
0.3"

24
0.6"

18
0.4" Legs stretched to 0.45"

24
0.4" Legs stretched to 0.45"

Notes:

1. The row numbers of the uncommitted rows, usable for TTL, etc. are:
   Top: 64 60 65 66 61 67 68 62 69 70 63 71 Bottom
2. Originally, the uncommitted rows were numbered for 24-pin chips.
   This is why pin 1 of the 24-pin chip in the B row is at B64, not 5B64!
3. 0.4" wide chips can be inserted by bending the legs out to 0.45".
4. The syntax for specifiying the board location of pin 1 of a chip is:

   # {_ {-} R-offset} { {^ }{-} D-offset} BoardLocation Modifier

   where R-offset is the number of positions DOWN in the picture above
   D-offset is the number of positions LEFT in the picture above
   { and } are metasymbols denoting optional omission.
   and Modifier may be ! or %, etc.

   Example: _3^1c1 is the location of the 24-pin 0.4" dip in the picture above.
   Example: _-1^-5B64 is the same as B1
   (_ and ^ actually specify offsets Right and Down to the chip hold vertically)

XEROX PARC-CSL	Project DORADO	Reference MW Board IC layout	File [Indigo]<DoradoLogic> MWBoardLayout.sil	Designer Overton/West	Date 07/15/82	Page 01