RIGHT
(C)

p

Even Pin#

C

I/O Connector

A

B

DispMhtTw

| Board Name | IFU | ProcH | ProcL | ContA | ContB | Base | |
|---|---|---|---|---|---|---|---|
| 5 | MemSH | StartCycle' | StartCycle' | MemSH | | CLK.OutBase' | 5 |
| 8 | CLKEnable'a | CLKEnable'c | CLKEnable'b | MemSH' | CLKEnable'a | CLK.ca' | 8 |
| 9 | CLK.ifu' | CLK.ph' | CLK.pl' | CLK.ca' | CLK.cb' | CLK.InBase' | 9 |
| 12 | MemClkEn'a | IOB.00 | Md.08 | CLKEnable'b | *IMLHPEdly* | CLK.cb' | 12 |
| 13 | JunkTW | IOB.01 | Md.09 | CLKEnable'c | *IMRHPEdly* | CLK.pl' | 13 |
| 16 | | IOB.02 | Md.10 | CLKEnable'a | | CLK.ph' | 16 |
| 17 | | IOB.03 | Md.11 | MemClkEn'a | | CLK.ifu' | 17 |
| 20 | IfuFaultInEc2 | IOB.04 | Md.12 | MemClkEn'b | | CLK.mc' | 20 |
| 21 | RefOutStdg' | Freeze | Freeze | Freeze | StartCycle' | CLK.mx' | 21 |
| 24 | SignIfuData | RSTK.0 | RSTK.0 | StartCycle' | RSTK.0 | CLK.md' | 24 |
| 25 | *CrryEvCntA* | RSTK.1 | RSTK.1 | _Dbuf | RSTK.1 | CLK.ms0Even' | 25 |
| 28 | GenIn.00 | RSTK.2 | RSTK.2 | | RSTK.2 | CLK.ms0Odd' | 28 |
| 29 | GenIn.01 | RSTK.3 | RSTK.3 | | RSTK.3 | CLK.ms1Even' | 29 |
| 32 | GenIn.02 | RBBypass | RBBypass | CramClock | CramClock | CLK.ms1Odd' | 32 |
| 33 | GenIn.03 | RBBypass' | RBBypass' | | | CLK.ms2Even' | 33 |
| 36 | GenIn.04 | IOB.05 | Md.13 | | | CLK.ms2Odd' | 36 |
| 37 | GenIn.05 | IOB.06 | Md.14 | StopMIRClk | StopMIRClk | CLK.ms3Even' | 37 |
| 40 | GenIn.06 | IOB.07 | Md.15 | IMRHPE' | IMRHPE' | CLK.ms3Odd' | 40 |
| 41 | GenIn.07 | IOB.16 | PrBlock' | PrBlock' | ASEL.0'mem | CLK.disk' | 41 |
| 44 | GenIn.08 | Md.00 | IOB.08 | TWReq.01 | IMLHPE' | CLK.display' | 44 |
| 45 | GenIn.09 | Md.01 | IOB.09 | JunkTW | | CLK.io20' | 45 |
| 48 | GenIn.10 | Md.02 | IOB.10 | DispYhtTW | | CLK.io21' | 48 |
| 49 | GenIn.11 | SelectRm'a | SelectRm'a | Error' | Error' | CLK.io22' | 49 |
| 52 | GenIn.12 | SelectStk'a | SelectStk'a | UseDMD | UseDMD | UseDMD | 52 |
| 53 | GenIn.13 | | QBit' | QBit' | | CLK.io23' | 53 |
| 56 | GenIn.14 | Md.03 | IOB.11 | DispMhtTW | | CLK.io24' | 56 |
| 57 | GenIn.15 | Md.04 | IOB.12 | TWReq.05 | CPIn.0 | CPIn.0 | 57 |
| 60 | GenOut.00 | Md.05 | IOB.13 | EthOutTW | CPIn.1 | CPIn.1 | 60 |
| 61 | GenOut.01 | Md.06 | IOB.14 | EthInTW | CPIn.2 | CPIn.2 | 61 |
| 64 | GenOut.02 | Md.07 | IOB.15 | TWReq.08 | CPIn.3 | CPIn.3 | 64 |
| 65 | GenOut.03 | Md.16 | IOB.17 | SetRun | | SetRun | 65 |
| 68 | GenOut.04 | SignIfuData | Md.17 | SetSS' | | SetSS' | 68 |
| 69 | GenOut.05 | Pdata.15 | Pdata.15 | CPOut.0 | CPOut.0 | CPOut.0 | 69 |
| 72 | GenOut.06 | StkAdr.0a | StkAdr.0a | CPOut.1 | CPOut.1 | CPOut.1 | 72 |
| 73 | GenOut.07 | StkAdr.1a | StkAdr.1a | CPOut.2 | CPOut.2 | CPOut.2 | 73 |
| 76 | GenOut.08 | StkAdr.2a | StkAdr.2a | CPOut.3 | CPOut.3 | CPOut.3 | 76 |
| 77 | GenOut.09 | StkAdr.3a | StkAdr.3a | CPOut.4 | CPOut.4 | CPOut.4 | 77 |
| 80 | GenOut.10 | StkAdr.4a | StkAdr.4a | CPOut.5 | CPOut.5 | CPOut.5 | 80 |
| 81 | GenOut.11 | StkAdr.5a | StkAdr.5a | CPOut.6 | CPOut.6 | CPOut.6 | 81 |
| 84 | GenOut.12 | StkAdr.6a | StkAdr.6a | CPOut.7 | CPOut.7 | CPOut.7 | 84 |
| 85 | GenOut.13 | StkAdr.7a | StkAdr.7a | CPOut.8 | CPOut.8 | CPOut.8 | 85 |
| 88 | GenOut.14 | RbAdr.0' | RbAdr.0' | _Map | | | 88 |
| 89 | GenOut.15 | RbAdr.1' | RbAdr.1' | CPStrb' | CPStrb' | CPStrb' | 89 |
| 92 | *EventA* | RbAdr.2' | RbAdr.2' | CPAddr.0' | CPAddr.0' | CPAddr.0' | 92 |
| 93 | *EventB* | RbAdr.3' | RbAdr.3' | CPAddr.1' | CPAddr.1' | CPAddr.1' | 93 |
| 96 | *Vcc+5v* | Alu.07 | Alu.07 | CPAddr.2' | CPAddr.2' | CPAddr.2' | 96 |
| 97 | *Vcc+5v* | Alu.08 | Alu.08 | | | | 97 |
| 100 | | Alu.15 | BMux.17 | BMux.17 | BMux.17 | SrtClkPulse | 100 |
| 101 | | BMux.16 | Alu.15 | BMux.16 | BMux.16 | dSrtClkPulse | 101 |
| 104 | BMux.15 | AluM | BMux.15 | BMux.15 | BMux.15 | | 104 |
| 105 | BMux.07 | BMux.07 | AluM | BMux.07 | BMux.07 | | 105 |
| 108 | BootNO | AluF0 | AluF0 | dIMOut.07 | dIMOut.07 | BootNO | 108 |
| 109 | MAR.15' | TaskSimTW | MAR.15' | dIMOut.08 | dIMOut.08 | RcvData | 109 |
| 112 | MAR.07' | MAR.07' | *RScopeClk0'* | dIMOut.09 | dIMOut.09 | Collision | 112 |
| 113 | MAR.14' | AluF1 | MAR.14' | dIMOut.10 | dIMOut.10 | XmtData' | 113 |
| 116 | MAR.06' | MAR.06' | AluF1 | dIMOut.11 | dIMOut.11 | Sequence.0' | 116 |
| 117 | BMux.14 | AluF2 | BMux.14 | BMux.14 | BMux.14 | | 117 |
| 120 | BMux.06 | BMux.06 | AluF2 | BMux.06 | BMux.06 | | 120 |
| 121 | BMux.13 | AluF3 | BMux.13 | BMux.13 | BMux.13 | | 121 |
| 124 | BMux.05 | BMux.05 | AluF3 | BMux.05 | BMux.05 | | 124 |
| 125 | IfuData.0 | TIOA.0 | IfuData.0 | | | | 125 |
| 128 | IfuData.1 | TIOA.1 | IfuData.1 | DispMwtTW | CBTempSense | CBTempSense | 128 |
| 129 | IfuData.2 | TIOA.2 | IfuData.2 | TaskSimTW | | | 129 |
| 132 | IfuData.3 | TIOA.3 | IfuData.3 | DispYwtTW | | | 132 |
| 133 | IfuData.4 | TIOA.4 | IfuData.4 | DiskTW | | | 133 |
| 136 | IfuData.5 | TIOA.5 | IfuData.5 | TWReq.13 | | | 136 |
| 137 | IfuData.6 | TIOA.6 | IfuData.6 | TWReq.14 | | | 137 |
| 140 | IfuData.7 | TIOA.7 | IfuData.7 | FaultTW | | | 140 |
| 141 | BMux.12 | | BMux.12 | BMux.12 | BMux.12 | | 141 |
| 144 | BMux.04 | BMux.04 | | BMux.04 | BMux.04 | | 144 |
| 145 | BMux.11 | AluCO | BMux.11 | BMux.11 | BMux.11 | | 145 |
| 148 | BMux.03 | BMux.03 | AluCO | BMux.03 | BMux.03 | | 148 |
| 149 | BMux.10 | AluG1 | BMux.10 | BMux.10 | BMux.10 | | 149 |
| 152 | BMux.02 | BMux.02 | AluG1 | BMux.02 | BMux.02 | | 152 |
| 153 | MAR.13' | AluP1 | MAR.13' | dIMOut.12 | dIMOut.12 | | 153 |
| 156 | MAR.05' | MAR.05' | AluP1 | dIMOut.13 | dIMOut.13 | RfshPeriod | 156 |
| 157 | MAR.12' | Shc.08 | MAR.12' | dIMOut.14 | dIMOut.14 | | 157 |
| 160 | MAR.04' | MAR.04' | Shc.08 | dIMOut.15 | dIMOut.15 | | 160 |
| 161 | MAR.11' | Shc.09 | MAR.11' | | | | 161 |
| 164 | MAR.03' | MAR.03' | Shc.09 | | | | 164 |
| 165 | BMux.09 | Shc.10 | BMux.09 | BMux.09 | BMux.09 | | 165 |
| 168 | BMux.01 | BMux.01 | Shc.10 | BMux.01 | BMux.01 | OISDataOut' | 168 |
| 169 | BMux.08 | Shc.11 | BMux.08 | BMux.08 | BMux.08 | OISDataOut | 169 |
| 172 | BMux.00 | BMux.00 | Shc.11 | BMux.00 | BMux.00 | | 172 |
| 173 | | BNTGtCT'a | BNTGtCT'a | BNTGtCT'a | BNTGtCT'a | | 173 |
| 176 | Pendulum | Shc.12 | Shc.12 | BNTGtCT'b | | Pendulum | 176 |
| 177 | MAR.10' | Shc.13 | MAR.10' | rMIRa | rMIRa | KBoardData | 177 |
| 180 | MAR.02' | MAR.02' | Shc.13 | SetRunRfsh | | SetRunRfsh | 180 |
| 181 | MAR.09' | Shc.14 | MAR.09' | | | | 181 |
| 184 | MAR.01' | MAR.01' | Shc.14 | | | | 184 |
| 185 | MAR.08' | Shc.15 | MAR.08' | | | | 185 |
| 188 | MAR.00' | MAR.00' | Shc.15 | | | | 188 |
| Board Socket# | 6 | 5 | 4 | 3 | 2 | 1 | |

**File: BPRight01.sil**

**Dated: 7/24/80**

**By: Mike Overton**

RIGHT
(C)

p

*Even Pin#*

I/O Connector

* Jumper connection to ContA board for desired Task wake up

| Board Name | MSA1Odd | MSA1Even | MSA0Odd | MSA0Even | MemD | MemX | MemC | |
|---|---|---|---|---|---|---|---|---|
| 5 | | | | | @MemSH | MemSH | MemSH | 5 |
| 8 | CLKEnable'b | CLKEnable'a | CLKEnable'c | CLKEnable'b | CLKEnable'a | CLKEnable'c | CLKEnable'b | 8 |
| 9 | CLK.ms1Odd' | CLK.ms1Even' | CLK.ms0Odd' | CLK.ms0Even' | CLK.md' | CLK.mx' | CLK.mc' | 9 |
| 12 | | | | | MemClkEn'a | MemClkEn'a | MemClkEn'a | 12 |
| 13 | | | | | Md.08 | TagInEc1 | TagInEc1 | 13 |
| 16 | | | | | Md.09 | CacheRefInEc1 | CacheRefInEc1 | 16 |
| 17 | | | | | Md.10 | Store_InEc1' | Store_InEc1' | 17 |
| 20 | | | | | Md.11 | IfuRefInEc1 | IfuRefInEc1 | 20 |
| 21 | | | | | Md.12 | _Config | RefOutstdg' | 21 |
| 24 | | | | | _Dbuf | _Pipe3 | _Config | 24 |
| 25 | | | | | _Pipe4 | _Pipe4 | _Pipe3 | 25 |
| 28 | Sout.08 | Sout.08 | Sout.08 | Sout.08 | Sout.08 | DirtyIoFinA' | _Pipe4 | 28 |
| 29 | Sout.09 | Sout.09 | Sout.09 | Sout.09 | Sout.09 | Mod0SinEn' | DirtyIoFinA' | 29 |
| 32 | Sout.10 | Sout.10 | Sout.10 | Sout.10 | Sout.10 | Mod1SinEn' | | 32 |
| 33 | Sout.11 | Sout.11 | Sout.11 | Sout.11 | Sout.11 | Mod2SinEn' | | 33 |
| 36 | Mod1SinEn' | Mod1SinEn' | Mod0SinEn' | Mod0SinEn' | Md.13 | Mod3SinEn' | | 36 |
| 37 | LoadSinO | LoadSinE | LoadSinO | LoadSinE | Md.14 | LoadSinE | | 37 |
| 40 | ShiftSoutO | ShiftSoutE | ShiftSoutO | ShiftSoutE | Md.15 | LoadSinO | | 40 |
| 41 | ShiftEcOut | ShiftEcOut | ShiftEcOut | ShiftEcOut | Md.00 | ShiftSoutE | ASEL.0'mem | 41 |
| 44 | Sin.08 | Sin.08 | Sin.08 | Sin.08 | Sin.08 | ShiftSoutO | DdataGood' | 44 |
| 45 | Sin.09 | Sin.09 | Sin.09 | Sin.09 | Sin.09 | ShiftEcOut | PrivRInPair | 45 |
| 48 | Sin.10 | Sin.10 | Sin.10 | Sin.10 | Sin.10 | ProcTagInA | ProcTagInA | 48 |
| 49 | Sin.11 | Sin.11 | Sin.11 | Sin.11 | Sin.11 | WpInEc1 | WpInEc1 | 49 |
| 52 | | | | | Md.01 | Mcr_' | Mcr_' | 52 |
| 53 | | | | | Md.02 | ProcSrn_' | ProcSrn_' | 53 |
| 56 | | | | | Md.03 | _Pipe2 | _Pipe2 | 56 |
| 57 | | | | | Md.04 | _FaultInfo | _FaultInfo | 57 |
| 60 | | | | | Md.05 | HoldMapBuf | HoldMapBuf | 60 |
| 61 | | | | | Md.06 | Store_InA' | Store_InA' | 61 |
| 64 | | | | | Md.07 | Map_InPair' | Map_InPair' | 64 |
| 65 | | | | | Md.16 | VicIfMiss' | VicIfMiss' | 65 |
| 68 | | | | | Md.17 | dHitPerr | dHitPerr | 68 |
| 69 | | | | | dDad.13 | IfuFaultInEc2 | dDad.13 | 69 |
| 72 | | | | | dDad.12 | DdataGood' | dDad.12 | 72 |
| 73 | | | | | dDad.11 | PrivRInPair | dDad.11 | 73 |
| 76 | | | | | dDad.10 | ErrFromEc2 | dDad.10 | 76 |
| 77 | | | | | dDad.09 | dPipe34Ad.0 | dDad.09 | 77 |
| 80 | | | | | dDad.08 | dPipe34Ad.1 | dDad.08 | 80 |
| 81 | | | | | dDad.07 | dPipe34Ad.2 | dDad.07 | 81 |
| 84 | | | | | dDad.06 | ECFault | dDad.06 | 84 |
| 85 | | | | | dDad.05 | MemError | dDad.05 | 85 |
| 88 | | | | | dDad.04 | dSTPerr | dDad.04 | 88 |
| 89 | | | | | dDad.03 | StartEcGen' | dDad.03 | 89 |
| 92 | | | | | dDad.02 | _Map | dDad.02 | 92 |
| 93 | | | | | Dad.01 | LargeHold | Dad.01 | 93 |
| 96 | | | | | Dad.00 | EcKeepsAB | EcKeepsAB | 96 |
| 97 | | | | | _dPipe34Ad.3 | dPipe34Ad.3 | Dad.00 | 97 |
| 100 | | | | | @BMux.17 | BMux.17 | | 100 |
| 101 | | | | | @BMux.16 | BMux.16 | | 101 |
| 104 | | | | | @BMux.15 | BMux.15 | BMux.15 | 104 |
| 105 | | | | | @BMux.07 | BMux.07 | BMux.07 | 105 |
| 108 | | | | | StartEcGen' | MapTrbInEc1 | MapTrbInEc1 | 108 |
| 109 | | | | | dMDMad.0' | dMDMad.0' | MAR.15' | 109 |
| 112 | | | | | dMDMad.1' | dMDMad.1' | MAR.07' | 112 |
| 113 | | | | | dMDMad.2' | dMDMad.2' | MAR.14' | 113 |
| 116 | | | | | dMDMad.3' | dMDMad.3' | MAR.06' | 116 |
| 117 | | | | | @BMux.14 | BMux.14 | BMux.14 | 117 |
| 120 | | | | | @BMux.06 | BMux.06 | BMux.06 | 120 |
| 121 | | | | | @BMux.13 | BMux.13 | BMux.13 | 121 |
| 124 | | | | | @BMux.05 | BMux.05 | BMux.05 | 124 |
| 125 | | | | | ECFault | TIOA.0 | IfuData.0 | 125 |
| 128 | | | | | MemError | TIOA.1 | IfuData.1 | 128 |
| 129 | | | | | StartEcChk' | StartEcChk' | IfuData.2 | 129 |
| 132 | | | | | dSTPerr | FaultTW | IfuData.3 | 132 |
| 133 | | | | | EcOut.0 | ShiftSinE | IfuData.4 | 133 |
| 136 | | | | | EcOut.2 | ShiftSinO | IfuData.5 | 136 |
| 137 | | | | | EcOut.4 | MemRASa | Ifudata.6 | 137 |
| 140 | EcOut.2 | EcOut.0 | EcOut.2 | EcOut.0 | EcOut.6 | MemCASa | IfuData.7 | 140 |
| 141 | EcOut.6 | EcOut.4 | EcOut.6 | EcOut.4 | @BMux.12 | BMux.12 | BMux.12 | 141 |
| 144 | | | | | @BMux.04 | BMux.04 | BMux.04 | 144 |
| 145 | ShiftSinO | ShiftSinE | ShiftSinO | ShiftSinE | @BMux.11 | BMux.11 | BMux.11 | 145 |
| 148 | MemRASa | MemRASa | MemRASa | MemRASa | @BMux.03 | BMux.03 | BMux.03 | 148 |
| 149 | MemCASa | MemCASa | MemCASa | MemCASa | @BMux.10 | BMux.10 | BMux.10 | 149 |
| 152 | MemWEa | MemWEa | MemWEa | MemWEa | @BMux.02 | BMux.02 | BMux.02 | 152 |
| 153 | | | | | ErrFromEc2 | MemWEa | MAR.13' | 153 |
| 156 | EcIn.0 | EcIn.0 | EcIn.0 | EcIn.0 | EcIn.0 | RfshPeriod | MAR.05' | 156 |
| 157 | Sin.00 | Sin.00 | Sin.00 | Sin.00 | Sin.00 | LoadEcOut' | MAR.12' | 157 |
| 160 | Sin.01 | Sin.01 | Sin.01 | Sin.01 | Sin.01 | Mod3StrEn' | MAR.04' | 160 |
| 161 | Sin.02 | Sin.02 | Sin.02 | Sin.02 | Sin.02 | LoadSoutE' | MAR.11' | 161 |
| 164 | Sin.03 | Sin.03 | Sin.03 | Sin.03 | Sin.03 | LoadSoutO' | MAR.03' | 164 |
| 165 | LoadSoutO' | LoadSoutE' | LoadSoutO' | LoadSoutE' | @BMux.09 | BMux.09 | BMux.09 | 165 |
| 168 | LoadEcOut' | LoadEcOut' | LoadEcOut' | LoadEcOut' | @BMux.01 | BMux.01 | BMux.01 | 168 |
| 169 | Mod1StrEn' | Mod1StrEn' | Mod0StrEn' | Mod0StrEn' | @BMux.08 | BMux.08 | BMux.08 | 169 |
| 172 | | | | | @BMux.00 | BMux.00 | BMux.00 | 172 |
| 173 | Sout.00 | Sout.00 | Sout.00 | Sout.00 | Sout.00 | BNTGtCT'a | | 173 |
| 176 | Sout.01 | Sout.01 | Sout.01 | Sout.01 | Sout.01 | Mod0StrEn' | | 176 |
| 177 | Sout.02 | Sout.02 | Sout.02 | Sout.02 | Sout.02 | Mod1StrEn' | MAR.10' | 177 |
| 180 | Sout.03 | Sout.03 | Sout.03 | Sout.03 | Sout.03 | Mod2StrEn' | MAR.02' | 180 |
| 181 | Gnd | Mb1 | Gnd | Mb0 | dPipe34Ad.0 | M0 | MAR.09' | 181 |
| 184 | Mb1 | M1 | Mb0 | M0 | dPipe34Ad.1 | M1 | MAR.01' | 184 |
| 185 | | | | | dPipe34Ad.2 | M2 | MAR.08' | 185 |
| 188 | | | | | | M3 | MAR.00' | 188 |
| Board Socket# | 13 | 12 | 11 | 10 | 9 | 8 | 7 | |

**File: BPRight02.sil**

**Dated: 7/24/80**

**By: Mike Overton**

RIGHT
(C)

p

*Even Pin#*

I/O Connector

* Jumper connection
to ContA board
for desired Task wake up

| Board Name | Dsk/Ether | MSA3-I/O | MSA3-I/O | MSA2-I/O | MSA2-I/O | |
|---|---|---|---|---|---|---|
| 5 | MemSH' | MemSH' | MemSH' | MemSH' | MemSH' | 5 |
| 8 | CLKEnable'a | CLKEnable'c | CLKEnable'b | CLKEnable'a | CLKEnable'c | 8 |
| 9 | CLK.disk' | CLK.ms3Odd' | CLK.ms3Even' | CLK.ms3Odd' | CLK.ms2Even' | 9 |
| 12 | IOB.00 | IOB.00 | IOB.00 | IOB.00 | IOB.00 | 12 |
| 13 | IOB.01 | IOB.01 | IOB.01 | IOB.01 | IOB.01 | 13 |
| 16 | IOB.02 | IOB.02 | IOB.02 | IOB.02 | IOB.02 | 16 |
| 17 | IOB.03 | IOB.03 | IOB.03 | IOB.03 | IOB.03 | 17 |
| 20 | IOB.04 | IOB.04 | IOB.04 | IOB.04 | IOB.04 | 20 |
| 21 | IOB.05 | IOB.05 | IOB.05 | IOB.05 | IOB.05 | 21 |
| 24 | IOB.06 | IOB.06 | IOB.06 | IOB.06 | IOB.06 | 24 |
| 25 | IOB.07 | IOB.07 | IOB.07 | IOB.07 | IOB.07 | 25 |
| 28 | Host.0 | @ Sout.08 | Sout.08 | Sout.08 | Sout.08 | 28 |
| 29 | Host.1 | Sout.09 | Sout.09 | Sout.09 | Sout.09 | 29 |
| 32 | Host.2 | Sout.10 | Sout.10 | Sout.10 | Sout.10 | 32 |
| 33 | Host.3 | @ Sout.11 | Sout.11 | Sout.11 | Sout.11 | 33 |
| 36 | Host.4 | Mod3SinEn' | Mod3SinEn' | Mod2SinEn' | Mod2SinEn' | 36 |
| 37 | Host.5 | @ LoadSinO | @ LoadSinE | LoadSinO | LoadSinE | 37 |
| 40 | Host.6 | ShiftSoutO | @ ShiftSoutE | ShiftSoutO | ShiftSoutE | 40 |
| 41 | Host.7 | ShiftEcOut | ShiftEcOut | ShiftEcOut | ShiftEcOut | 41 |
| 44 | RcvData | Sin.08 | Sin.08 | Sin.08 | Sin.08 | 44 |
| 45 | Collision | Sin.09 | Sin.09 | Sin.09 | Sin.09 | 45 |
| 48 | XmtData' | Sin.10 | Sin.10 | Sin.10 | Sin.10 | 48 |
| 49 | MemClkEn'a | @ Sin.11 | Sin.11 | Sin.11 | Sin.11 | 49 |
| 52 | IOB.16 | IOB.16 | IOB.16 | IOB.16 | IOB.16 | 52 |
| 53 | IOB.08 | IOB.08 | IOB.08 | IOB.08 | IOB.08 | 53 |
| 56 | IOB.09 | IOB.09 | IOB.09 | IOB.09 | IOB.09 | 56 |
| 57 | IOB.10 | IOB.10 | IOB.10 | IOB.10 | IOB.10 | 57 |
| 60 | IOB.11 | IOB.11 | IOB.11 | IOB.11 | IOB.11 | 60 |
| 61 | IOB.12 | IOB.12 | IOB.12 | IOB.12 | IOB.12 | 61 |
| 64 | IOB.13 | IOB.13 | IOB.13 | IOB.13 | IOB.13 | 64 |
| 65 | IOB.14 | IOB.14 | IOB.14 | IOB.14 | IOB.14 | 65 |
| 68 | IOB.15 | IOB.15 | IOB.15 | IOB.15 | IOB.15 | 68 |
| 69 | IOB.17 | IOB.17 | IOB.17 | IOB.17 | IOB.17 | 69 |
| 72 | Secindx0' | | | | | 72 |
| 73 | Selected0' | | | | | 73 |
| 76 | Select0' | | | | | 76 |
| 77 | Sequence0' | | | | | 77 |
| 80 | AlwsOnVCC | | | | | 80 |
| 81 | AlwsOnVCC | | | | | 81 |
| 84 | DataP0 | | | | | 84 |
| 85 | DataM0 | | | | | 85 |
| 88 | ClockP0 | | | | | 88 |
| 89 | ClockM0 | | | | | 89 |
| 92 | | | | | | 92 |
| 93 | Eth+5v | | | | | 93 |
| 96 | Secindx1' | | | | | 96 |
| 97 | Selected1' | | | | | 97 |
| 100 | Select1' | | | | | 100 |
| 101 | Sequence1' | | | | | 101 |
| 104 | AlwsOnVCC | | | | | 104 |
| 105 | AlwsOnVCC | | | | | 105 |
| 108 | DataP1 | | | | | 108 |
| 109 | DataM1 | | | | | 109 |
| 112 | ClockP1 | | | | | 112 |
| 113 | ClockM1 | | | | | 113 |
| 116 | | | | | | 116 |
| 117 | DiskTW | | | | | 117 |
| 120 | EthInTW | TWReq.xx* | TWReq.xx* | TWReq.xx* | TWReq.xx* | 120 |
| 121 | EthOutTW | TWReq.xx* | TWReq.xx* | TWReq.xx* | TWReq.xx* | 121 |
| 124 | TIOA.0 | TIOA.0 | TIOA.0 | TIOA.0 | TIOA.0 | 124 |
| 125 | TIOA.1 | TIOA.1 | TIOA.1 | TIOA.1 | TIOA.1 | 125 |
| 128 | TIOA.2 | TIOA.2 | TIOA.2 | TIOA.2 | TIOA.2 | 128 |
| 129 | TIOA.3 | TIOA.3 | TIOA.3 | TIOA.3 | TIOA.3 | 129 |
| 132 | TIOA.4 | TIOA.4 | TIOA.4 | TIOA.4 | TIOA.4 | 132 |
| 133 | TIOA.5 | TIOA.5 | TIOA.5 | TIOA.5 | TIOA.5 | 133 |
| 136 | TIOA.6 | TIOA.6 | TIOA.6 | TIOA.6 | TIOA.6 | 136 |
| 137 | TIOA.7 | TIOA.7 | TIOA.7 | TIOA.7 | TIOA.7 | 137 |
| 140 | Secindx2' | @ EcOut.2 | @ EcOut.0 | EcOut.2 | EcOut.0 | 140 |
| 141 | Selected2' | @ EcOut.6 | @ EcOut.4 | EcOut.6 | EcOut.4 | 141 |
| 144 | Select2' | | | | | 144 |
| 145 | Sequence2' | @ ShiftSinO | @ ShiftSinE | ShiftSinO | ShiftSinE | 145 |
| 148 | AlwsOnVCC | MemRASa | MemRASa | MemRASa | MemRASa | 148 |
| 149 | AlwsOnVCC | MemCASa | MemCASa | MemCASa | MemCASa | 149 |
| 152 | DataP2 | @ MemWEa | MemWEa | MemWEa | MemWEa | 152 |
| 153 | DataM2 | | | | | 153 |
| 156 | ClockP2 | @ EcIn.0 | EcIn.0 | EcIn.0 | EcIn.0 | 156 |
| 157 | ClockM2 | Sin.00 | Sin.00 | Sin.00 | Sin.00 | 157 |
| 160 | | Sin.01 | Sin.01 | Sin.01 | Sin.01 | 160 |
| 161 | | Sin.02 | Sin.02 | Sin.02 | Sin.02 | 161 |
| 164 | Secindx3' | Sin.03 | Sin.03 | Sin.03 | Sin.03 | 164 |
| 165 | Selected3' | LoadSoutO' | @ LoadSoutE' | LoadSoutO' | LoadSoutE' | 165 |
| 168 | Select3' | @ LoadEcOut' | LoadEcOut' | LoadEcOut' | LoadEcOut' | 168 |
| 169 | Sequence3' | Mod3StrEn' | Mod3StrEn' | Mod2StrEn' | Mod2StrEn' | 169 |
| 172 | AlwsOnVCC | | | | | 172 |
| 173 | AlwsOnVCC | @ Sout.00 | Sout.00 | Sout.00 | Sout.00 | 173 |
| 176 | DataP3 | Sout.01 | Sout.01 | Sout.01 | Sout.01 | 176 |
| 177 | DataM3 | Sout.02 | Sout.02 | Sout.02 | Sout.02 | 177 |
| 180 | ClockP3 | @ Sout.03 | Sout.03 | Sout.03 | Sout.03 | 180 |
| 181 | ClockM3 | Gnd | Mb3 | Gnd | Mb2 | 181 |
| 184 | | Mb3 | M3 | Mb2 | M2 | 184 |
| 185 | Pendulum | Pendulum | Pendulum | Pendulum | Pendulum | 185 |
| 188 | BNTGtCT'b | BNTGtCT'b | BNTGtCT'b | BNTGtCT'b | BNTGtCT'b | 188 |
| Board Socket# | 18 | 17 | 16 | 15 | 14 | |

**File: BPRight03.sil**

**Dated: 7/24/80**

**By: Mike Overton**

The Terminators at the end of slot24 are for the following:

StartCycle'b
CLKEnable'a
CLKEnable'c

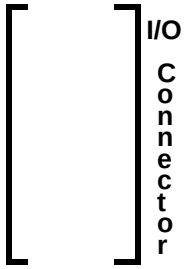
The Terminators between slots23&24 are for the following

StartCycle'a
CLKEnable'b

RIGHT
(C)

p

*Even Pin#*




* Jumper connection to ContA board for desired Task wake up

| Board Name | Fast I/O | Fast I/O | Fast I/O | Fast I/O | DispM | DispY | |
|---|---|---|---|---|---|---|---|
| 5 | @ MemSH' | MemSH' | MemSH' | MemSH' | MemSH' | MemSH' | 5 |
| 8 | @ CLKEnable'a | @ CLKEnable'c | @ CLKEnable'b | CLKEnable'a | CLKEnable'c | CLKEnable'b | 8 |
| 9 | CLK.io24' | CLK.io23' | CLK.io22' | CLK.io21' | CLK.io20' | CLK.display' | 9 |
| 12 | @ IOB.00 | IOB.00 | IOB.00 | IOB.00 | IOB.00 | IOB.00 | 12 |
| 13 | IOB.01 | IOB.01 | IOB.01 | IOB.01 | IOB.01 | IOB.01 | 13 |
| 16 | IOB.02 | IOB.02 | IOB.02 | IOB.02 | IOB.02 | IOB.02 | 16 |
| 17 | IOB.03 | IOB.03 | IOB.03 | IOB.03 | IOB.03 | IOB.03 | 17 |
| 20 | @ IOB.04 | IOB.04 | IOB.04 | IOB.04 | IOB.04 | IOB.04 | 20 |
| 21 | IOB.05 | IOB.05 | IOB.05 | IOB.05 | IOB.05 | IOB.05 | 21 |
| 24 | IOB.06 | IOB.06 | IOB.06 | IOB.06 | IOB.06 | IOB.06 | 24 |
| 25 | @ IOB.07 | IOB.07 | IOB.07 | IOB.07 | IOB.07 | IOB.07 | 25 |
| 28 | | | | | Modes.0 | Modes.0 | 28 |
| 29 | | | | | Modes.1 | Modes.1 | 29 |
| 32 | | | | | Modes.2 | Modes.2 | 32 |
| 33 | | | | | Modes.3 | Modes.3 | 33 |
| 36 | | | | | XHSync | XHSync | 36 |
| 37 | | | | | XYSync | XYSync | 37 |
| 40 | | | | | XSyncEn | XSyncEn | 40 |
| 41 | | | | | HSync | HSync | 41 |
| 44 | | | | | VSync | VSync | 44 |
| 45 | | | | | BOff | BOff | 45 |
| 48 | | | | | AOff | AOff | 48 |
| 49 | @ MemClkEn'b | MemClkEn'b | MemClkEn'b | MemClkEn'b | MemClkEn'b | @ MemClkEn'a | 49 |
| 52 | IOB.16 | IOB.16 | IOB.16 | IOB.16 | IOB.16 | IOB.16 | 52 |
| 53 | IOB.08 | IOB.08 | IOB.08 | IOB.08 | IOB.08 | IOB.08 | 53 |
| 56 | IOB.09 | IOB.09 | IOB.09 | IOB.09 | IOB.09 | IOB.09 | 56 |
| 57 | IOB.10 | IOB.10 | IOB.10 | IOB.10 | IOB.10 | IOB.10 | 57 |
| 60 | IOB.11 | IOB.11 | IOB.11 | IOB.11 | IOB.11 | IOB.11 | 60 |
| 61 | IOB.12 | IOB.12 | IOB.12 | IOB.12 | IOB.12 | IOB.12 | 61 |
| 64 | @ IOB.13 | IOB.13 | IOB.13 | IOB.13 | IOB.13 | IOB.13 | 64 |
| 65 | IOB.14 | IOB.14 | IOB.14 | IOB.14 | IOB.14 | IOB.14 | 65 |
| 68 | IOB.15 | IOB.15 | IOB.15 | IOB.15 | IOB.15 | IOB.15 | 68 |
| 69 | @ IOB.17 | IOB.17 | IOB.17 | IOB.17 | IOB.17 | IOB.17 | 69 |
| 72 | | | | | Video.1 | Video | 72 |
| 73 | | | | | HSync.1 | HSync | 73 |
| 76 | | | | | VSync'.1 | VSync' | 76 |
| 77 | | | | | CSync'.1 | CSync' | 77 |
| 80 | | | | | HBlank | HBlank | 80 |
| 81 | | | | | HalfLine | HalfLine | 81 |
| 84 | | | | | VBlank | VBlank | 84 |
| 85 | | | | | Altem.0 | Altem.0 | 85 |
| 88 | | | | | Altem.1 | Altem.1 | 88 |
| 89 | | | | | Altem.2 | Altem.2 | 89 |
| 92 | | | | | Altem.3 | Altem.3 | 92 |
| 93 | | | | | Altem.4 | Altem.4 | 93 |
| 96 | | | | | Altem.5 | Altem.5 | 96 |
| 97 | | | | | Altem.6 | Altem.6 | 97 |
| 100 | | | | | Altem.7 | Altem.7 | 100 |
| 101 | | | | | BItem.0 | BItem.0 | 101 |
| 104 | | | | | BItem.1 | BItem.1 | 104 |
| 105 | | | | | BItem.2 | BItem.2 | 105 |
| 108 | | | | | BItem.3 | BItem.3 | 108 |
| 109 | | | | | BItem.4 | BItem.4 | 109 |
| 112 | | | | | BItem.5 | BItem.5 | 112 |
| 113 | | | | | BItem.6 | BItem.6 | 113 |
| 116 | | | | | BItem.7 | BItem.7 | 116 |
| 117 | | | | | CursorData | CursorData | 117 |
| 120 | TWReq.xx* | TWReq.xx* | TWReq.xx* | TWReq.xx* | DispMwtTW | DispYwtTW | 120 |
| 121 | TWReq.xx* | TWReq.xx* | TWReq.xx* | TWReq.xx* | DispMhtTW | DispYhtTW | 121 |
| 124 | @ TIOA.0 | TIOA.0 | TIOA.0 | TIOA.0 | TIOA.0 | TIOA.0 | 124 |
| 125 | TIOA.1 | TIOA.1 | TIOA.1 | TIOA.1 | TIOA.1 | TIOA.1 | 125 |
| 128 | TIOA.2 | TIOA.2 | TIOA.2 | TIOA.2 | TIOA.2 | TIOA.2 | 128 |
| 129 | TIOA.3 | TIOA.3 | TIOA.3 | TIOA.3 | TIOA.3 | TIOA.3 | 129 |
| 132 | TIOA.4 | TIOA.4 | TIOA.4 | TIOA.4 | TIOA.4 | TIOA.4 | 132 |
| 133 | TIOA.5 | TIOA.5 | TIOA.5 | TIOA.5 | TIOA.5 | TIOA.5 | 133 |
| 136 | TIOA.6 | TIOA.6 | TIOA.6 | TIOA.6 | TIOA.6 | TIOA.6 | 136 |
| 137 | @ TIOA.7 | TIOA.7 | TIOA.7 | TIOA.7 | TIOA.7 | TIOA.7 | 137 |
| 140 | | | | | AltemClkEn | AltemClkEn | 140 |
| 141 | | | | | BItemClkEn | BItemClkEn | 141 |
| 144 | | | | | OISData.0 | OISData.0 | 144 |
| 145 | | | | | OISData.0' | OISData.0' | 145 |
| 148 | | | | | OISData.1 | OISData.1 | 148 |
| 149 | | | | | OISData.1' | OISData.1' | 149 |
| 152 | | | | | OISData.2 | OISData.2 | 152 |
| 153 | | | | | OISData.2' | OISData.2' | 153 |
| 156 | | | | | OISData.3 | OISData.3 | 156 |
| 157 | | | | | OISData.3' | OISData.3' | 157 |
| 160 | | | | | OISClkA' | OISClkA' | 160 |
| 161 | | | | | OISClkA | OISClkA | 161 |
| 164 | | | | | OISClkB | OISClkB | 164 |
| 165 | | | | | OISClkB' | OISClkB' | 165 |
| 168 | | | | | OISDataOut' | OISDataOut' | 168 |
| 169 | | | | | OISDataOut | OISDataOut | 169 |
| 172 | | | | | DAC | DAC | 172 |
| 173 | | | | | DACGnd | DACGnd | 173 |
| 176 | | | | | | | 176 |
| 177 | | | | | KBoardData | KBoardData | 177 |
| 180 | | | | | PixelClkVCO | PixelClkVCO | 180 |
| 181 | | | | | Crystal | Crystal | 181 |
| 184 | | | | | RawPixelClk | RawPixelClk | 184 |
| 185 | @ Pendulum | Pendulum | Pendulum | Pendulum | Pendulum | Pendulum | 185 |
| 188 | @ BNTGtCT'b | BNTGtCT'b | BNTGtCT'b | BNTGtCT'b | BNTGtCT'b | BNTGtCT'b | 188 |
| Board Socket# | 24 | 23 | 22 | 21 | 20 | 19 | |

**File: BPRight04.sil**

**Dated: 7/24/80**

**By: Mike Overton**

LEFT

(E)

P

*Odd Pin#*

I/O Connector

| Board Name | IFU | ProcH | ProcL | ContA | ContB | Base | |
|---|---|---|---|---|---|---|---|
| 6 | *EventC* | NEXT.0 | NEXT.0 | NEXT.0 | | | 6 |
| 7 | | NEXT.1 | NEXT.1 | NEXT.1 | | | 7 |
| 10 | | NEXT.2 | NEXT.2 | NEXT.2 | | | 10 |
| 11 | EmuOrFT' | NEXT.3 | NEXT.3 | NEXT.3 | | | 11 |
| 14 | MemBM.0 | MemBM.0 | SubTask.0 | ASEL.0'a | ASEL.0'a | | 14 |
| 15 | MemBM.1 | MemBM.1 | SubTask.1 | dFF.0 | dFF.0 | | 15 |
| 18 | | | _MD | dFF.1 | dFF.1 | | 18 |
| 19 | NextData' | NextData' | _MDI | BLOCK | ASEL.0 | | 19 |
| 22 | WantIfuHold' | ASEL.0' | ASEL.0' | CHoldReq | ASEL.0' | | 22 |
| 23 | ASEL.0' | ASEL.1' | ASEL.1' | WantIfuHold' | ASEL.1' | | 23 |
| 26 | | ASEL.2' | ASEL.2' | Hold | ASEL.2' | ACPI.0 | 26 |
| 27 | | ShcAlu.0 | ShcAlu.0 | dFF.3 | dFF.3 | ACPIGnd.0 | 27 |
| 30 | | ShcAlu.1 | ShcAlu.1 | dFF.4 | dFF.4 | ACPI.1 | 30 |
| 31 | | ShcAlu.2 | FF.ok'b | FF.ok'b | | ACPIGnd.1 | 31 |
| 34 | | FF.ok'a | ShcAlu.2 | FF.ok'a | | ACPI.2 | 34 |
| 35 | | ShcAlu.3 | ShcAlu.3 | dFF.2 | dFF.2 | ACPIGnd.2 | 35 |
| 38 | | Q.07 | Q.07 | dFF.5 | dFF.5 | ACPI.3 | 38 |
| 39 | | Q.08 | Q.08 | dFF.6 | dFF.6 | ACPIGnd.3 | 39 |
| 42 | | PRhold | PRhold | dFF.7 | dFF.7 | ACPI.4 | 42 |
| 43 | CountMiss | FF.0 | FF.0 | FF.0 | CBHold | ACPIGnd.4 | 43 |
| 46 | FF.2 | FF.2 | FF.2 | FF.2 | | | 46 |
| 47 | FF.3 | FF.3 | FF.3 | FF.3 | | | 47 |
| 50 | | FF.1 | FF.1 | FF.1 | | ACPBus.0' | 50 |
| 51 | | FF.0mem' | _MDI' | DoCBr | DoCBr | ACPGnd.00 | 51 |
| 54 | | FF.1mem | *LScopeFH* | dJCN.0 | dJCN.0 | ACPBus.1' | 54 |
| 55 | | | | dJCN.1 | dJCN.1 | ACPGnd.01 | 55 |
| 58 | | | | dJCN.2 | dJCN.2 | ACPBus.2' | 58 |
| 59 | | | | dJCN.3 | dJCN.3 | ACPGnd.02 | 59 |
| 62 | *EventD* | | | dJCN.4 | dJCN.4 | ACPBus.3' | 62 |
| 63 | MemBM34 | MemBM34 | IfuRBaseSel' | dJCN.5 | dJCN.5 | ACPGnd.03 | 63 |
| 66 | IfuRBaseSel' | alu=Zero' | alu=Zero' | RmLsZero' | | ACPBus.4' | 66 |
| 67 | IOReset | RmLsZero' | RmOdd' | RmOdd' | | ACPGnd.04 | 67 |
| 70 | TempRef | FA=0' | IOin' | dJCN.6 | dJCN.6 | ACPBus.5' | 70 |
| 71 | FA=1' | FA=1' | IOout' | dJCN.7 | dJCN.7 | ACPGnd.05 | 71 |
| 74 | FF.4 | FF.4 | FF.4 | FF.4 | | ACPBus.6' | 74 |
| 75 | FF.5 | FF.5 | FF.5 | FF.5 | | ACPGnd.06 | 75 |
| 78 | FF.6 | FF.6 | FF.6 | FF.6 | | ACPBus.7' | 78 |
| 79 | FF.7 | FF.7 | FF.7 | FF.7 | | ACPGnd.07 | 79 |
| 82 | IfuHold | Shc.02 | Shc.02 | dBLOCK' | dBLOCK' | ACPBus.8' | 82 |
| 83 | FG.8 | Shc.03 | Shc.03 | dIMRH | dIMRH | ACPGnd.08 | 83 |
| 86 | GDv' | MemBase.0 | SimHoldReq | TNIA.04 | TNIA.04 | ACPStrb' | 86 |
| 87 | PcFG.15 | MemBase.1 | PrHoldReq | TNIA.05 | TNIA.05 | ACPGnd.09 | 87 |
| 90 | EnableFG' | MemBase.2 | MemBase.2 | TNIA.06 | TNIA.06 | ACPABus.0' | 90 |
| 91 | GLd' | MemBase.3 | MemBase.3 | TNIA.07 | TNIA.07 | ACPGnd.10 | 91 |
| 94 | FG.0 | MemBase.4 | StkError | TNIA.08 | TNIA.08 | ACPABus.1' | 94 |
| 95 | FG.1 | | | TNIA.09 | TNIA.09 | ACPGnd.11 | 95 |
| 98 | FG.2 | | | TNIA.10 | TNIA.10 | ACPABus.2' | 98 |
| 99 | FG.3 | CkMdParity' | CkMdParity' | TNIA.11 | TNIA.11 | ACPGnd.12 | 99 |
| 102 | FG.4 | TempRef | TempRef | BNPC.04 | BNPC.04 | ACPBit13 | 102 |
| 103 | FG.5 | Shc.04b | Shc.04b | BNPC.05 | BNPC.05 | ACPGnd.13 | 103 |
| 106 | FG.6 | Shc.05b | Shc.05b | IfuAddr.04' | MemPE | ACPBit14 | 106 |
| 107 | IfuAddr.04' | BSEL.0' | BSEL.0' | BSEL.0' | BSEL.0' | ACPGnd.14 | 107 |
| 110 | FG.7 | BSEL.1' | BSEL.1' | IfuAddr.05' | BSEL.1' | | 110 |
| 111 | IfuAddr.05' | BSEL.2' | BSEL.2' | IfuAddr.06' | BSEL.2' | | 111 |
| 114 | IfuAddr.06' | Shc.06b | Shc.06b | IfuAddr.07' | | SkipWait' | 114 |
| 115 | IfuAddr.07' | MdPE | MdPE | IfuAddr.08' | MdPE | | 115 |
| 118 | IfuAddr.08' | RamPE | RamPE | IfuAddr.09' | RamPE | | 118 |
| 119 | IfuAddr.09' | IOPE | IOPE | IfuAddr.10' | IOPE | | 119 |
| 122 | IfuAddr.10' | Shc.07b | Shc.07b | BNPC.06 | BNPC.06 | | 122 |
| 123 | MakeF_D | Sha.00 | Sha.00 | BNPC.07 | BNPC.07 | TurnOnDisk' | 123 |
| 126 | IfuAddr.11' | LC.0 | LC.0 | IfuAddr.11' | LC.0 | DiskOnRet | 126 |
| 127 | IfuAddr.12' | LC.1 | LC.1 | IfuAddr.12' | LC.1 | | 127 |
| 130 | IfuAddr.13' | LC.2 | LC.2 | IfuAddr.13' | LC.2 | IOReset | 130 |
| 131 | WantIfuRef' | Sha.01 | Sha.01 | BNPC.08 | BNPC.08 | TTLIOReset' | 131 |
| 134 | IfuNextMacro' | Sha.02 | Sha.02 | BNPC.09 | BNPC.09 | | 134 |
| 135 | *StartMap'* | Sha.03 | Sha.03 | BNPC.10 | BNPC.10 | TempRef | 135 |
| 138 | *MapRfsh'* | Sha.04 | Sha.04 | IfuNextMacro' | TempRef | | 138 |
| 139 | *AwDifHit* | Sha.05 | Sha.05 | BNPC.11 | BNPC.11 | CIDD | 139 |
| 142 | | Sha.06 | Sha.06 | TNIA.12 | TNIA.12 | CIDDRet | 142 |
| 143 | | Sha.07 | Sha.07 | TNIA.13 | TNIA.13 | CICC | 143 |
| 146 | | aluCout | aluCout | TNIA.14 | TNIA.14 | CICCRet | 146 |
| 147 | | Sha.08 | Sha.08 | TNIA.15 | TNIA.15 | CITT | 147 |
| 150 | | Sha.09 | Sha.09 | BNPC.12 | BNPC.12 | CITTRet | 150 |
| 151 | | Sha.10 | Sha.10 | BNPC.13 | BNPC.13 | CIEE | 151 |
| 154 | | Sha.11 | Sha.11 | BNPC.14 | BNPC.14 | CIEERet | 154 |
| 155 | | NextMacro | NextMacro | NextMacro | | Serial.200 | 155 |
| 158 | | Sha.12 | Sha.12 | BNPC.15 | BNPC.15 | Serial.100 | 158 |
| 159 | | IOatt | jcnt | jcnt | | Serial.40 | 159 |
| 162 | | Sha.13 | Sha.13 | IOatt | | Serial.20 | 162 |
| 163 | | Sha.14 | Sha.14 | TNIA.02 | TNIA.02 | Serial.10 | 163 |
| 166 | | Sha.15 | Sha.15 | SW | SW | Serial.4 | 166 |
| 167 | | ALUF.0 | | SW' | TNIA.03 | Serial.2 | 167 |
| 170 | | ALUF.1 | ALUF.0 | TNIA.03 | ALUF.0 | Serial.1 | 170 |
| 171 | | ResEqZero' | ALUF.1 | ResEqZero' | ALUF.1 | PwrOnRet | 171 |
| 174 | | ResGeZero' | ALUF.2 | ResGeZero' | ALUF.2 | TurnOnPwr' | 174 |
| 175 | | Overflow' | ALUF.3 | Overflow' | ALUF.3 | TurnOnLED' | 175 |
| 178 | *EventE* | ALUF.2 | | BNPC.02 | BNPC.02 | LEDOnRet | 178 |
| 179 | | AluCarry | AluCarry | AluCarry | *IMLHPEdly* | BootMC | 179 |
| 182 | | Cnt=Zero' | Cnt=Zero' | Cnt=Zero' | *IMRHPEdly* | TurnOff2v | 182 |
| 183 | IfuAck' | DecCnt' | DecCnt' | BNPC.03 | BNPC.03 | | 183 |
| 186 | DmuxData | DmuxData | DmuxData | DmuxData | DmuxData | DmuxData | 186 |
| 187 | DmuxCLK | DmuxCLK | DmuxCLK | DmuxCLK | DmuxCLK | DmuxCLK | 187 |
| Board Socket# | 6 | 5 | 4 | 3 | 2 | 1 | |

**File: BPLeft01.sil**

**Dated: 7/24/80**

**By: Mike Overton**

LEFT

(E)

P

Odd pin# C A I/O Connector

| Board Name | MSA1Odd | MSA1Even | MSA0Odd | MSA0Even | MemD | MemX | MemC | |
|---|---|---|---|---|---|---|---|---|
| 6 | | | | | | NEXT.0 | ExtHoldReq | 6 |
| 7 | | | | | | NEXT.1 | DisHold | 7 |
| 10 | | | | | McrD_' | NEXT.2 | McrD_' | 10 |
| 11 | | | | | | NEXT.3 | FF.0mem' | 11 |
| 14 | | | | | | SubTask.0 | EmuOrFT' | 14 |
| 15 | | | | | | SubTask.1 | ASEL.0 | 15 |
| 18 | | | | | | _MD | _MD | 18 |
| 19 | Sout.07 | Sout.07 | Sout.07 | Sout.07 | Sout.07 | FinTsk.0 | _MDI | 19 |
| 22 | Sout.06 | Sout.06 | Sout.06 | Sout.06 | Sout.06 | FinTsk.1 | FF.1mem | 22 |
| 23 | Sout.05 | Sout.05 | Sout.05 | Sout.05 | Sout.05 | FinTsk.2 | @ASEL.1' | 23 |
| 26 | Sout.04 | Sout.04 | Sout.04 | Sout.04 | Sout.04 | FinTsk.3 | @ASEL.2' | 26 |
| 27 | Sin.07 | Sin.07 | Sin.07 | Sin.07 | Sin.07 | FinSubT.0 | Hold | 27 |
| 30 | Sin.06 | Sin.06 | Sin.06 | Sin.06 | Sin.06 | FinSubT.1 | CBHold | 30 |
| 31 | Sin.05 | Sin.05 | Sin.05 | Sin.05 | Sin.05 | MXHold | MXHold | 31 |
| 34 | Sin.04 | Sin.04 | Sin.04 | Sin.04 | Sin.04 | ProcTag | ProcTag | 34 |
| 35 | EcIn.1 | EcIn.1 | EcIn.1 | EcIn.1 | EcIn.1 | MDMtag' | MDMtag' | 35 |
| 38 | | | | | Fin.17 | At=Curt' | At=Curt' | 38 |
| 39 | | | | | Fin.15 | DCForCt' | DCForCt' | 39 |
| 42 | | | | | Fin.14 | EmuOrFT' | PRhold | 42 |
| 43 | | | | | Fin.13 | CountMiss | | 43 |
| 46 | MemAd.1 | MemAd.1 | MemAd.1 | MemAd.1 | Fin.12 | MemAd.1 | @FF.2 | 46 |
| 47 | MemAd.2 | MemAd.2 | MemAd.2 | MemAd.2 | Fin.11 | MemAd.2 | @FF.3 | 47 |
| 50 | | | | | Fin.10 | UseAsrn | UseAsrn | 50 |
| 51 | ChipsAre4k | ChipsAre4k | ChipsAre4k | ChipsAre4k | Fin.09 | ChipsAre4k | _MDI' | 51 |
| 54 | ChipsAre16k | ChipsAre16k | ChipsAre16k | ChipsAre16k | Fin.08 | ChipsAre16k | VicOrFS1C | 54 |
| 55 | ChipsAre64k | ChipsAre64k | ChipsAre64k | ChipsAre64k | Fin.07 | ChipsAre64k | CHoldreq | 55 |
| 58 | MemAd.3 | MemAd.3 | MemAd.3 | MemAd.3 | Fin.06 | MemAd.3 | CacheRef' | 58 |
| 59 | MemAd.4 | MemAd.4 | MemAd.4 | MemAd.4 | Fin.05 | MemAd.4 | MakeD_CD | 59 |
| 62 | MemCASb | MemCASb | MemCASb | MemCASb | Fin.04 | MemCASb | _MDdly' | 62 |
| 63 | MemRASb | MemRASb | MemRASb | MemRASb | Fin.03 | MemRASb | PairFull' | 63 |
| 66 | EcOut.7 | EcOut.5 | EcOut.7 | EcOut.5 | Fin.02 | StartMap' | StartMap' | 66 |
| 67 | EcOut.3 | EcOut.1 | EcOut.3 | EcOut.1 | Fin.01 | FinNext | IOhold | 67 |
| 70 | | | | | Fin.00 | CacheRef' | | 70 |
| 71 | | | | | Fin.16 | VicOrFS1C | FA=1' | 71 |
| 74 | | | | | EcOut.7 | _MDdly' | @FF.4 | 74 |
| 75 | | | | | EcOut.5 | PairFull' | @FF.5 | 75 |
| 78 | | | | | EcOut.3 | DisHold | @FF.6 | 78 |
| 79 | | | | | EcOut.1 | MapAd.8 | @FF.7 | 79 |
| 82 | | | | | | MakeD_CD | IfuHold | 82 |
| 83 | | | | | MakeD_CD | AchMap' | AchMap' | 83 |
| 86 | | | | | MakeMD_D' | MakeMD_D' | MemBase.0 | 86 |
| 87 | | | | | MakeMDM_D' | MakeMDM_D' | MemBase.1 | 87 |
| 90 | | | | | MakeSout_D | MakeSout_D | MemBase.2 | 90 |
| 91 | | | | | MakeFout_D | MakeFout_D | MemBase.3 | 91 |
| 94 | | | | | FG.0 | MemPE | MemBase.4 | 94 |
| 95 | | | | | FG.1 | StkError | PrHoldReq | 95 |
| 98 | | | | | FG.2 | MapAd.1 | MapAd.1 | 98 |
| 99 | | | | | FG.3 | MapAd.0 | MapAd.0 | 99 |
| 102 | | | | | FG.4 | MapRfsh' | MapRfsh' | 102 |
| 103 | | | | | FG.5 | IoFetchInA' | IoFetchInA' | 103 |
| 106 | | | | | FG.6 | MapAd.2 | MapAd.2 | 106 |
| 107 | | | | | FG.7 | MapAd.3 | MapAd.3 | 107 |
| 110 | | | | | FG.8 | MapAd.4 | MapAd.4 | 110 |
| 111 | | | | | GDv' | MapAd.5 | MapAd.5 | 111 |
| 114 | | | | | PcFG.15 | Hita | Hita | 114 |
| 115 | | | | | EnableFG' | MemColSel | MemColSel | 115 |
| 118 | | | | | GLd' | MapAd.6 | MapAd.6 | 118 |
| 119 | | | | | | MapAd.7 | MapAd.7 | 119 |
| 122 | | | | | TempRef | Transport' | Transport' | 122 |
| 123 | | | | | Transport' | FoutNext | MapAd.8 | 123 |
| 126 | | | | | MakeD_Dbuf | XWantsPipe | XWantsPipe | 126 |
| 127 | | | | | MakeF_D | MakeF_D | MakeF_D | 127 |
| 130 | | | | | FastD_Dbuf | Fout.flt | FastD_Dbuf | 130 |
| 131 | MemWEb | MemWEb | MemWEb | MemWEb | Dbuf_' | MemWEb | WantIfuRef' | 131 |
| 134 | MemAd.5 | MemAd.5 | MemAd.5 | MemAd.5 | Fout.17 | MemAd.5 | MemAd.5 | 134 |
| 135 | MemAd.6 | MemAd.6 | MemAd.6 | MemAd.6 | Fout.15 | MemAd.6 | MemAd.6 | 135 |
| 138 | MemAd.7 | MemAd.7 | MemAd.7 | MemAd.7 | Fout.14 | MemAd.7 | MemAd.7 | 138 |
| 139 | MemAd.8 | MemAd.8 | MemAd.8 | MemAd.8 | Fout.13 | MemAd.8 | MemAd.8 | 139 |
| 142 | | | | | Fout.12 | EcWantsA | EcWantsA | 142 |
| 143 | | | | | Fout.11 | ReadInA' | ReadInA' | 143 |
| 146 | | | | | Fout.10 | LdPipeVAdly' | LdPipeVAdly' | 146 |
| 147 | | | | | Fout.09 | VicInPair' | VicInPair' | 147 |
| 150 | | | | | Fout.08 | dPipe02Ad.0 | dPipe02Ad.0 | 150 |
| 151 | | | | | Fout.07 | dPipe02Ad.1 | dPipe02Ad.1 | 151 |
| 154 | | | | | Fout.06 | dPipe02Ad.2 | dPipe02Ad.2 | 154 |
| 155 | Sin.15 | Sin.15 | Sin.15 | Sin.15 | Fout.05 | dPipe02Ad.3 | dPipe02Ad.3 | 155 |
| 158 | Sin.14 | Sin.14 | Sin.14 | Sin.14 | Sin.15 | STfree' | STfree' | 158 |
| 159 | | | | | Sin.14 | IOStoreInA | IOStoreInA | 159 |
| 162 | Sin.13 | Sin.13 | Sin.13 | Sin.13 | Sin.13 | AfreeOrEc'b | AfreeOrEc'b | 162 |
| 163 | Sin.12 | Sin.12 | Sin.12 | Sin.12 | Sin.12 | MapWait-D | MapWait-D | 163 |
| 166 | | | | | Fout.04 | MakeD_Dbuf | MakeD_Dbuf | 166 |
| 167 | | | | | Fout.03 | MemRfsh | MemRfsh | 167 |
| 170 | | | | | Fout.02 | SW' | Dbuf_' | 170 |
| 171 | | | | | Fout.01 | AwDifHit' | AwDifHit' | 171 |
| 174 | | | | | Fout.00 | FoutSubT.0 | | 174 |
| 175 | | | | | Fout.16 | FoutSubT.1 | | 175 |
| 178 | Sout.15 | Sout.15 | Sout.15 | Sout.15 | Sout.15 | FoutTsk.0 | | 178 |
| 179 | Sout.14 | Sout.14 | Sout.14 | Sout.14 | Sout.14 | FoutTsk.1 | | 179 |
| 182 | Sout.13 | Sout.13 | Sout.13 | Sout.13 | Sout.13 | FoutTsk.2 | | 182 |
| 183 | Sout.12 | Sout.12 | Sout.12 | Sout.12 | Sout.12 | FoutTsk.3 | IfuAck' | 183 |
| 186 | | | | | DmuxData | DmuxData | DmuxData | 186 |
| 187 | | | | | DmuxCLK | DmuxCLK | DmuxCLK | 187 |
| Board Socket# | 13 | 12 | 11 | 10 | 9 | 8 | 7 | |

File: BPLeft02.sil

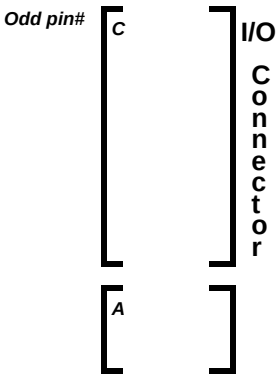
Dated: 7/24/80

By: Mike Overton

LEFT

(E)

P

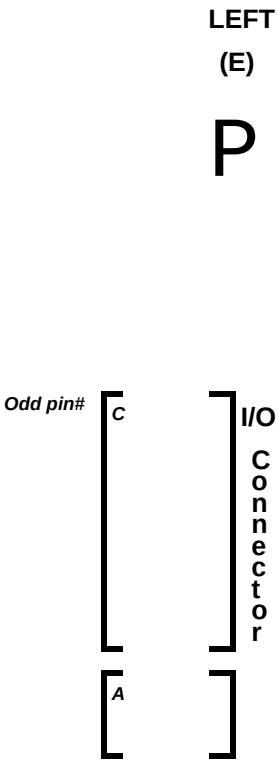



| Board Name | Dsk/Ether | MSA3-I/O | MSA3-I/O | MSA2-I/O | MSA2-I/O | |
|---|---|---|---|---|---|---|
| 6 | NEXT.0 | NEXT.0 | NEXT.0 | NEXT.0 | NEXT.0 | 6 |
| 7 | NEXT.1 | NEXT.1 | NEXT.1 | NEXT.1 | NEXT.1 | 7 |
| 10 | NEXT.2 | NEXT.2 | NEXT.2 | NEXT.2 | NEXT.2 | 10 |
| 11 | NEXT.3 | NEXT.3 | NEXT.3 | NEXT.3 | NEXT.3 | 11 |
| 14 | SubTask.0 | SubTask.0 | SubTask.0 | SubTask.0 | SubTask.0 | 14 |
| 15 | SubTask.1 | SubTask.1 | SubTask.1 | SubTask.1 | SubTask.1 | 15 |
| 18 | BLOCK | BLOCK | BLOCK | BLOCK | BLOCK | 18 |
| 19 | FinTsk.0 | @Sout.07 | Sout.07 | Sout.07 | Sout.07 | 19 |
| 22 | FinTsk.1 | @Sout.06 | Sout.06 | Sout.06 | Sout.06 | 22 |
| 23 | FinTsk.2 | @Sout.05 | Sout.05 | Sout.05 | Sout.05 | 23 |
| 26 | FinTsk.3 | @Sout.04 | Sout.04 | Sout.04 | Sout.04 | 26 |
| 27 | FinSubT.0 | @Sin.07 | Sin.07 | Sin.07 | Sin.07 | 27 |
| 30 | FinSubT.1 | @Sin.06 | Sin.06 | Sin.06 | Sin.06 | 30 |
| 31 | Fin.17 | @Sin.05 | Sin.05 | Sin.05 | Sin.05 | 31 |
| 34 | Fin.15 | @Sin.04 | Sin.04 | Sin.04 | Sin.04 | 34 |
| 35 | Fin.14 | @EcIn.1 | EcIn.1 | EcIn.1 | EcIn.1 | 35 |
| 38 | Fin.13 | | | | | 38 |
| 39 | Fin.12 | | | | | 39 |
| 42 | Fin.11 | | | | | 42 |
| 43 | Fin.10 | | | | | 43 |
| 46 | Fin.09 | @MemAd.1 | MemAd.1 | MemAd.1 | MemAd.1 | 46 |
| 47 | Fin.08 | @MemAd.2 | MemAd.2 | MemAd.2 | MemAd.2 | 47 |
| 50 | Fin.07 | | | | | 50 |
| 51 | Fin.06 | @ChipsAre4k | ChipsAre4k | ChipsAre4k | ChipsAre4k | 51 |
| 54 | Fin.05 | @ChipsAre16k | ChipsAre16k | ChipsAre16k | ChipsAre16k | 54 |
| 55 | Fin.04 | @ChipsAre64k | ChipsAre64k | ChipsAre64k | ChipsAre64k | 55 |
| 58 | Fin.03 | @MemAd.3 | MemAd.3 | MemAd.3 | MemAd.3 | 58 |
| 59 | Fin.02 | @MemAd.4 | MemAd.4 | MemAd.4 | MemAd.4 | 59 |
| 62 | Fin.01 | @MemCASb | MemCASb | MemCASb | MemCASb | 62 |
| 63 | Fin.00 | @MemRASb | MemRASb | MemRASb | MemRASb | 63 |
| 66 | Fin.16 | @EcOut.7 | @EcOut.5 | EcOut.7 | EcOut.5 | 66 |
| 67 | FinNext | @EcOut.3 | @EcOut.1 | EcOut.3 | EcOut.1 | 67 |
| 70 | IOhold | IOhold | IOhold | IOhold | IOhold | 70 |
| 71 | IOin' | IOin' | IOin' | IOin' | IOin' | 71 |
| 74 | IOout' | IOout' | IOout' | IOout' | IOout' | 74 |
| 75 | | | | | | 75 |
| 78 | TtlIndex' | | | | | 78 |
| 79 | TtlReady' | | | | | 79 |
| 82 | TtlOnLine' | | | | | 82 |
| 83 | TtlDevChk' | | | | | 83 |
| 86 | TtlSeekInc' | | | | | 86 |
| 87 | TtlEndOfCyl' | | | | | 87 |
| 90 | TtlTerm' | | | | | 90 |
| 91 | TtlReadOnly' | | | | | 91 |
| 94 | TtlOffSet' | | | | | 94 |
| 95 | DriveTag' | | | | | 95 |
| 98 | CylinderTag' | | | | | 98 |
| 99 | HeadTag' | | | | | 99 |
| 102 | ContTag' | | | | | 102 |
| 103 | TagBus.9' | | | | | 103 |
| 106 | TagBus.8' | | | | | 106 |
| 107 | TagBus.7' | | | | | 107 |
| 110 | TagBus.6' | | | | | 110 |
| 111 | TagBus.5' | | | | | 111 |
| 114 | TagBus.4' | | | | | 114 |
| 115 | TagBus.3' | | | | | 115 |
| 118 | TagBus.2' | | | | | 118 |
| 119 | TagBus.1' | | | | | 119 |
| 122 | TagBus.0' | | | | | 122 |
| 123 | TagBus.00' | | | | | 123 |
| 126 | | | | | | 126 |
| 127 | TempRef | | | | | 127 |
| 130 | IOReset | IOReset | IOReset | IOReset | IOReset | 130 |
| 131 | FoutNext | @MemWEb | MemWEb | MemWEb | MemWEb | 131 |
| 134 | Fout.flt | @MemAd.5 | MemAd.5 | MemAd.5 | MemAd.5 | 134 |
| 135 | Fout.17 | @MemAd.6 | MemAd.6 | MemAd.6 | MemAd.6 | 135 |
| 138 | Fout.15 | @MemAd.7 | MemAd.7 | MemAd.7 | MemAd.7 | 138 |
| 139 | Fout.14 | @MemAd.8 | MemAd.8 | MemAd.8 | MemAd.8 | 139 |
| 142 | Fout.13 | | | | | 142 |
| 143 | Fout.12 | | | | | 143 |
| 146 | Fout.11 | | | | | 146 |
| 147 | Fout.10 | | | | | 147 |
| 150 | Fout.09 | | | | | 150 |
| 151 | Fout.08 | | | | | 151 |
| 154 | Fout.07 | | | | | 154 |
| 155 | Fout.06 | @Sin.15 | Sin.15 | Sin.15 | Sin.15 | 155 |
| 158 | Fout.05 | @Sin.14 | Sin.14 | Sin.14 | Sin.14 | 158 |
| 159 | IOatt | IOatt | IOatt | IOatt | IOatt | 159 |
| 162 | Fout.04 | @Sin.13 | Sin.13 | Sin.13 | Sin.13 | 162 |
| 163 | Fout.03 | @Sin.12 | Sin.12 | Sin.12 | Sin.12 | 163 |
| 166 | Fout.02 | | | | | 166 |
| 167 | Fout.01 | | | | | 167 |
| 170 | Fout.00 | | | | | 170 |
| 171 | Fout.16 | | | | | 171 |
| 174 | FoutSubT.0 | | | | | 174 |
| 175 | FoutSubT.1 | | | | | 175 |
| 178 | FoutTsk.0 | @Sout.15 | Sout.15 | Sout.15 | Sout.15 | 178 |
| 179 | FoutTsk.1 | @Sout.14 | Sout.14 | Sout.14 | Sout.14 | 179 |
| 182 | FoutTsk.2 | @Sout.13 | Sout.13 | Sout.13 | Sout.13 | 182 |
| 183 | FoutTsk.3 | @Sout.12 | Sout.12 | Sout.12 | Sout.12 | 183 |
| 186 | DmuxData | DmuxData | DmuxData | DmuxData | DmuxData | 186 |
| 187 | DmuxCLK | DmuxCLK | DmuxCLK | DmuxCLK | DmuxCLK | 187 |
| Board Socket# | 18 | 17 | 16 | 15 | 14 | |

**File: BPLeft03.sil**

**Dated: 7/24/80**

**By: Mike Overton**




| Board Name | Fast I/O | Fast I/O | Fast I/O | Fast I/O | DispM | DispY | |
|---|---|---|---|---|---|---|---|
| 6 | @NEXT.0 | NEXT.0 | NEXT.0 | NEXT.0 | NEXT.0 | NEXT.0 | 6 |
| 7 | NEXT.1 | NEXT.1 | NEXT.1 | NEXT.1 | NEXT.1 | NEXT.1 | 7 |
| 10 | NEXT.2 | NEXT.2 | NEXT.2 | NEXT.2 | NEXT.2 | NEXT.2 | 10 |
| 11 | NEXT.3 | NEXT.3 | NEXT.3 | NEXT.3 | NEXT.3 | NEXT.3 | 11 |
| 14 | SubTask.0 | SubTask.0 | SubTask.0 | SubTask.0 | SubTask.0 | SubTask.0 | 14 |
| 15 | SubTask.1 | SubTask.1 | SubTask.1 | SubTask.1 | SubTask.1 | SubTask.1 | 15 |
| 18 | BLOCK | BLOCK | BLOCK | BLOCK | BLOCK | BLOCK | 18 |
| 19 | @FinTsk.0 | FinTsk.0 | FinTsk.0 | FinTsk.0 | FinTsk.0 | FinTsk.0 | 19 |
| 22 | FinTsk.1 | FinTsk.1 | FinTsk.1 | FinTsk.1 | FinTsk.1 | FinTsk.1 | 22 |
| 23 | **FinTsk.2** | **FinTsk.2** | **FinTsk.2** | **FinTsk.2** | **FinTsk.2** | **FinTsk.2** | 23 |
| 26 | FinTsk.3 | FinTsk.3 | FinTsk.3 | FinTsk.3 | FinTsk.3 | FinTsk.3 | 26 |
| 27 | FinSubT.0 | FinSubT.0 | FinSubT.0 | FinSubT.0 | FinSubT.0 | FinSubT.0 | 27 |
| 30 | FinSubT.1 | FinSubT.1 | FinSubT.1 | FinSubT.1 | FinSubT.1 | FinSubT.1 | 30 |
| 31 | Fin.17 | Fin.17 | Fin.17 | Fin.17 | Fin.17 | Fin.17 | 31 |
| 34 | @Fin.15 | Fin.15 | Fin.15 | Fin.15 | Fin.15 | Fin.15 | 34 |
| 35 | Fin.14 | Fin.14 | Fin.14 | Fin.14 | Fin.14 | Fin.14 | 35 |
| 38 | Fin.13 | Fin.13 | Fin.13 | Fin.13 | Fin.13 | Fin.13 | 38 |
| 39 | Fin.12 | Fin.12 | Fin.12 | Fin.12 | Fin.12 | Fin.12 | 39 |
| 42 | Fin.11 | Fin.11 | Fin.11 | Fin.11 | Fin.11 | Fin.11 | 42 |
| 43 | Fin.10 | Fin.10 | Fin.10 | Fin.10 | Fin.10 | Fin.10 | 43 |
| 46 | Fin.09 | Fin.09 | Fin.09 | Fin.09 | Fin.09 | Fin.09 | 46 |
| 47 | @Fin.08 | Fin.08 | Fin.08 | Fin.08 | Fin.08 | Fin.08 | 47 |
| 50 | Fin.07 | Fin.07 | Fin.07 | Fin.07 | Fin.07 | Fin.07 | 50 |
| 51 | Fin.06 | Fin.06 | Fin.06 | Fin.06 | Fin.06 | Fin.06 | 51 |
| 54 | Fin.05 | Fin.05 | Fin.05 | Fin.05 | Fin.05 | Fin.05 | 54 |
| 55 | Fin.04 | Fin.04 | Fin.04 | Fin.04 | Fin.04 | Fin.04 | 55 |
| 58 | Fin.03 | Fin.03 | Fin.03 | Fin.03 | Fin.03 | Fin.03 | 58 |
| 59 | Fin.02 | Fin.02 | Fin.02 | Fin.02 | Fin.02 | Fin.02 | 59 |
| 62 | @Fin.01 | Fin.01 | Fin.01 | Fin.01 | Fin.01 | Fin.01 | 62 |
| 63 | Fin.00 | Fin.00 | Fin.00 | Fin.00 | Fin.00 | Fin.00 | 63 |
| 66 | Fin.16 | Fin.16 | Fin.16 | Fin.16 | Fin.16 | Fin.16 | 66 |
| 67 | FinNext | FinNext | FinNext | FinNext | FinNext | FinNext | 67 |
| 70 | IOhold | IOhold | IOhold | IOhold | IOhold | IOhold | 70 |
| 71 | IOin' | IOin' | IOin' | IOin' | IOin' | IOin' | 71 |
| 74 | @IOout' | IOout' | IOout' | IOout' | IOout' | IOout' | 74 |
| 75 | | | | | | | 75 |
| 78 | | | | | | | 78 |
| 79 | | | | | | | 79 |
| 82 | | | | | | | 82 |
| 83 | | | | | | | 83 |
| 86 | | | | | | | 86 |
| 87 | | | | | | | 87 |
| 90 | | | | | | | 90 |
| 91 | | | | | | | 91 |
| 94 | | | | | | | 94 |
| 95 | | | | | TTLCSync' | | 95 |
| 98 | | | | | TTLCSync'Gnd | | 98 |
| 99 | | | | | | | 99 |
| 102 | | | | | RedGnd | | 102 |
| 103 | | | | | Red | | 103 |
| 106 | | | | | | | 106 |
| 107 | | | | | | | 107 |
| 110 | | | | | GreenGnd | | 110 |
| 111 | | | | | Green | | 111 |
| 114 | | | | | | | 114 |
| 115 | | | | | | | 115 |
| 118 | | | | | BlueGnd | | 118 |
| 119 | | | | | Blue | | 119 |
| 122 | | | | | | | 122 |
| 123 | | | | | | | 123 |
| 126 | | | | | | | 126 |
| 127 | | | | | | | 127 |
| 130 | @IOReset | IOReset | IOReset | IOReset | IOReset | IOReset | 130 |
| 131 | FoutNext | FoutNext | FoutNext | FoutNext | FoutNext | FoutNext | 131 |
| 134 | Fout.flt | Fout.flt | Fout.flt | Fout.flt | Fout.flt | Fout.flt | 134 |
| 135 | Fout.17 | Fout.17 | Fout.17 | Fout.17 | Fout.17 | Fout.17 | 135 |
| 138 | Fout.15 | Fout.15 | Fout.15 | Fout.15 | Fout.15 | Fout.15 | 138 |
| 139 | Fout.14 | Fout.14 | Fout.14 | Fout.14 | Fout.14 | Fout.14 | 139 |
| 142 | Fout.13 | Fout.13 | Fout.13 | Fout.13 | Fout.13 | Fout.13 | 142 |
| 143 | @Fout.12 | Fout.12 | Fout.12 | Fout.12 | Fout.12 | Fout.12 | 143 |
| 146 | Fout.11 | Fout.11 | Fout.11 | Fout.11 | Fout.11 | Fout.11 | 146 |
| 147 | Fout.10 | Fout.10 | Fout.10 | Fout.10 | Fout.10 | Fout.10 | 147 |
| 150 | Fout.09 | Fout.09 | Fout.09 | Fout.09 | Fout.09 | Fout.09 | 150 |
| 151 | Fout.08 | Fout.08 | Fout.08 | Fout.08 | Fout.08 | Fout.08 | 151 |
| 154 | Fout.07 | Fout.07 | Fout.07 | Fout.07 | Fout.07 | Fout.07 | 154 |
| 155 | Fout.06 | Fout.06 | Fout.06 | Fout.06 | Fout.06 | Fout.06 | 155 |
| 158 | @Fout.05 | Fout.05 | Fout.05 | Fout.05 | Fout.05 | Fout.05 | 158 |
| 159 | IOatt | IOatt | IOatt | IOatt | IOatt | IOatt | 159 |
| 162 | Fout.04 | Fout.04 | Fout.04 | Fout.04 | Fout.04 | Fout.04 | 162 |
| 163 | Fout.03 | Fout.03 | Fout.03 | Fout.03 | Fout.03 | Fout.03 | 163 |
| 166 | Fout.02 | Fout.02 | Fout.02 | Fout.02 | Fout.02 | Fout.02 | 166 |
| 167 | Fout.01 | Fout.01 | Fout.01 | Fout.01 | Fout.01 | Fout.01 | 167 |
| 170 | Fout.00 | Fout.00 | Fout.00 | Fout.00 | Fout.00 | Fout.00 | 170 |
| 171 | @Fout.16 | Fout.16 | Fout.16 | Fout.16 | Fout.16 | Fout.16 | 171 |
| 174 | FoutSubT.0 | FoutSubT.0 | FoutSubT.0 | FoutSubT.0 | FoutSubT.0 | FoutSubT.0 | 174 |
| 175 | FoutSubT.1 | FoutSubT.1 | FoutSubT.1 | FoutSubT.1 | FoutSubT.1 | FoutSubT.1 | 175 |
| 178 | FoutTsk.0 | FoutTsk.0 | FoutTsk.0 | FoutTsk.0 | FoutTsk.0 | FoutTsk.0 | 178 |
| 179 | FoutTsk.1 | FoutTsk.1 | FoutTsk.1 | FoutTsk.1 | FoutTsk.1 | FoutTsk.1 | 179 |
| 182 | FoutTsk.2 | FoutTsk.2 | FoutTsk.2 | FoutTsk.2 | FoutTsk.2 | FoutTsk.2 | 182 |
| 183 | FoutTsk.3 | FoutTsk.3 | FoutTsk.3 | FoutTsk.3 | FoutTsk.3 | FoutTsk.3 | 183 |
| 186 | @DmuxData | DmuxData | DmuxData | DmuxData | DmuxData | DmuxData | 186 |
| 187 | @DmuxCLK | DmuxCLK | DmuxCLK | DmuxCLK | DmuxCLK | DmuxCLK | 187 |
| Board Socket# | 24 | 23 | 22 | 21 | 20 | 19 | |

**File: BPLeft04.sil**

**Dated: 7/24/80**

**By: Mike Overton**