D O R A D O S C H E M A T I C S

L o w B y t e

P R O C E S S O R

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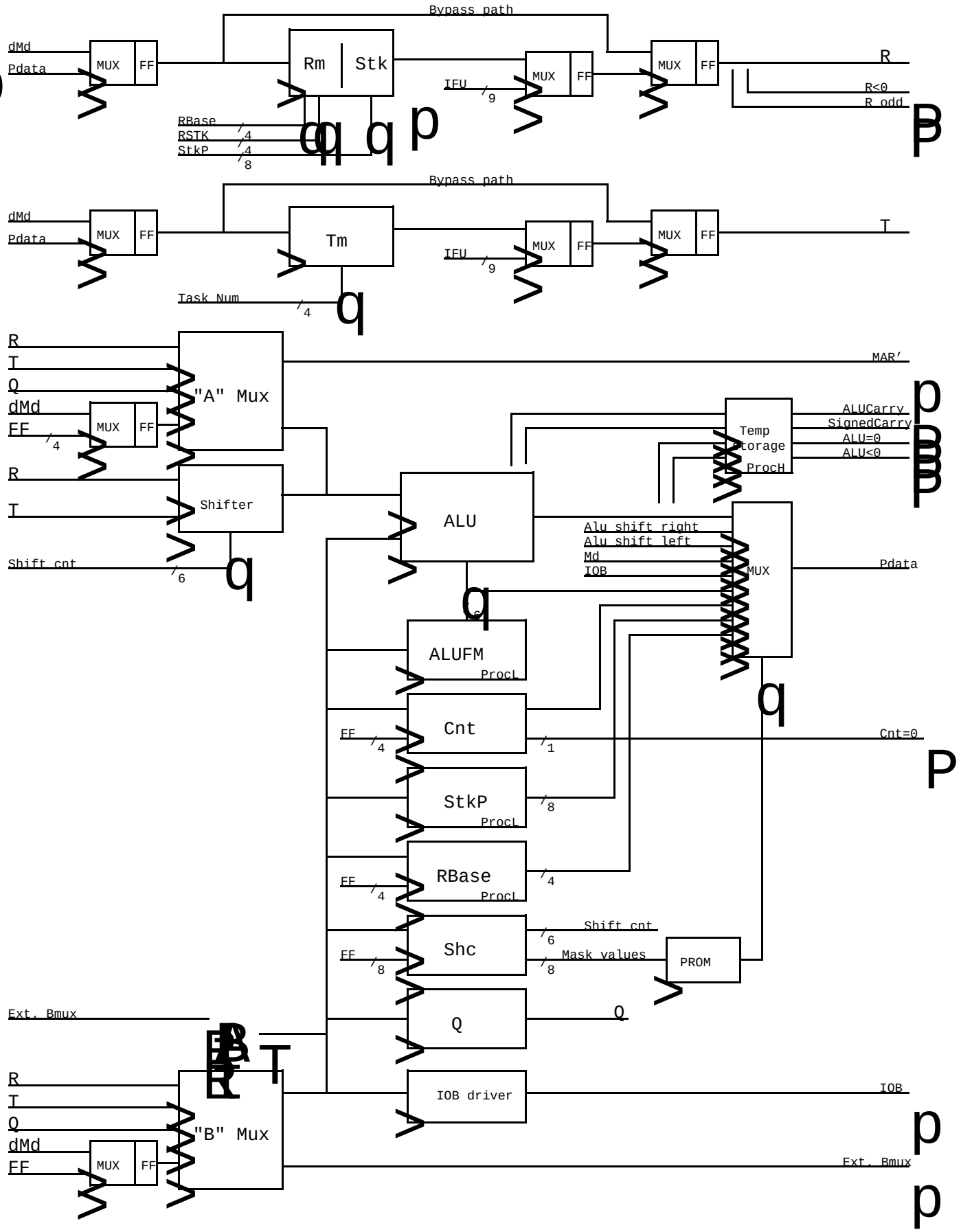
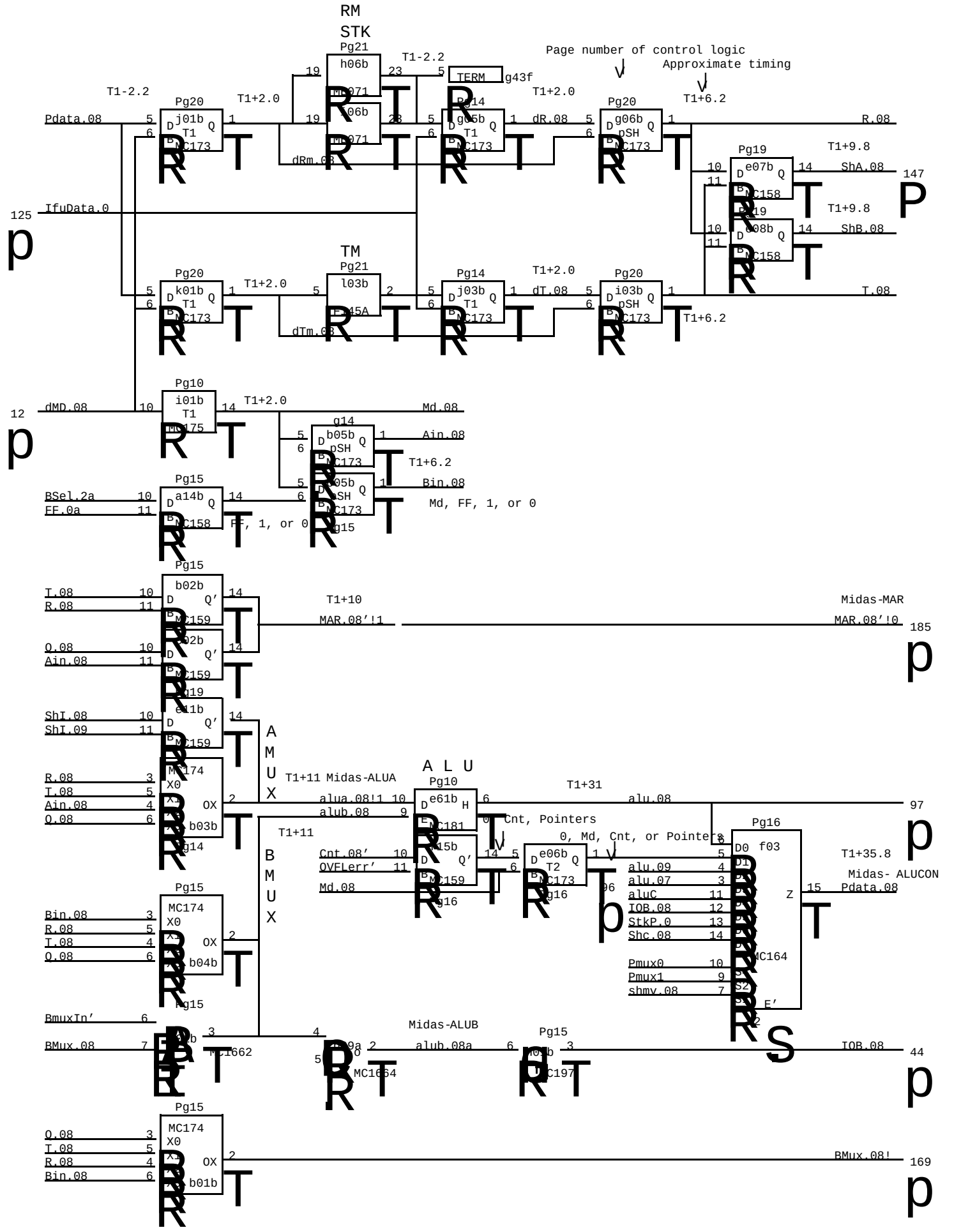


Note: all busses 16 wide unless noted otherwise

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Block Diagram	ProcL01.sil	R Bates	Da	6/27/79	01



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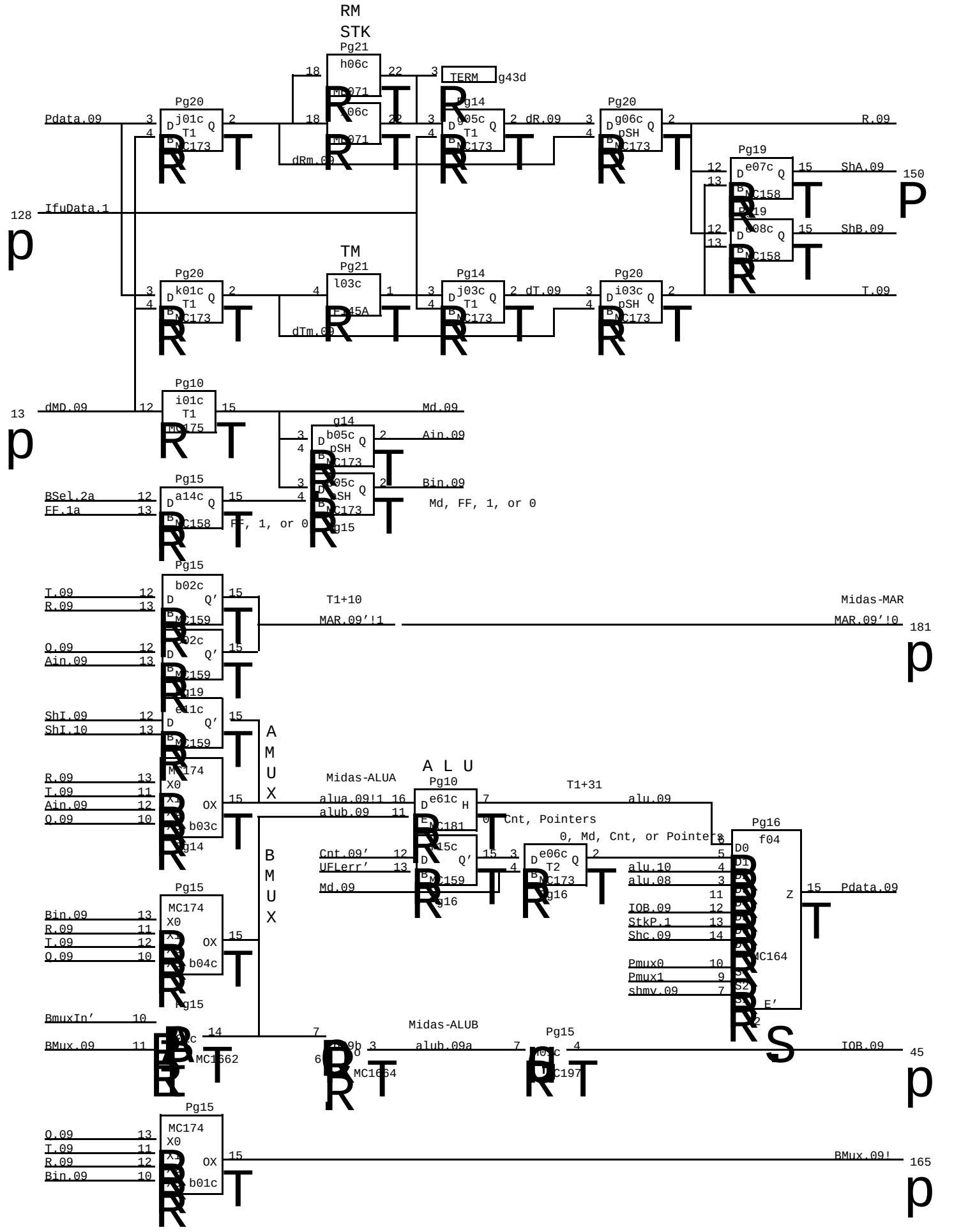
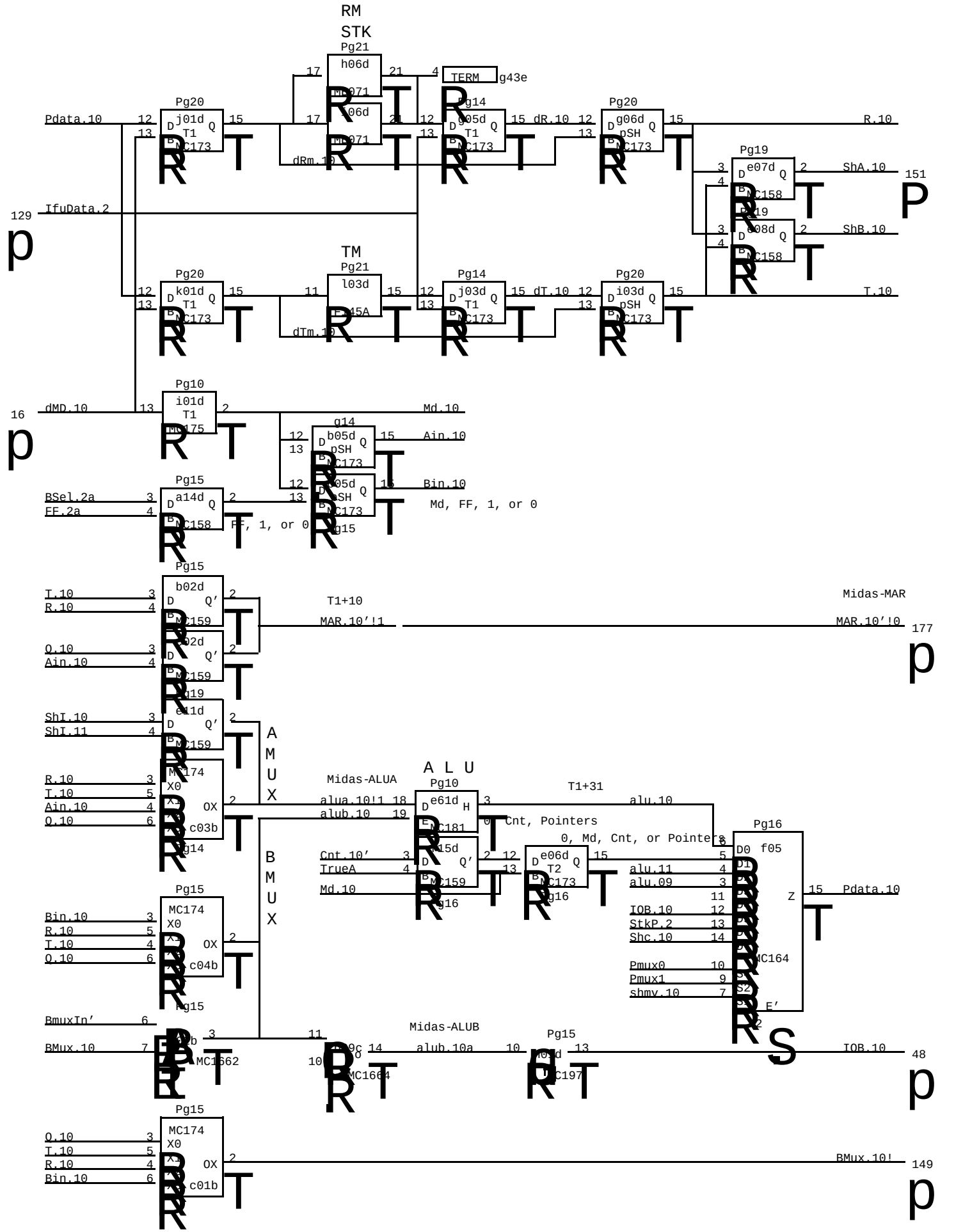
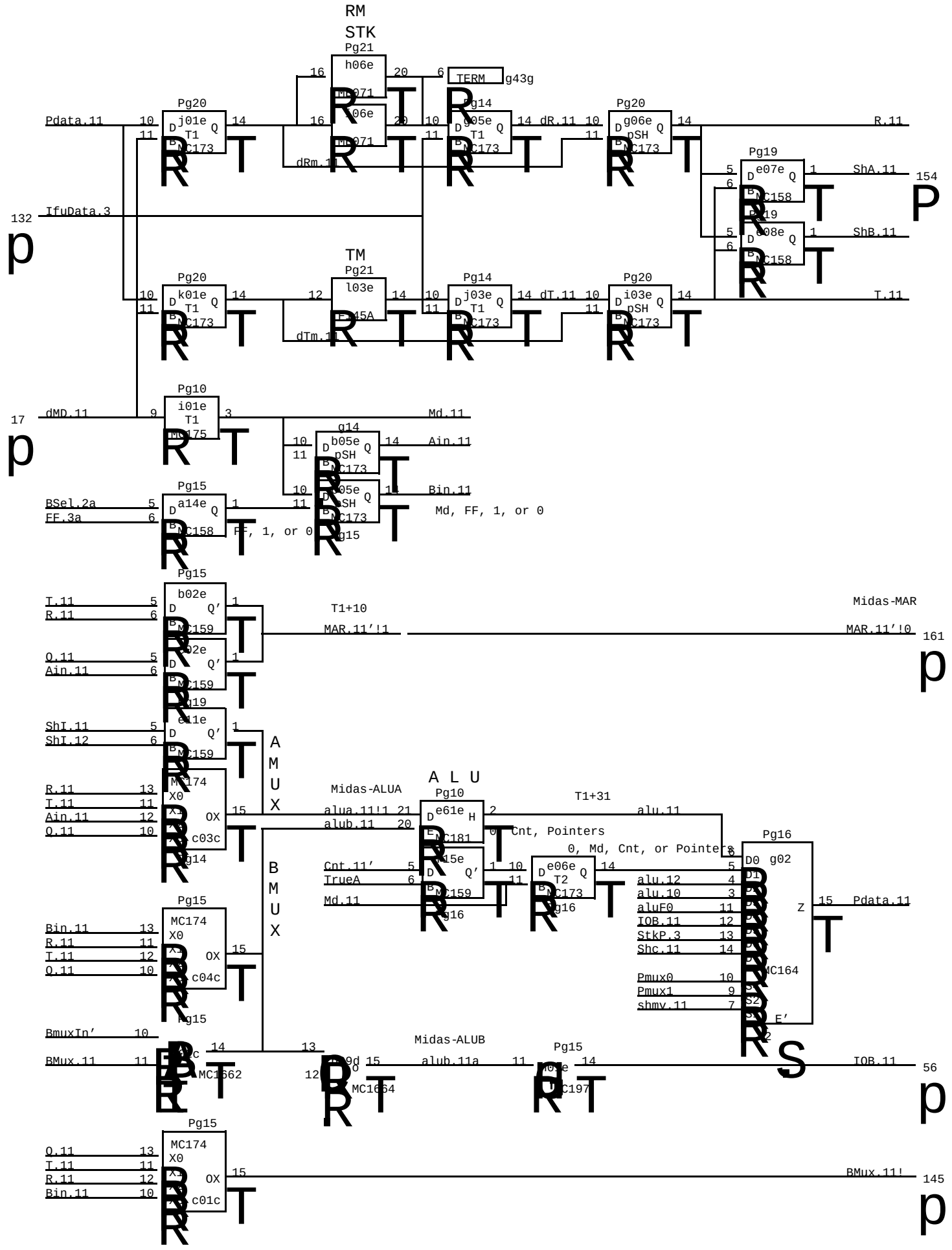
	Dorado	BIT SLICE 08	ProcL02.sil	R Bates	Da	6/27/79	02



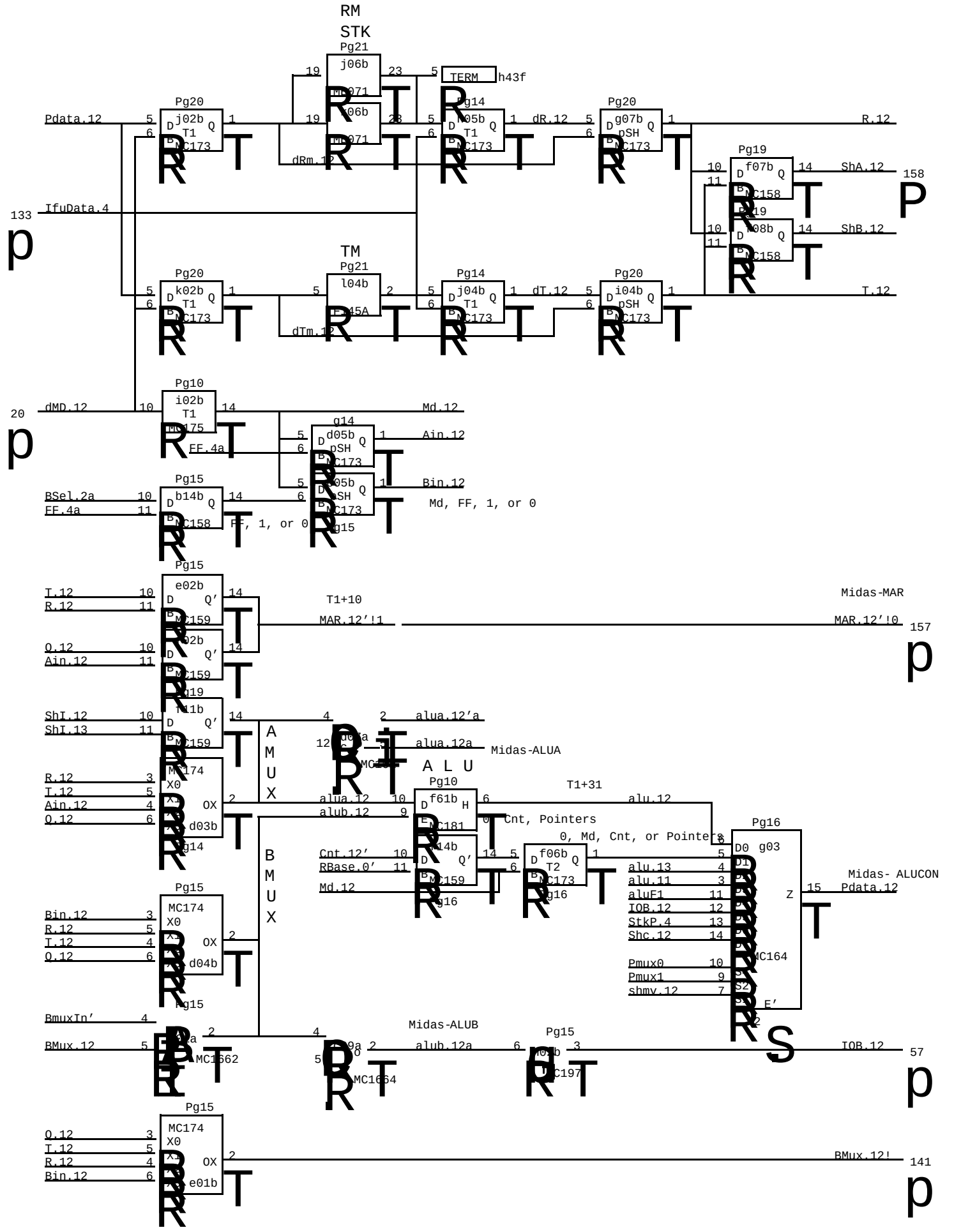
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 09	ProcL03.sil	R Bates	Da	6/27/79	03



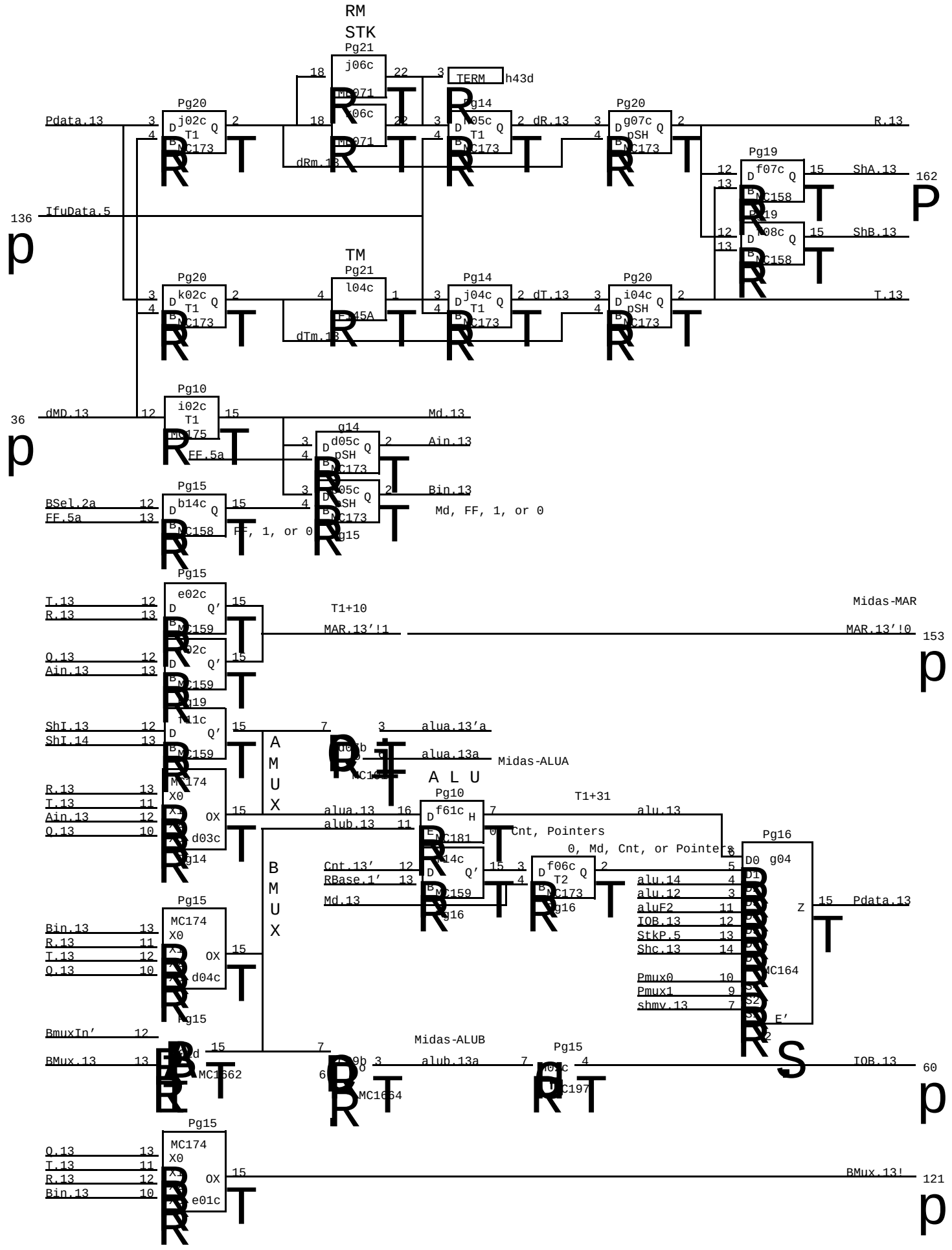
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 10	ProcL04.sil	R Bates	Da	6/27/79	04



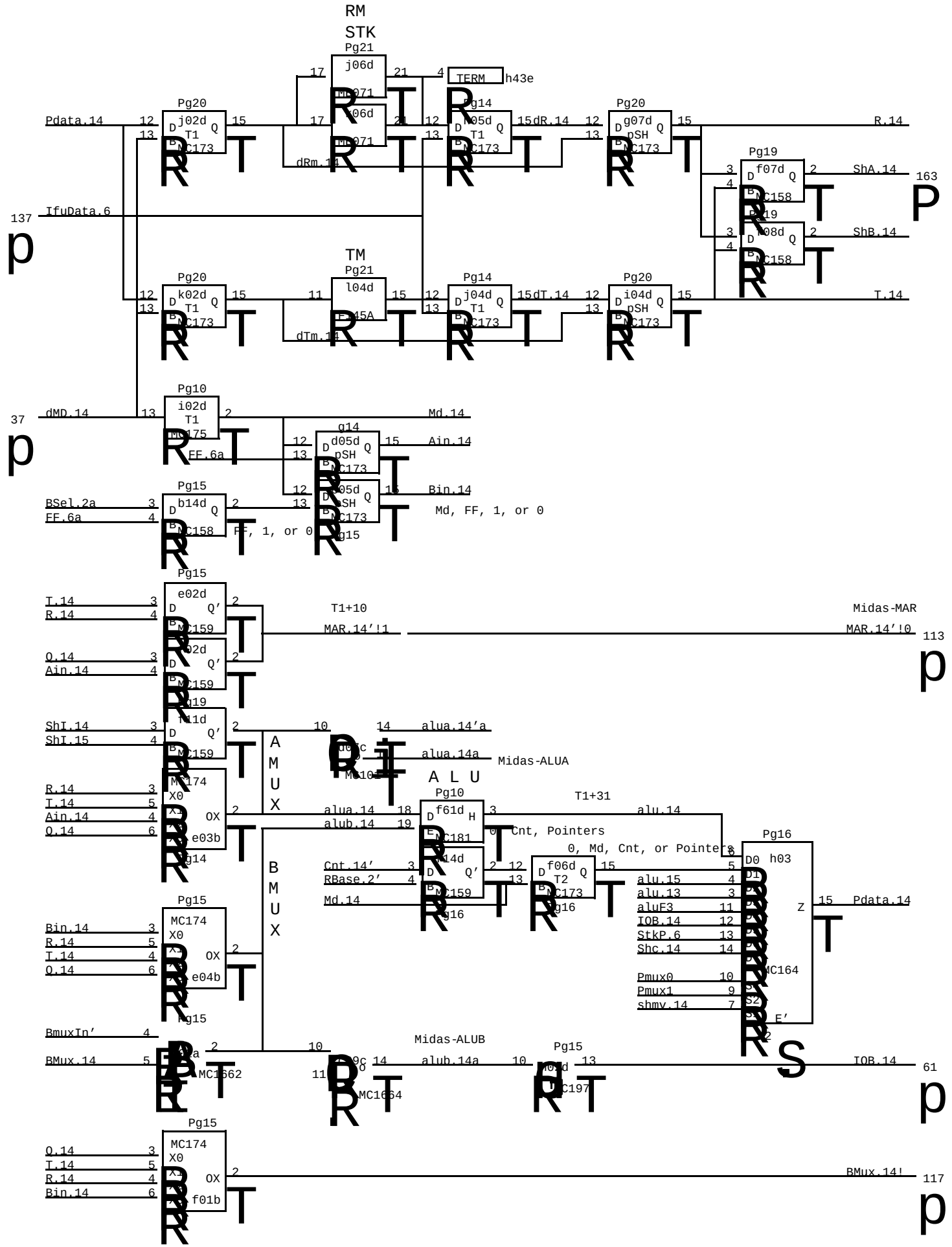
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 11	ProcL05.sil	R Bates	Da	6/27/79	05



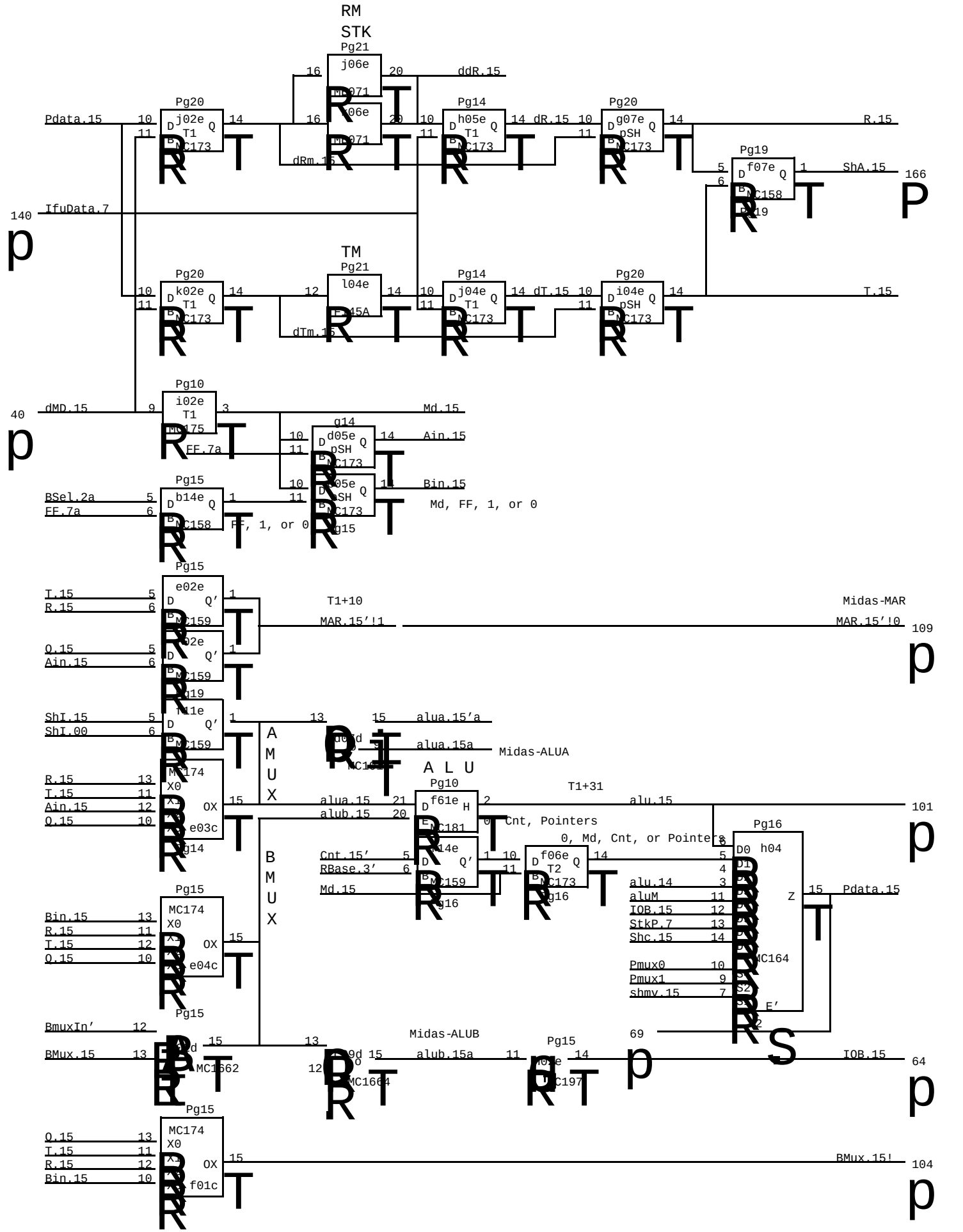
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 12	ProcL06.sil	R Bates	Da	6/27/79	06



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 13	ProcL07.sil	R Bates	Da	6/27/79	07



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 14	ProcL08.sil	R Bates	Da	6/08/79	08



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 15	ProcL09.sil	R Bates	Da	6/27/79	09

ALU delays

Logical function to output = 11.9

Arithmetic operation to data = 20.0

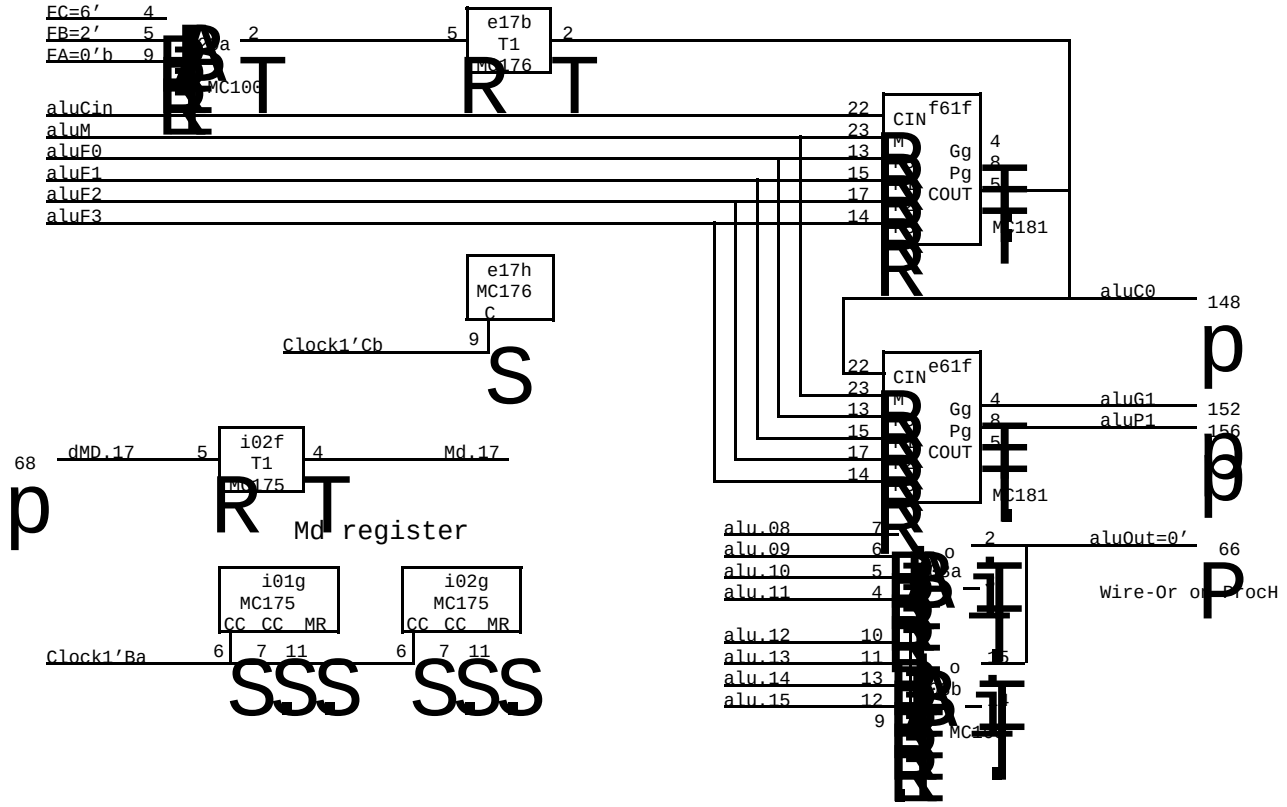
Arithmetic operation to carry = 17.9

ALU output (assuming 10.2 ns to output of BMux)

Logical Function = 22.0

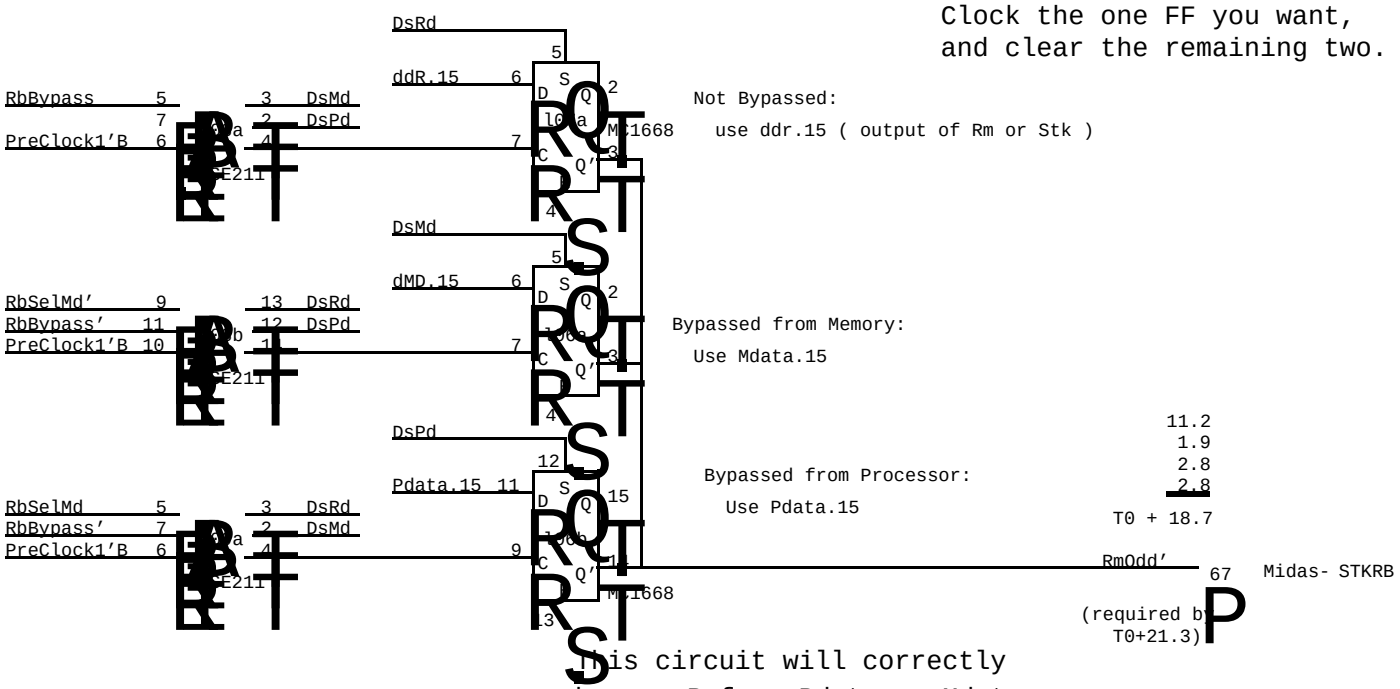
Arithmetic operation to data = 30.1

Arithmetic operation to carry = 28.0



Fast Branch
on Rm odd

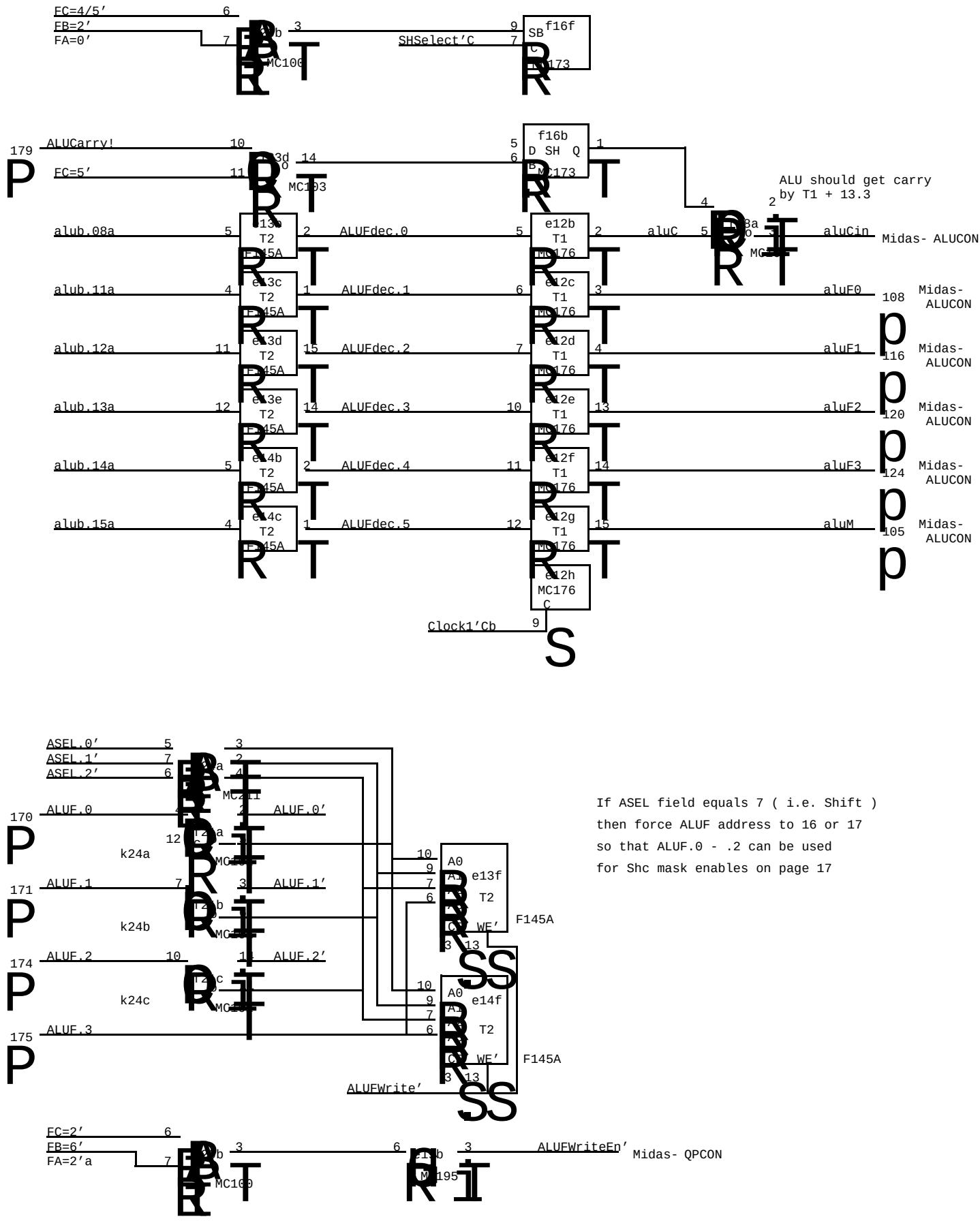
Clock the one FF you want,
and clear the remaining two.



This circuit will correctly
bypass R from Pdata or Mdata
When "RisIfData" is in effect, the fast branch
will be based on the contents of the addressed
RM or STK, bypassed if necessary.

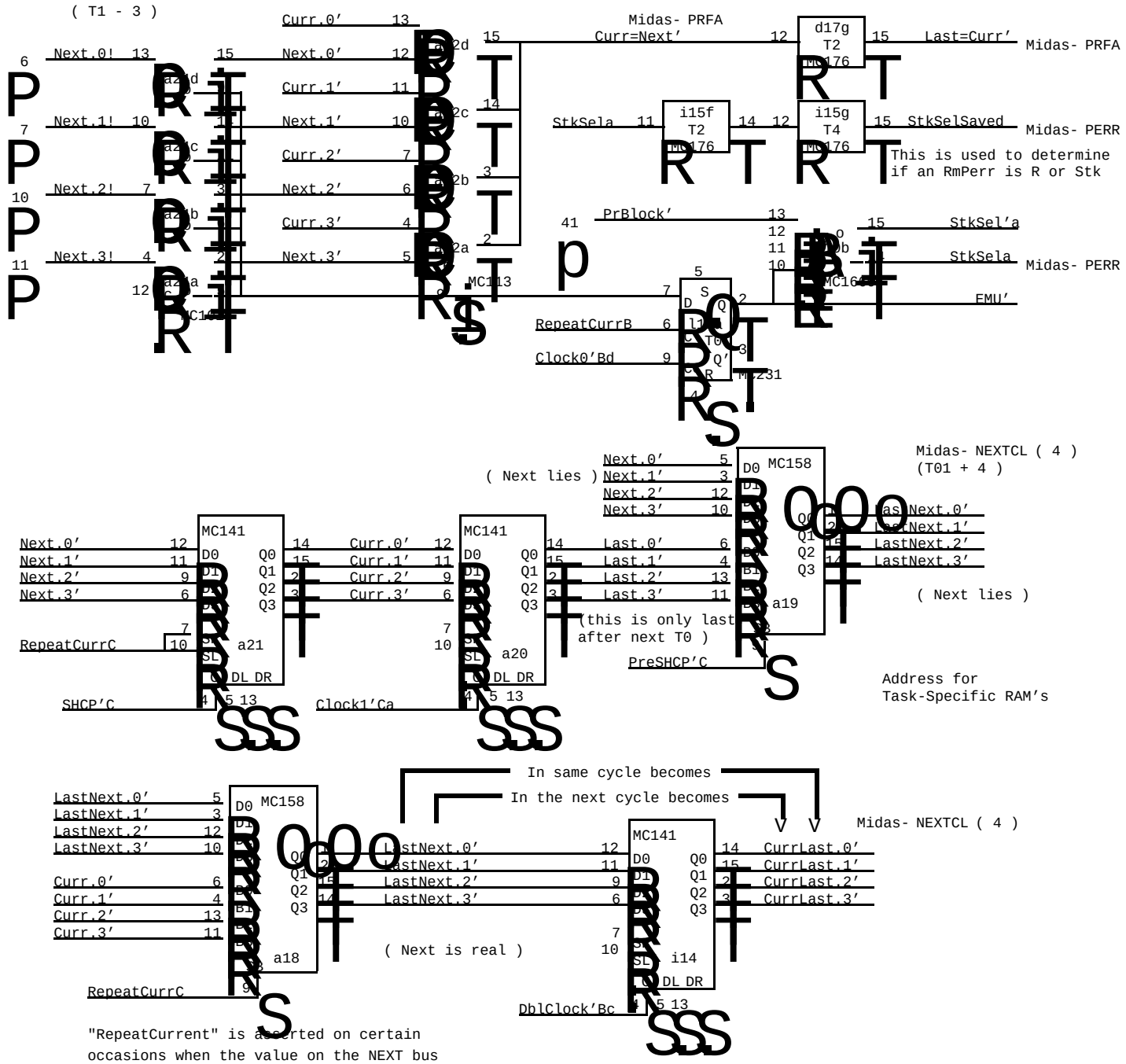
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Atithmetic Logic Unit	ProcL10.sil	R Bates	Da	6/27/79	10

FF = Cin xor 1
or
FF = Cin xor Cout



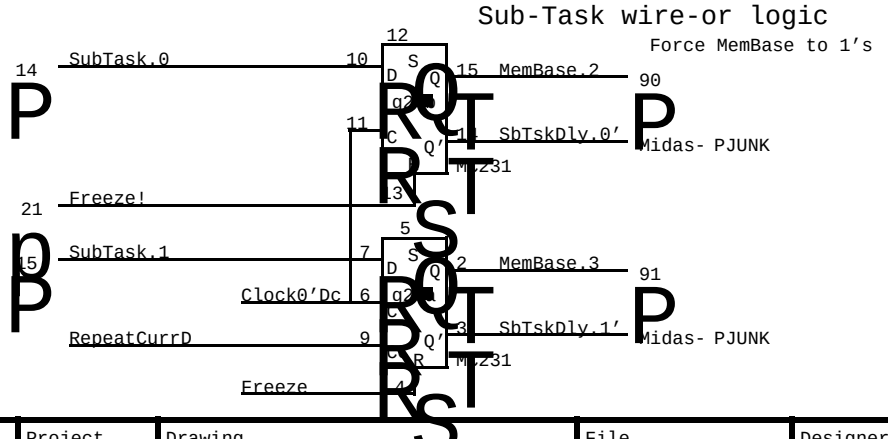
NOTE: Moving k24 to f21 saves 0.4 ns

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	ALU FUNCTION RAM	ProcL11.sil	R Bates	Da	6/27/79	11



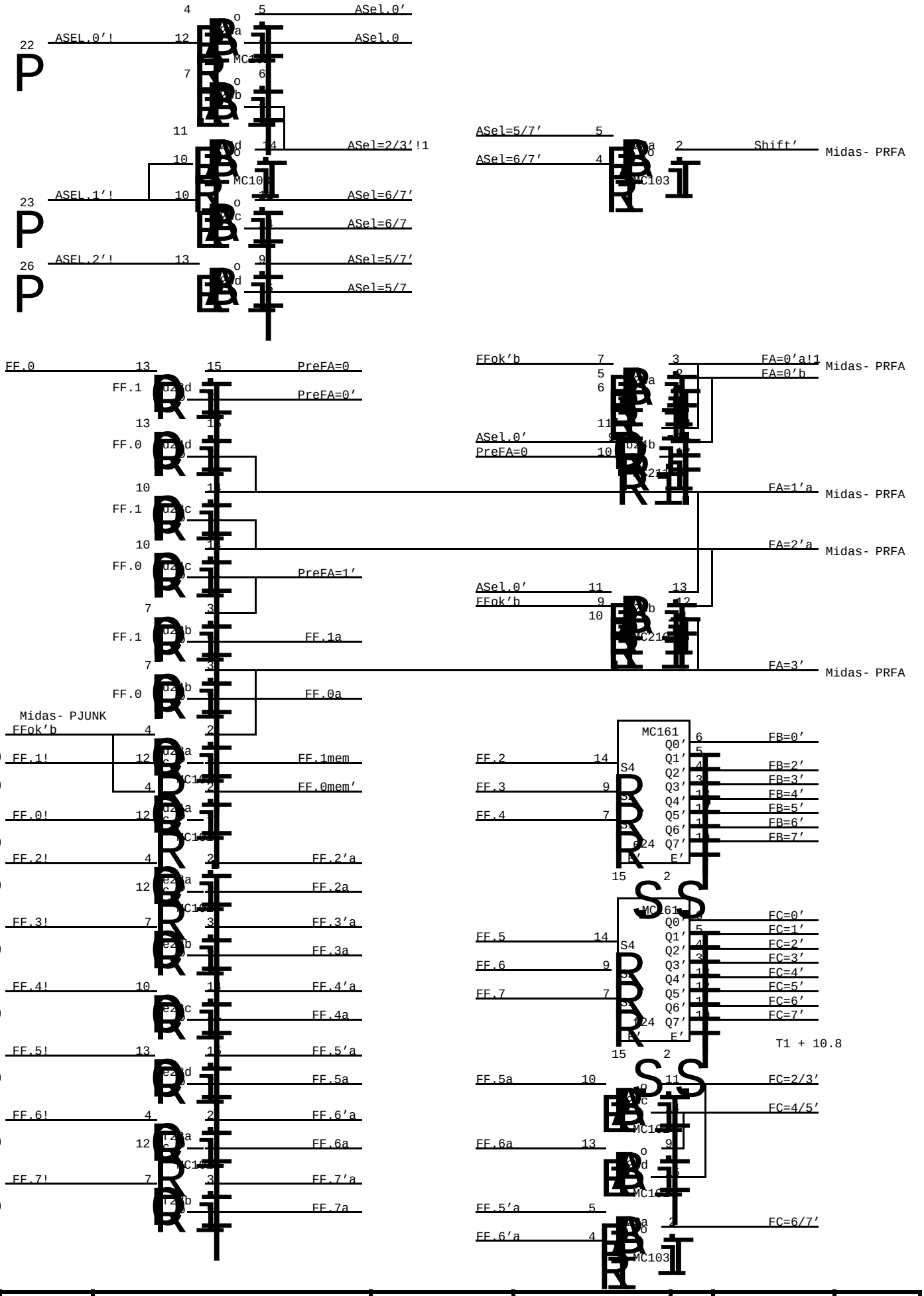
Task number tracking logic

Sub-Task wire-or logic



RBase is forces to 1's on Pages 24 & 25

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Task logic	ProcL12.sil	R. Bates	Da	6/27/79	12



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Function Field Decoding	ProcL13.sil	R Bates	Da	6/27/79	13

AMux decoding

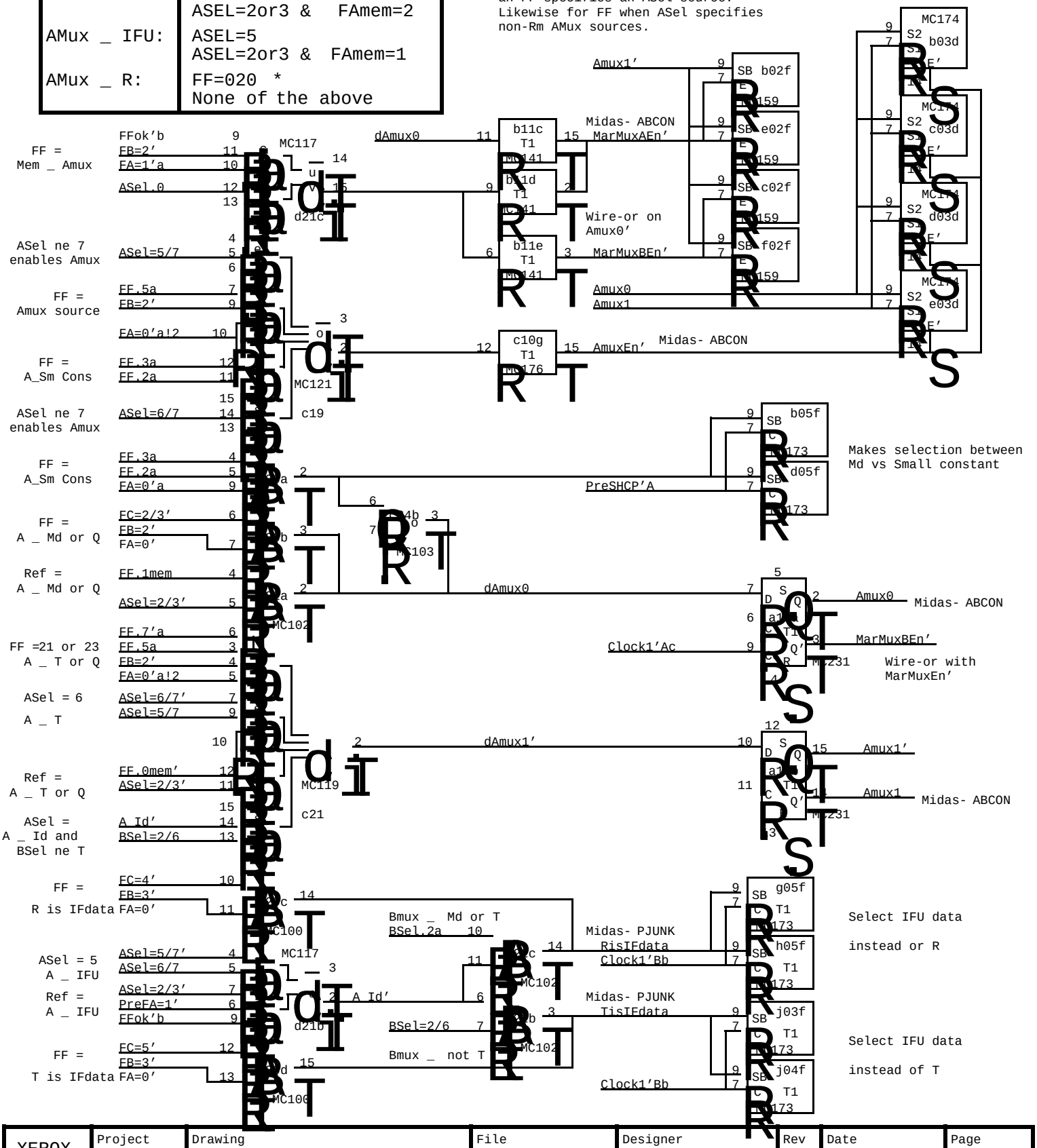
AMux _ FF:	FF=0-17 *
AMux _ T:	FF=021 * ASEL=2or3 & FAmem=3 ASEL=6
AMux _ Md:	FF=022 * ASEL=2or3 & FAmem=0
AMux _ Q:	FF=023 * ASEL=2or3 & FAmem=2
AMux _ IFU:	ASEL=5 ASEL=2or3 & FAmem=1
AMux _ R:	FF=020 * None of the above

* The Amux is disabled by ASEL=7 unless one of these codes are in effect

NOTE: ASel selects and FF selects for the AMux are "OR'd" by this hardware. Thus ASel codes selecting non-Rm sources of Amux must not be used when an FF specifies an ASel source. Likewise for FF when ASel specifies non-Rm AMux sources.

AMux encoding

Mux Input	Source
0	R or IFU data
1	T or IFU data
2	Md or Small Const.
3	Q



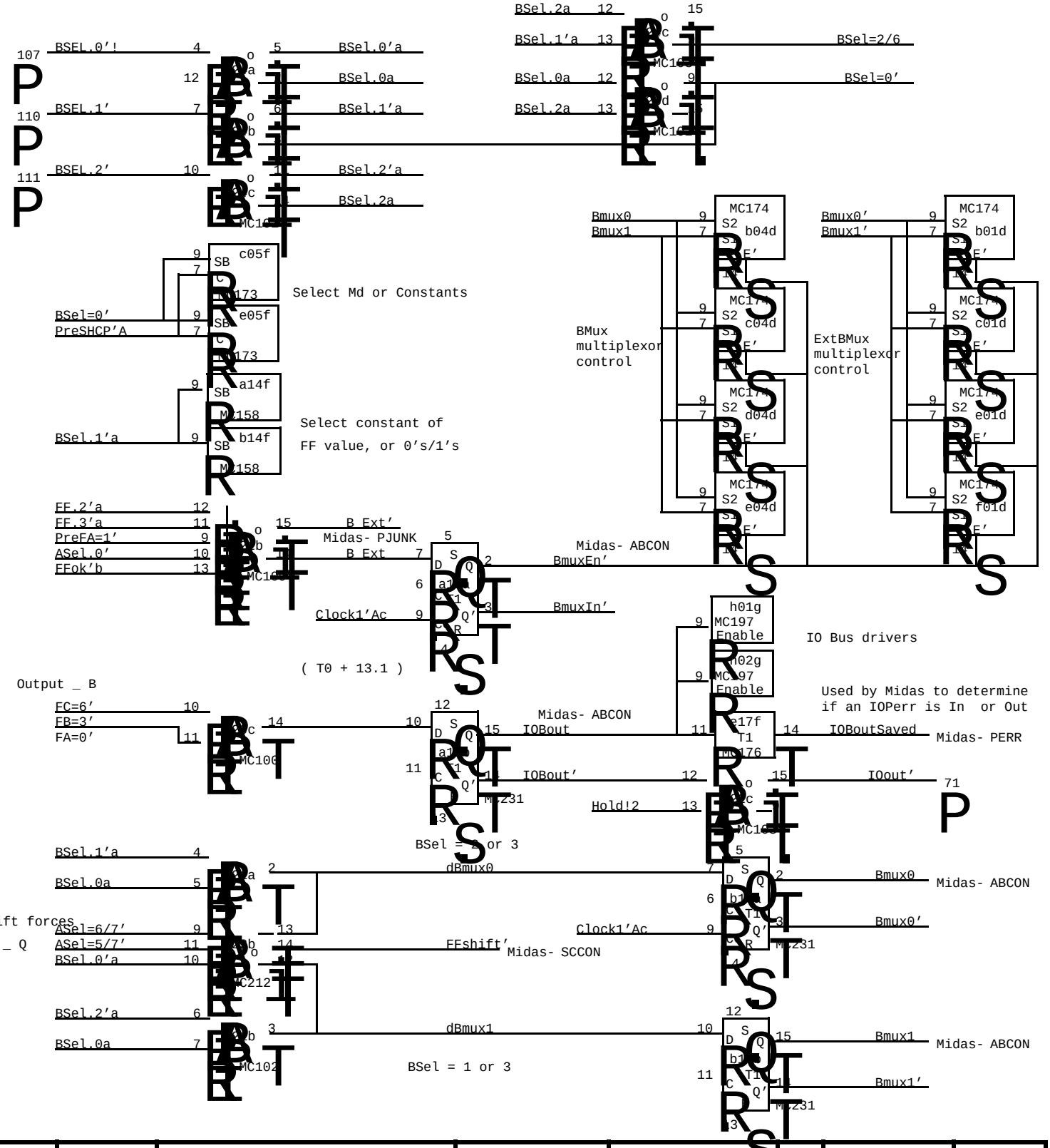
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	"A" Multiplexor Control	ProcL14.sil	R. Bates	Da	6/27/79	14

BSEL field decoding

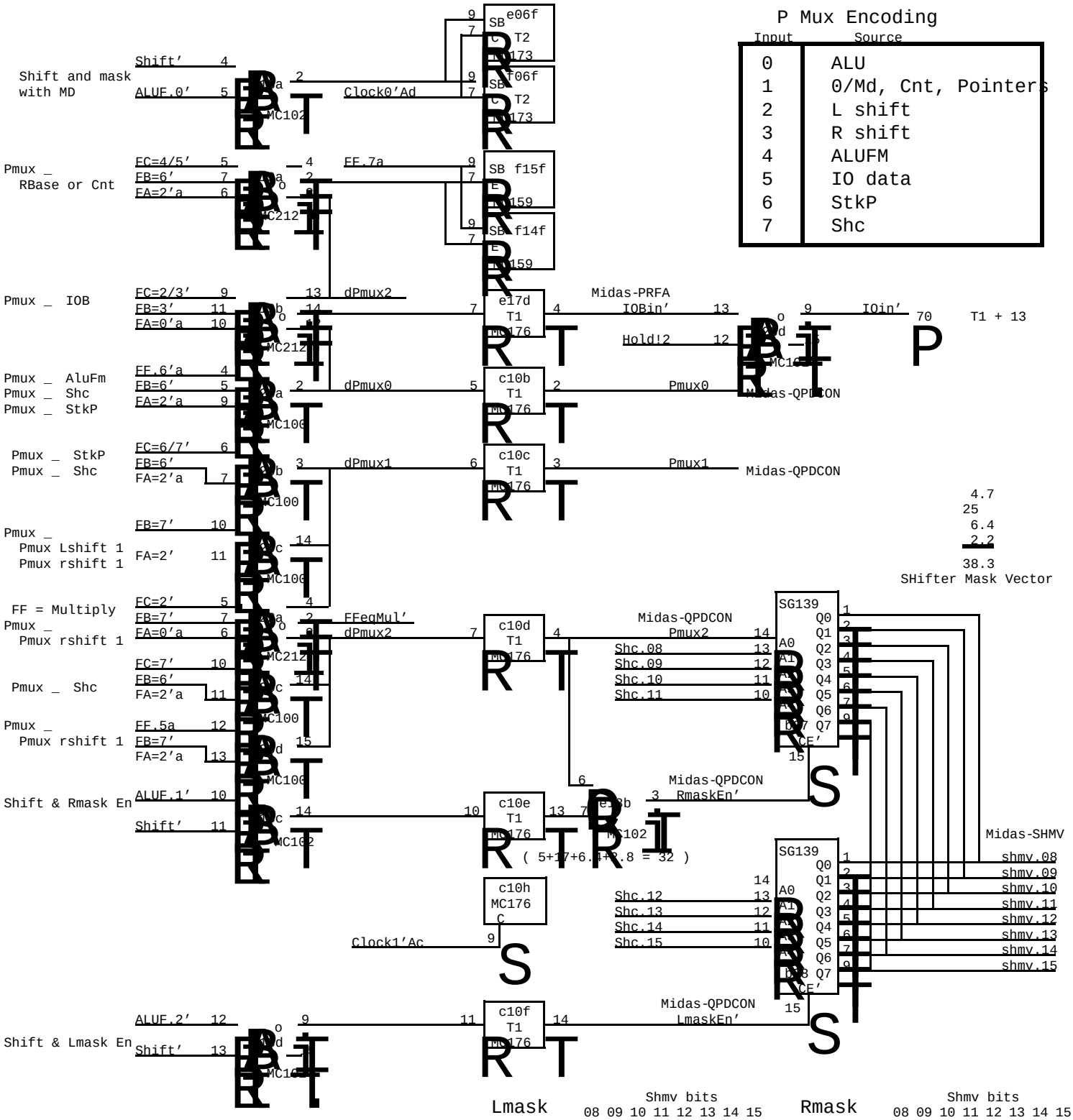
BSEL	INTERNAL	EXTERNAL
0	Md	--
1	R	--
2	T	Hold_B
3	Q	Q _ B
4	0,,FF	--
5	377,FF	--
6	FF,,0	--
7	FF,,377	--

BMux encoding

BMux	
0	Md or Constant
1	R
2	T
3	Q



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	"B" Multiplexor & Cont.	ProcL15.sil	R Bates	Da	6/27/79	15



Lmask

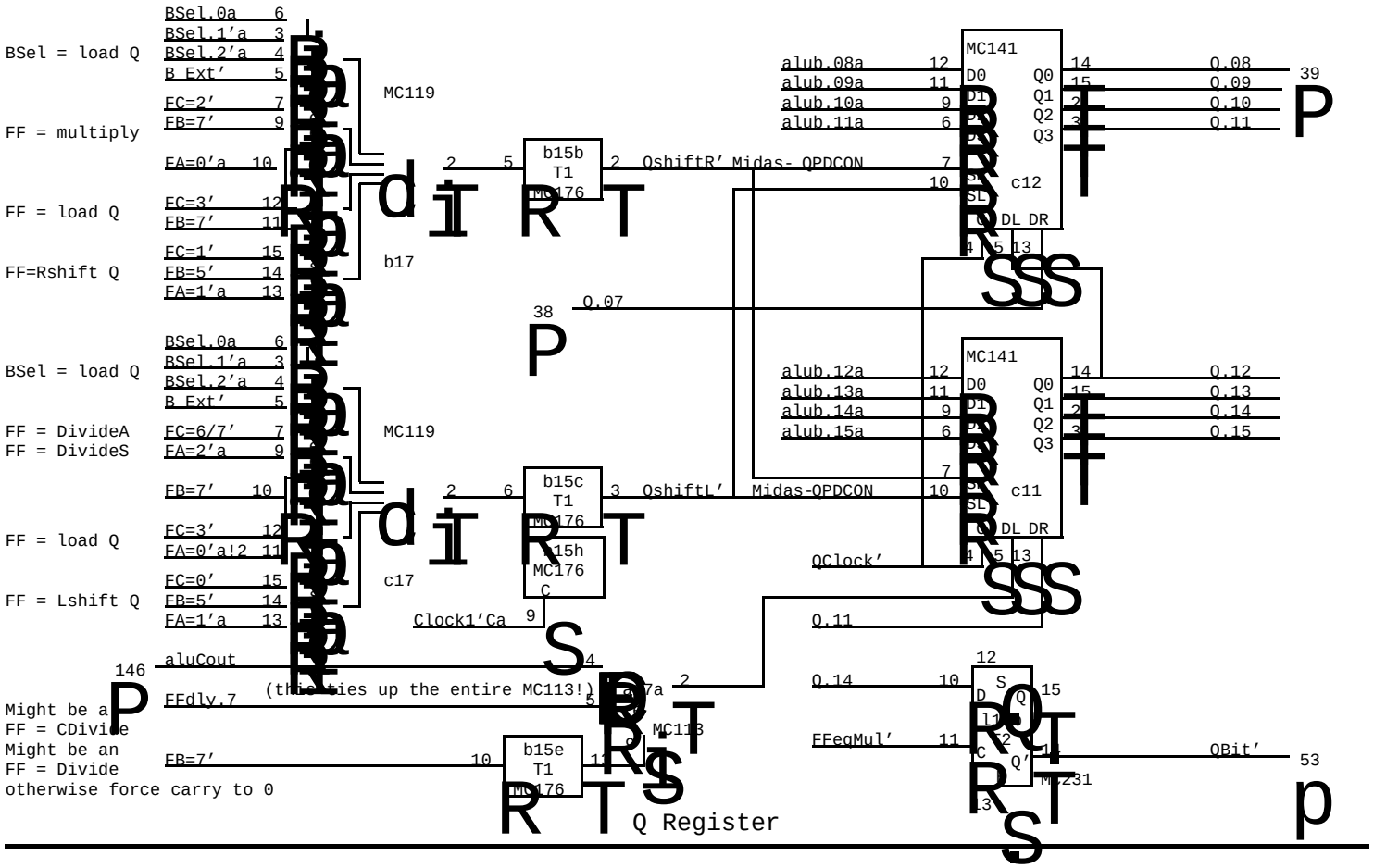
Shc.12-15	Shmv bits 08	09	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	1	0	0	0	0	0	0	0
12	1	1	0	0	0	0	0	0
13	1	1	1	0	0	0	0	0
14	1	1	1	1	0	0	0	0
15	1	1	1	1	1	0	0	0
16	1	1	1	1	1	1	0	0
17	1	1	1	1	1	1	1	0
20- 37	1	1	1	1	1	1	1	1

Rmask

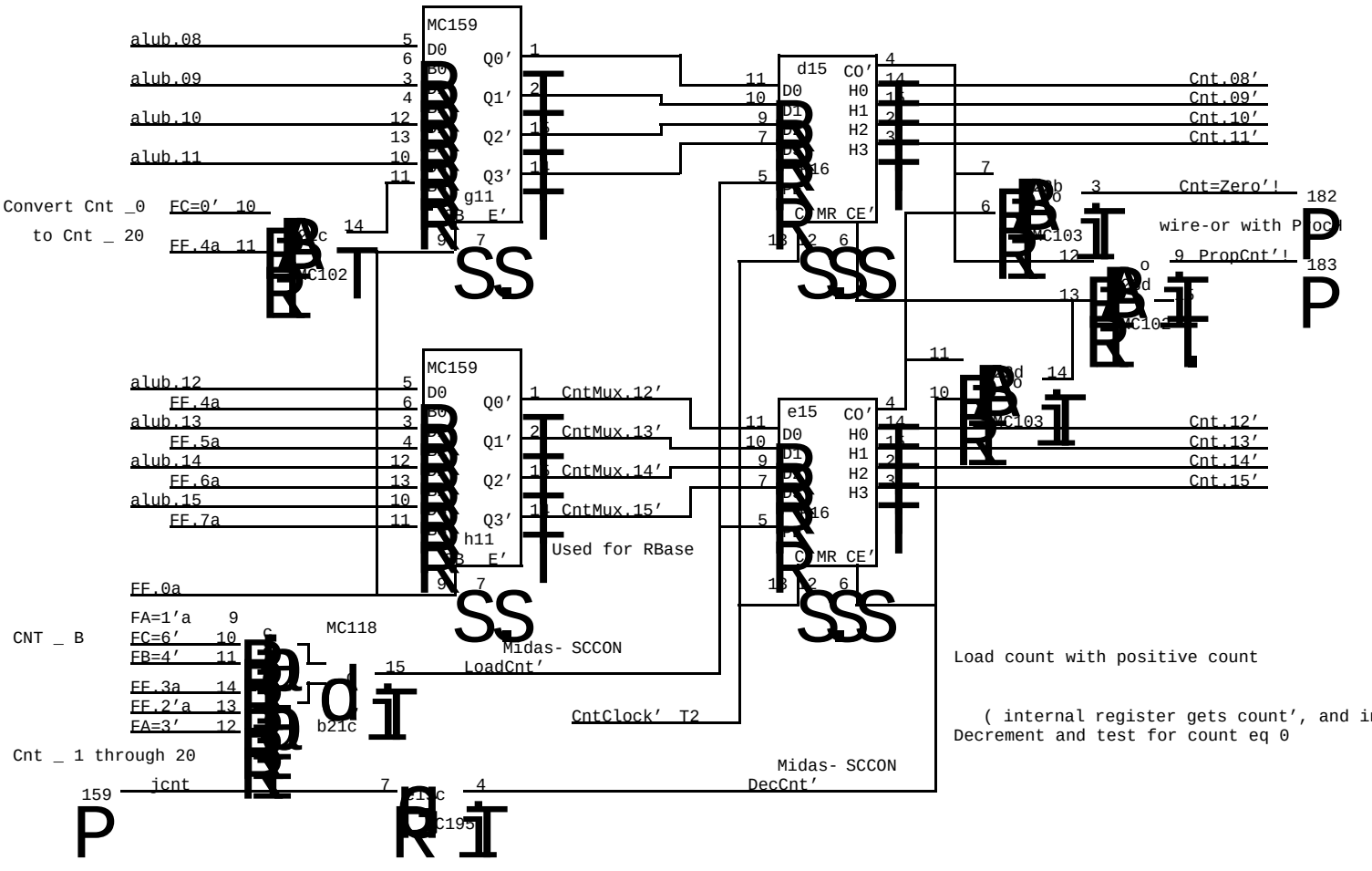
Shc.08-11	Shmv bits 08	09	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	1
3	0	0	0	0	0	1	1	1
4	0	0	0	0	1	1	1	1
5	0	0	0	1	1	1	1	1
6	0	0	1	1	1	1	1	1
7	0	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1
12	1	1	1	1	1	1	1	1
13	1	1	1	1	1	1	1	1
14	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1
16	1	1	1	1	1	1	1	1
17	1	1	1	1	1	1	1	1
20- 37	1	1	1	1	1	1	1	1

NOTE: The prom patterns are designed so that a one into address bit 0 will produce all 1's on the output. This allows the odd address inputs to Pmux to be selected.

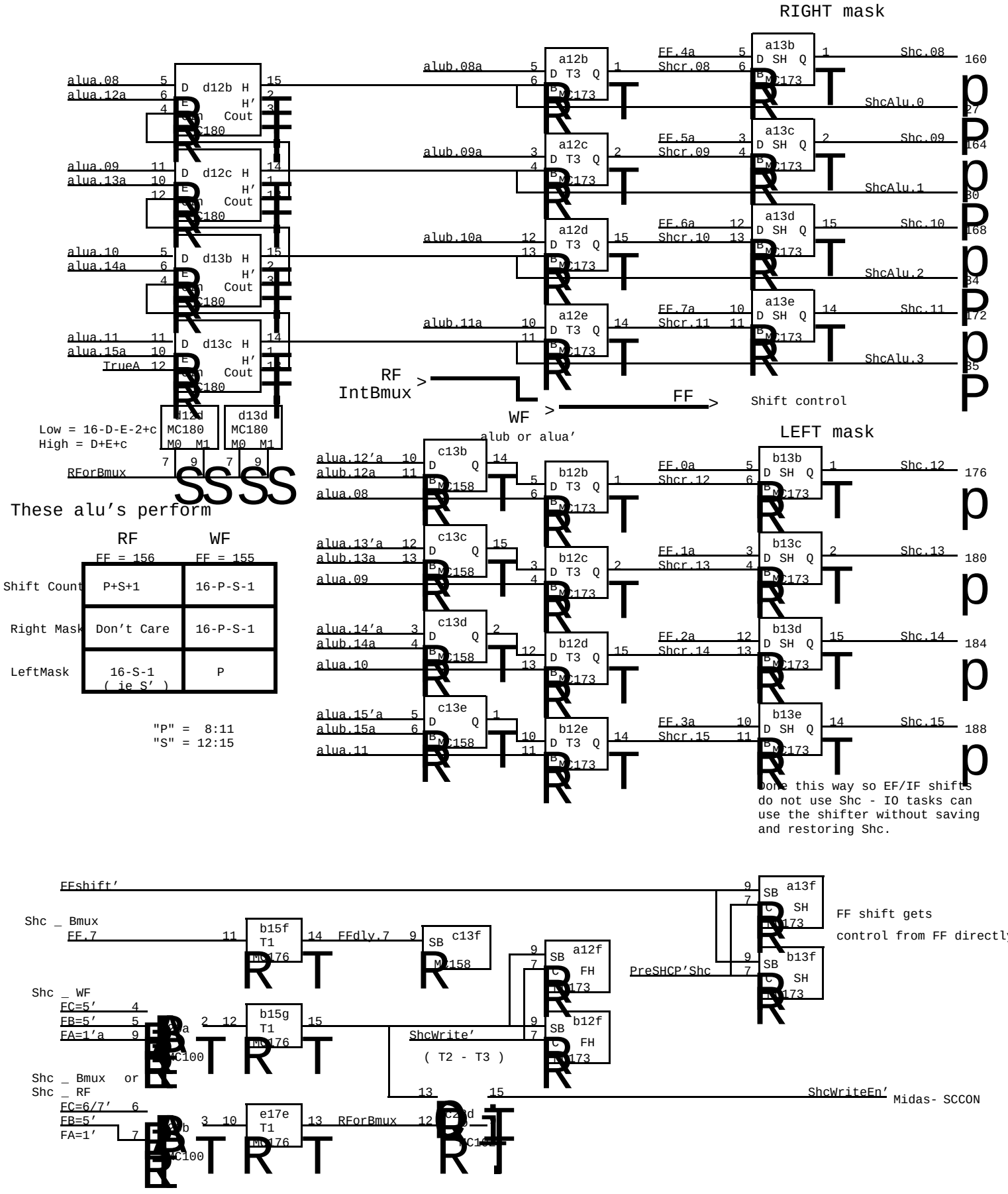
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Proc Multiplexor & Shift mask Prom	ProcL16.sil	R Bates	Da	6/27/79	16



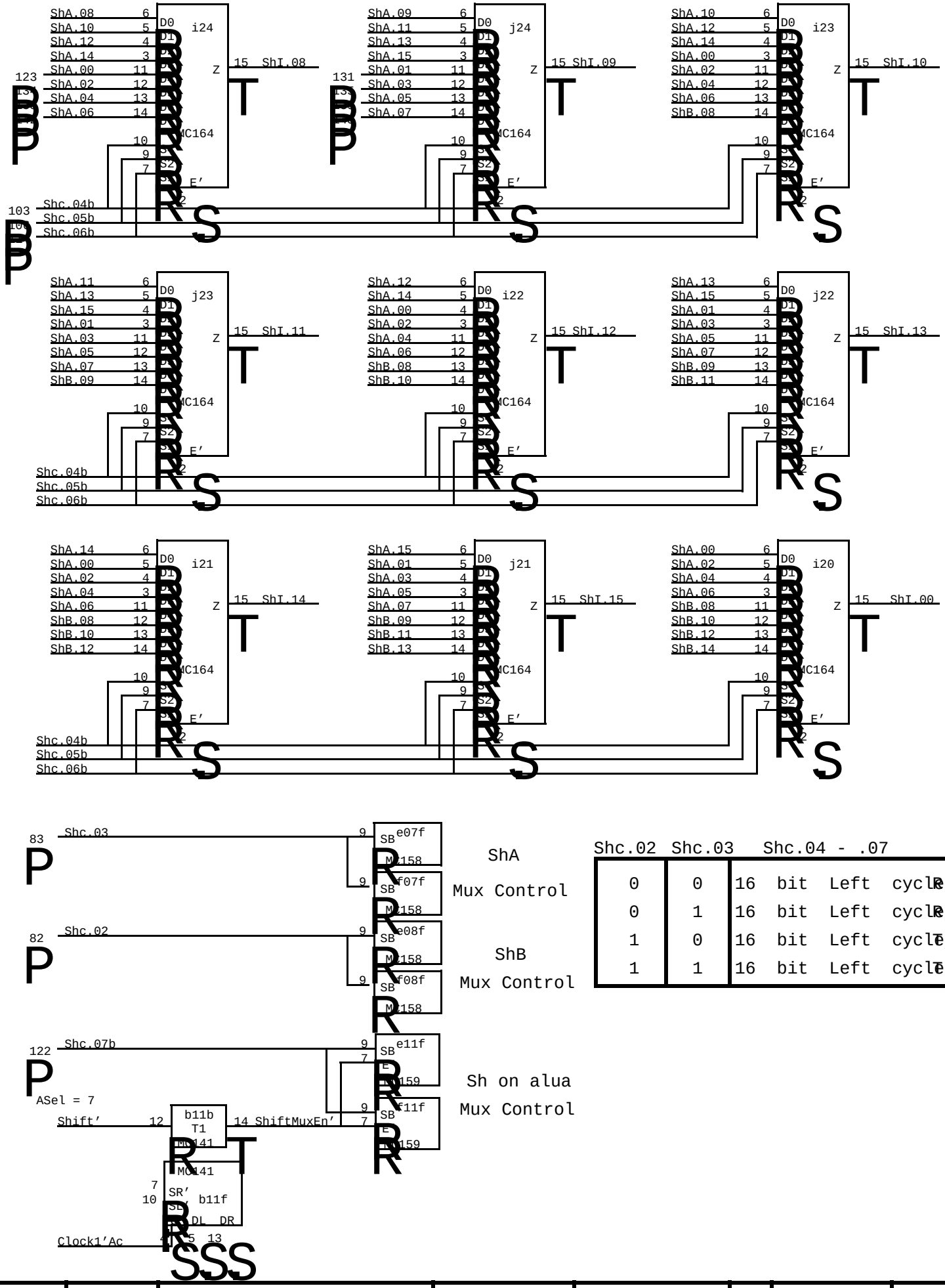
Count Register



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Q Register and Task Simulator	ProcL17.sil	R Bates	Da	6/27/79	17



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Shift Register Control	ProcL18.sil	R Bates	Da	6/27/79	18



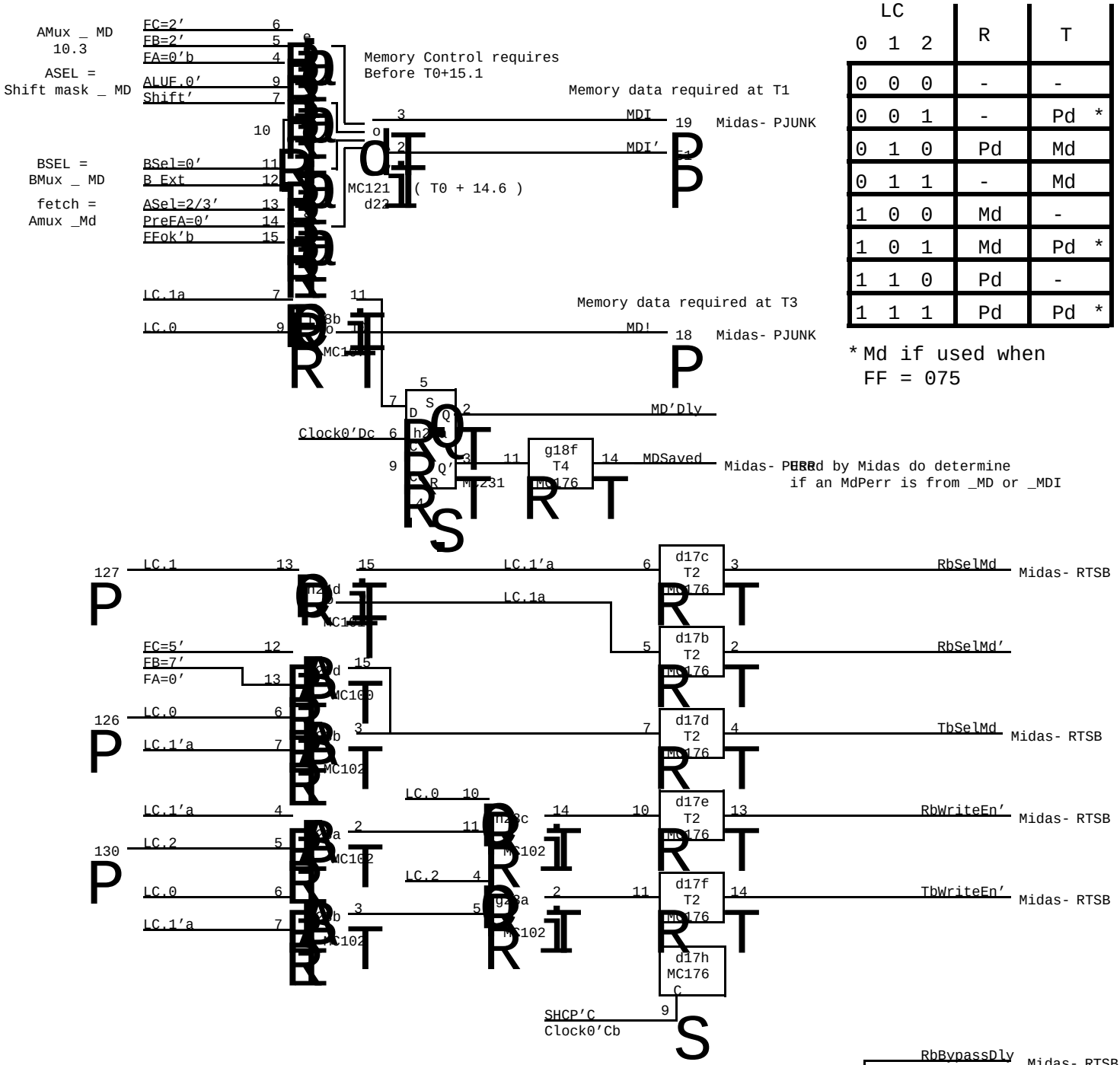
ShA Mux Control

ShB Mux Control

Sh on alua Mux Control

Shc.02	Shc.03	Shc.04 - .07
0	0	16 bit Left cycle of
0	1	16 bit Left cycle of
1	0	16 bit Left cycle of
1	1	16 bit Left cycle of

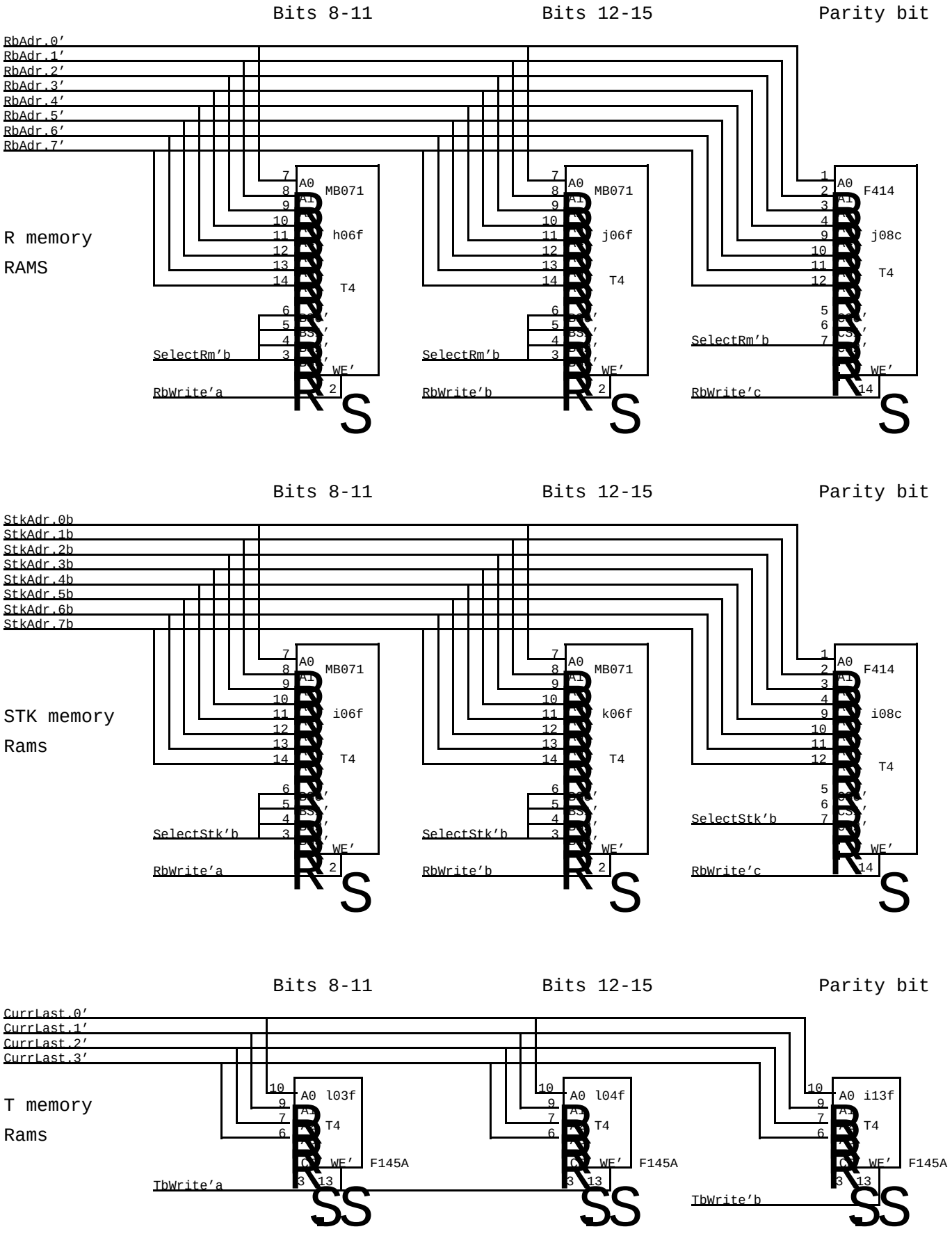
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Shifter	ProcL19.sil	R Bates	Da	6/27/79	19



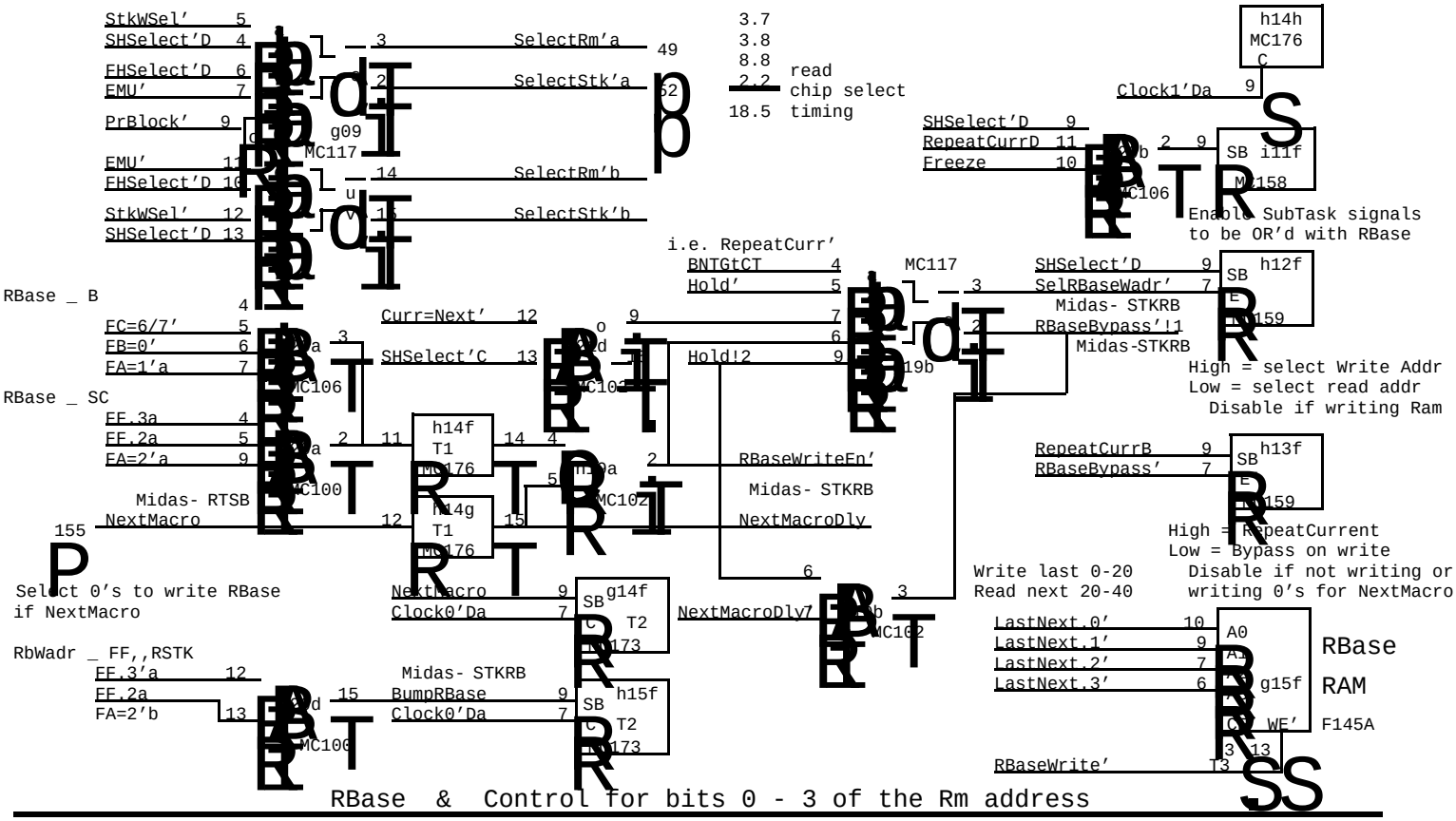
LC 0 1 2	R	T
0 0 0	-	-
0 0 1	-	Pd *
0 1 0	Pd	Md
0 1 1	-	Md
1 0 0	Md	-
1 0 1	Md	Pd *
1 1 0	Pd	-
1 1 1	Pd	Pd *

* Md if used when
FF = 075

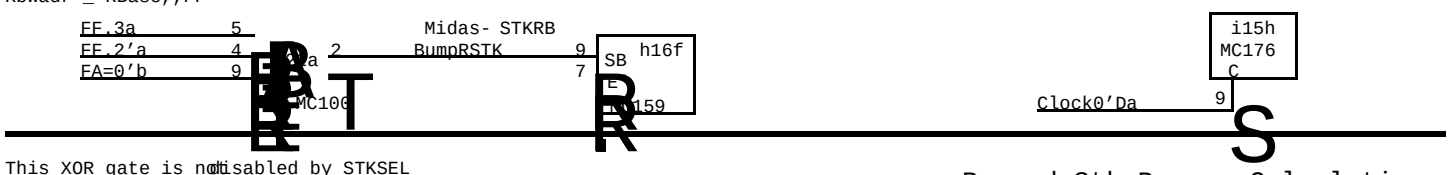
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	LC FIELD RAM ADDRESSES	ProcL20.sil	R Bates	Da	6/27/79	20



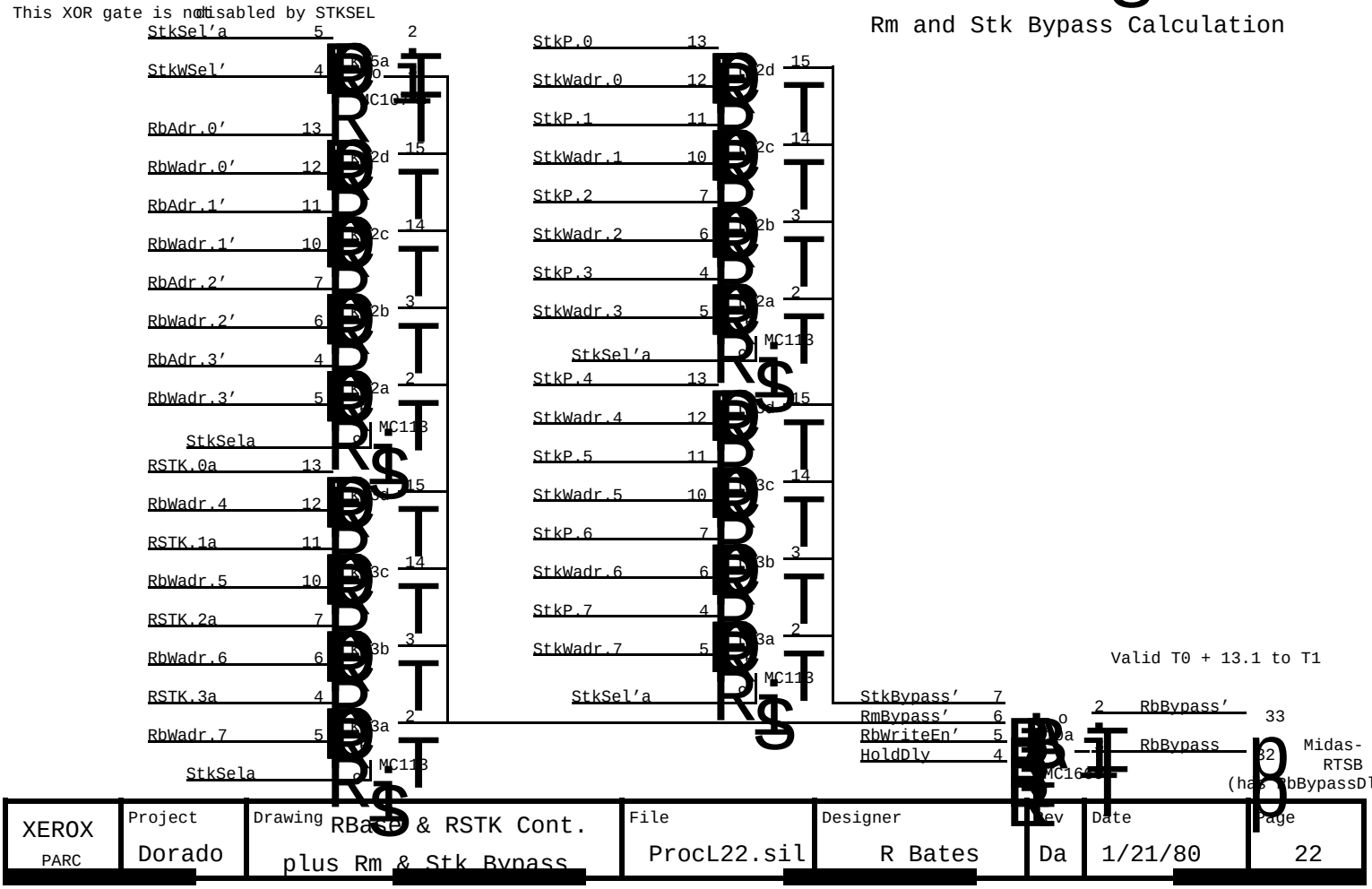
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	RM & STK addressing	ProcL21.sil	R Bates	Da	6/27/79	21



RBase & Control for bits 0 - 3 of the Rm address

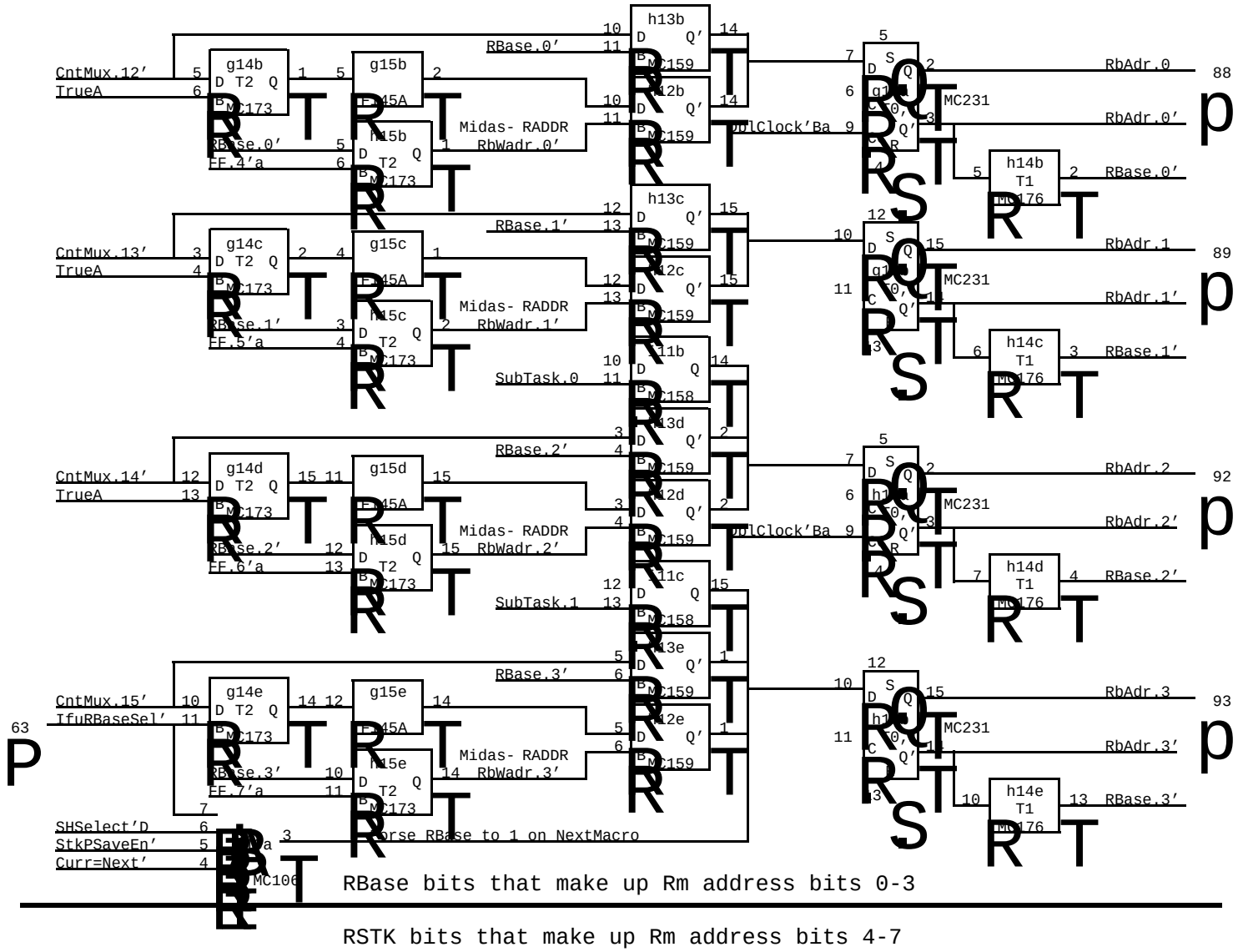


RSTK & Control for bits 4 - 7 of the Rm address

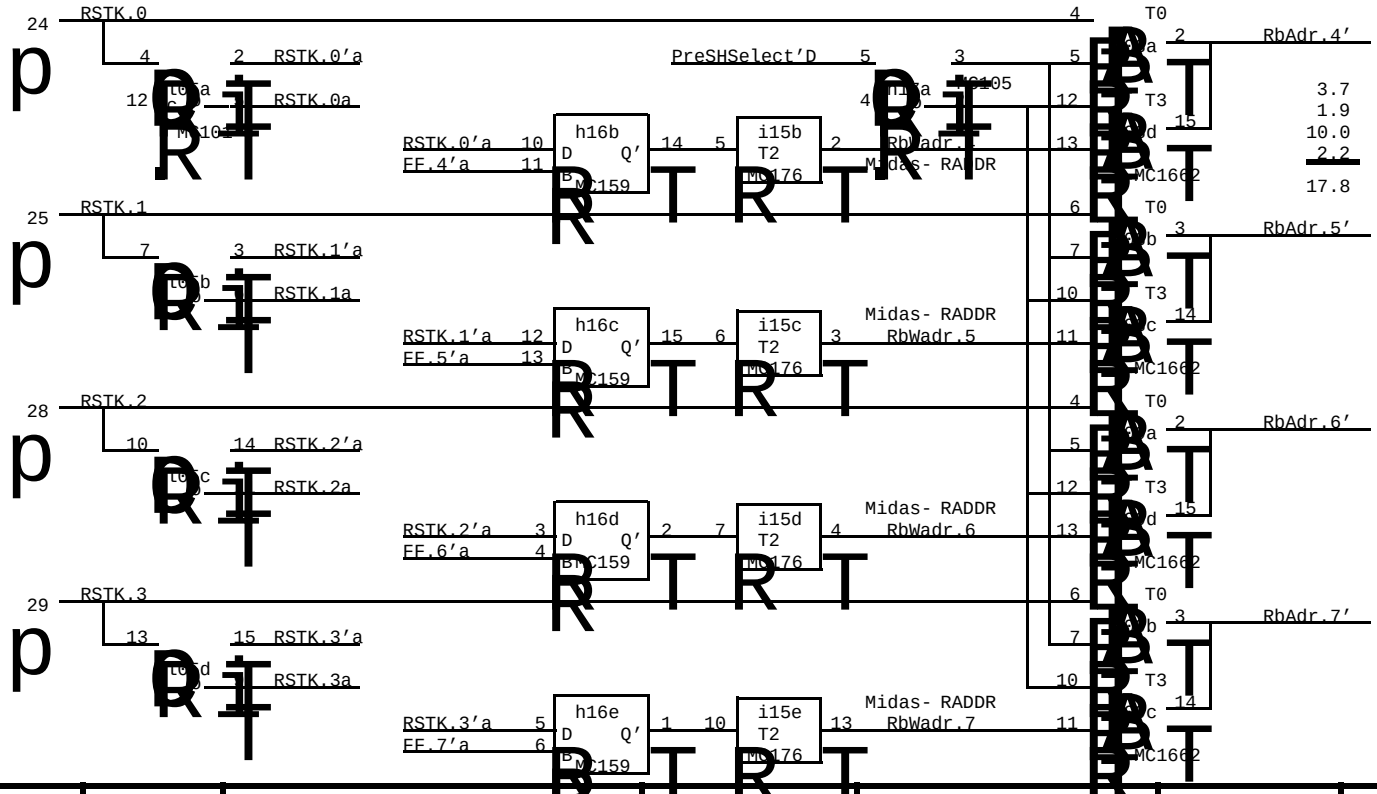


Rm and Stk Bypass Calculation

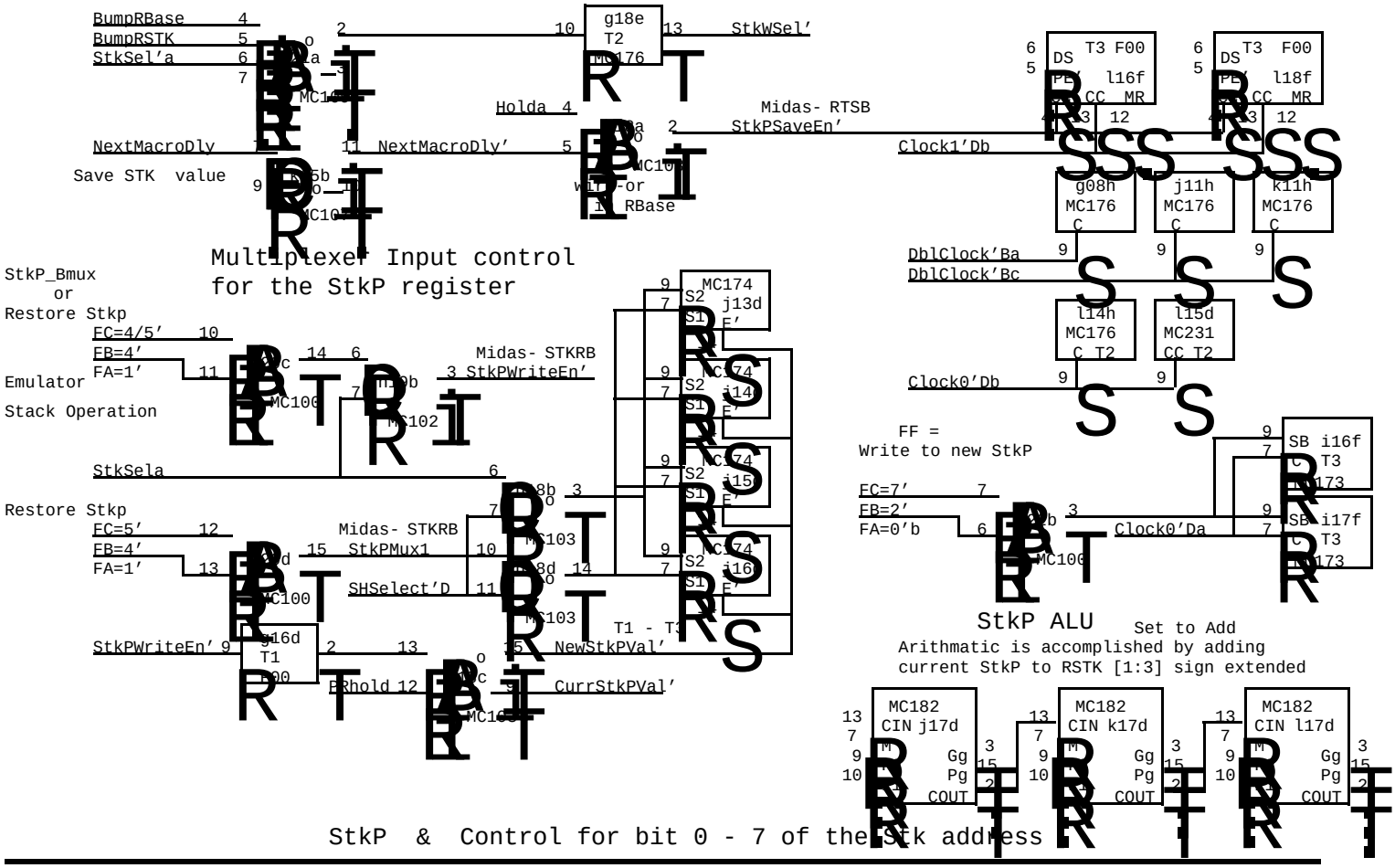
XEROX PARC	Project: Dorado	Drawing: RBase & RSTK Cont. plus Rm & Stk Bypass	File: ProcL22.sil	Designer: R Bates	Rev: Da	Date: 1/21/80	Page: 22

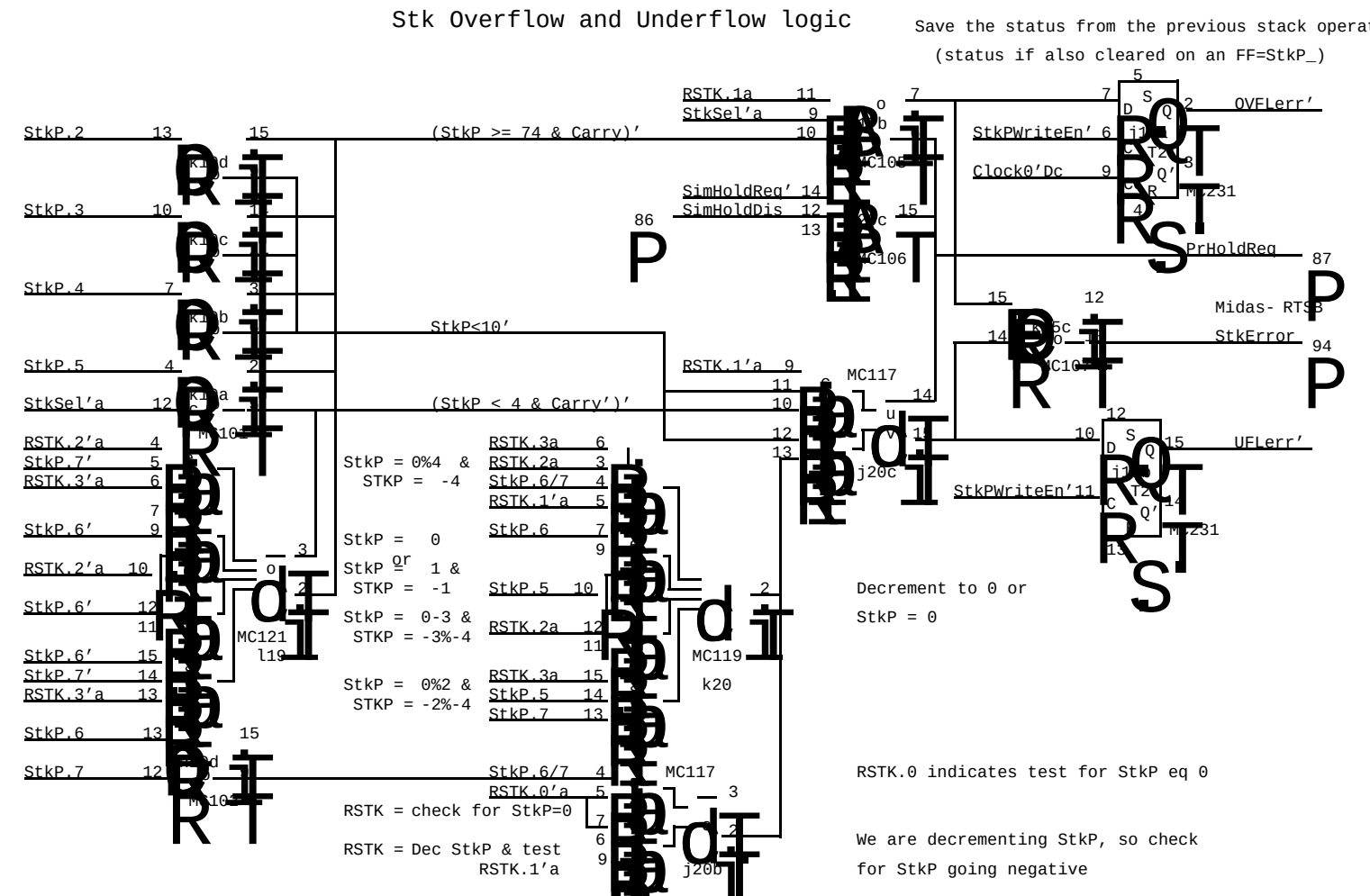


RSTK bits that make up Rm address bits 4-7

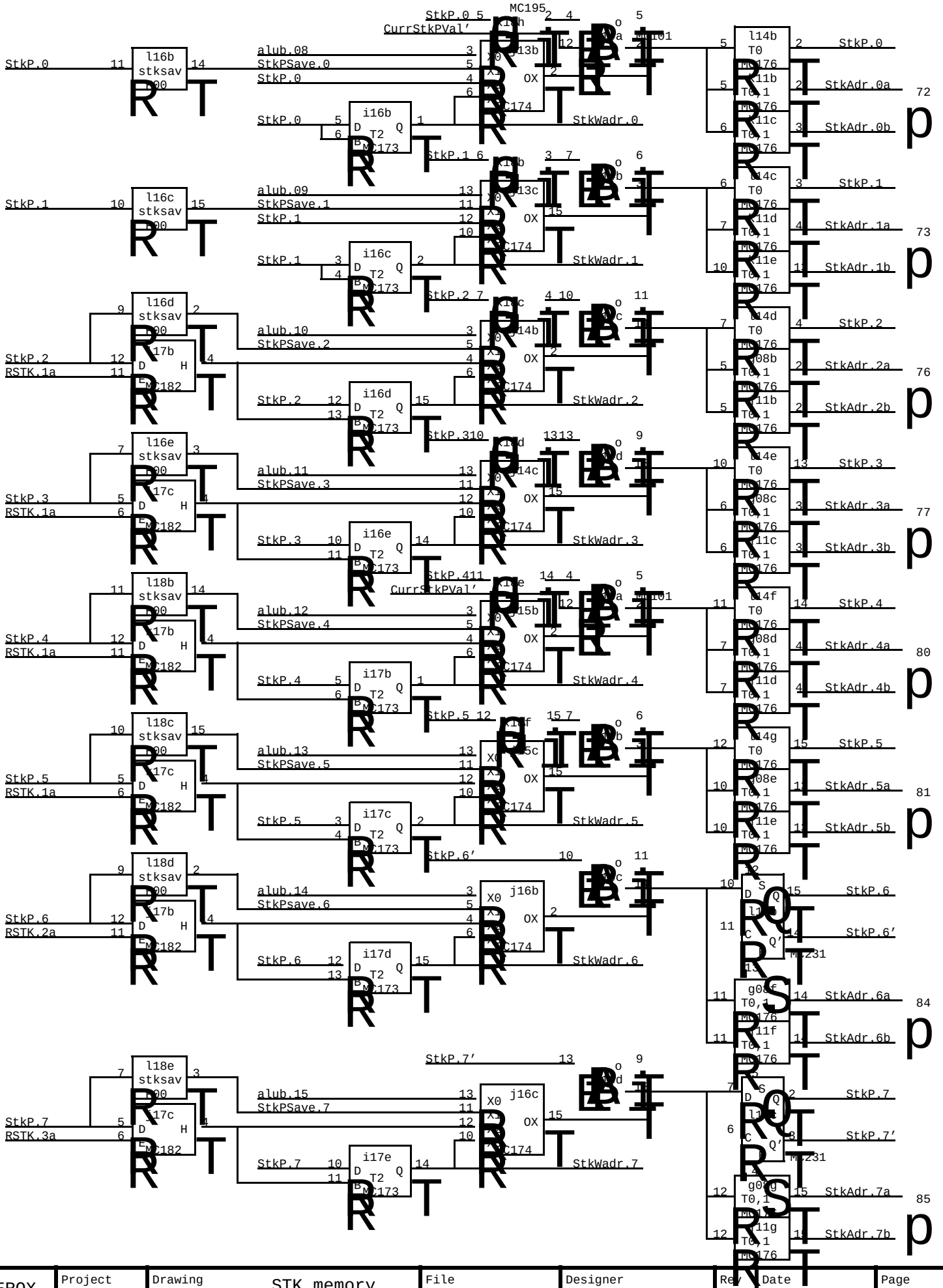


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	R memory Address logic	ProcL23.sil	R Bates	Da	1/21/80	23

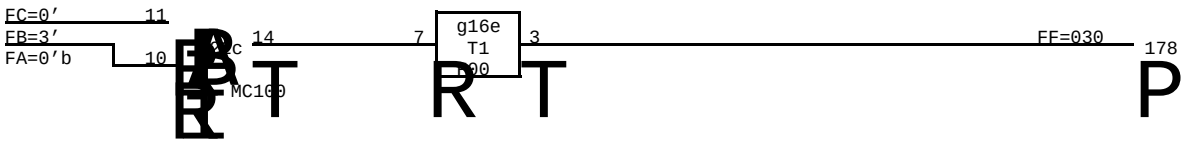




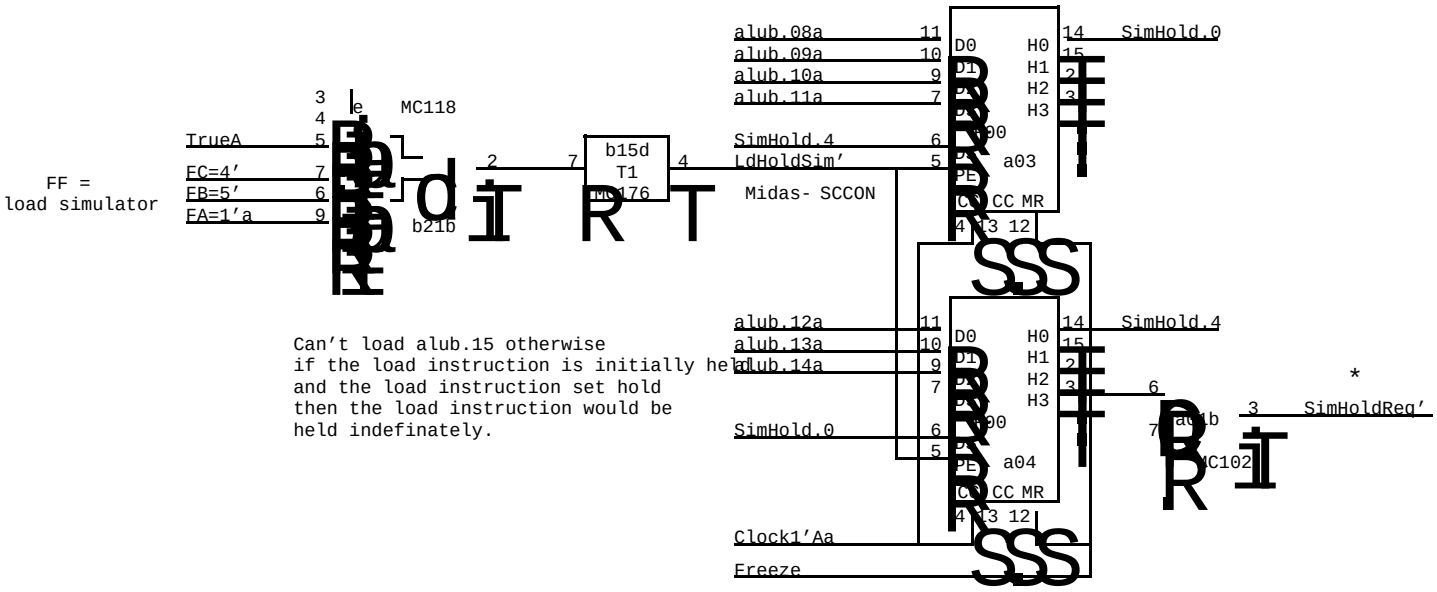
XEROX PARC	Project	Drawing	Title	Designer	Rev	Date	Page
	Dorado	Stk Control and Overflow / Underflow Ck	ProcL24.sil	R Bates	Da	1/21/80	24



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	STK memory Address logic	ProcL25.sil	R Bates	Da	6/28/79	25

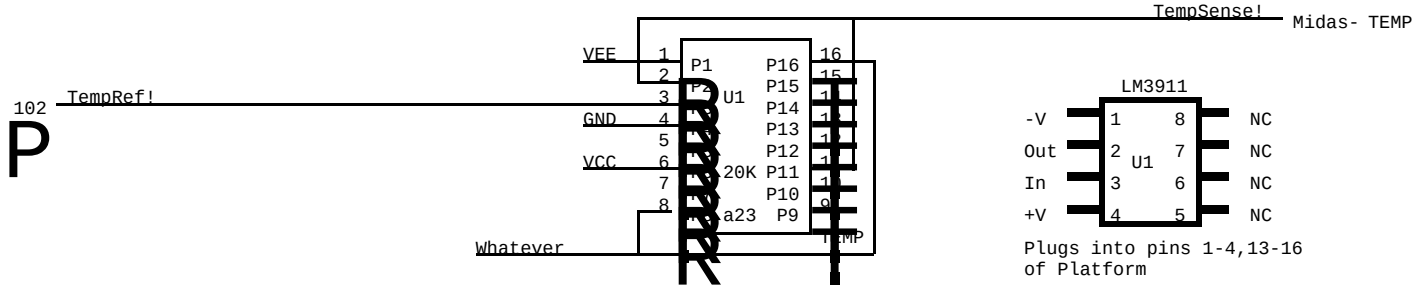


Spare FF Decode

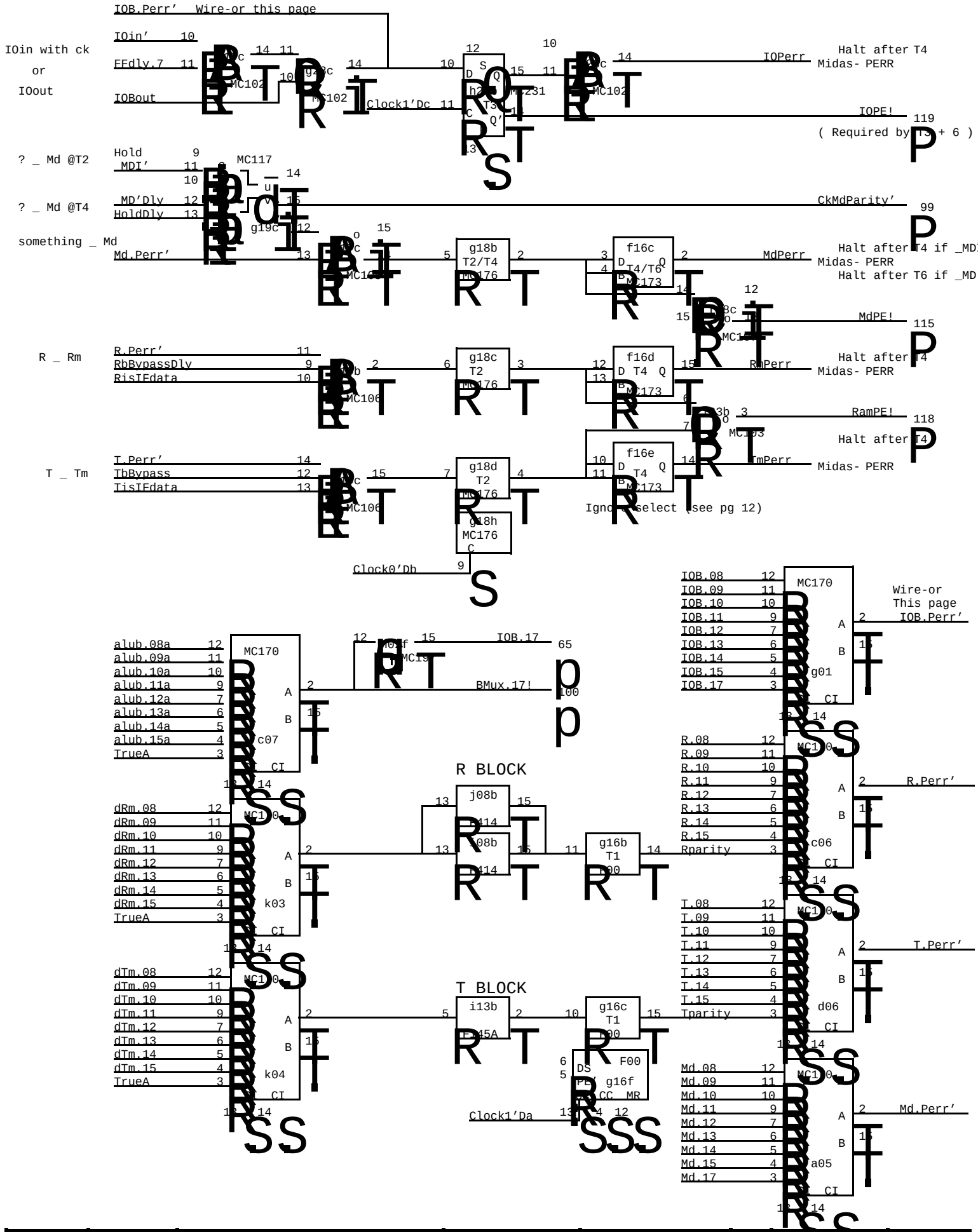


Hold Simulator

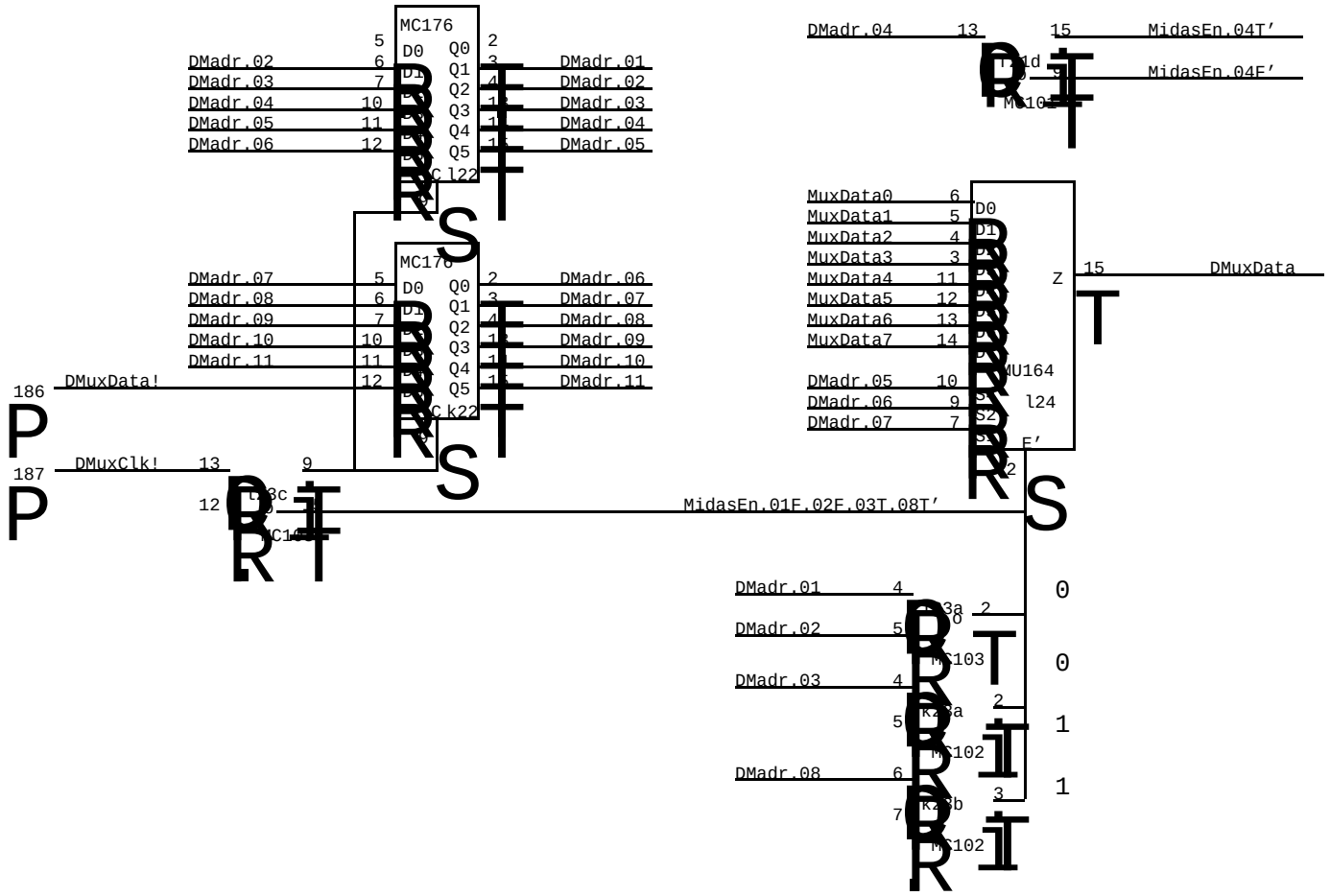
Temperature Sensing Ckt



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Task Simulator and Temperature Sense	ProcL26.sil	R Bates	Da	6/28/79	26

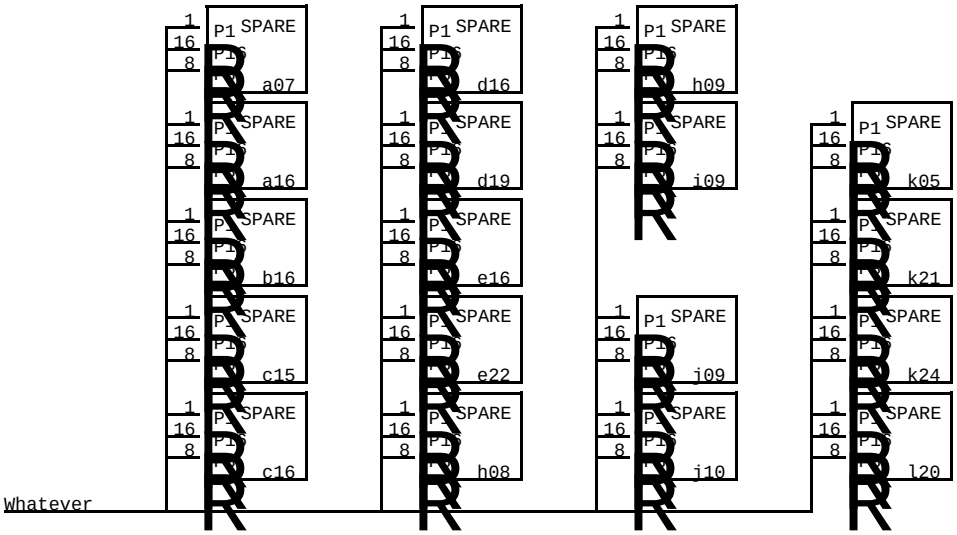


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Parity Logic	ProcL27.sil	R Bates	Da	6/27/79	27



Midas Control

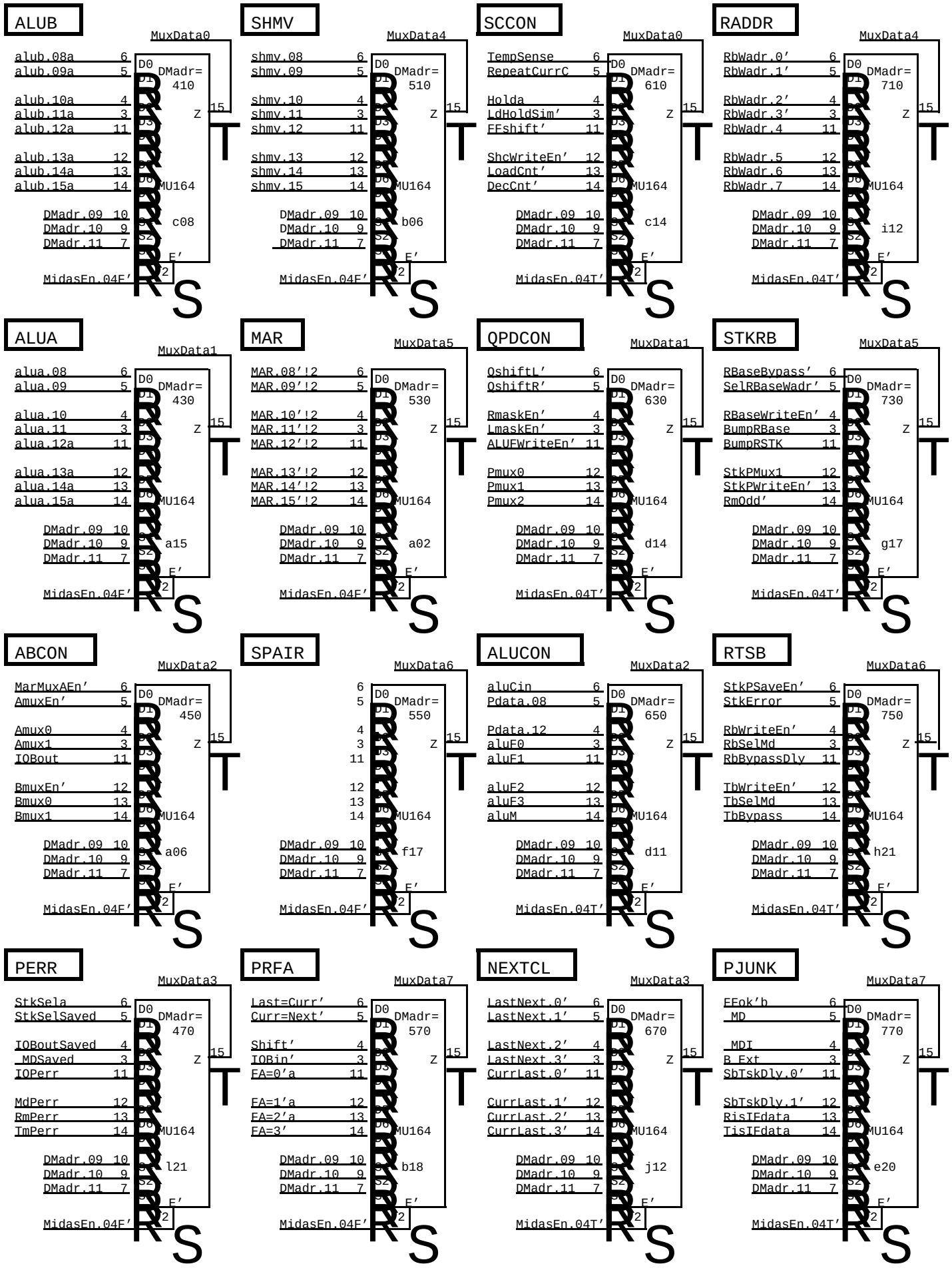
Spair Socket Declarations



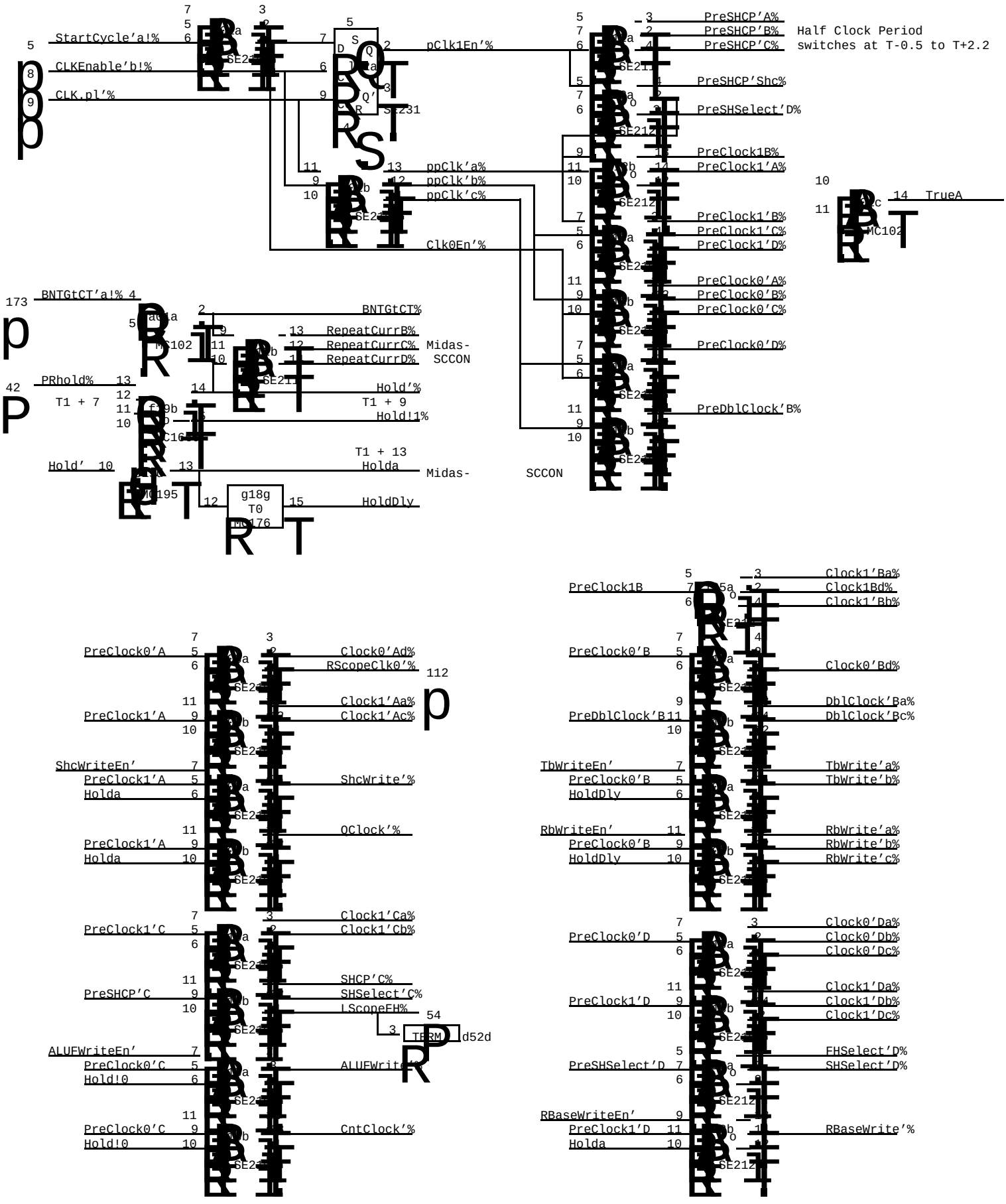
These should be the entire collection of unused locations.

This declaration will cause holes to be drilled in these locations on multiwire boards.

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Midas Control	ProcL28.sil	R Bates	Da	1/21/80	28



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	DMUX MUFFLERS	ProcL29.sil	R Bates	Da	6/27/79	29



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CLOCK DRIVERS	ProcL30.sil	R Bates	Da	6/27/79	30

-2v TIOA IOB IOB Clk +12v

	A (184)	B (168)	C (152)	D (136)	E (120)	F (102)	G (84)	H (68)	I (52)	J (36)	K (20)	L	
1	MC102 III.	Ex Bmux MC174 X	Ex Bmux MC174 X	Ex Bmux MC1662 X	Ex Bmux MC174 X	Ex Bmux MC174 X	IOB par MC170 X	IOB MC197 X	Md MC175 X	dRm Reg MC173 X	dTm Reg MC173 X	Clocks SE210 II	1
41													41
2	MAR MU164 X	Mar Mux MC159 X	Mar Mux MC159 X	Ex Bmux MC1662 X	Mar Mux MC159 X	Mar Mux MC159 X	Pdata MC164 X	IOB MC197 X	Md MC175 X	dRm Reg. MC173 X	dTm Reg. MC173 X	Clocks SE231 II	2
3	SimTW F00 X	Amux MC174 X	Amux MC174 X	Amux MC174 X	Amux MC174 X	Pdata MC164 X	Pdata MC164 X	Pdata MC164 X	T Reg. MC173 X	dT Reg. MC173 X	dRm Par. MC170 X	T Mem. MC145 X	3
42													42
4	SimTW F00 X	Bmux MC174 X	Bmux MC174 X	Bmux MC174 X	Bmux MC174 X	Pdata MC164 X	Pdata MC164 X	Pdata MC164 X	T Reg. MC173 X	dT Reg. MC173 X	dT par. MC170 X	T Mem. MC145 X	4
5	Md Parity MC170 X	Amux In MC173 X	Bmux In MC173 X	Amux In MC173 X	Bmux In MC173 X	Pdata MC164 X	dR Reg. MC173 X	dR Reg. MC173 X	Clocks SE212 I.	Clocks SE210 II		RSTK MC101	5
43													43
6	Mux Cont MU164	Shmv MU164 X	R Parity MC170 X	T Parity MC170 X	Pdata in MC173 X	Pdata in MC173 X	R Reg. MC173 X	Rm Mem. MB071 X	Stk Mem. MB071 X	Rm Mem. MB071 X	Stk Mem. MB071 X	Rodd MC1668 II	6
7		Shmv MC139 X	alub Par MC170 X	alua-a MC101	ShA MC158 X	ShA MC158 X	R Reg. MC173 X					Rodd MC1668 II	7
44													44
8	Clocks SE210 II	Shmv MC139 X	alub MU164 X	alu=0 MC109 II	AhB MC158 X	AhB MC158 X	StkPadrT01 MC176 X		Stk parity F414 X	Rm parity F414 X	RbAdr MC1662 X	Rodd MC211 II	8
9	Clocks SE210 II	alub-a MC1664 X	alub-a MC1664 X	alu MC181 X		alu MC181 X	R/stk sel MC117 X				RbAdr MC1662 X	Rodd MC211 II	9
45													45
10	Amux T1 MC231 II	Bmux T1 MC231 II	Mux T1 MC176 IIIIII				RbAdr MC231 X	RbAdr MC231 X	RBase MC102		Clocks SE210 II	RbBypass MC1660 II	10
11	Amux T1 MC231 II	Mux T1 MC141 IIII	Q Reg. MC141 X	ALUFM MU164 X	alua sh MC159 X	alua sh MC159 X	CntMux MC159 X	CntMux MC159 X	RBase MC158 X	StkAdr T01 MC176 IIIIII	StkAdr T01 MC176 IIII.	Misc. MC231 II	11
46													46
12	Shc MC173 X	Shc MC173 X	Q Reg. MC141 X	Shc MC180 X	ALUFM MC176 IIIIII	Clocks SE212 II	Clocks SE211 II	RBase MC159 X	RmWadr MU164 X	NextLast MU164 X	RmBypass MC113 X	StkBypass MC113 X	12
13	Shc MC173 X	Shc MC173 X	Shc MC158 X	Shc MC180 X	ALUFM MC145 X	Clocks SE210 II	Clocks SE210 II	RBase MC159 X	T mem-P MC145 X	StkAdr MC174 X	RmBypass MC113 X	StkBypass MC113 X	13
47													47
14	Bmux In MC158 X	Bmux In MC158 X	Shc MU164 X	P mux MU164 X	ALUFM MC145 X	Pdata in MC159 X	RBase MC173 X	RbAdr T1 MC176 IIIIII	CurrLast' MC141 X	StkAdr MC174 X	StkAdr MC158 X	StkP MC176 X	14
15	alua MU164 X	Q Reg. MC176 IIIIII		Cnt Reg. F16 X	Cnt Reg. F16 X	Pdata in MC159 X	RBase MC145 X	RBase MC173 X	RBase T0 MC176 IIIIII	StkAdr MC174 X	Misc. MC107 III	StkP MC231 X	15
48													48
16						aluCin MC173 IIII	Parity T1 F00 IIII	RBase MC159 X	StkAdr MC173 X	StkAdr MC174 X	StkAdr MC158 X	StkPsave F00 X	16
17	Q Reg. MC113 X	Q Reg. MC119 X	Q Reg. MC119 X	Misc. T0 MC176 IIIIII	Misc. T1 MC176 I.III.	SPAIR MU164 X	Rm cont MU164 X	Misc. MC105 III	StkAdr MC173 X	StkP MC182 X	StkP MC182	StkP MC182 X	17
49													49
18	LastNext' MC158 X	FA MU164 X	Clocks SE210 II	Clocks SE210 II	P mux MC102 IIII	Misc. MC107 III	Misc. T0 MC176 IIIIII	RBase MC103 IIII	Clocks SE212 II	Clocks SE210 II	StkP MC195 X	StkPsave F00 X	18
19	LastNext' MC158 X	Misc. MC212 II	Amux MC121 X		Misc. MC195 III..,	MC1660 II	Parity MC117 II	Misc. MC102 IIII	Parity MC106 III	Ovfl-Ufl MC231 II	Ovfl-Ufl MC101 IIII	Ovfl-Ufl MC121 X	19
50													50
20	Last' MC141 X	FA=0 MC100 IIII	FA=2 MC100 IIII	FA=1 MC100 IIII	Misc. MU164 X	FA=0 MC100 IIII	FA=2 MC100 IIII	FA=0 MC106 III	ShI MC164 X	Ovfl-Ufl MC117 X	Ovfl-Ufl MC119 X		20
21	Curr' MC141 X	FA=1 MC118 II	Amux MC119 X	Amux MC117 X	Misc. MC102 IIII	ALUF MC101 IIII	B_Ext MC109 II	Rm cont MU164 X	ShI MC164 X	ShI MC164 X		Parity MU164 X	21
51													51
22	Next=Curr MC113 X	P mux MC212 II	Misc. MC102 IIII	_MDI MC121 X		FA=0 MC100 III.	Misc. MC103 IIII	Parity MC231 II	ShI MC164 X	ShI MC164 X	Midas MC176 X	Midas MC176 X	22
23	Temp LM3911 X	ASel MC101 IIII	FF dec. MC210 II	FF dec. MC101 X	FF-a MC101 X	FF-a MC101 X	Misc. MC102 IIII	LC dec. MC102 IIII	ShI MC164 X	ShI MC164 X	Misc. MC102 IIII	Misc. MC103 IIII	23
52													52
24	Next MC101 X	ALUF MC211 II	Misc. MC103 IIII	FF dec. MC101 X	FF dec. MC161 X	FF dec. MC161 X	MemBase MC231 II	BSel dec. MC101 IIII	ShI MC164 X	ShI MC164 X		Midas MU164 X	24

A (10) B (26) C (42) D (58) E (74) F (92) G (110) H (126) I (142) J (158) K (174) L

-5v Muffler +5v

Spare = 19

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Board Layout	ProcL31.sil	R. Bates	Da	1/21/80	31

Use Dorado Proms to define the following Proms:

Board Name	Prom Name		location
PorcL	Lmask	(low bite)	b07
	Rmask	(low bite)	b08