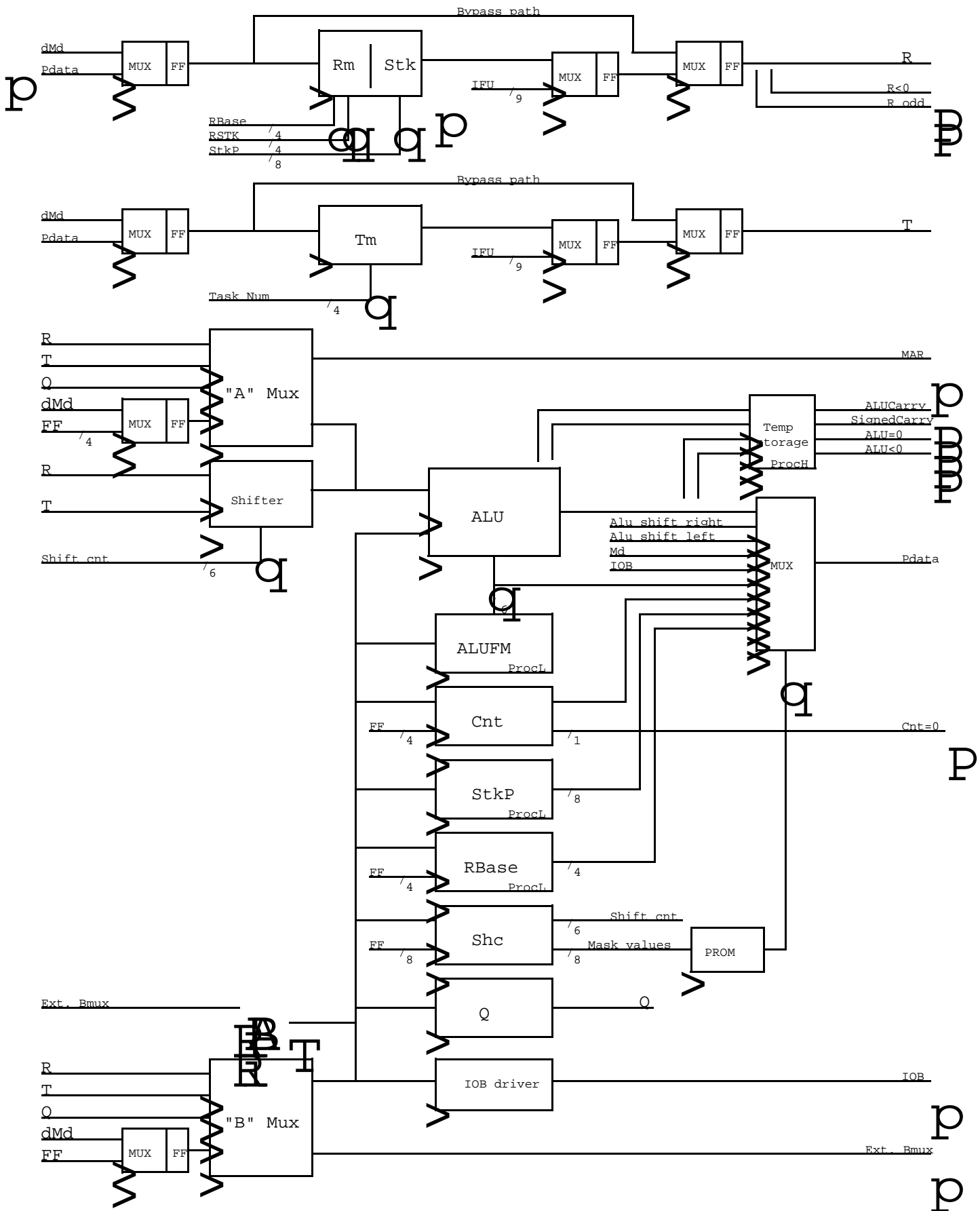
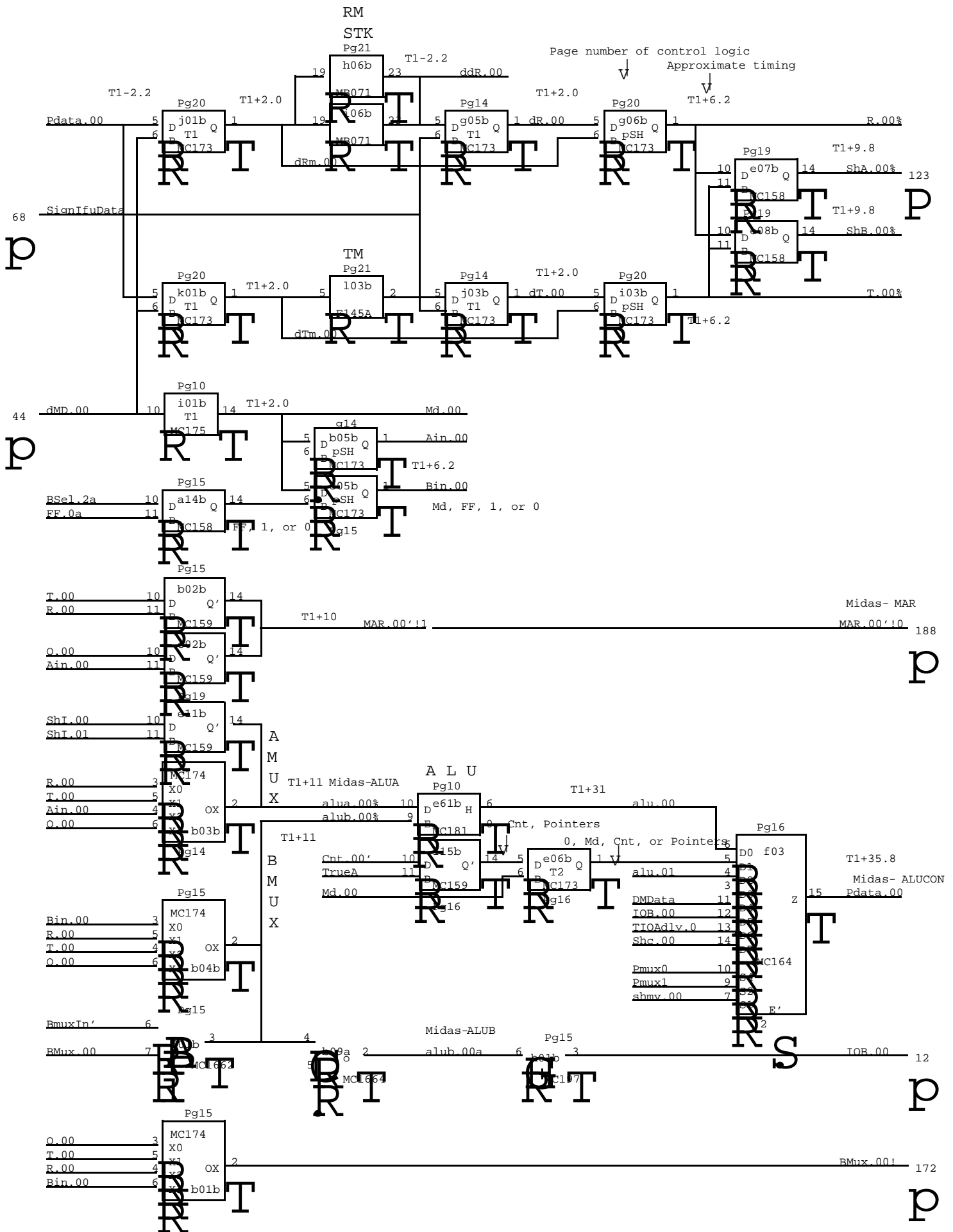


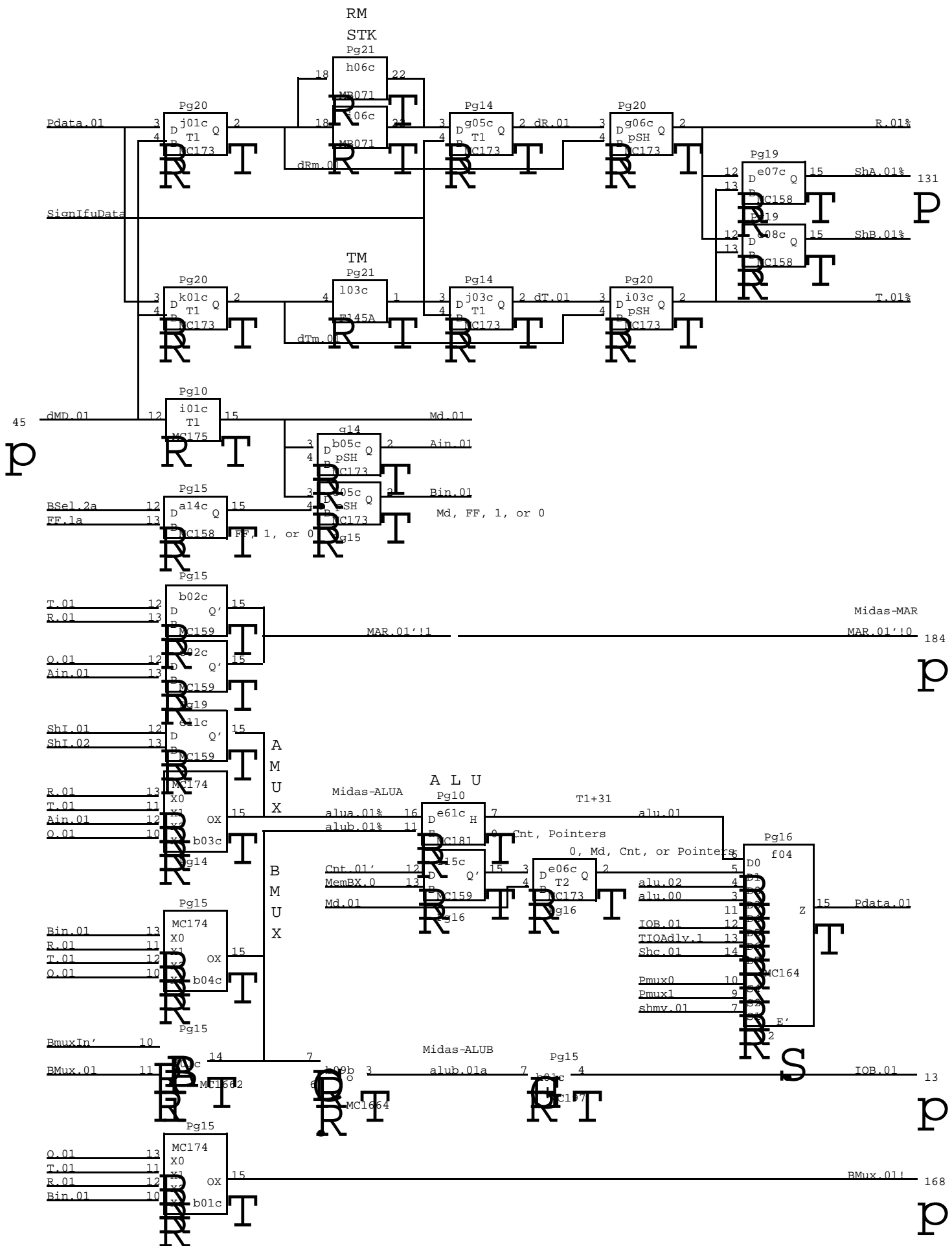
D O R A D O S C H E M A T I C S
H i B y t e
P R O C E S S O R

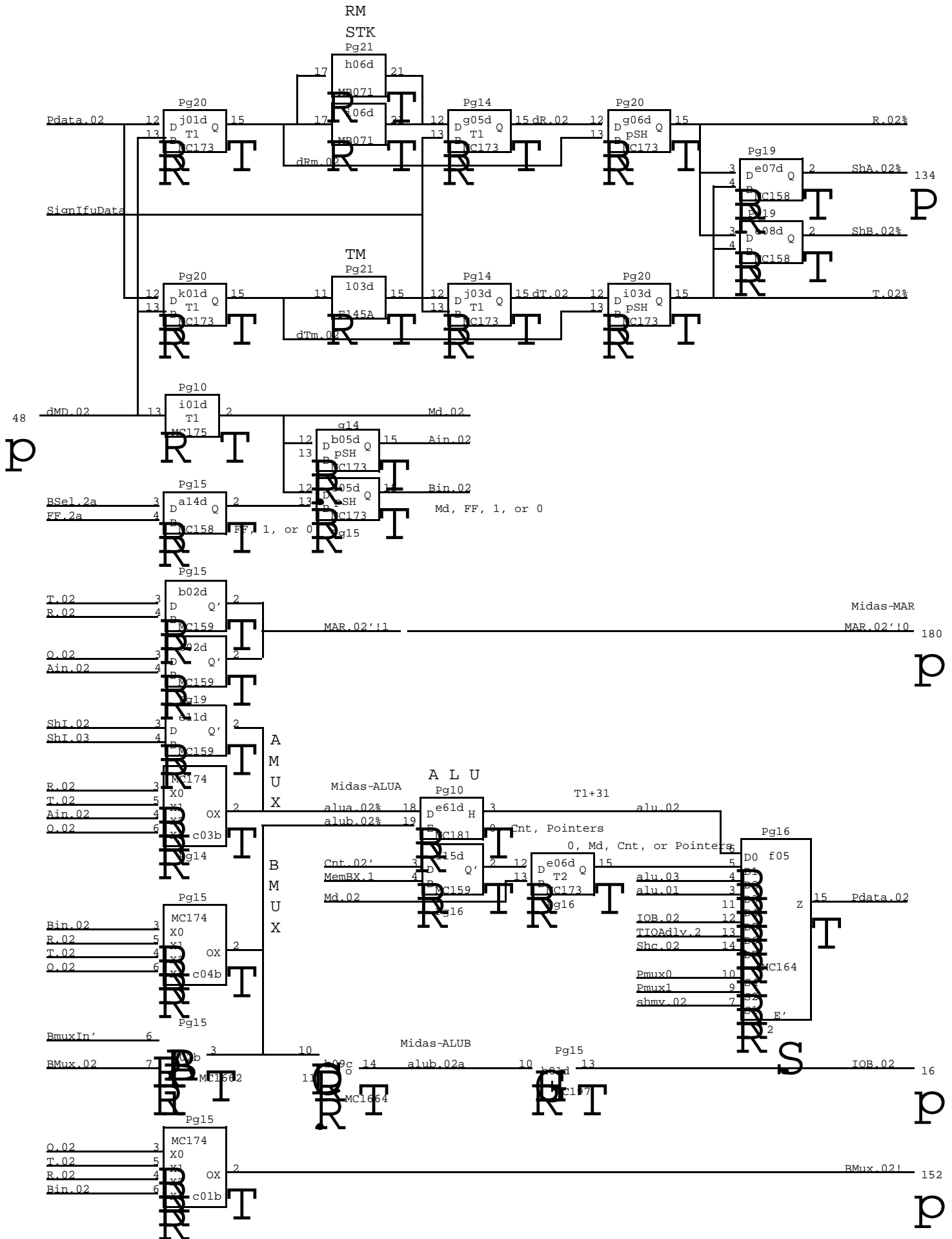
Table of contents

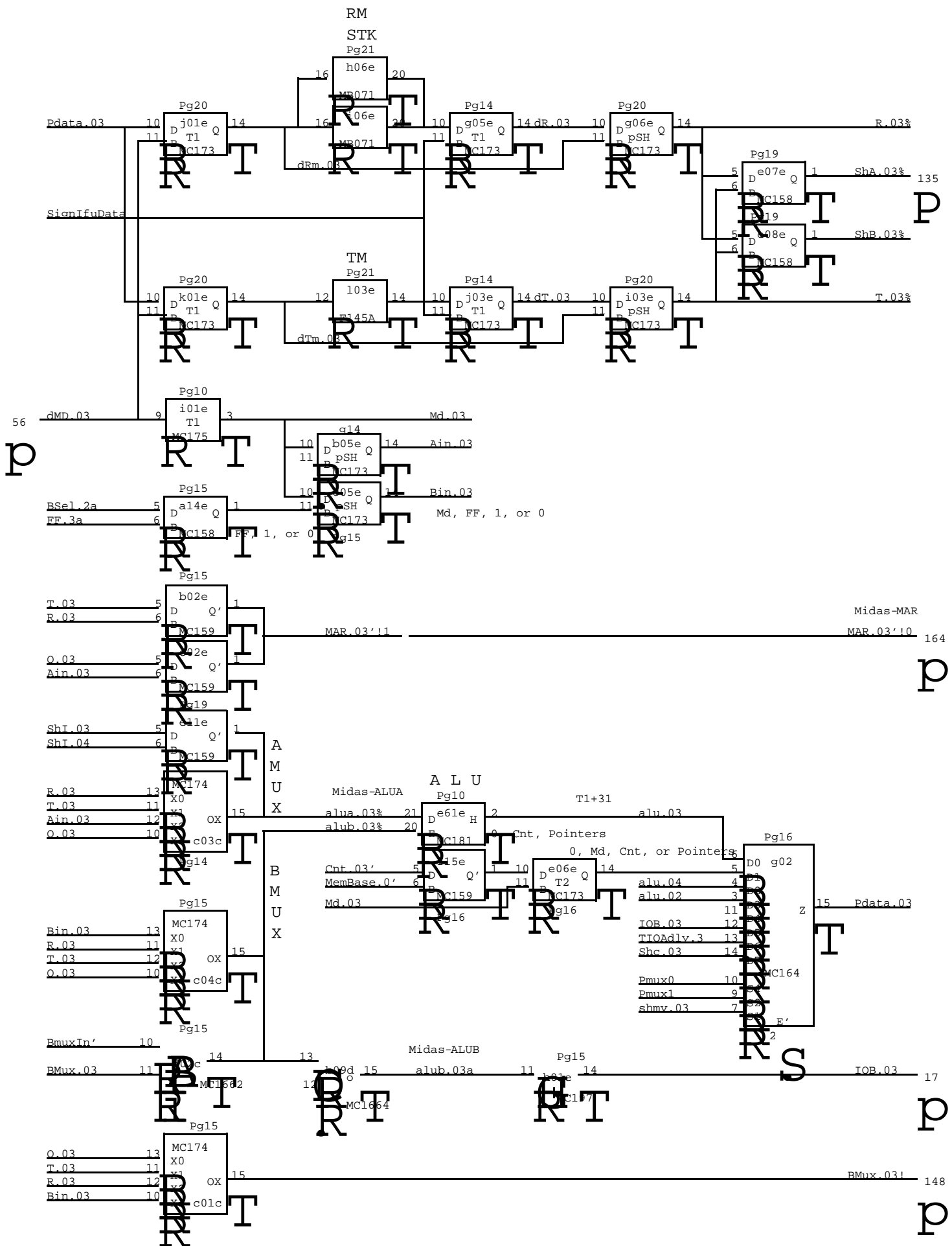
<u>TITLE</u>	<u>Page</u>
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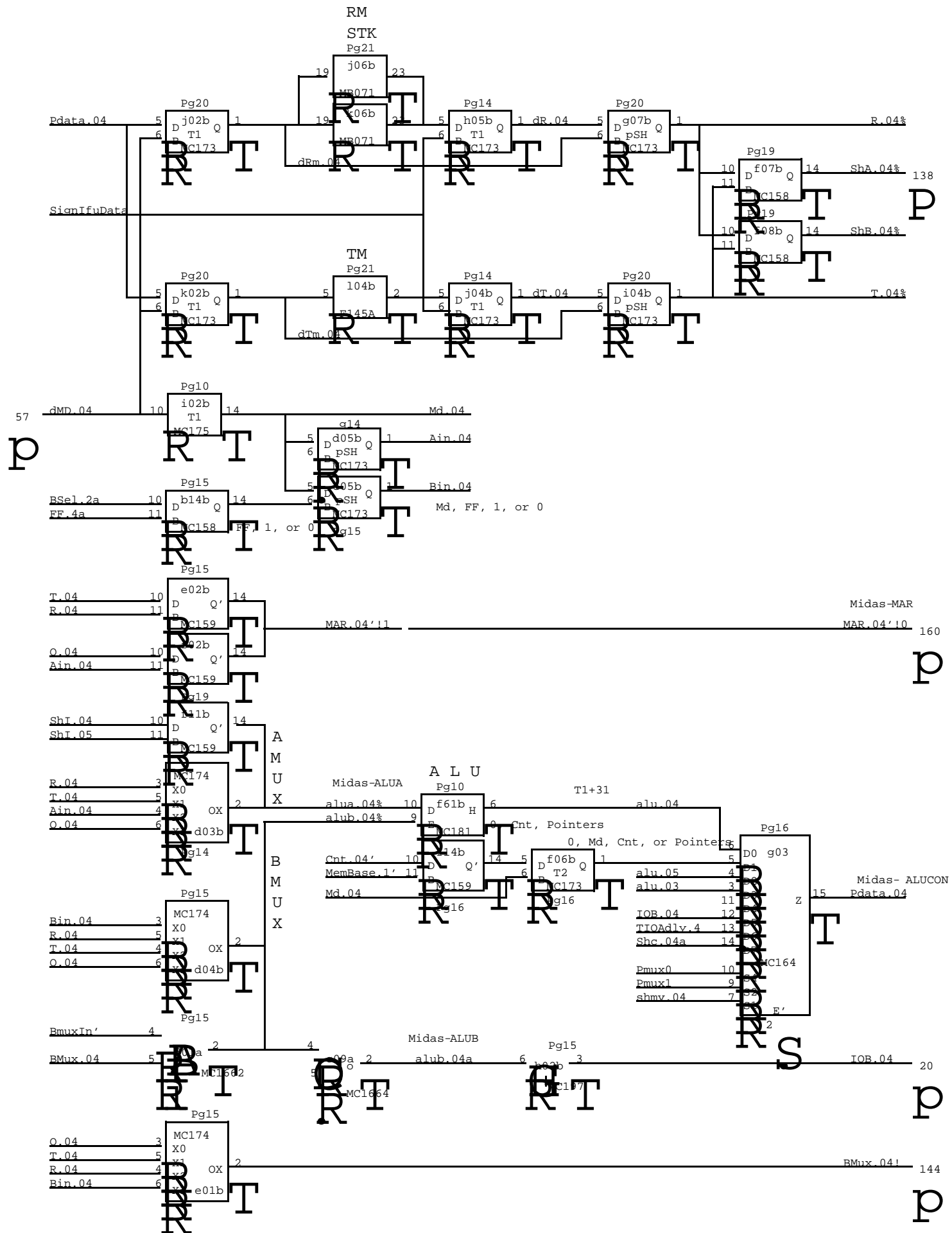


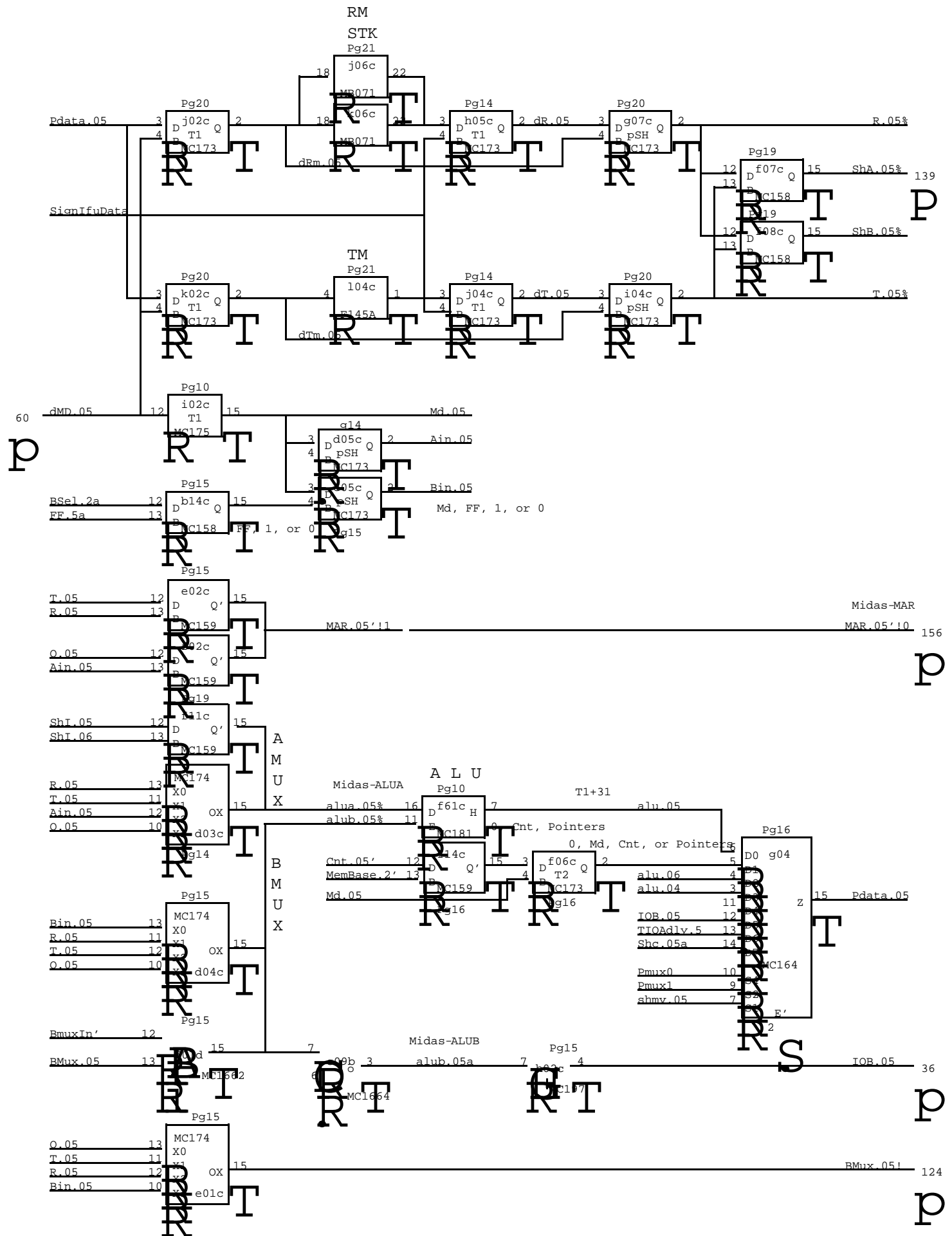


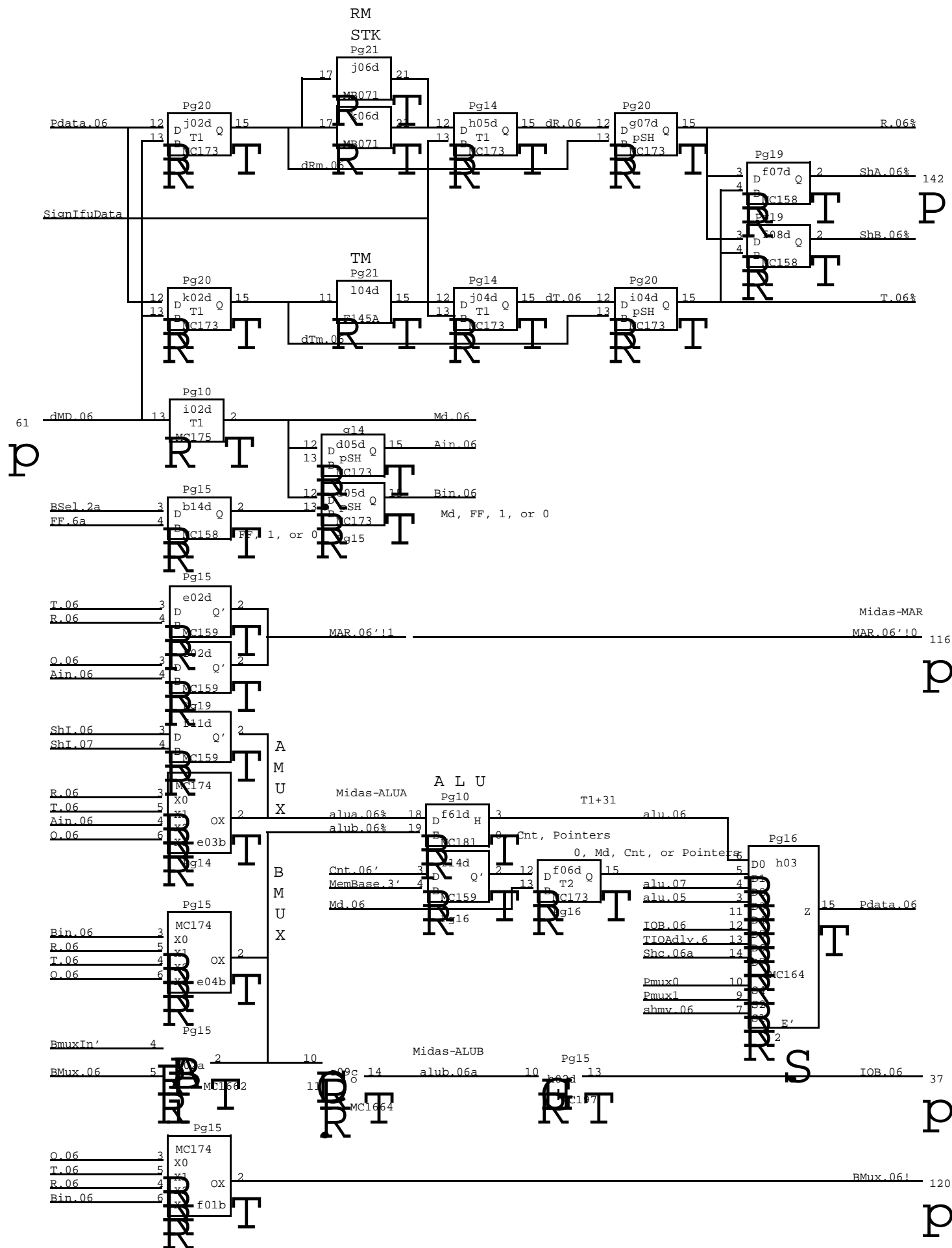


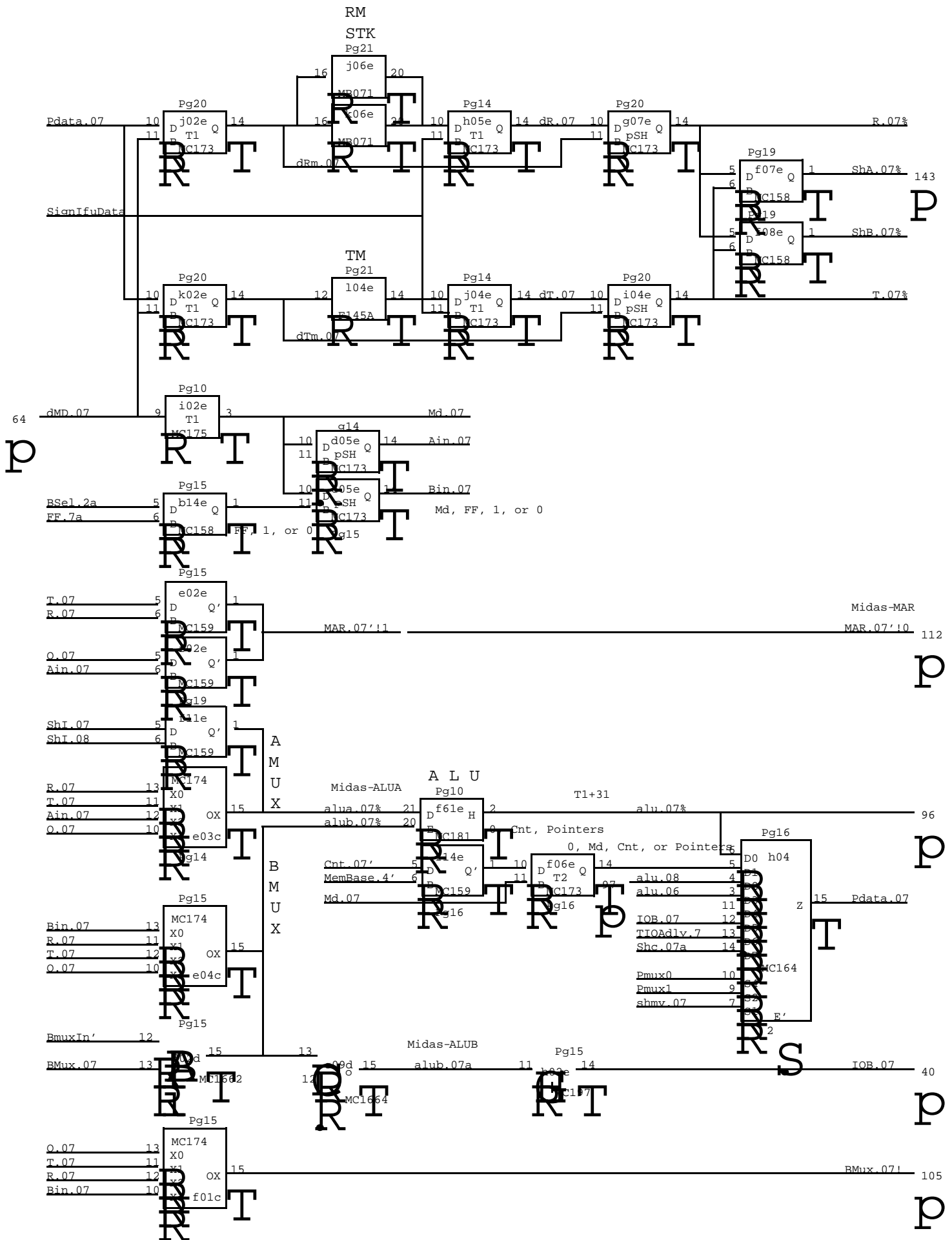










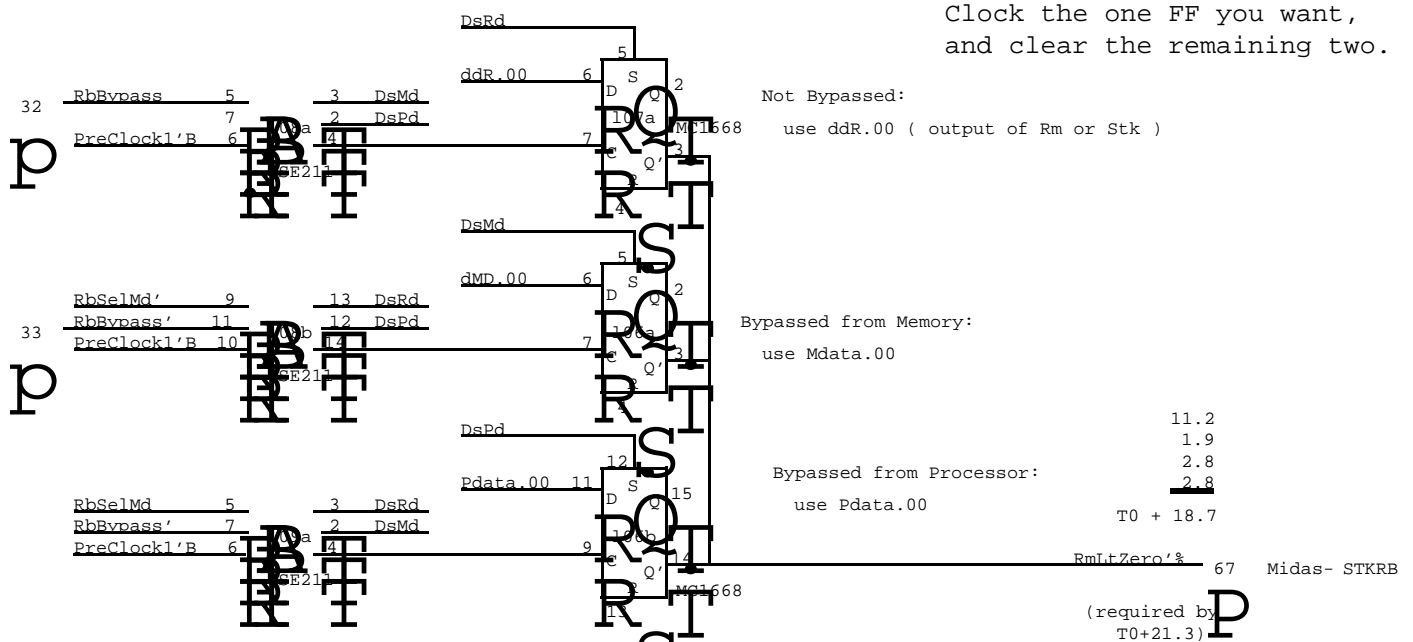
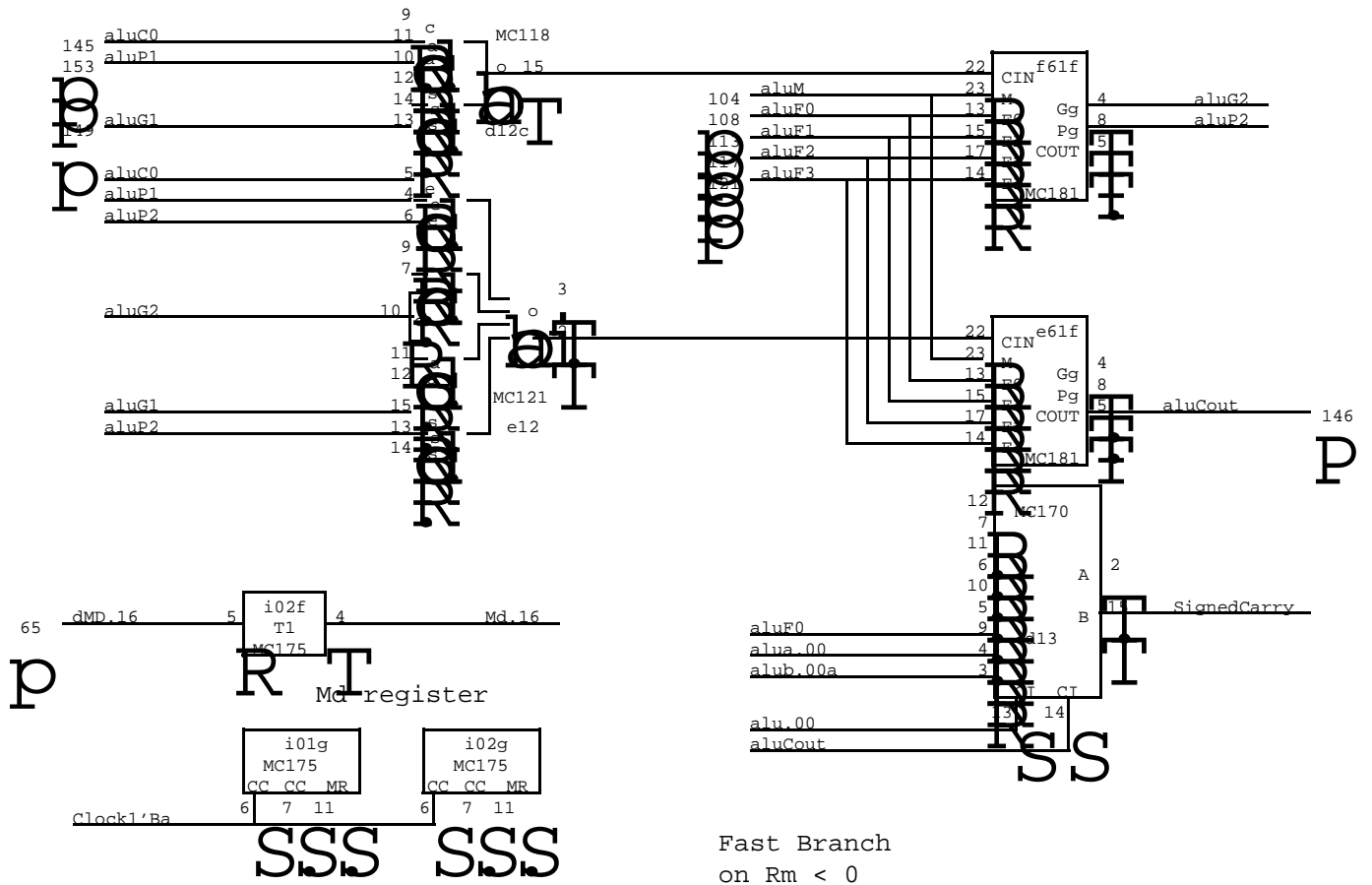


ALU delays

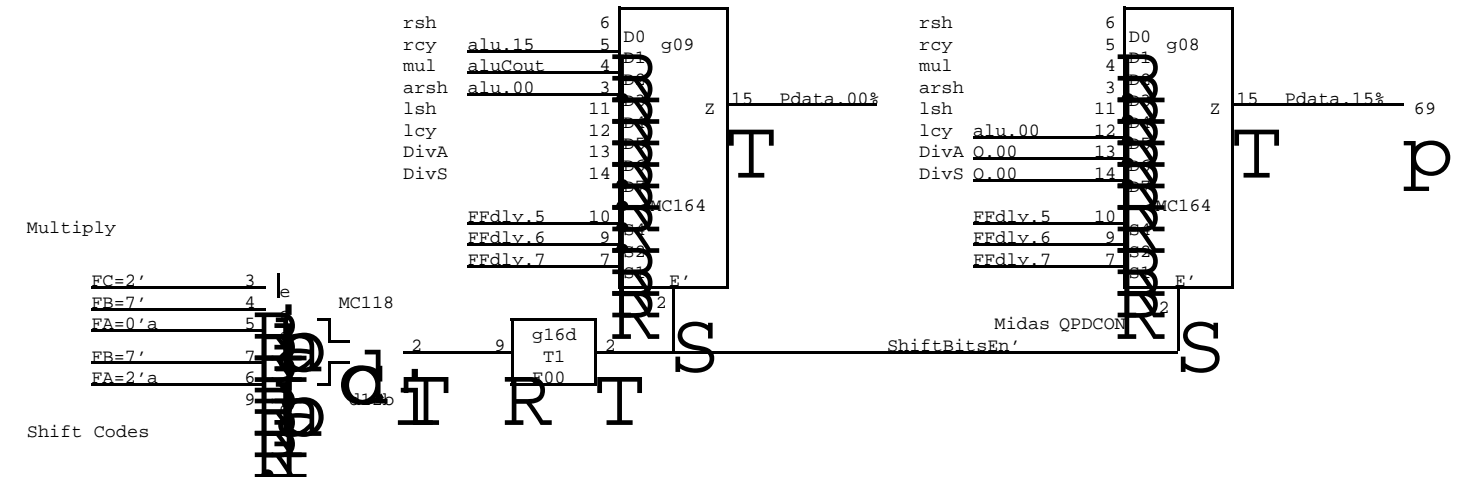
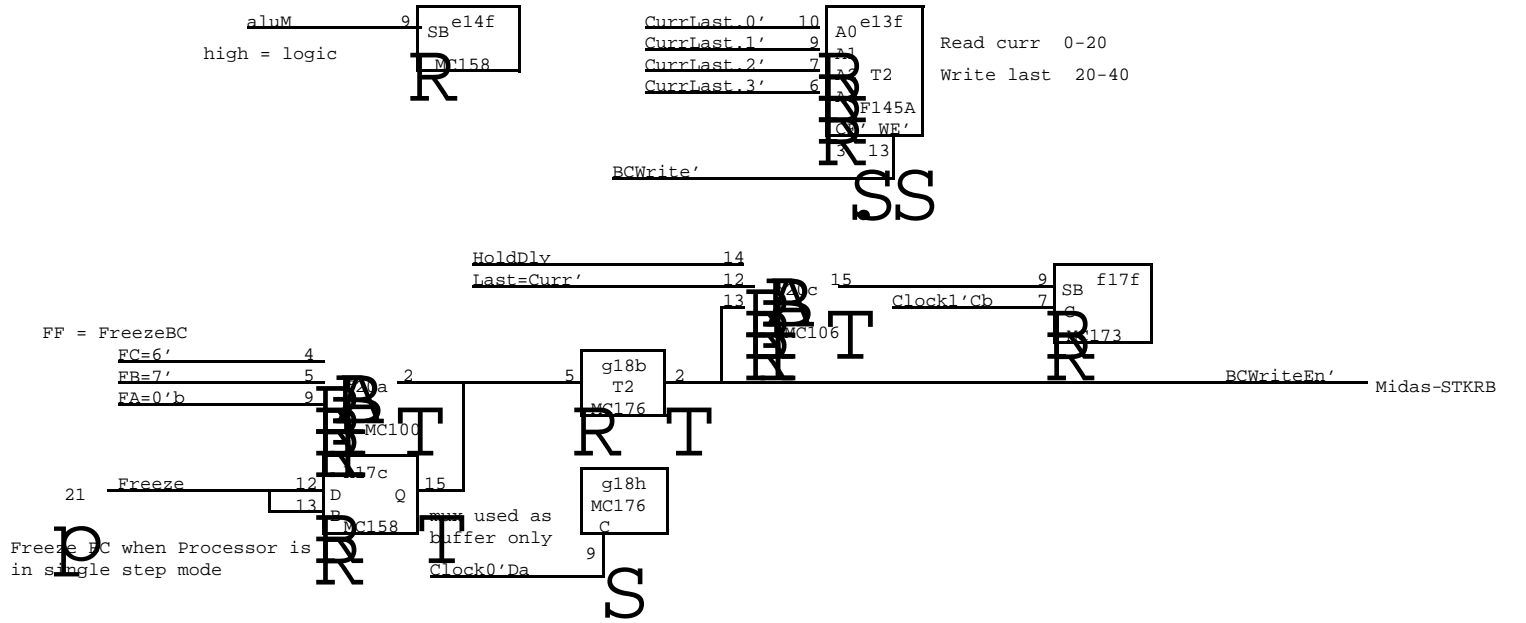
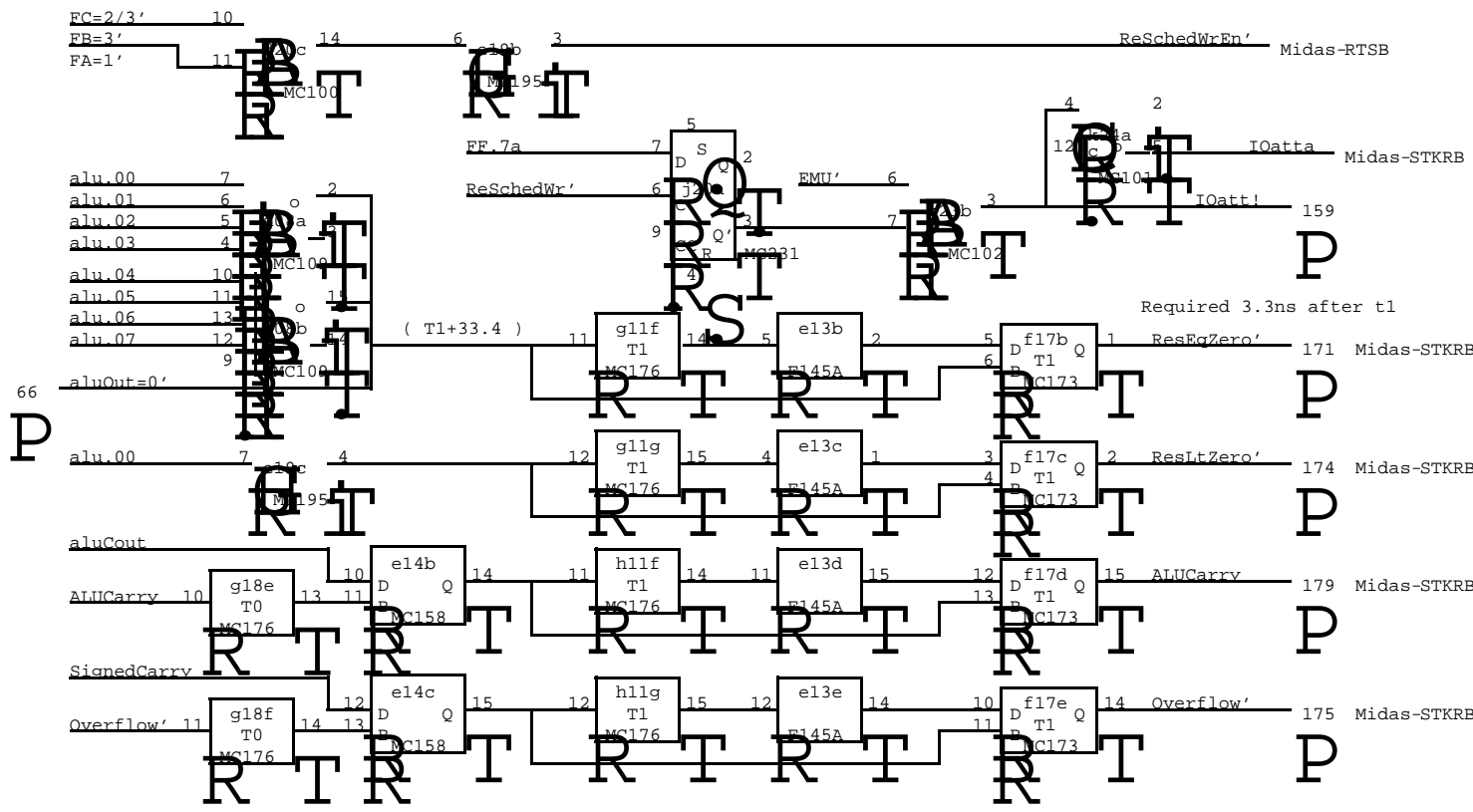
Logical function to output = 11.9
 Arithmetic operation to data = 20.0
 Arithmetic operation to carry = 17.9

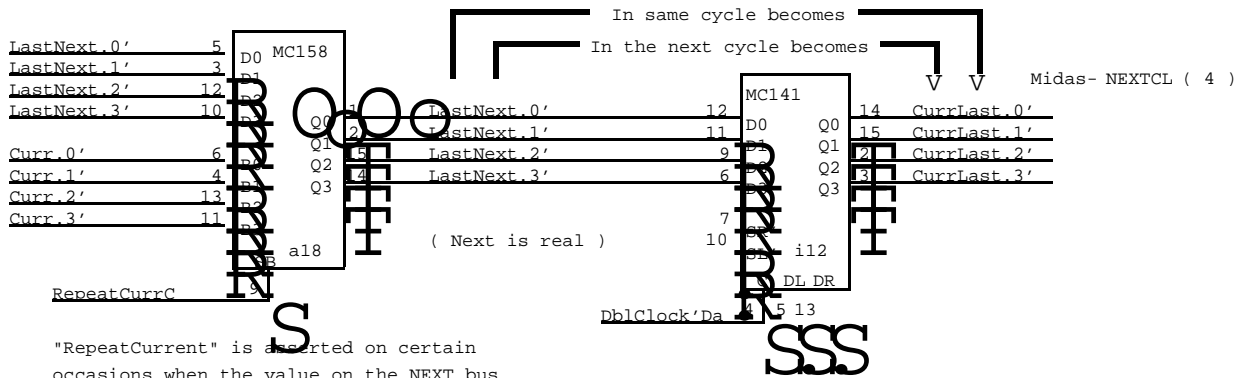
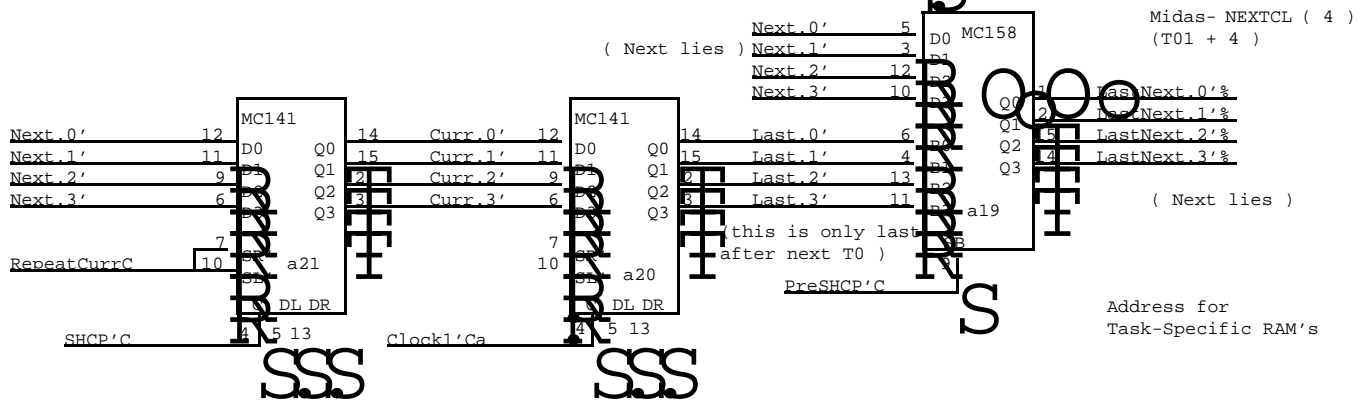
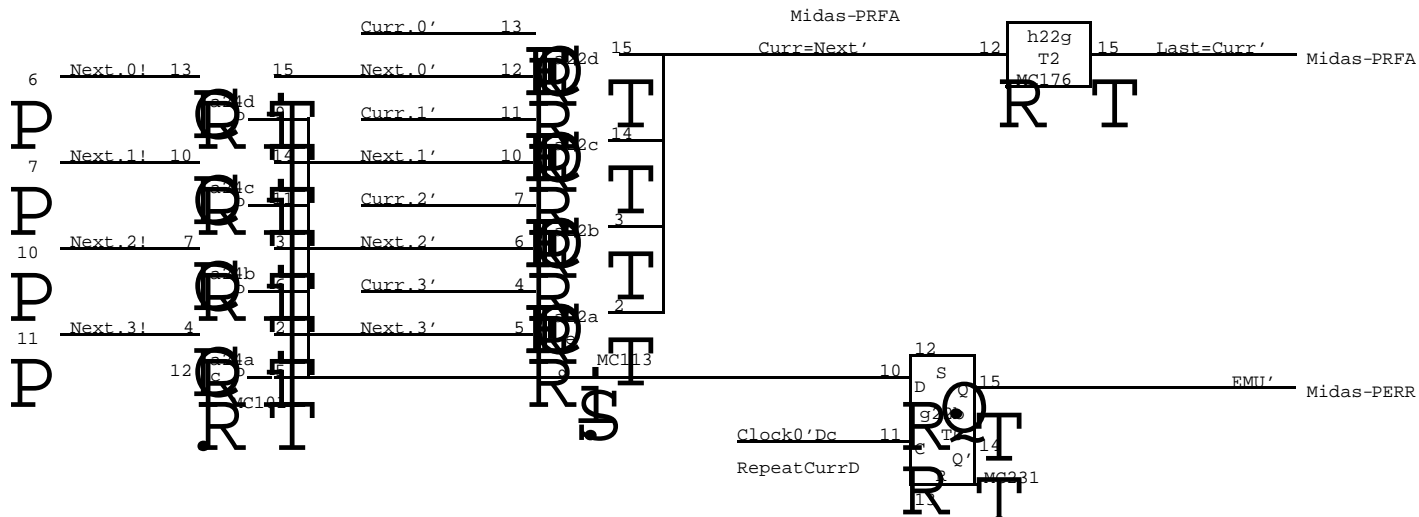
ALU output (assuming 10.2 ns to output of BMux)

Logical Function = 22.0
 Arithmetic operation to data = 30.1
 Arithmetic operation to carry = 28.0



This circuit will correctly bypass R from Pdata or Mdata. When "RisIfData" is in effect, the fast branch will be based on the contents of the addressed RM or STK, bypassed if necessary.

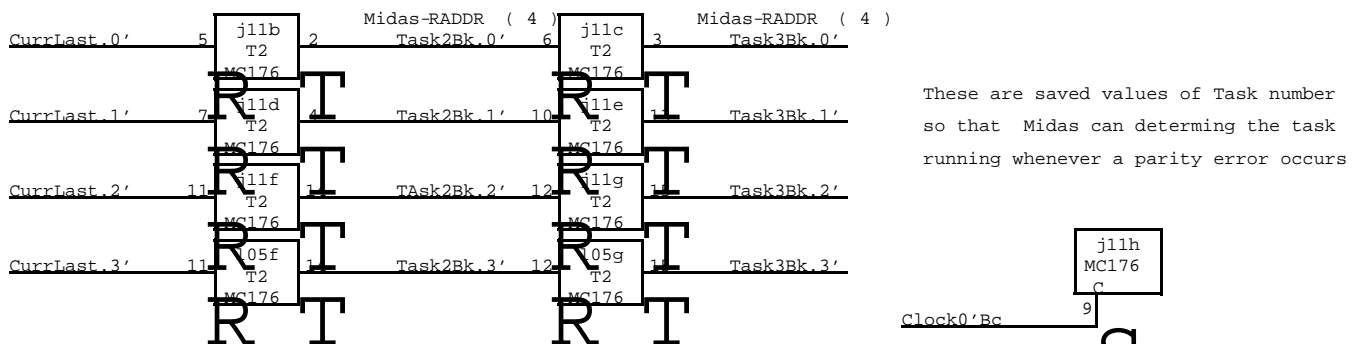




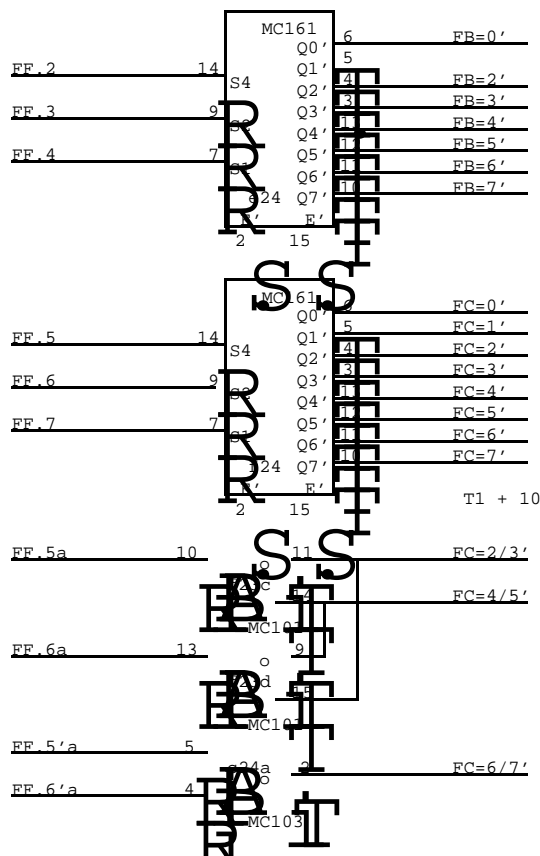
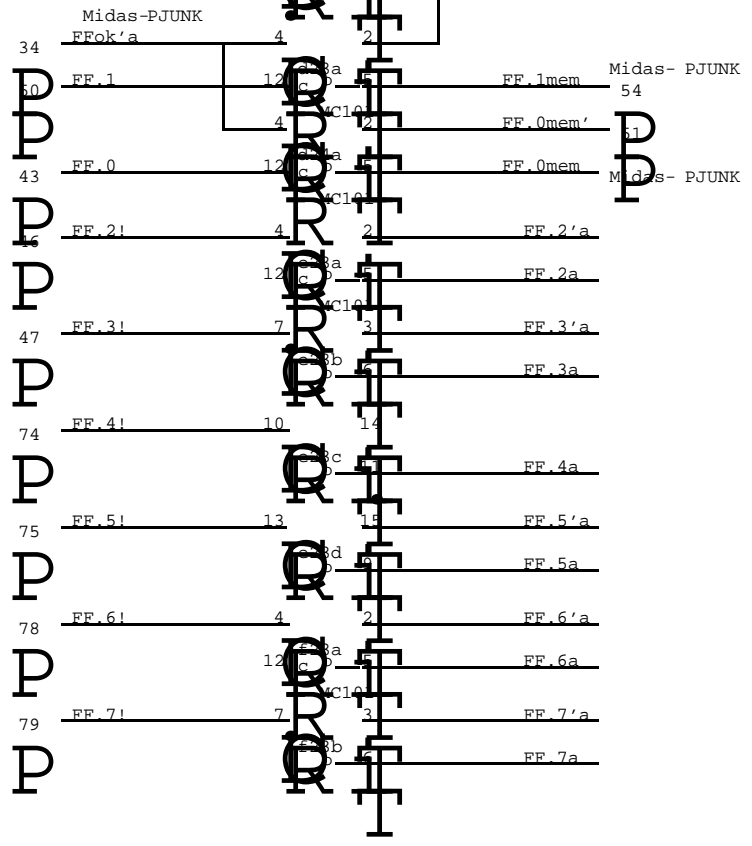
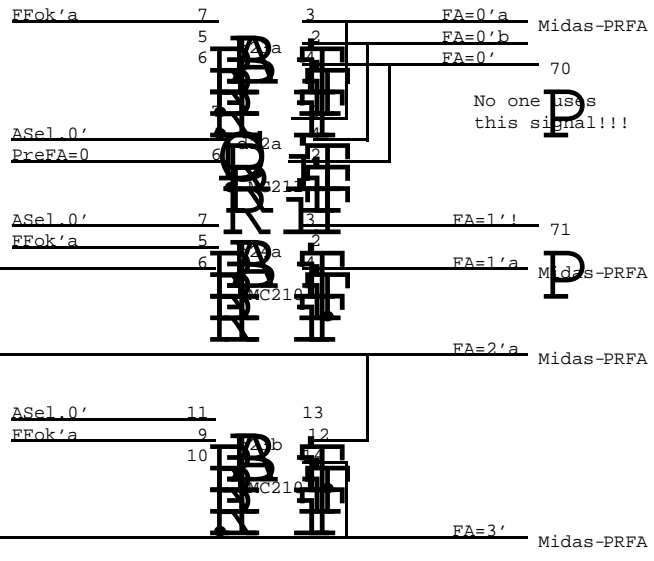
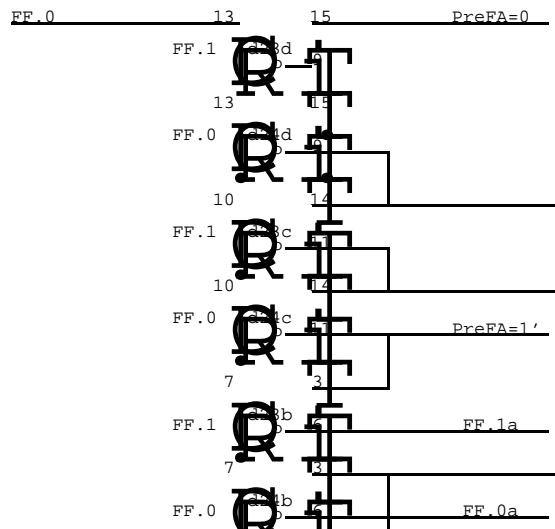
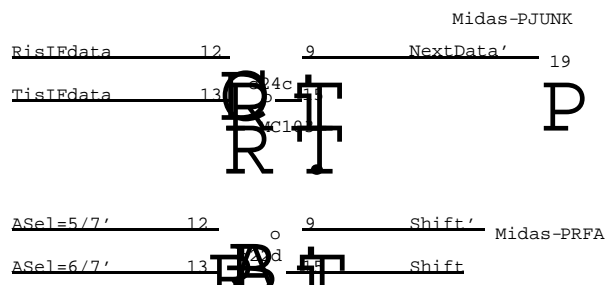
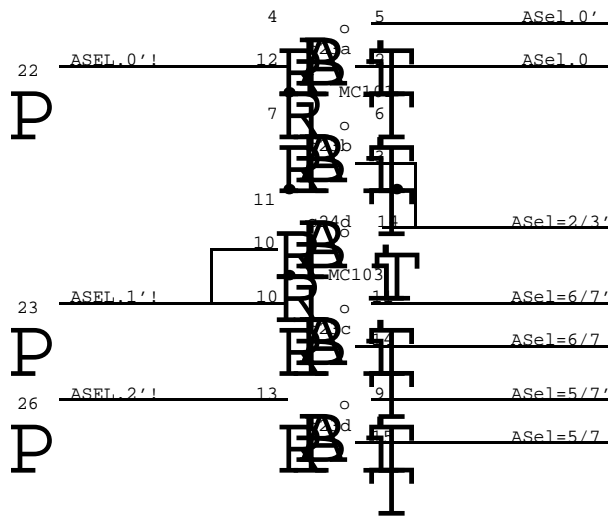
"RepeatCurrent" is asserted on certain occasions when the value on the NEXT bus may be invalid ("Next Lies") due to the combination of Block and Hold.

Task number tracking logic

Task number tracking logic (for Midas)



These are saved values of Task number so that Midas can determine the task running whenever a parity error occurs



AMux decoding

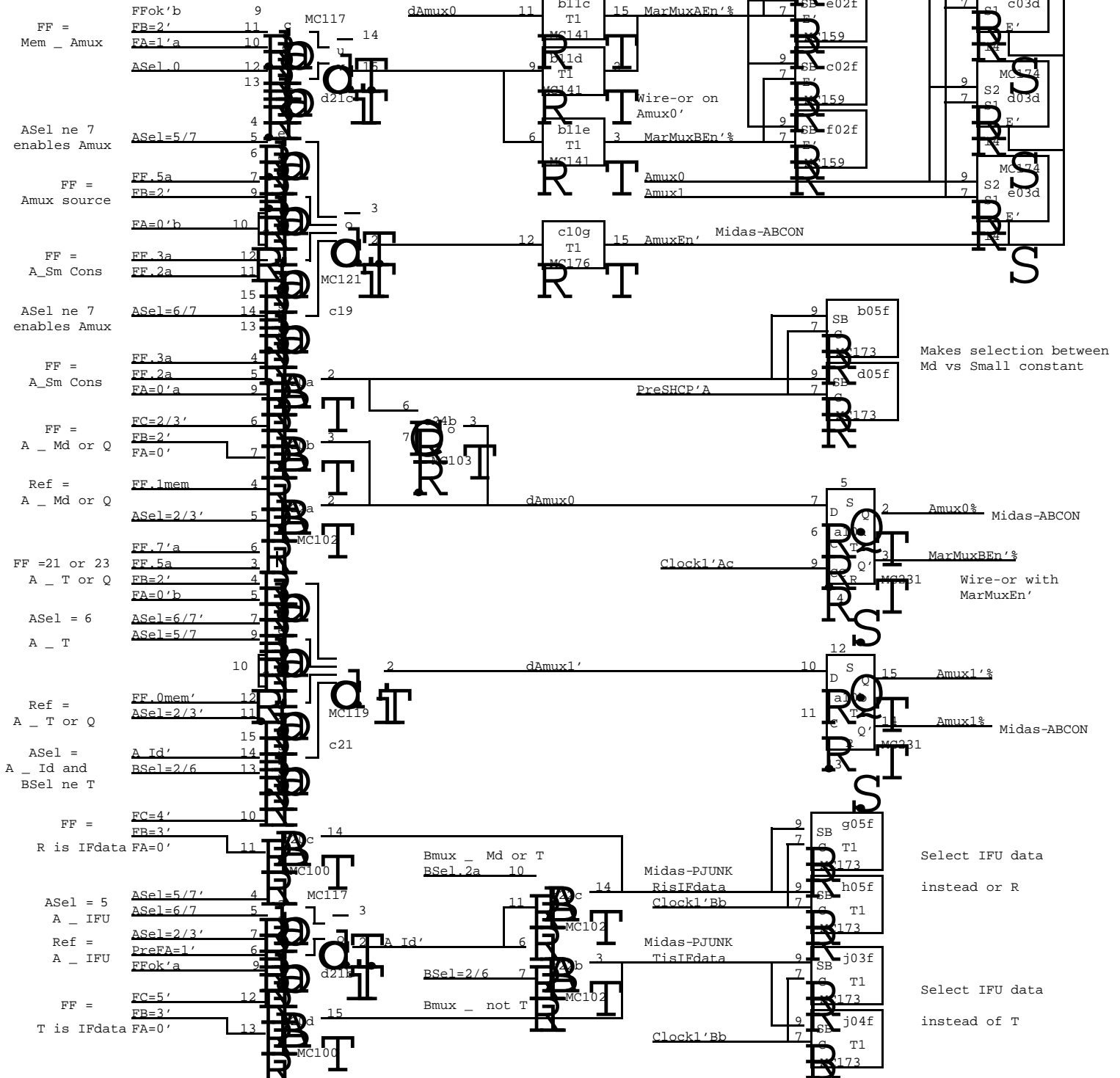
AMux _ FF:	FF=0-17 *
AMux _ T:	FF=021 * ASEL=2or3 & FAmem=3 ASEL=6
AMux _ Md:	FF=022 * ASEL=2or3 & FAmem=0
AMux _ Q:	FF=023 * ASEL=2or3 & FAmem=2
AMux _ IFU:	ASEL=5 ASEL=2or3 & FAmem=1
AMux _ R:	FF=020 * None of the above

AMux encoding

Mux Input	Source
0	R or IFU data
1	T or IFU data
2	Md or Small Const.
3	Q

* The Amux is disabled by ASEL=7 unless one of these codes are in effect

NOTE: ASEL selects and FF selects for the AMUX are "OR'd" by this hardware. Thus ASEL codes selecting non-Rm sources of Amux must not be used when an FF specifies an ASEL source. Likewise for FF when ASEL specifies non-Rm AMux sources.

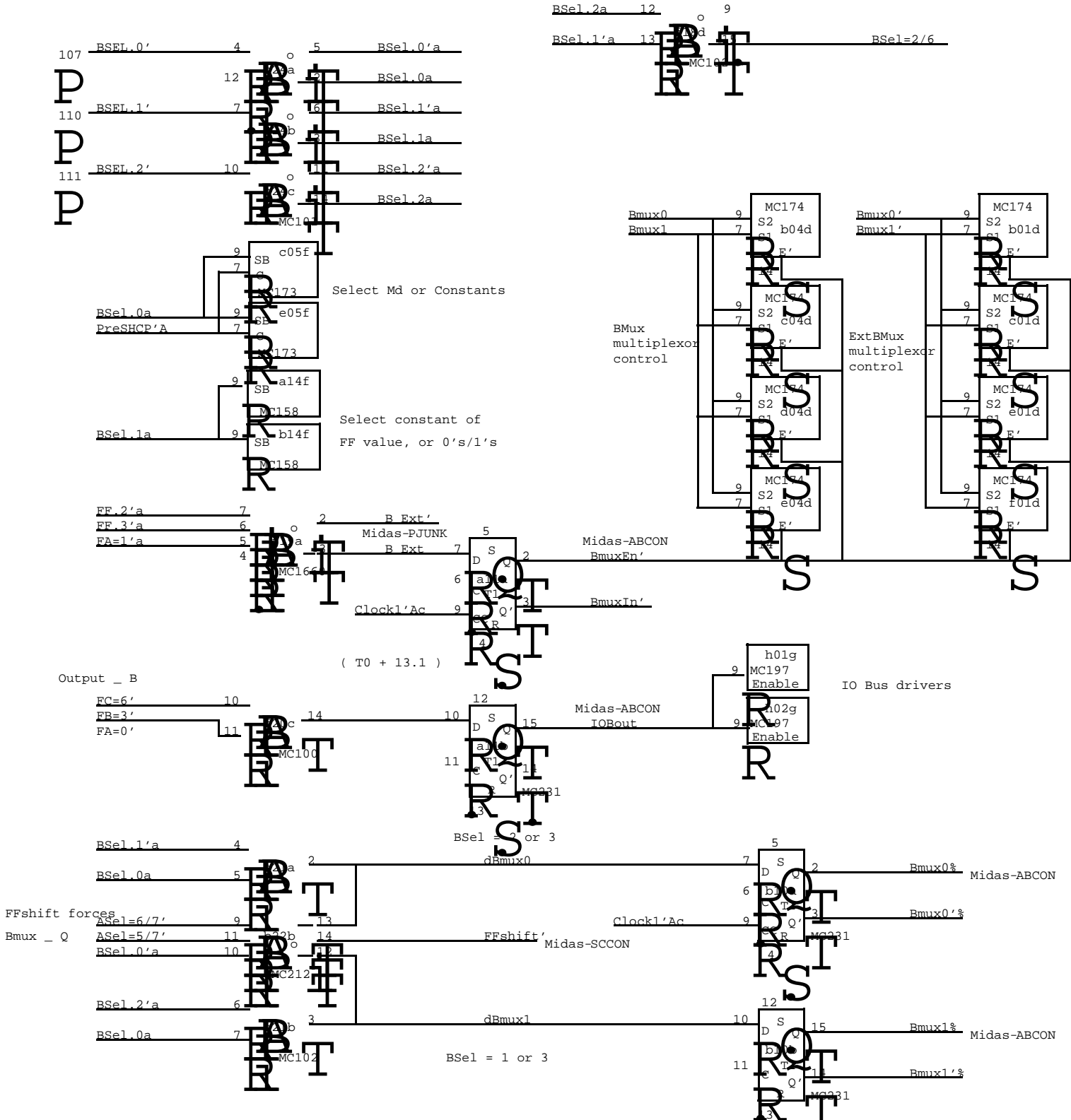


BSEL field decoding

BSEL	INTERNAL	EXTERNAL
0	Md	--
1	R	--
2	T	Hold_B
3	Q	Q _ B
4	0,,FF	--
5	377,FF	--
6	FF,,0	--
7	FF,,377	--

BMux encoding

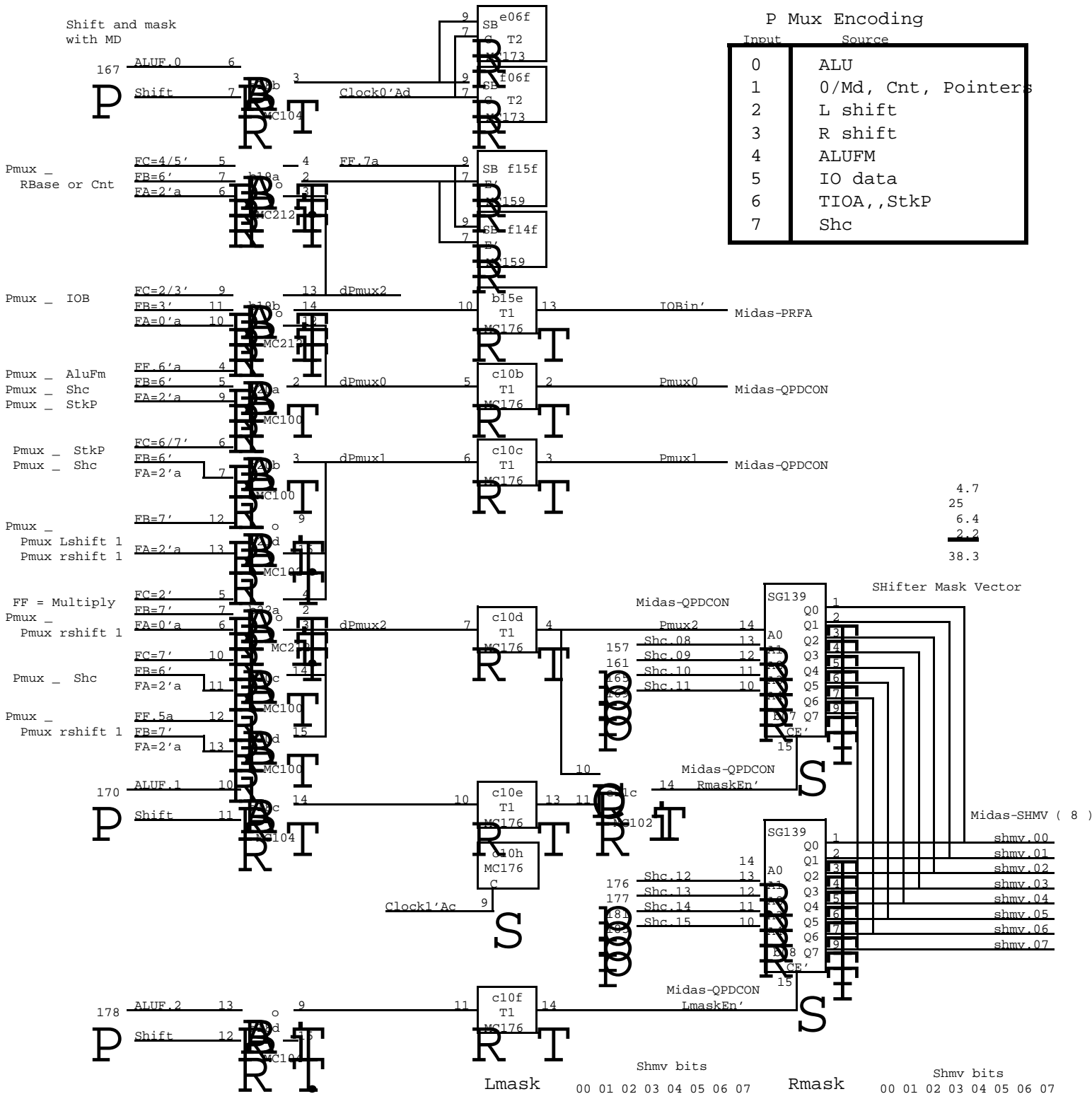
BMux	
0	Md or Constant
1	R
2	T
3	Q



Shift and mask
with MD

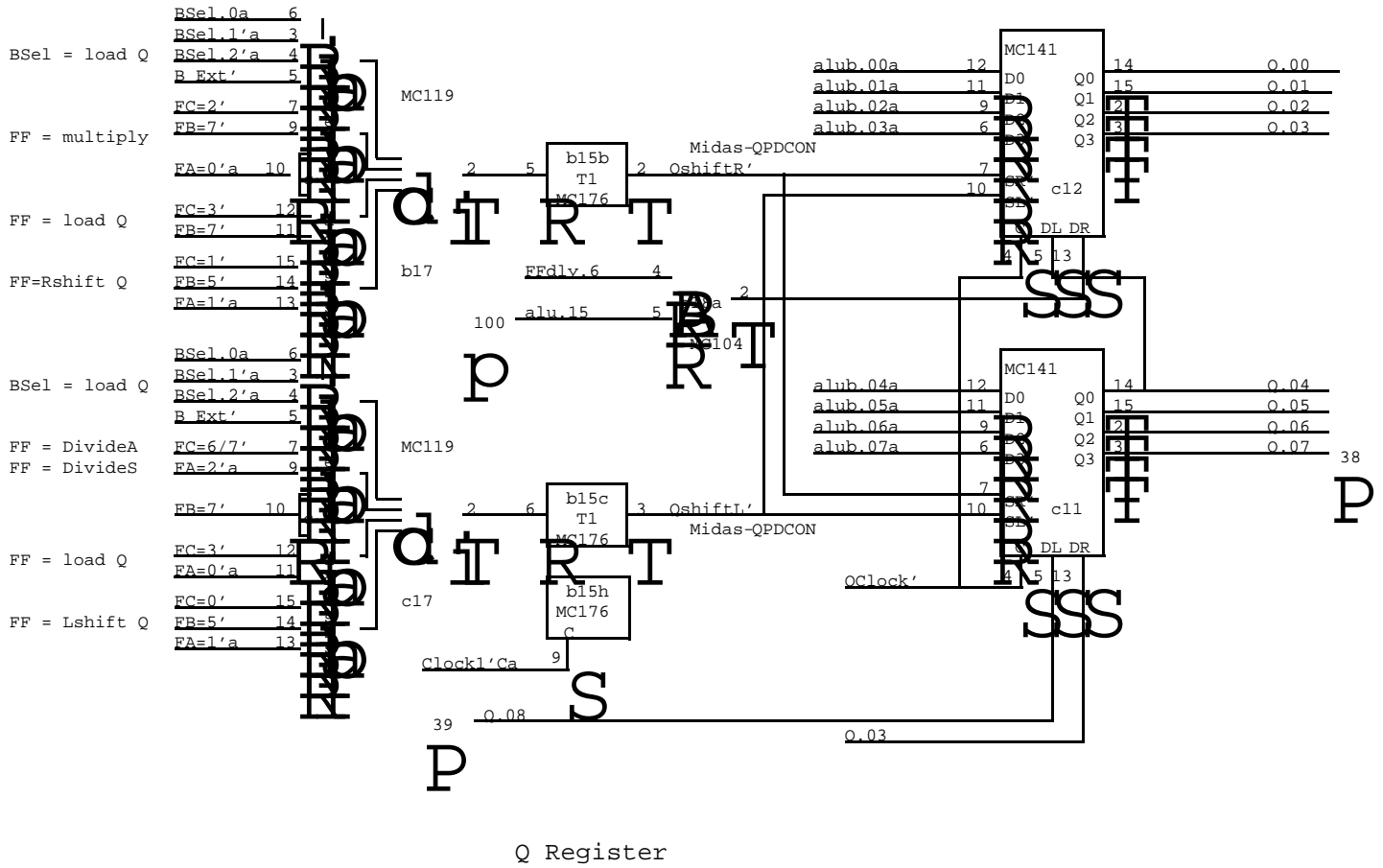
P Mux Encoding

Input	Source
0	ALU
1	0/Md, Cnt, Pointers
2	L shift
3	R shift
4	ALUFM
5	IO data
6	TIOA,,StkP
7	Shc

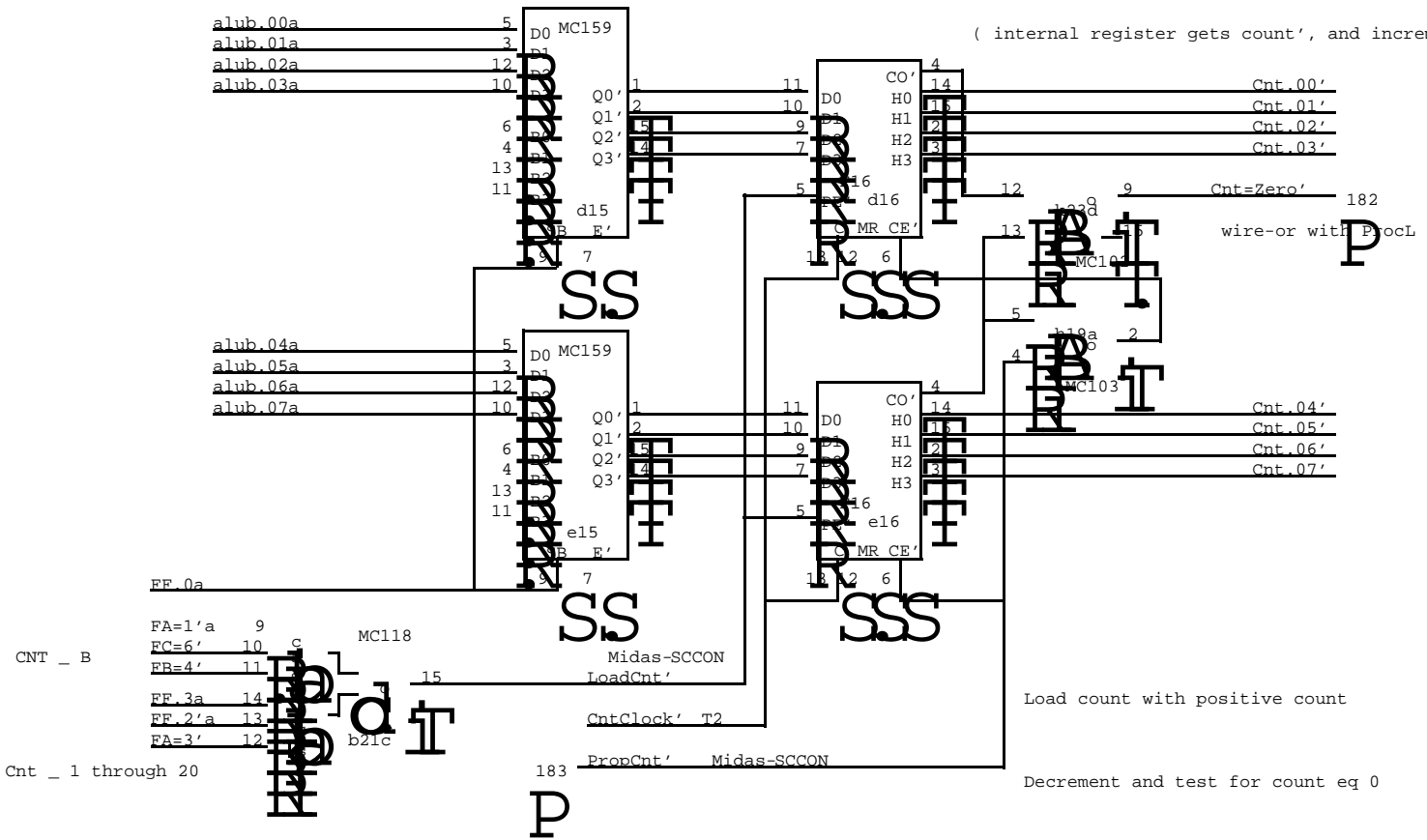


NOTE: The prom patterns are designed so that a one into address bit 0 will produce all 1's on the output. This allows the odd address inputs to Pmux to be selected.

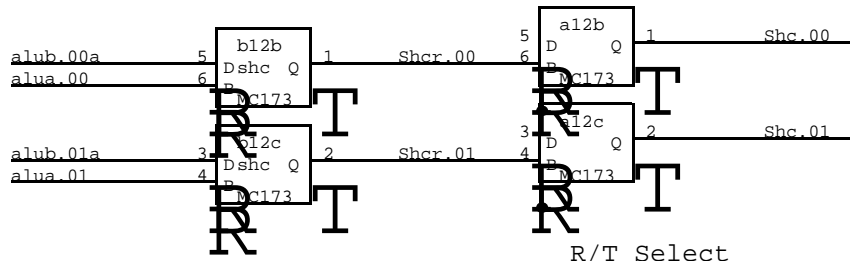
Lmask	Shmv bits	Rmask	Shmv bits
Shc.12-15	00 01 02 03 04 05 06 07	Shc.08-11	00 01 02 03 04 05 06 07
0	0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0
1	1 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0 0
2	1 1 0 0 0 0 0 0	2	0 0 0 0 0 0 0 0
3	1 1 1 0 0 0 0 0	3	0 0 0 0 0 0 0 0
4	1 1 1 1 0 0 0 0	4	0 0 0 0 0 0 0 0
5	1 1 1 1 1 0 0 0	5	0 0 0 0 0 0 0 0
6	1 1 1 1 1 1 0 0	6	0 0 0 0 0 0 0 0
7	1 1 1 1 1 1 1 0	7	0 0 0 0 0 0 0 0
10	1 1 1 1 1 1 1 1	10	0 0 0 0 0 0 0 0
11	1 1 1 1 1 1 1 1	11	0 0 0 0 0 0 0 1
12	1 1 1 1 1 1 1 1	12	0 0 0 0 0 0 0 1
13	1 1 1 1 1 1 1 1	13	0 0 0 0 0 0 1 1
14	1 1 1 1 1 1 1 1	14	0 0 0 0 0 1 1 1
15	1 1 1 1 1 1 1 1	15	0 0 0 0 1 1 1 1
16	1 1 1 1 1 1 1 1	16	0 0 0 1 1 1 1 1
17	1 1 1 1 1 1 1 1	17	0 1 1 1 1 1 1 1
20-37	1 1 1 1 1 1 1 1	20-37	1 1 1 1 1 1 1 1



Count Register



Extra Bits

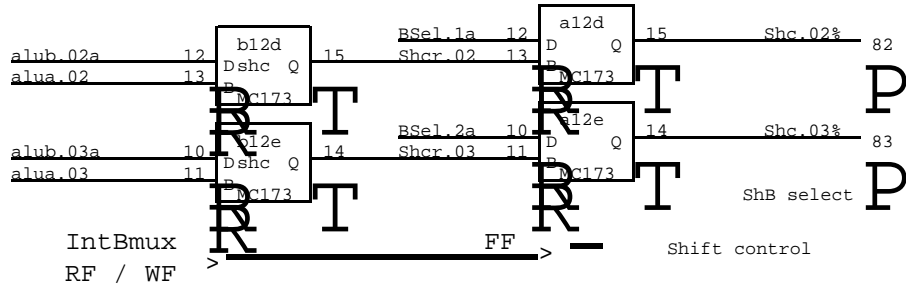


ProcH ProcL

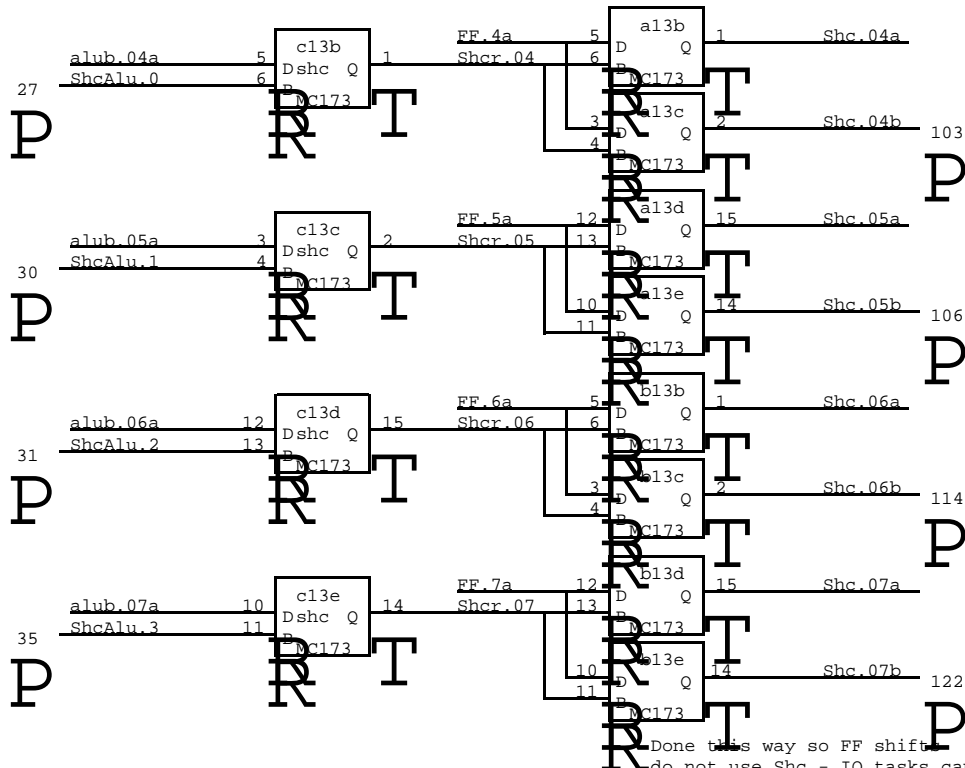
Shc.02 Shc.03 ShA ShB ShA ShB

R,,R	0	0	R	R	R	R
R,,T	0	1	R	T	T	R
T,,R	1	0	T	R	R	T
T,,T	1	1	T	T	T	T

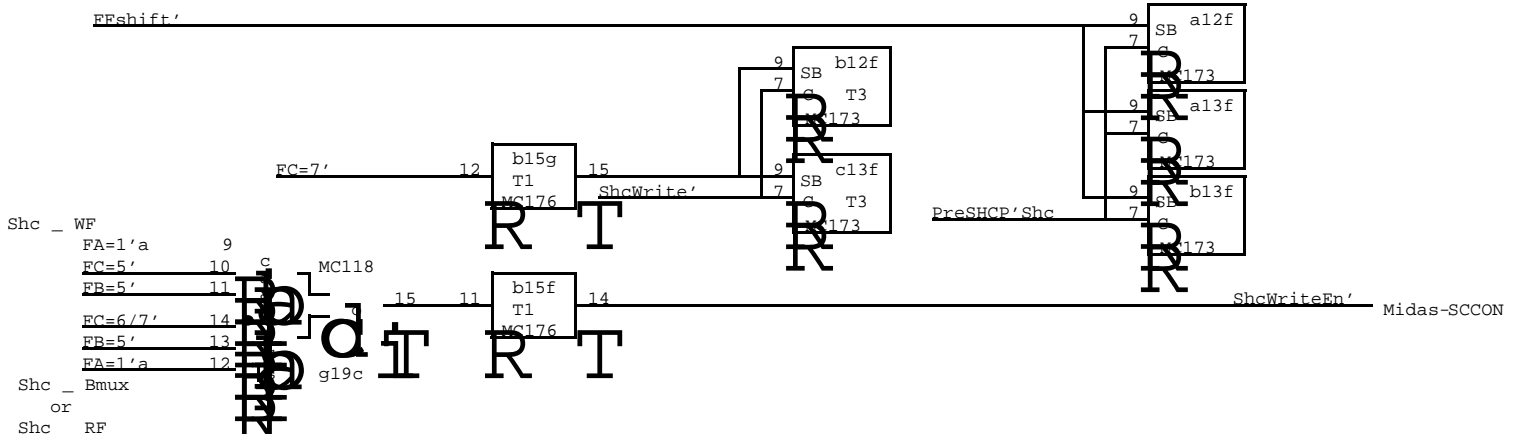
Note R selected with "0"
T selected with "1"

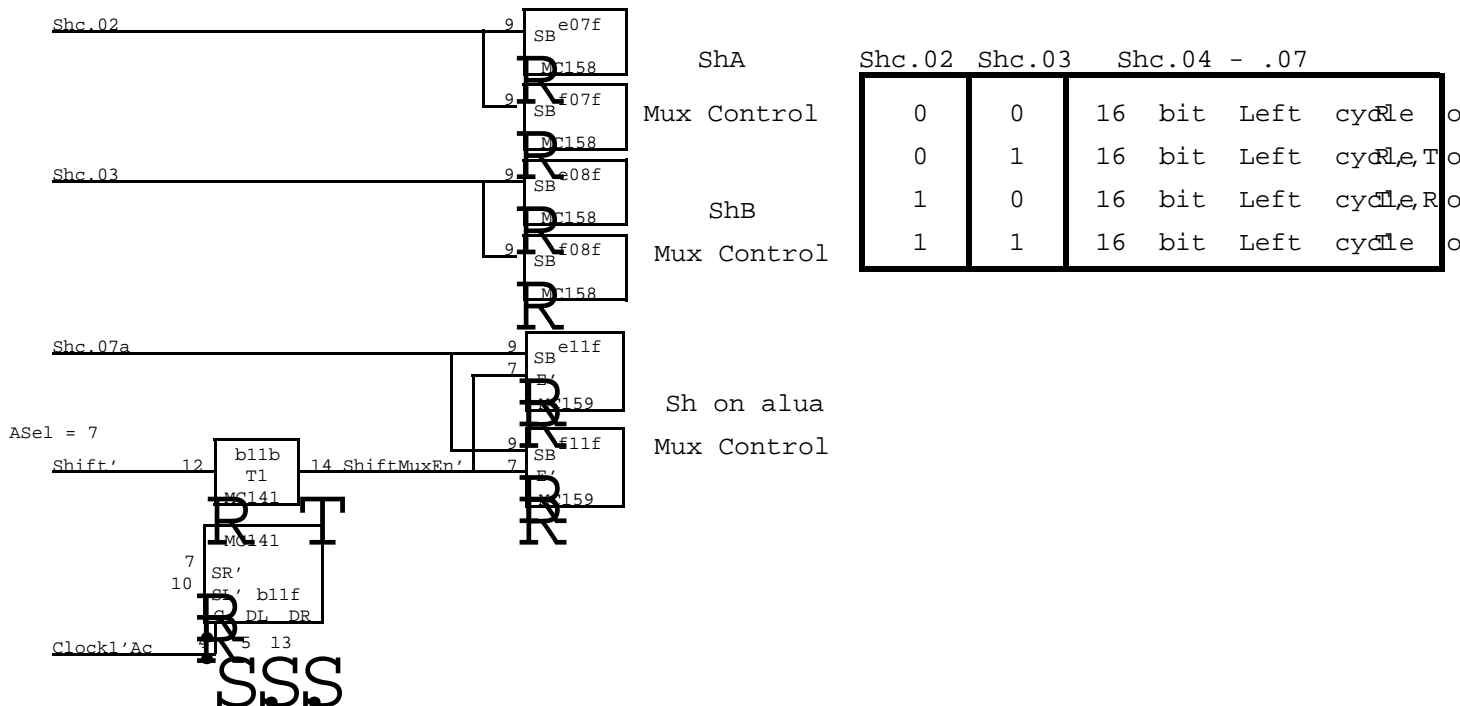
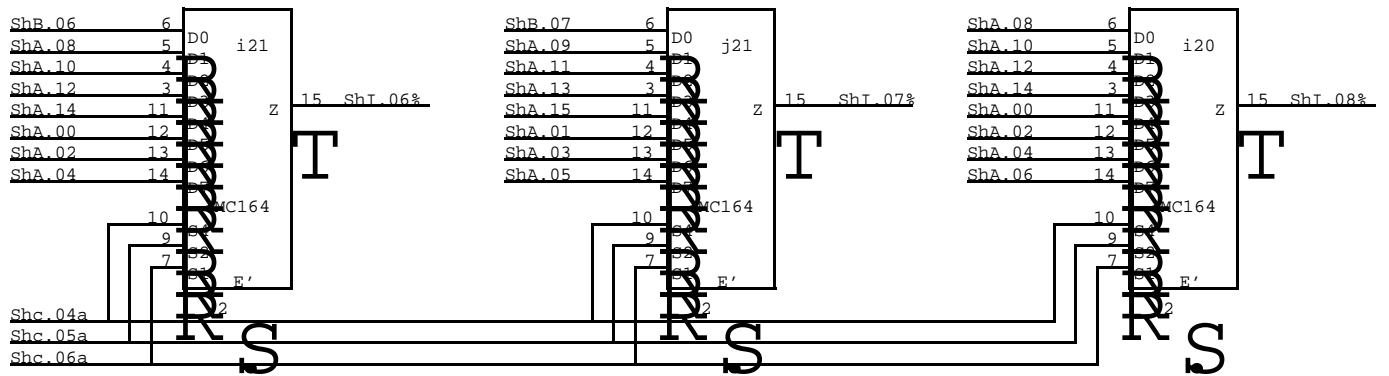
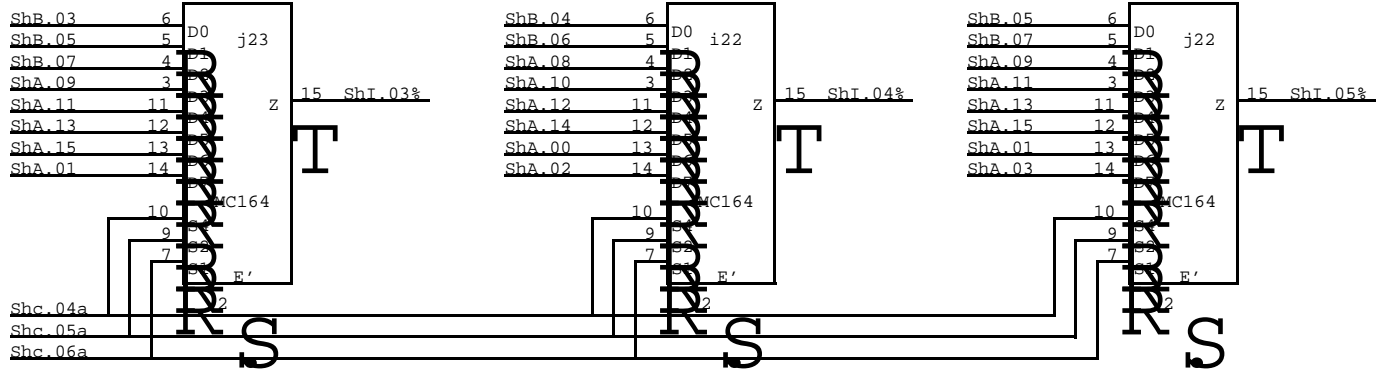
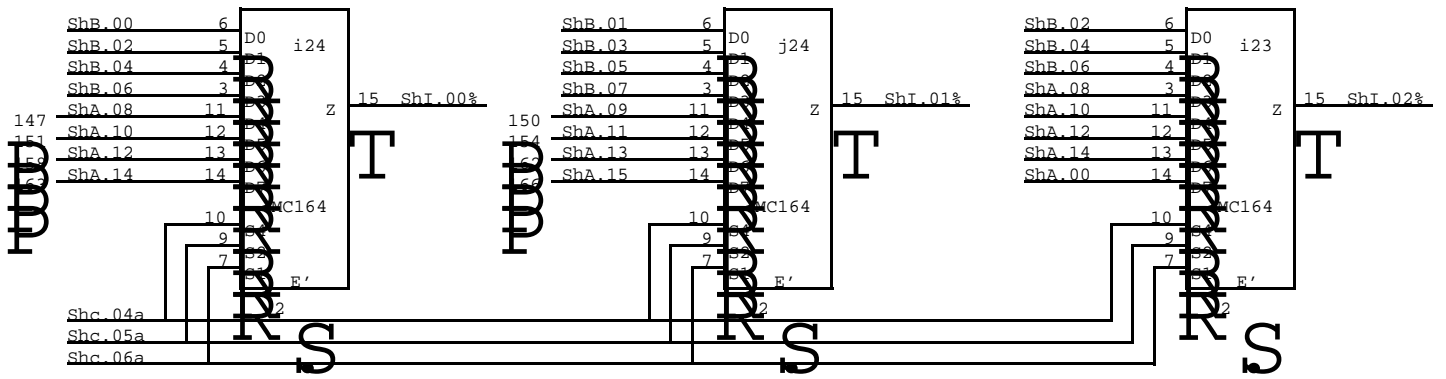


Shift Count



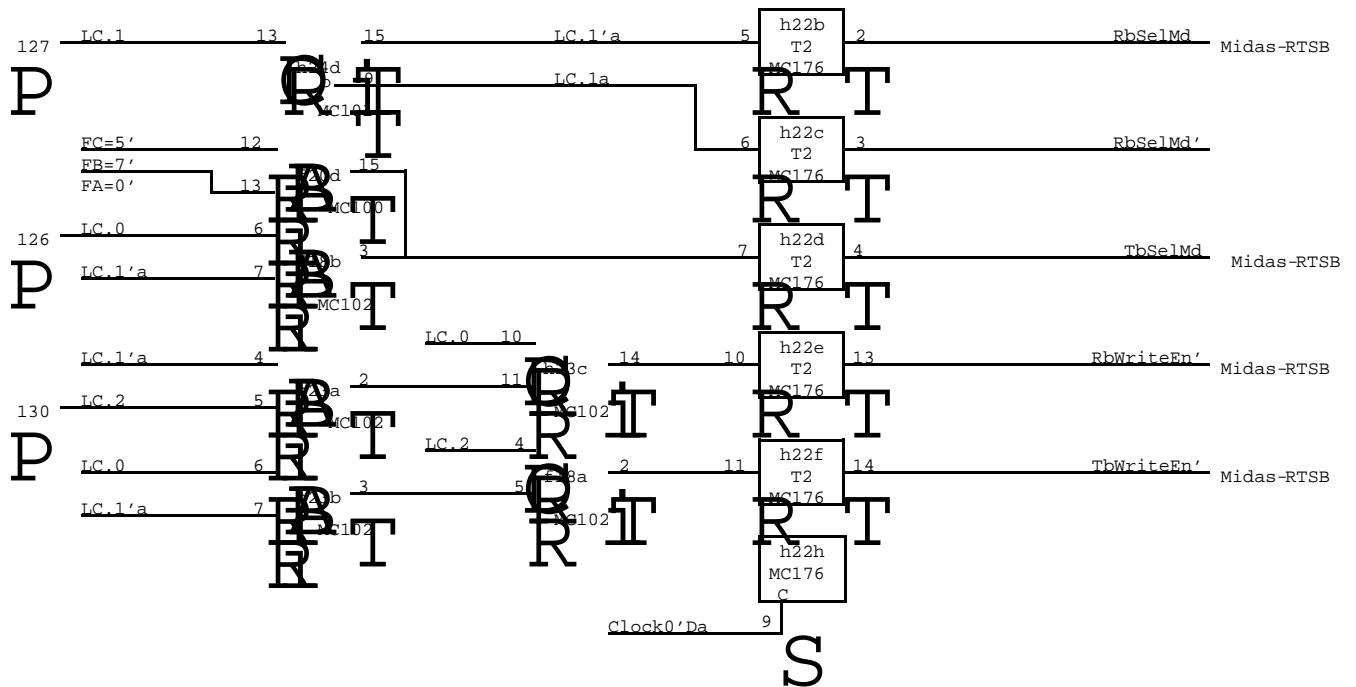
Done this way so FF shift do not use Shc - IO tasks can use the shifter without saving and restoring Shc.



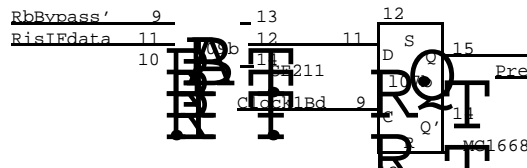
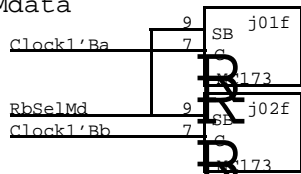


LC			R	T
0	1	2		
0	0	0	-	-
0	0	1	-	Pd *
0	1	0	Pd	Md
0	1	1	-	Md
1	0	0	Md	-
1	0	1	Md	Pd *
1	1	0	Pd	-
1	1	1	Pd	Pd *

* Md if used when
FF = 075



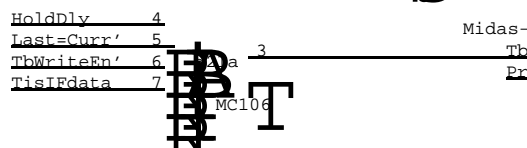
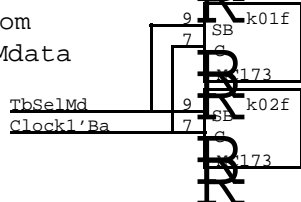
Write RFrom
Pdata or Mdata



RbBypassDly Midas-RTSB

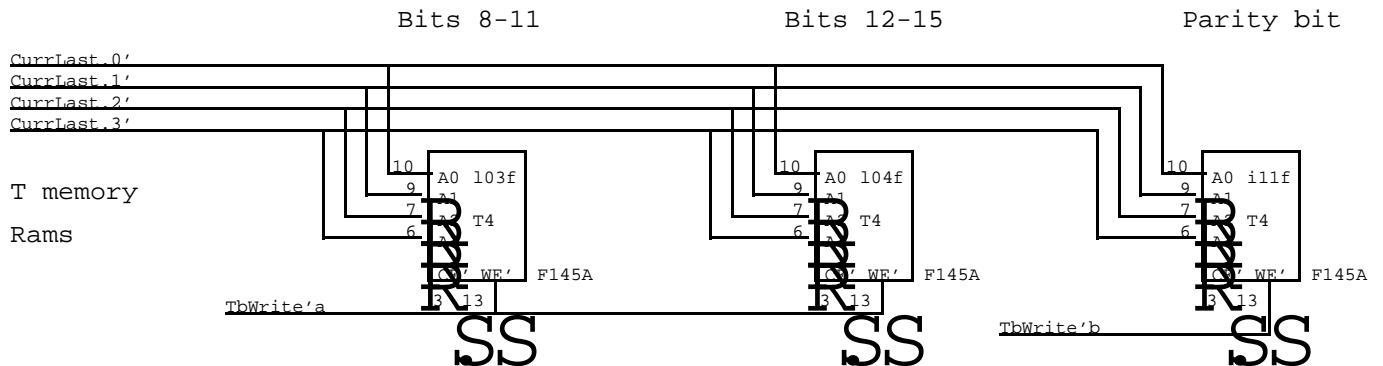
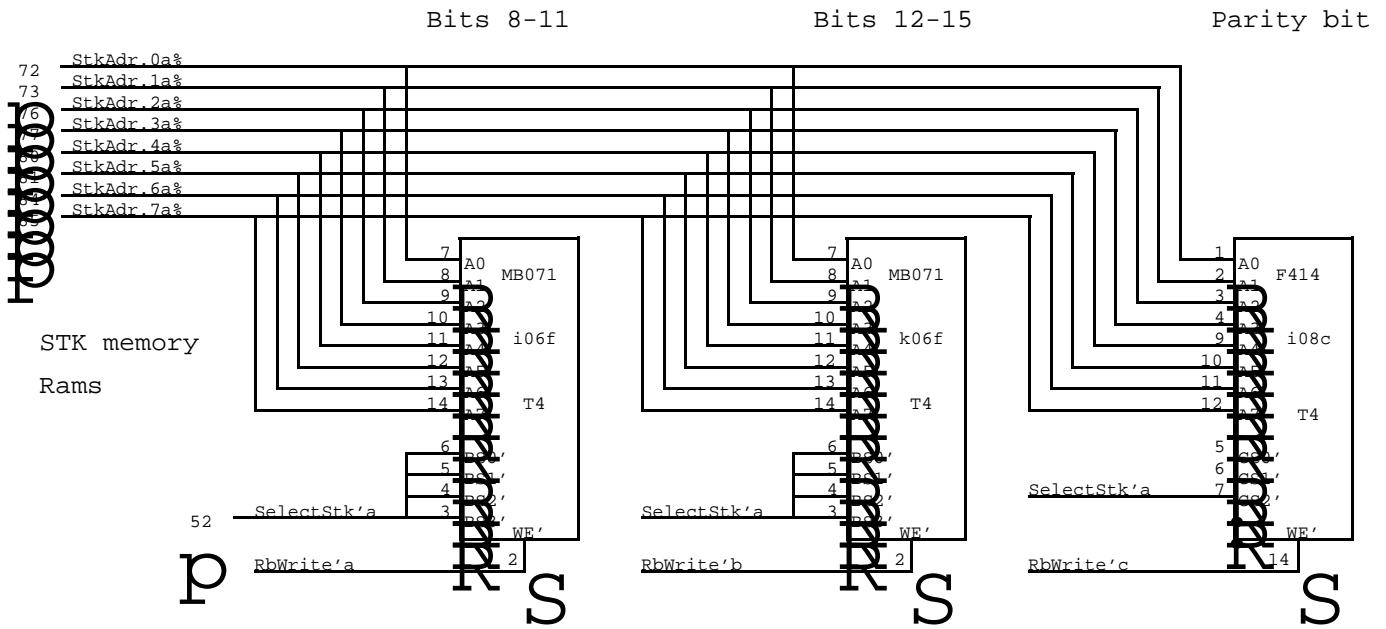
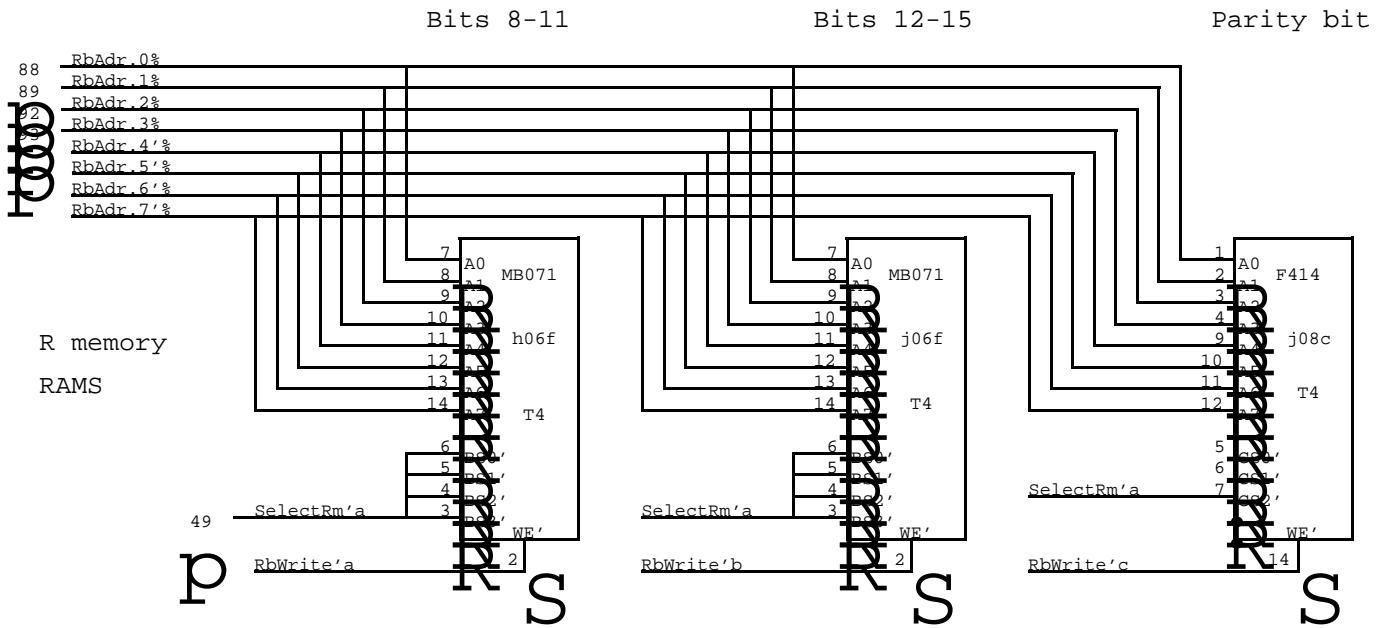
Bypass R from
Pdata or Mdata

Write TFrom
Pdata or Mdata

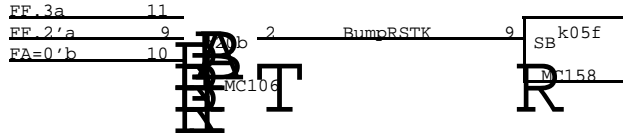


Midas-RTSB

Bypass T from
Pdata or Mdata

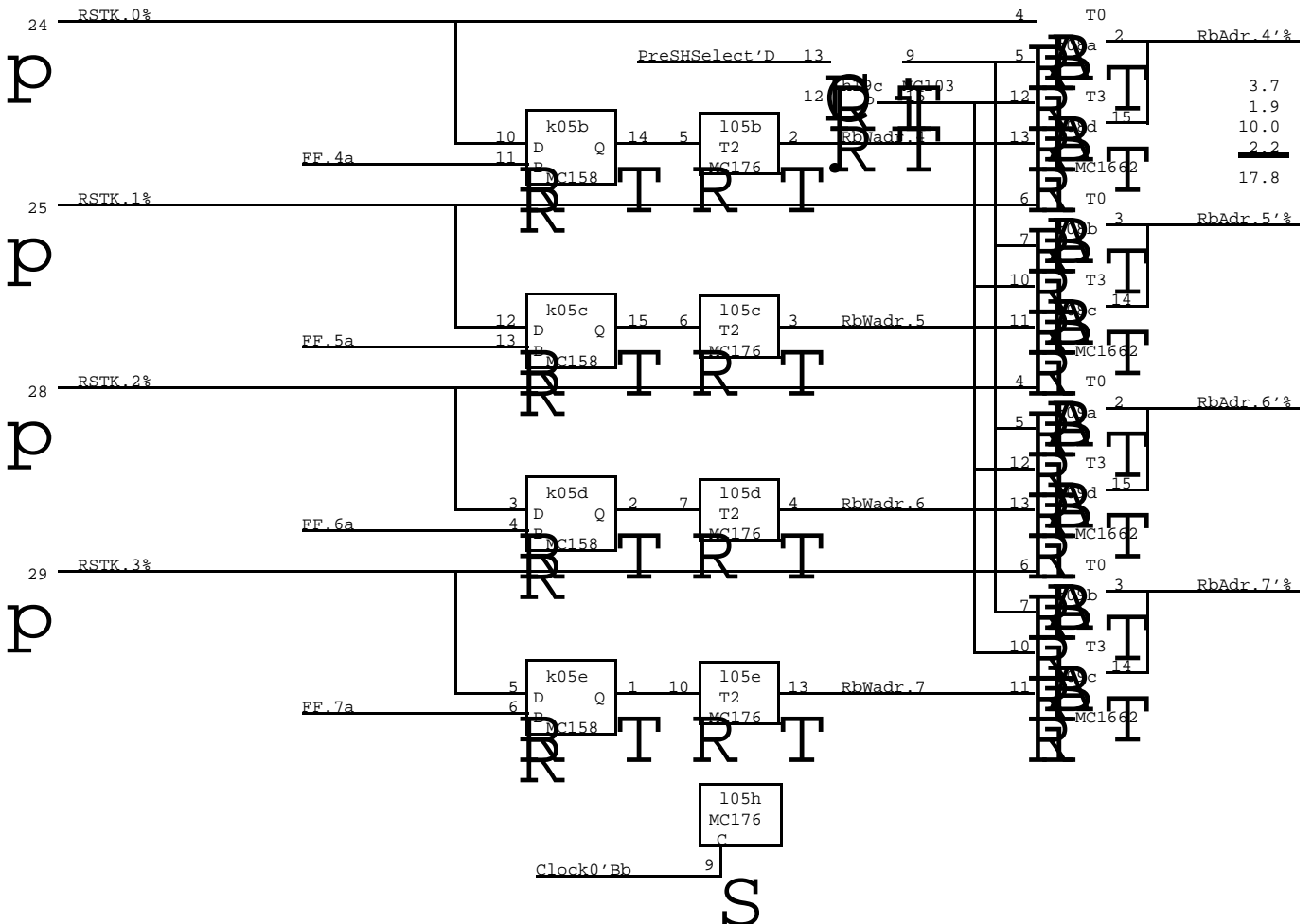


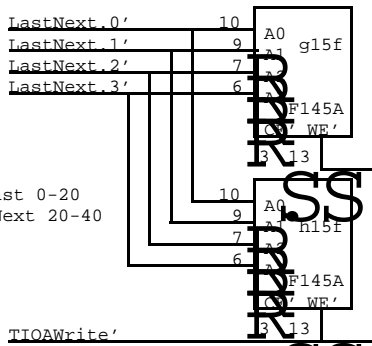
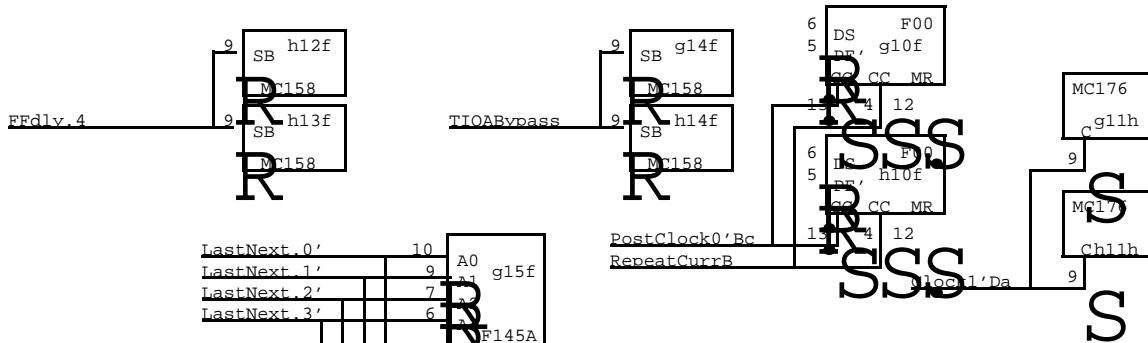
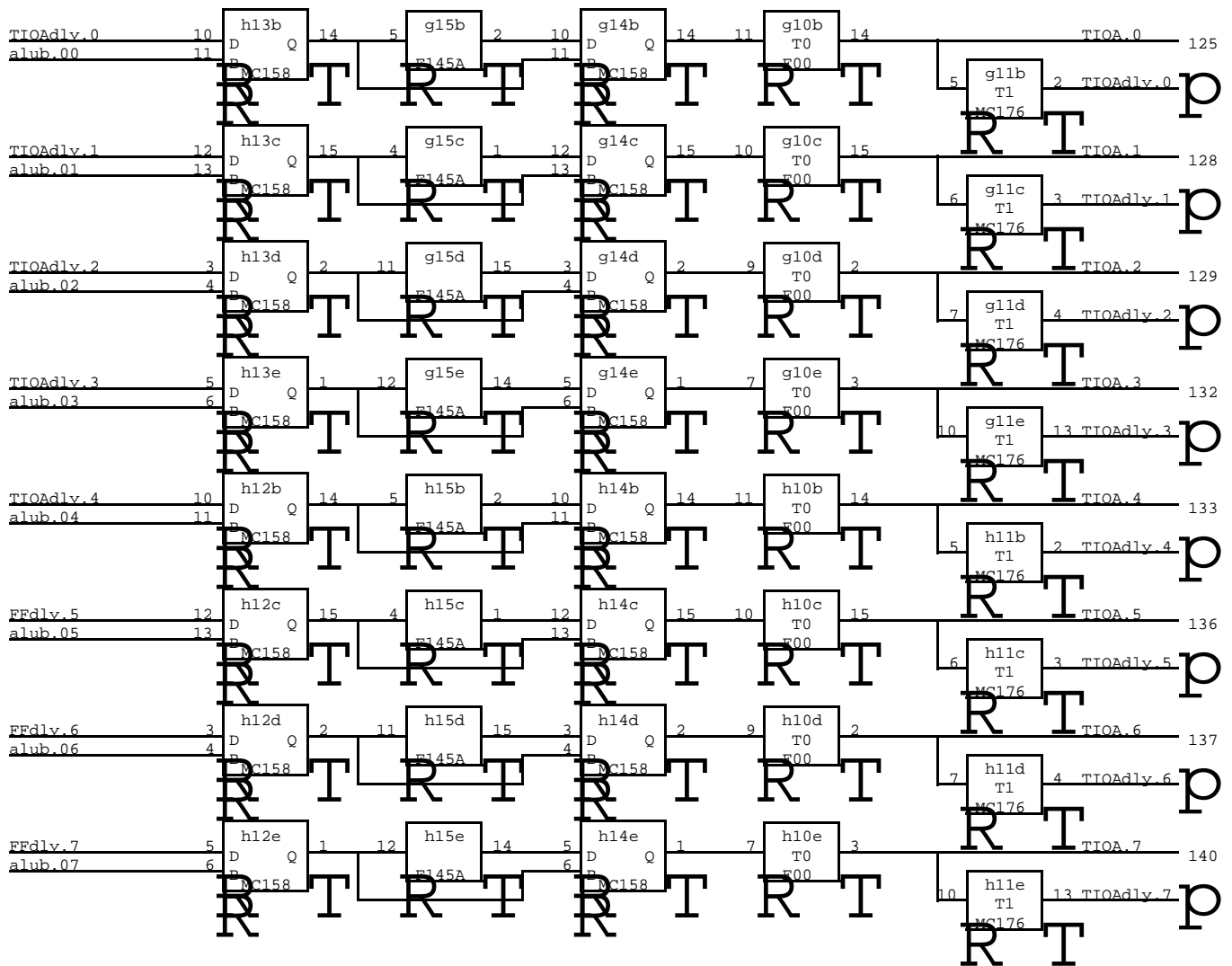
RbWadr _ RBase, ,FF



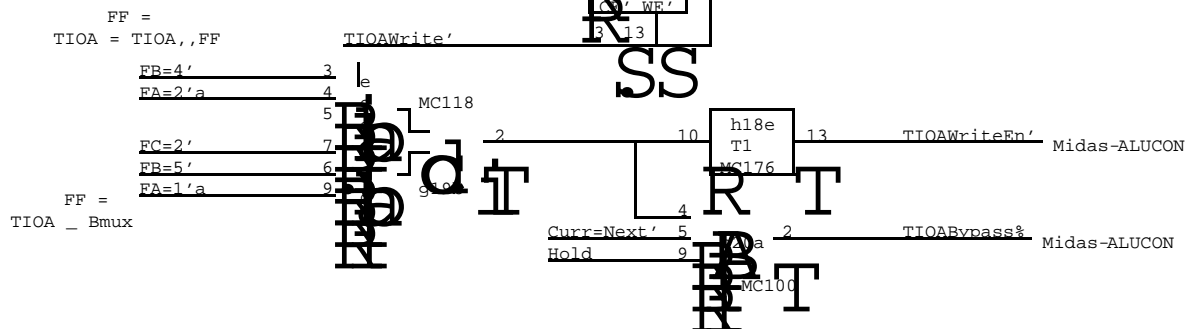
RSTK Control for bits 4 - 7 of the Rm address

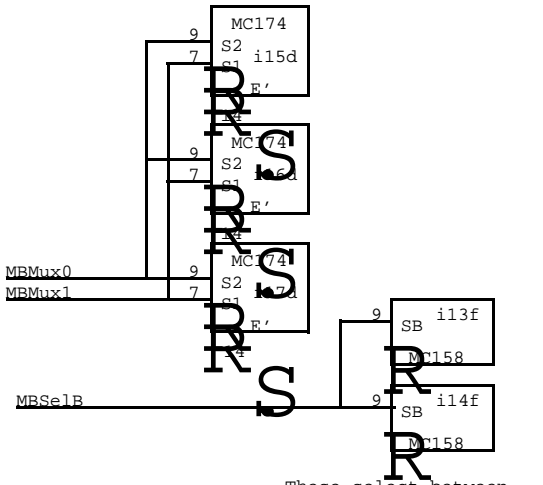
RSTK bits that make up Rm address bits 4-7



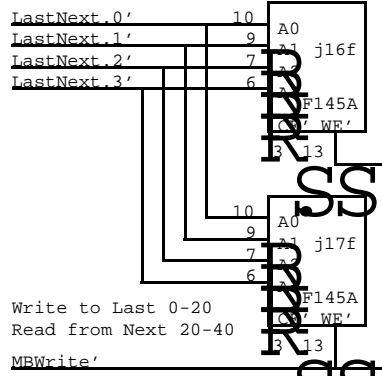


Write to Last 0-20
Read from Next 20-40

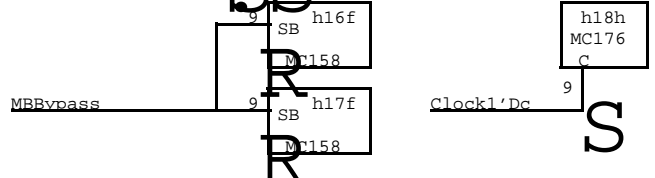




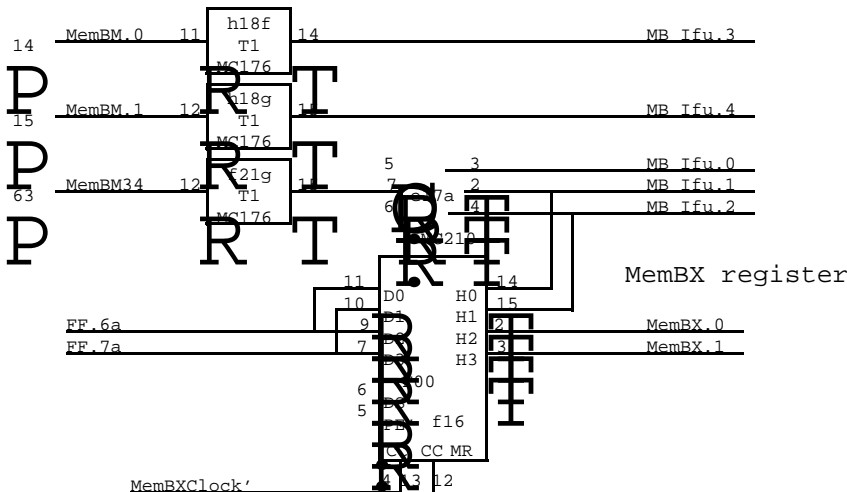
These select between BMux and "other" source to the MemBase RAM, and are always selected.



Write to Last 0-20
Read from Next 20-40



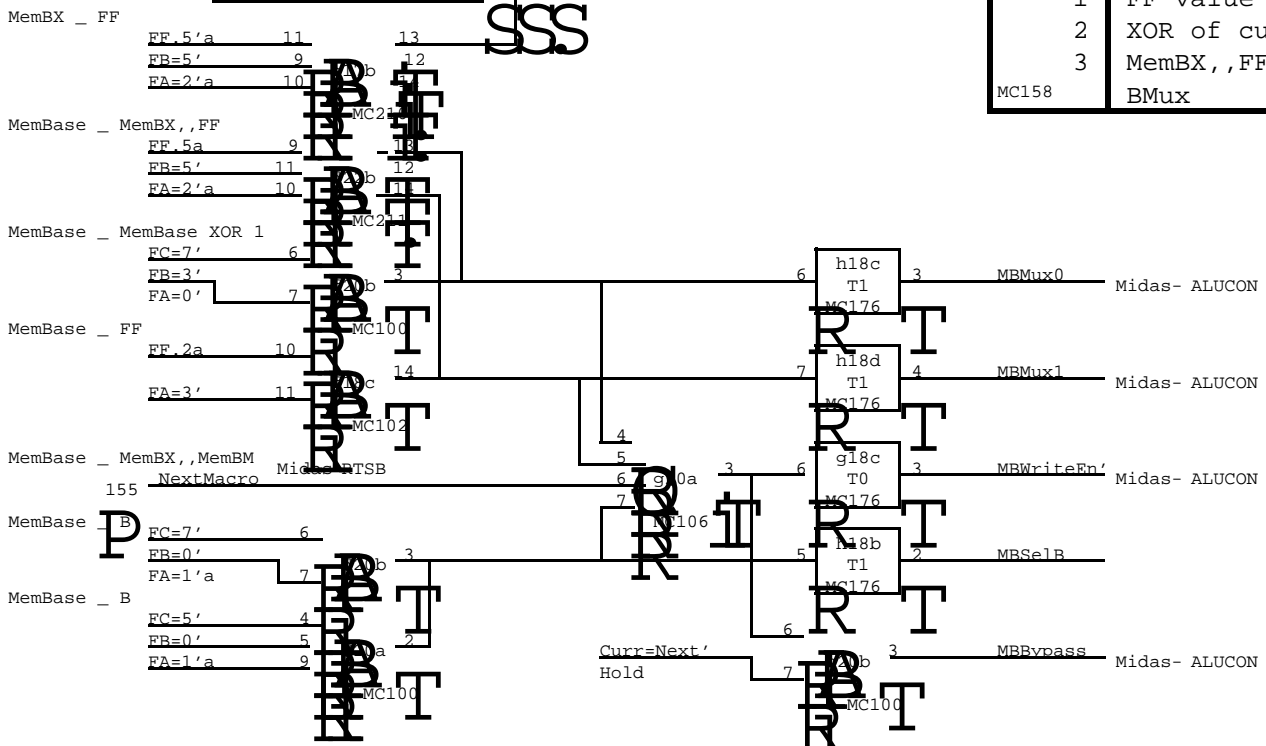
These select between task specific RAM (normal) and the input to the RAM for Bypassing

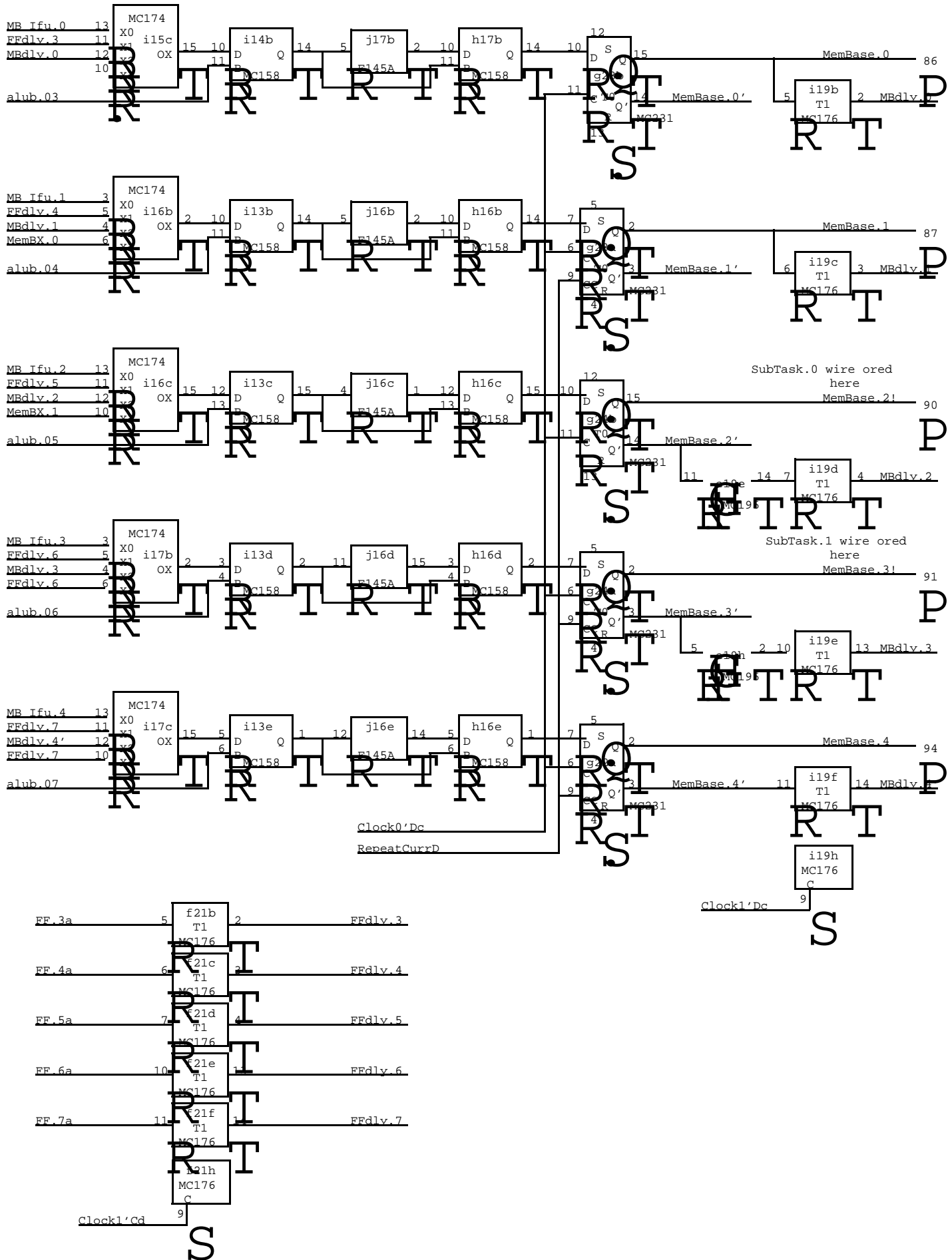


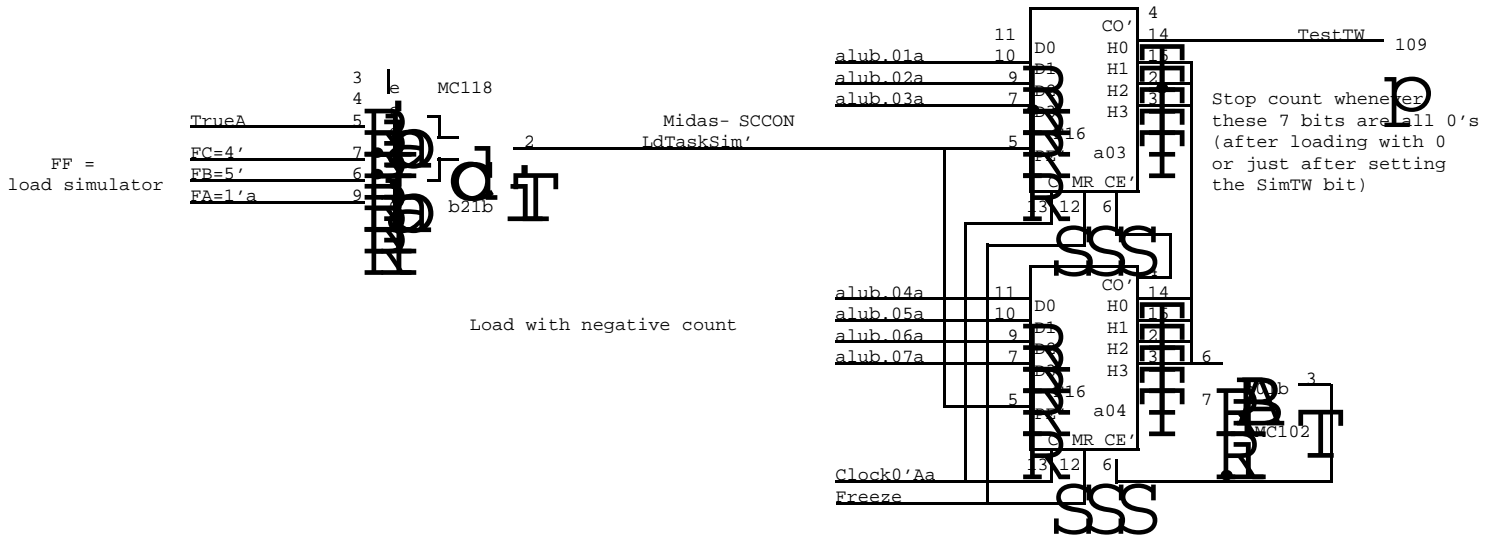
MemBX register

Mux encoding

MC174	0	MemBX,,IfuMB
	1	FF value
	2	XOR of current
	3	MemBX,,FF
MC158		BMux



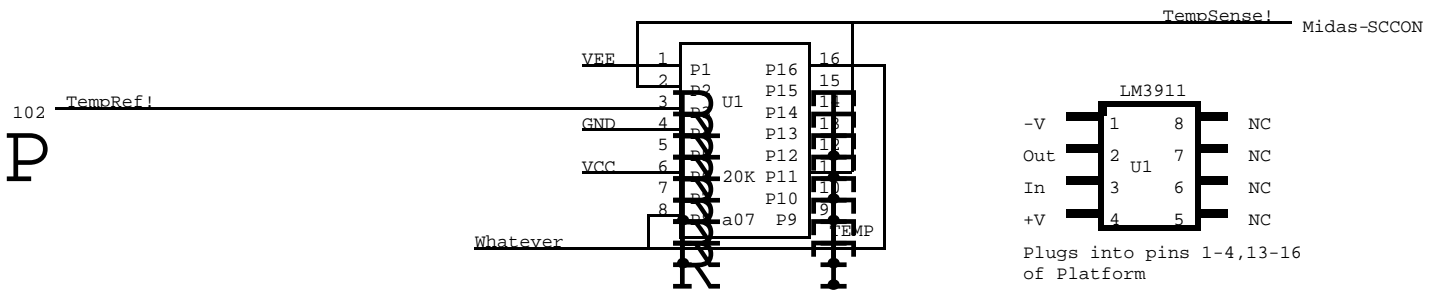


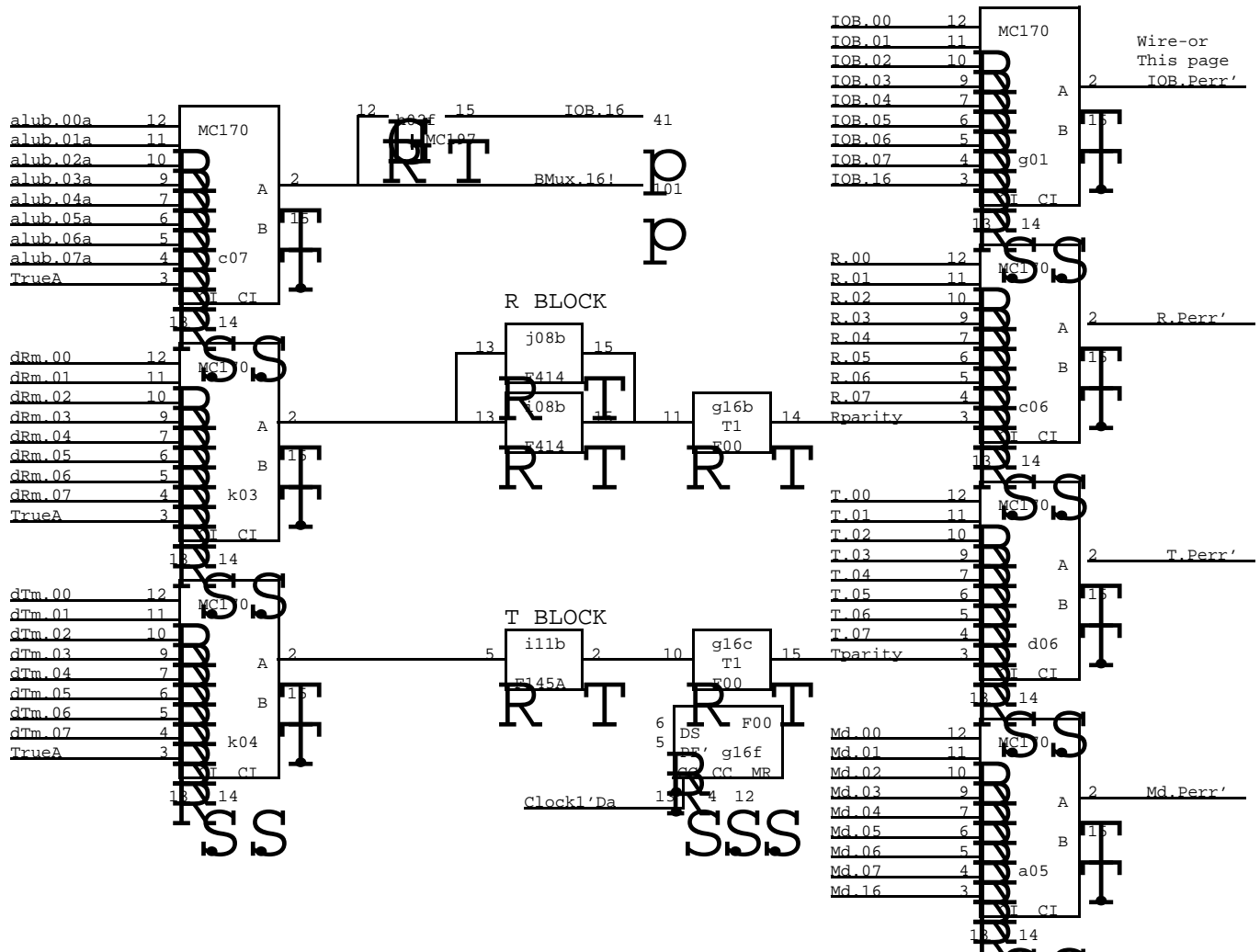
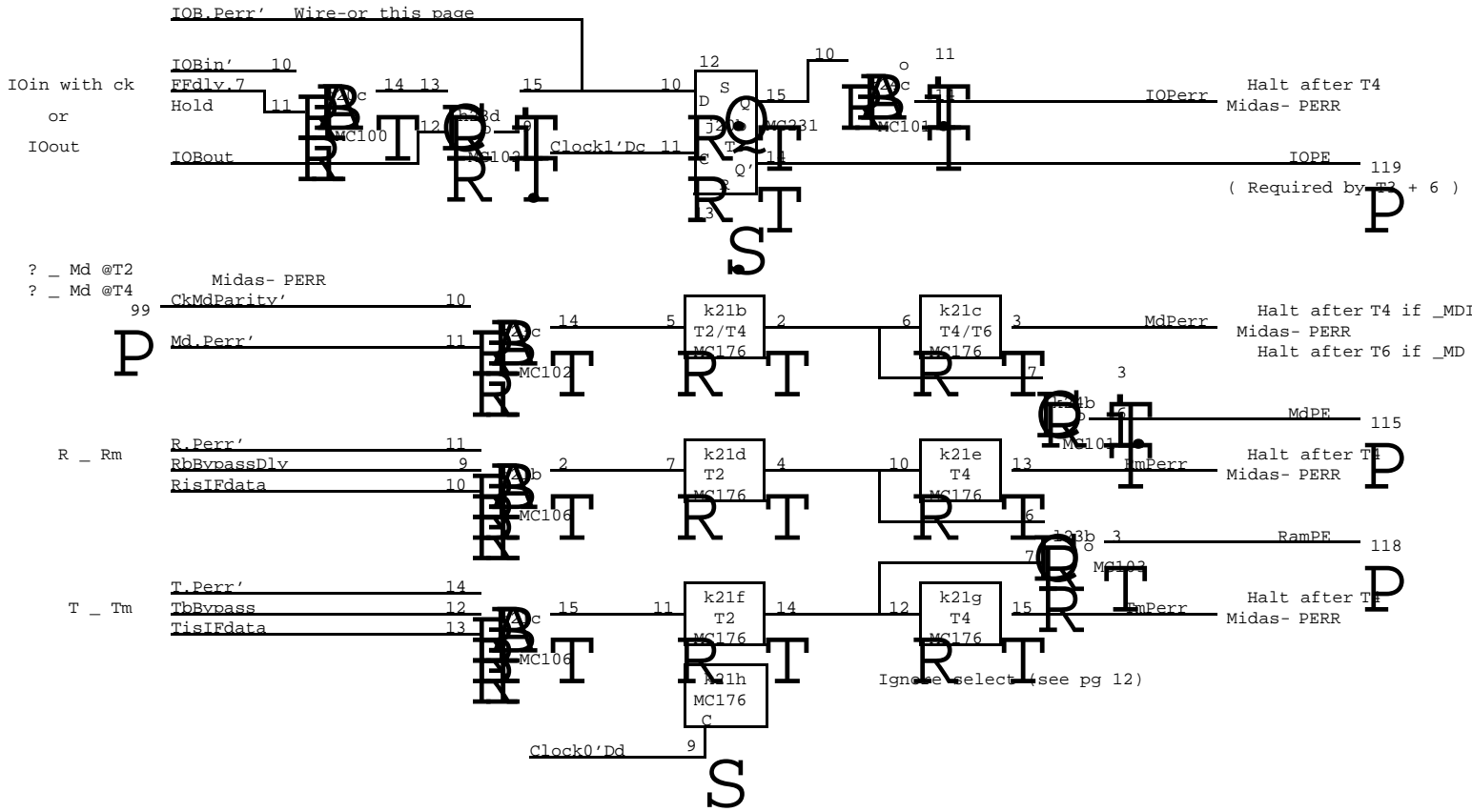


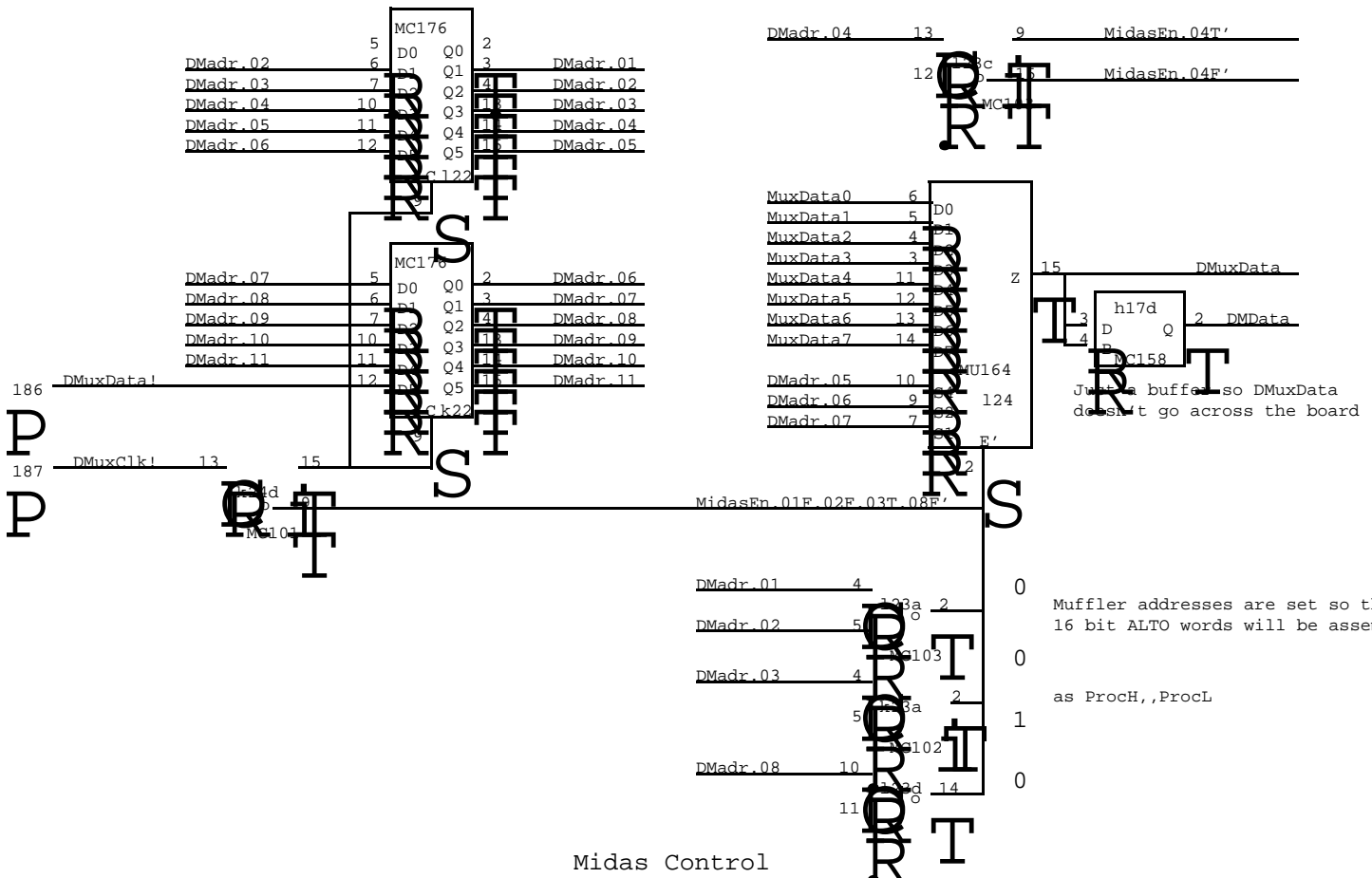
To enable this test circuit be sure there is a jumper
 Connect TestTW (<109>) to ContA pin <140>

Task Simulator

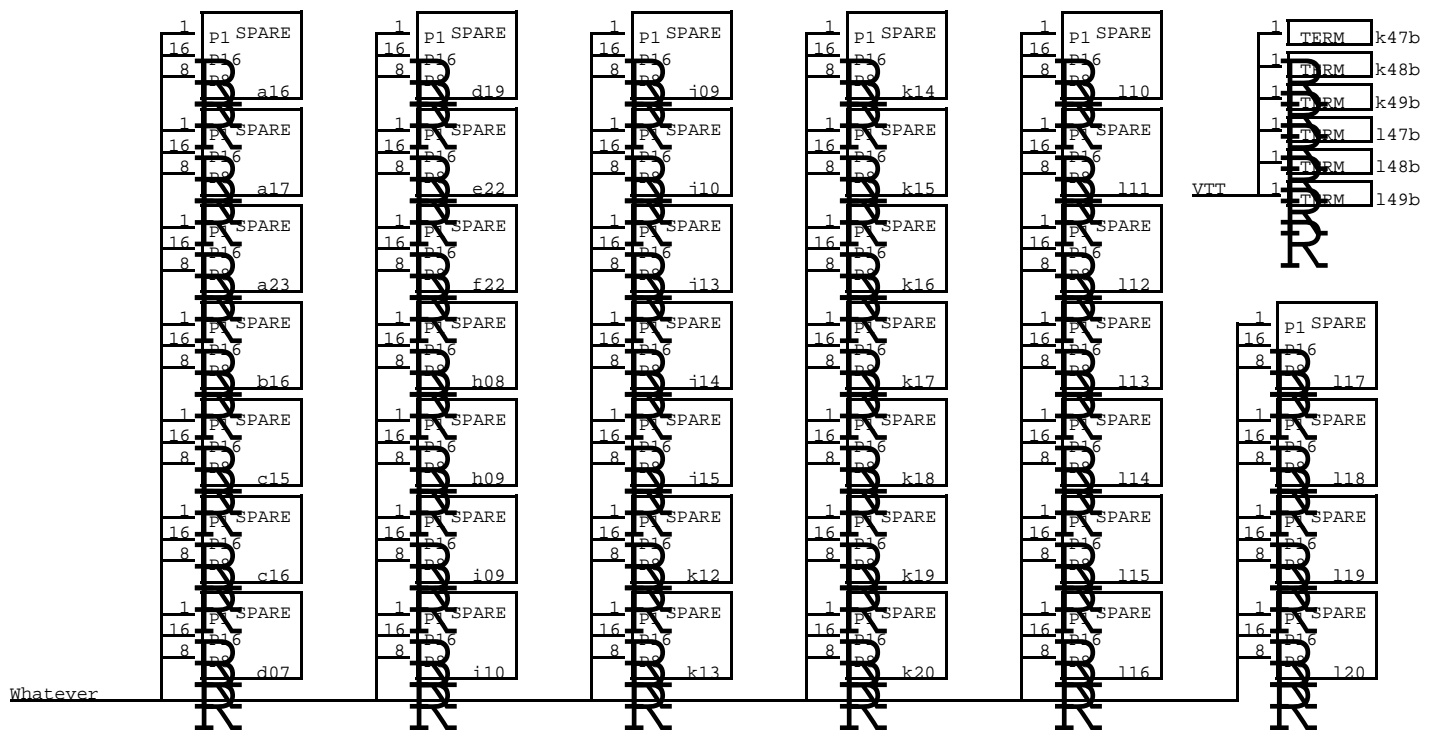
Temperature Sensing Ckt







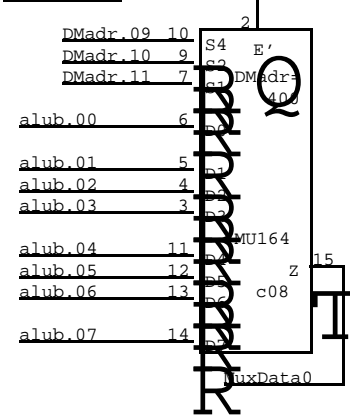
Spare Sockets for Multiwire



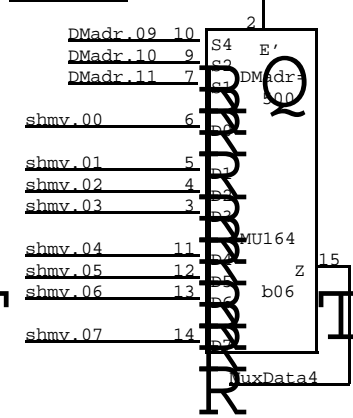
The following Platforms are entered so that route will cause multi-wire drill pattern to include a number of unused locations just in case they need to be used in some way.

XEROX PARC	Project Dorado	Drawing Midas Control	File Proch28.sil	Designer R Bates	Rev Da	Date 6/18/79	Page 28
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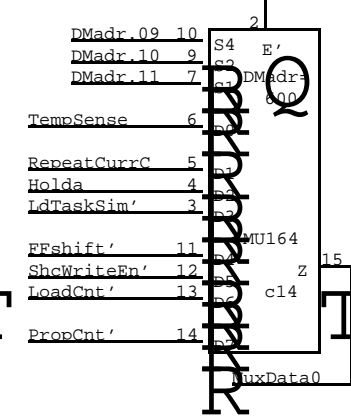
ALUB



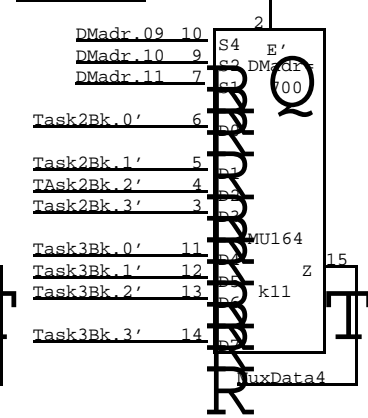
SHMV



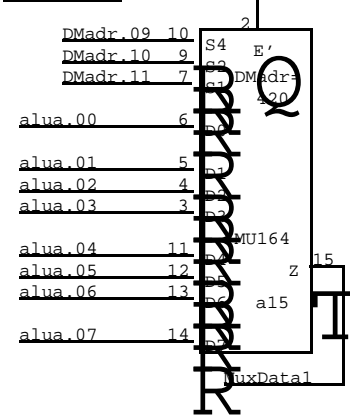
SCCON



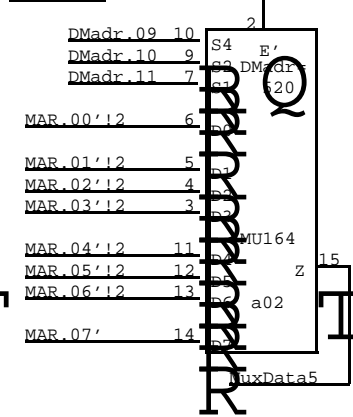
RADDR



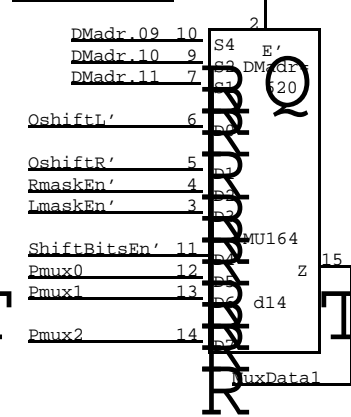
ALUA



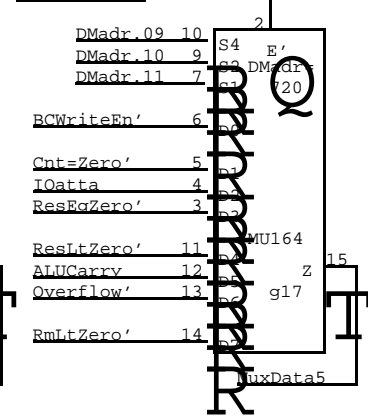
MAR



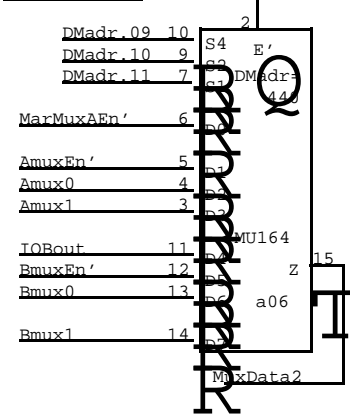
QPDCON



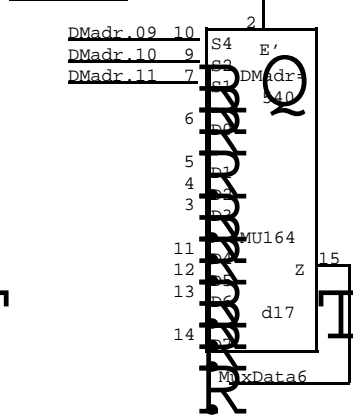
STKRB



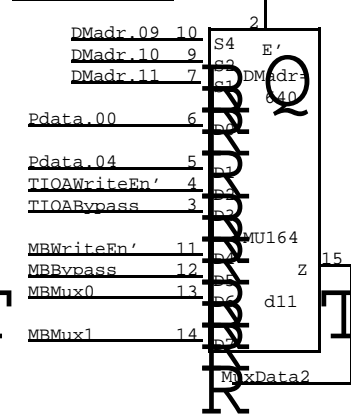
ABCON



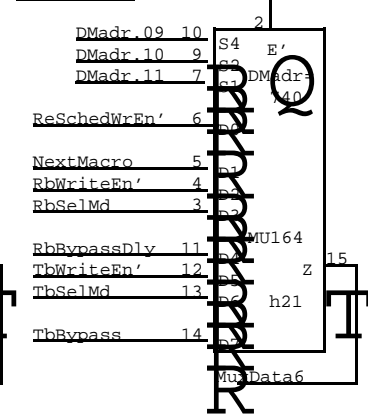
SPARE



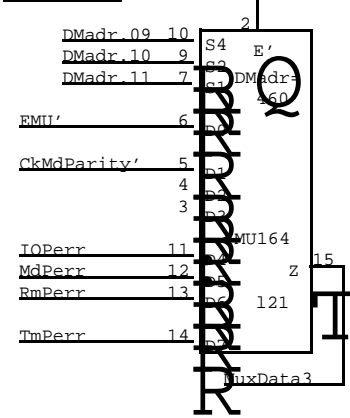
ALUCON



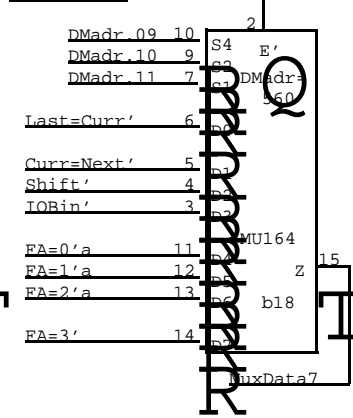
RTSB



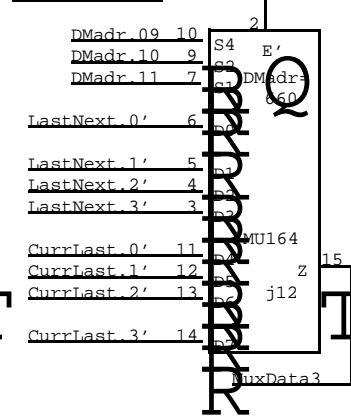
PERR



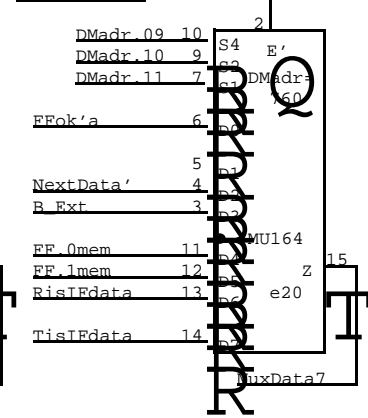
PRFA

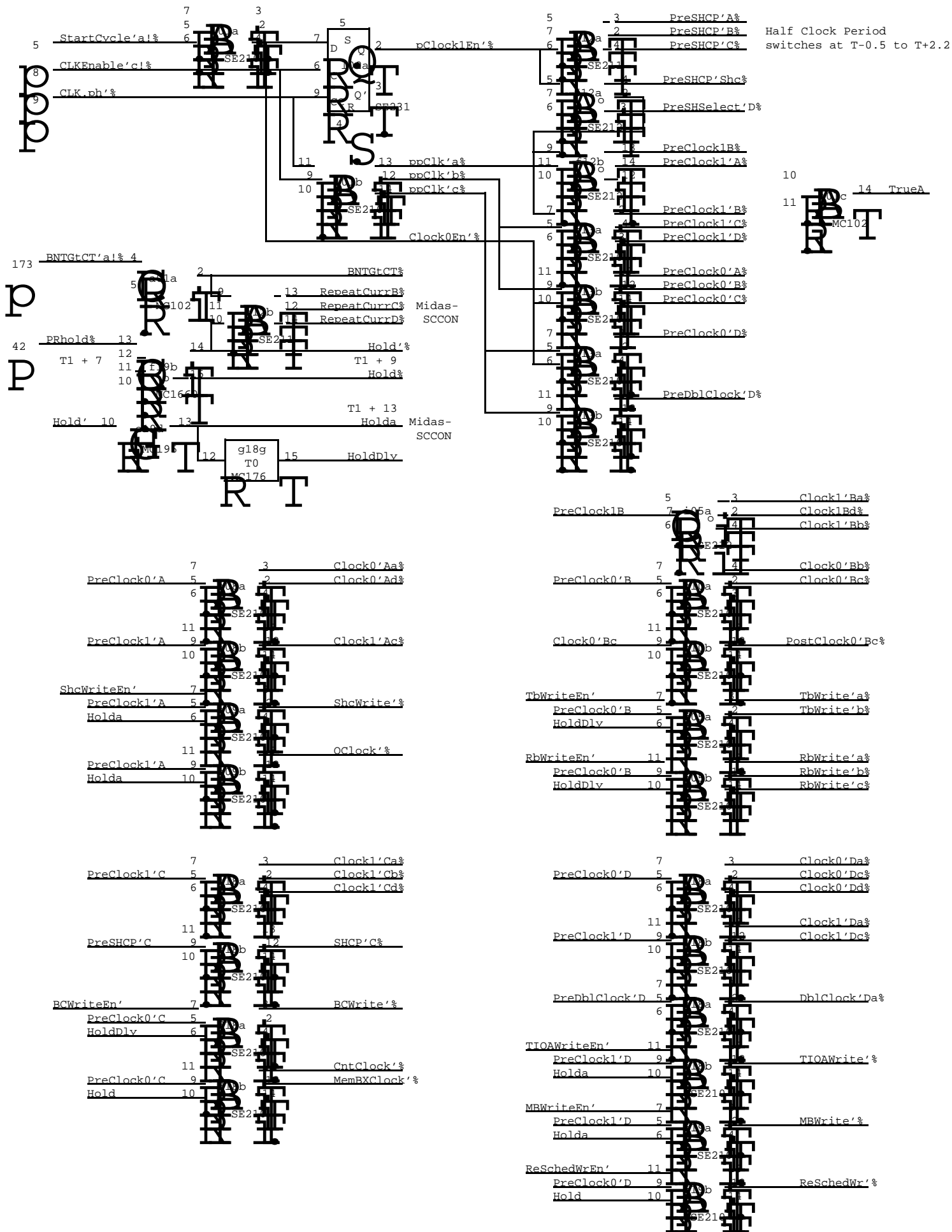


NEXTCL



PJUNK





	TIOA														IOB				IOB				Clk	+12v
	184		168		152		136		120		102		84		68		52		36		20			
	A	B	C	D	E	F	G	H	I	J	K	L												
1	MC102	Ex Bmux MC174	Ex Bmux MC174	Ex Bmux MC1662	Ex Bmux MC174	Ex Bmux MC174	IOB par MC170	IOB MC197	IOB MC175	IOB MC173	IOB MC173	Clocks SE210												
41	MAR MU164	Mar Mux MC159	Mar Mux MC159	Ex Bmux MC1662	Mar Mux MC159	Mar Mux MC159	Pdata MC164	IOB MC197	Md MC175	dRm Reg. MC173	dTm Reg. MC173	Clocks SE231												
2	X	X	X	X	X	X	X	X	X	X	X	II												
3	SimHold F141	Amux MC174	Amux MC174	Amux MC174	Amux MC174	Pdata MC164	Pdata MC164	Pdata MC164	T Reg. MC173	dT Reg. MC173	dRm Par. MC170	T Mem. MC145												
42	X	X	X	X	X	X	X	X	X	X	X	X												
4	SimHold F141	Bmux MC174	Bmux MC174	Bmux MC174	Bmux MC174	Pdata MC164	Pdata MC164	Pdata MC164	T Reg. MC173	dT Reg. MC173	dT par. MC170	T Mem. MC145												
5	Md Parity MC170	Amux In MC173	Bmux In MC173	Amux In MC173	Bmux In MC173	Pdata MC164	dR Reg. MC173	dR Reg. MC173	Clocks SE212	Clocks SE210	RSTK MC158	RSTK MC176												
43	X	X	X	X	X	X	X	X	II	II	X	IIIIII												
6	Mux Cont MU164	Shmv MU164	R Parity MC170	T Parity MC170	Pdata in MC173	Pdata in MC173	R Reg. MC173	Rm Mem.	Stk Mem.	Rm Mem.	Stk Mem.	R < 0 MC1668												
7	Temp LM3911	Shmv MC139	alub Par MC170		ShA MC158	ShA MC158	R Reg. MC173	MB071 X	MB071 X	MB071 X	MB071 X	R < 0 MC1668												
44	X	X	X	X	X	X	X	X	X	X	X	II												
8	Clocks SE210	Shmv MC139	alub MU164	alu=0 MC109	AhB MC158	AhB MC158	Pdata MC164		Stk parity F414	Rm parity F414	RbAdr MC1662	R < 0 MC211												
9	II	X	X	II	X	X			X	X	X	II												
9	Clocks SE210	alub-a MC101	alub-a MC101	alu	alu		Pdata MC164				RbAdr MC1662	R < 0 MC211												
45	II	X	X								X	II												
10	Amux T1 MC231	Bmux T1 MC231	Mux T1 MC176	MC181		MC181		TIOA F00	TIOA F00			Clocks SE210												
11	II	II	IIIIII	X	X			X	X			II												
11	Bmux T1 MC231	Mux T1 MC141	Q Reg. MC141	ALUFM MU164	alua sh MC159	alua sh MC159	TIOA MC176	TIOA MC176	T mem-P MC145	TASKs MC176	TASKs MU164													
46	II	IIII	X	X	X	X	IIIIII	IIIIII	X	IIIIII	X													
12	Shc MC173	Shc MC173	Q Reg. MC141	Carry MC118	Carry MC121	Clocks SE212	Clocks SE211	TIOA MC158	CurrLast MC141	NextLast MU164														
13	X	X	X	II	II	II	II	X	X	X														
13	Shc MC173	Shc MC173	Shc MC173	Branches MC170	Branches MC145	Clocks SE210	Clocks SE210	TIOA MC158	MemBase MC158															
47	X	X	X	X	X	II	II	X	X															
14	Bmux In MC158	Bmux In MC158	Shc MU164	P mux MU164	Branches MC158	Pdata in MC159	TIOA MC158	TIOA MC158	MemBase MC158															
15	X	X	X	II	II	X	X	X	X	X														
15	alua MU164	Q Reg. T1 MC176		CntMux MC159	CntMux MC159	Pdata in MC159	TIOA MC145	TIOA MC145	MemBase MC174															
48	X	IIIIII		X	X	X	X	X	X	X														
16				Cnt Reg. F16	Cnt Reg. F16	MemBX F00	Parity T1 F00	MemBase MC158	MemBase MC174	MemBase MC145														
17				X	X	X	IIII	X	X	X														
17		Q Reg. MC119	Q Reg. MC119	SPAIR MU164	MemBX MC210	Branches MC173	MU164	MemBase MC158	MemBase MC174	MemBase MC145														
49	X	X	X	X	II	X	X	X	X	X														
18	CurrLast MC158	FA MU164	Clocks SE210	Clocks SE210	P mux MC104	Misc. MC102	Misc. T0 MC176	T1 MC176	Clocks SE210	Clocks SE210														
19	X	X	II	II	IIII	IIII	II,III	IIIIII	II	II														
19	LastNext' MC158	Misc. MC212	Amux MC121		Misc. MC195	MC1660	MC118	Misc. MC103	MBdly MC176	Clocks SE210														
50	X	II	X		IIII, I	II	II	L, L, L	IIII, L	II														
20	Last' MC141	FA=0 MC100	FA=2 MC100	FA=1 MC100	Misc. MU164	FA=0 MC100	Misc. MC106	Bypass MC100	ShI MC164	MC231														
21	X	IIII	IIII	II, L	X	IIII	III	III, L	X	II														
21	Curr' MC141	FA=1 MC118	Amux MC119	Amux MC117	Misc. MC102	FPdly T1 MC176	Parity MC106	Rm cont MU164	ShI MC164	ShI MC164	Parity MC176	Parity MU164												
51	X	II	X	X	IIII	IIII, L	III	X	X	X	IIIIII	X												
22	Next=Curr MC113	P mux MC212	Misc. MC102	ALUF MC211			MemBase MC231	Misc. T0 MC176	ShI MC164	ShI MC164	Midas MC176	Midas MC176												
23	X	II	IIII	II			II	IIIIII	X	X	X	X												
23		ASel MC101	FF dec. MC210	FF dec. MC101	FF-a MC101	FF-a MC101	MemBase MC231	LC dec. MC102	ShI MC164	ShI MC164	Misc. MC102	Misc. MC103												
52	X	IIII	II	X	X	X	II	IIII	X	X	IIII	IIII												
24	Next MC101	MC210	Misc. MC103	FF dec. MC101	FF dec. MC161	FF dec. MC161	MemBase MC231	BSel dec. MC101	ShI MC164	ShI MC164	ALUF MC101	Midas MU164												
24	X	L	IIII	X	X	X	II	IIII	X	X	III	X												

-5v P P P P P P P P P P P P P P P Muffler +5v
Spare = 40

XEROX PARC	Project Dorado	Reference Board Layout	File Proch31.sil	Designer R. Bates	Rev Da	Date 6/18/79	Page 31
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Use Dorado Proms to define the following Proms:

Board Name	Prom Name	location
Porch	Lmask (High byte)	b07
	Rmask (High byte)	b08