D O R A D O S C H E M A T I C S

H i B y t e

P R O C E S S O R

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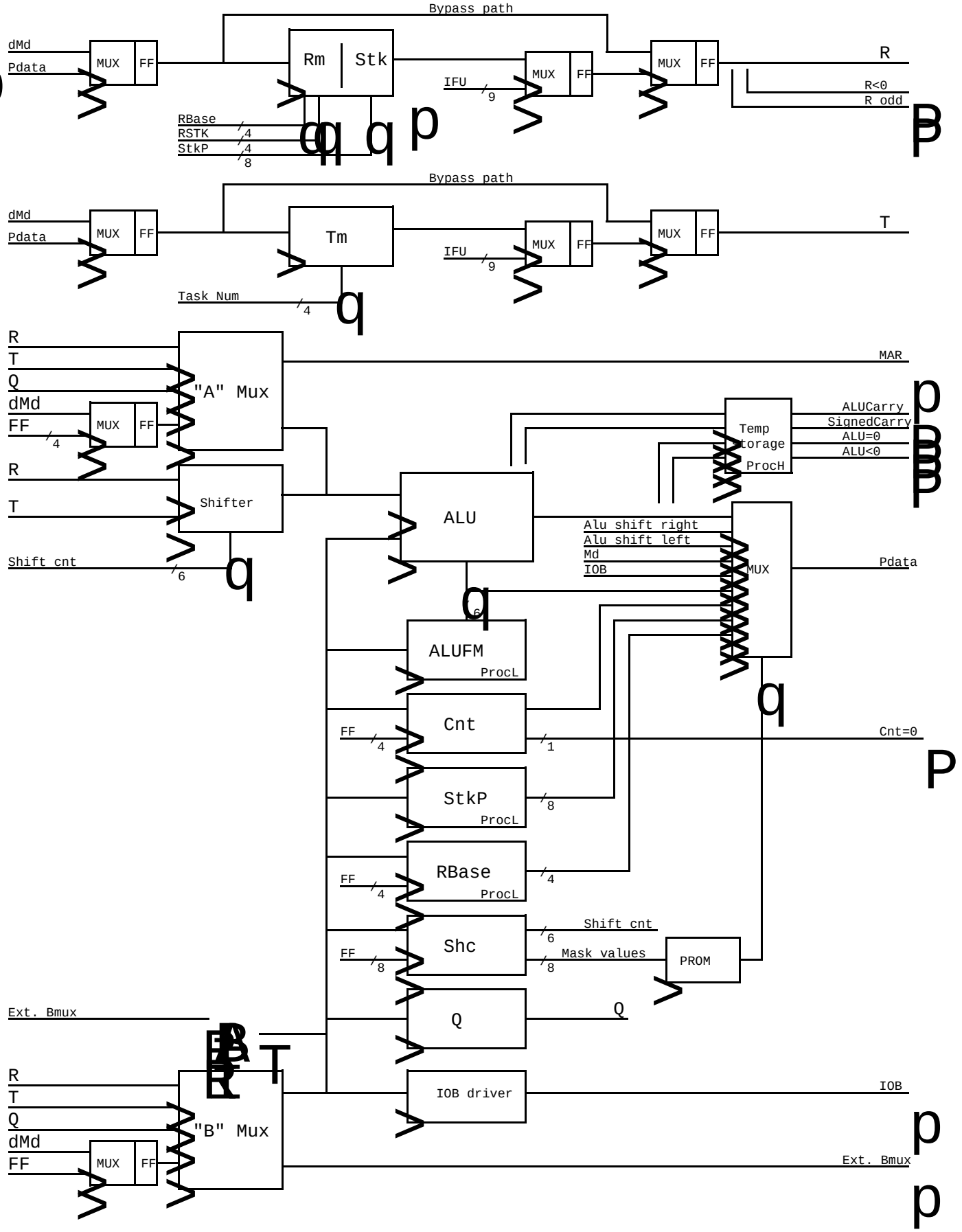
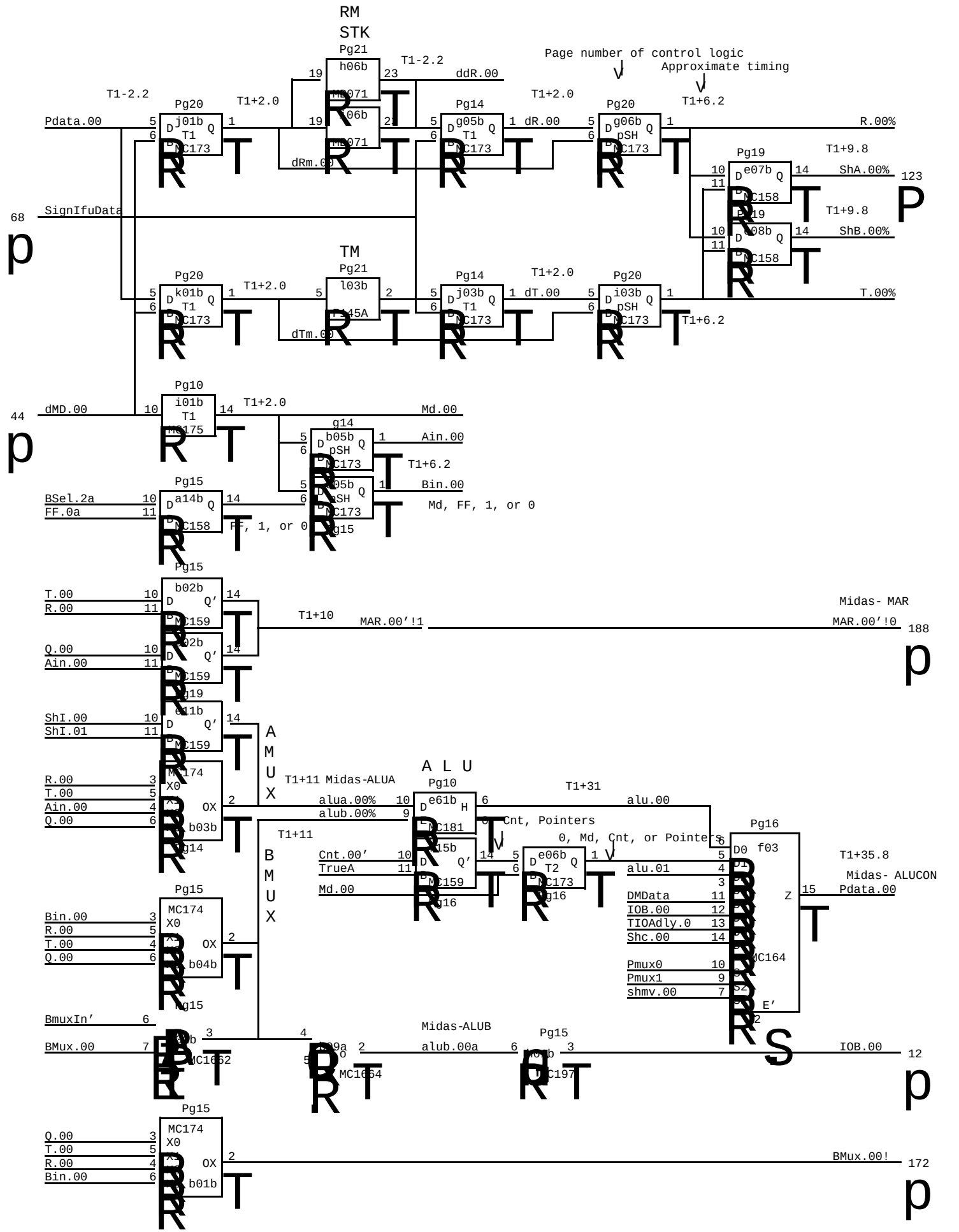
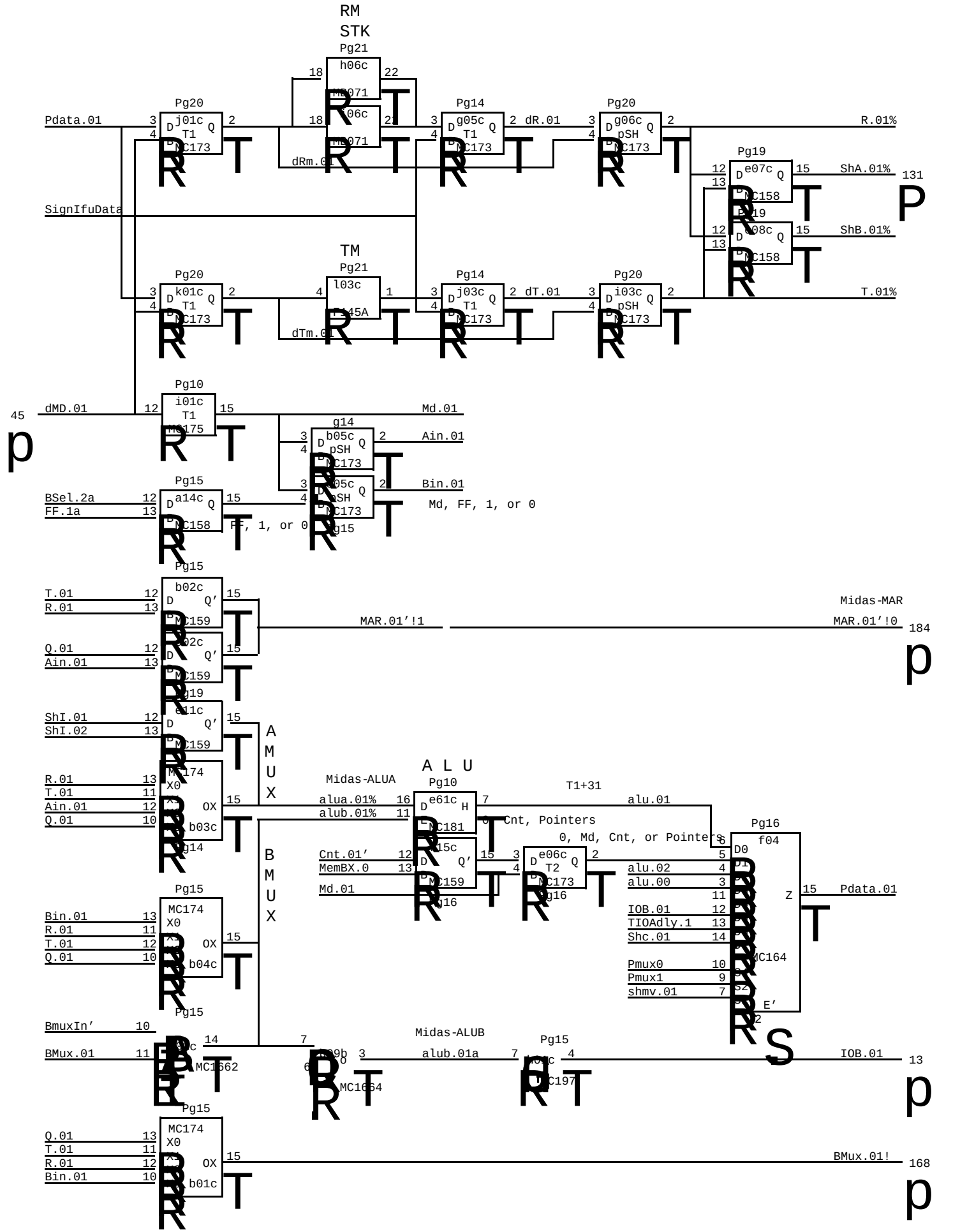


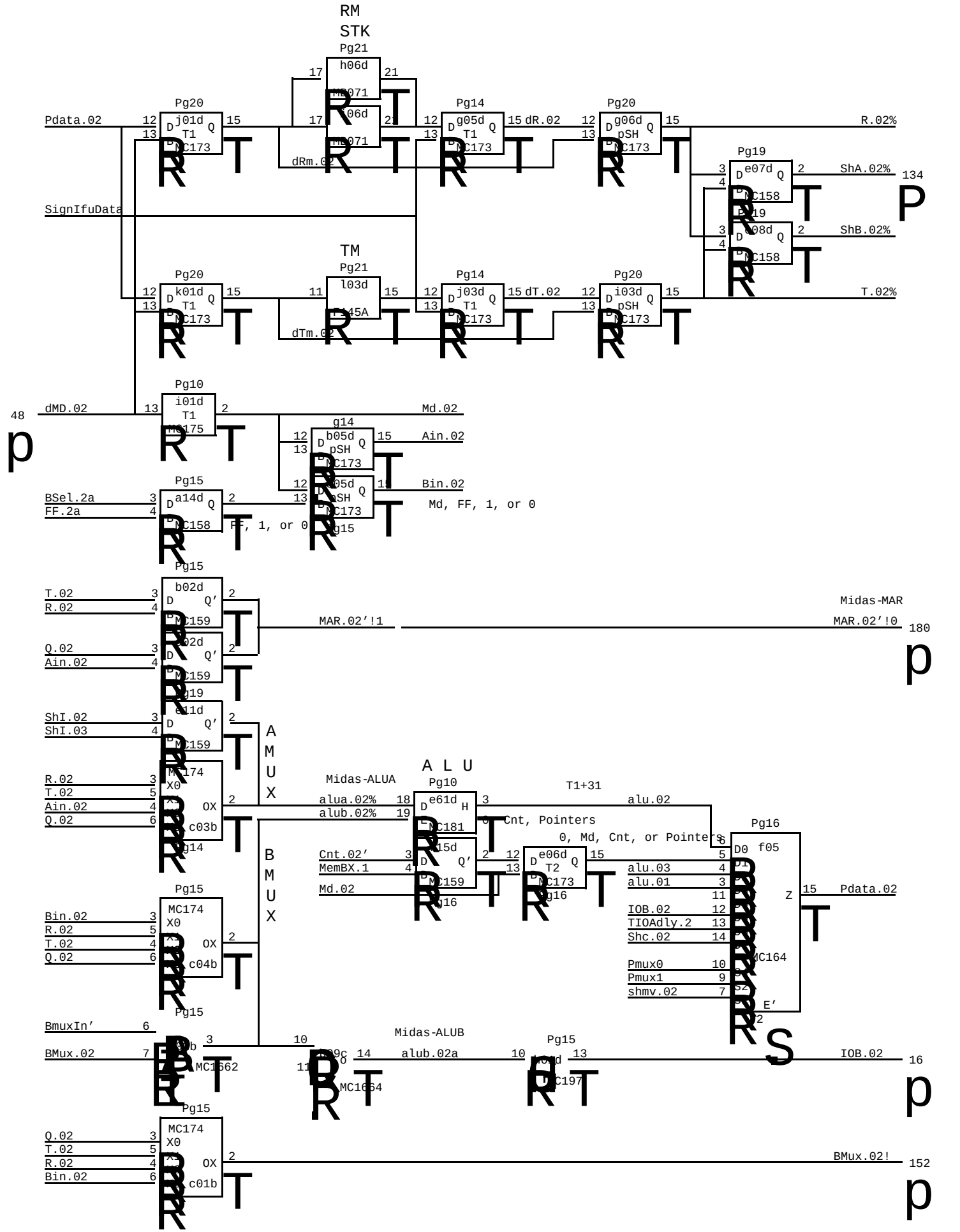
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Block Diagram	ProcH01.sil	R Bates	Ce	11/15/78	01



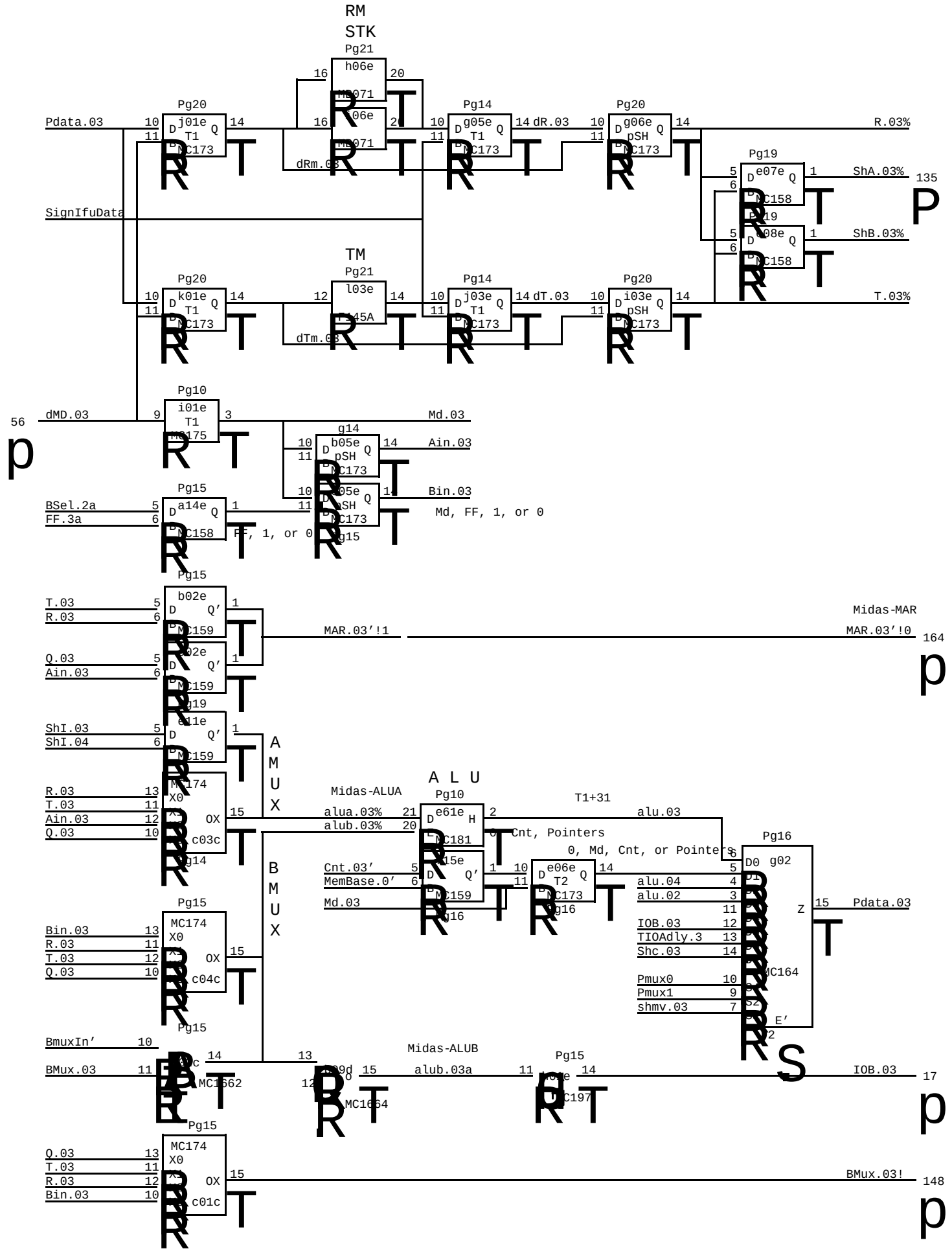
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 00	ProcH02.sil	R Bates	Ce	6/18/79	02



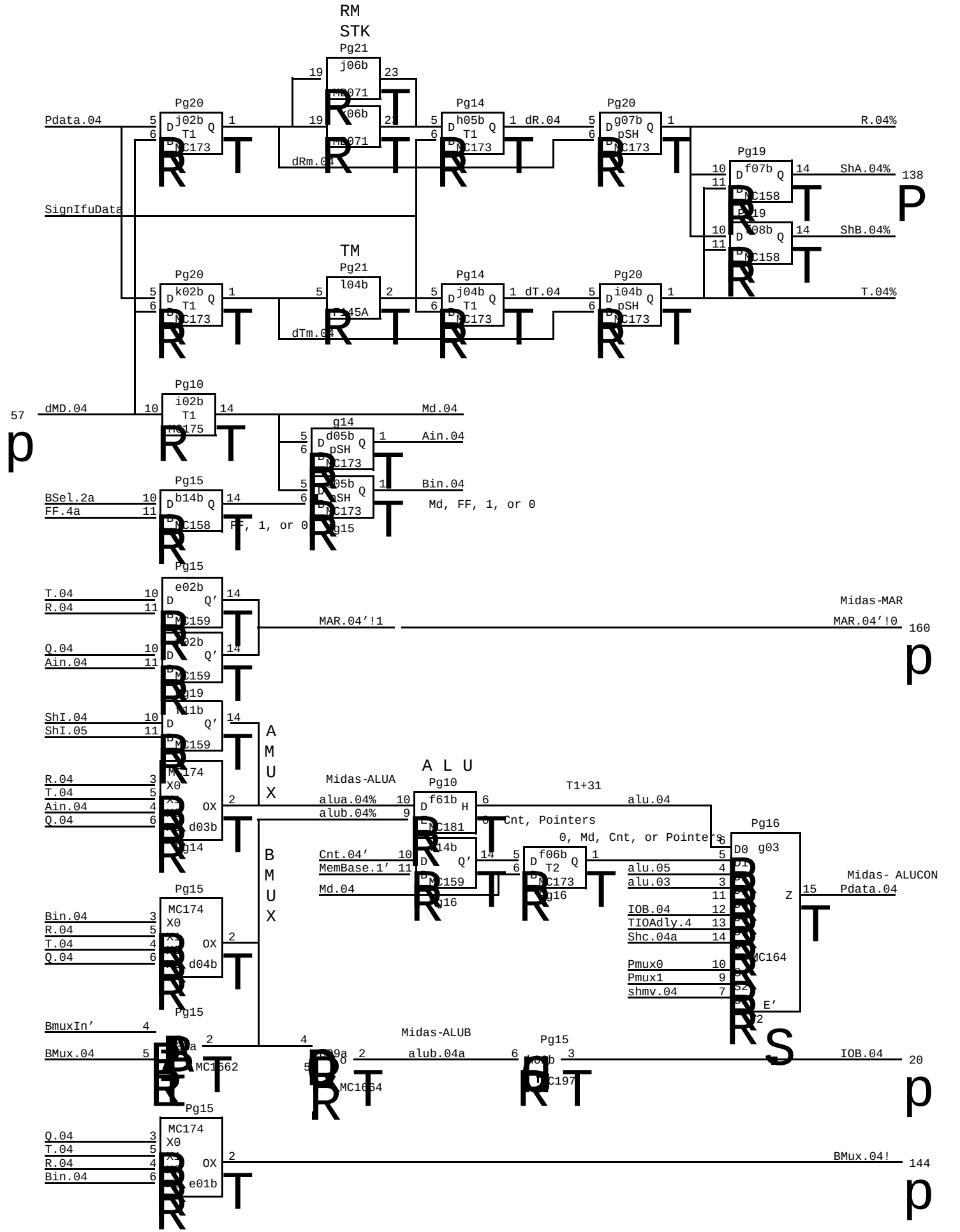
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 01	ProcH03.sil	R Bates	Ce	6/18/79	03



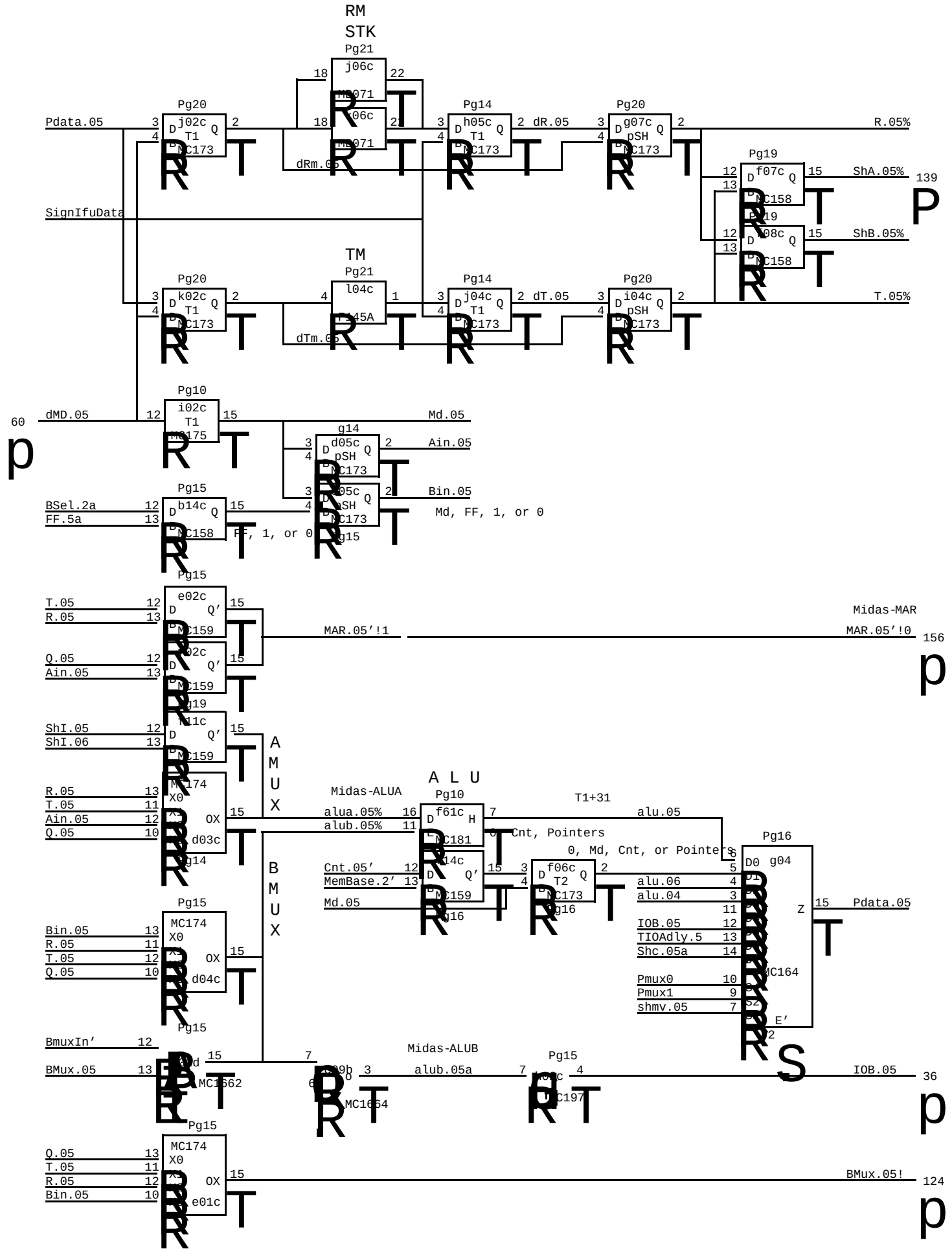
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 02	ProcH04.sil	R Bates	Ce	6/19/79	04



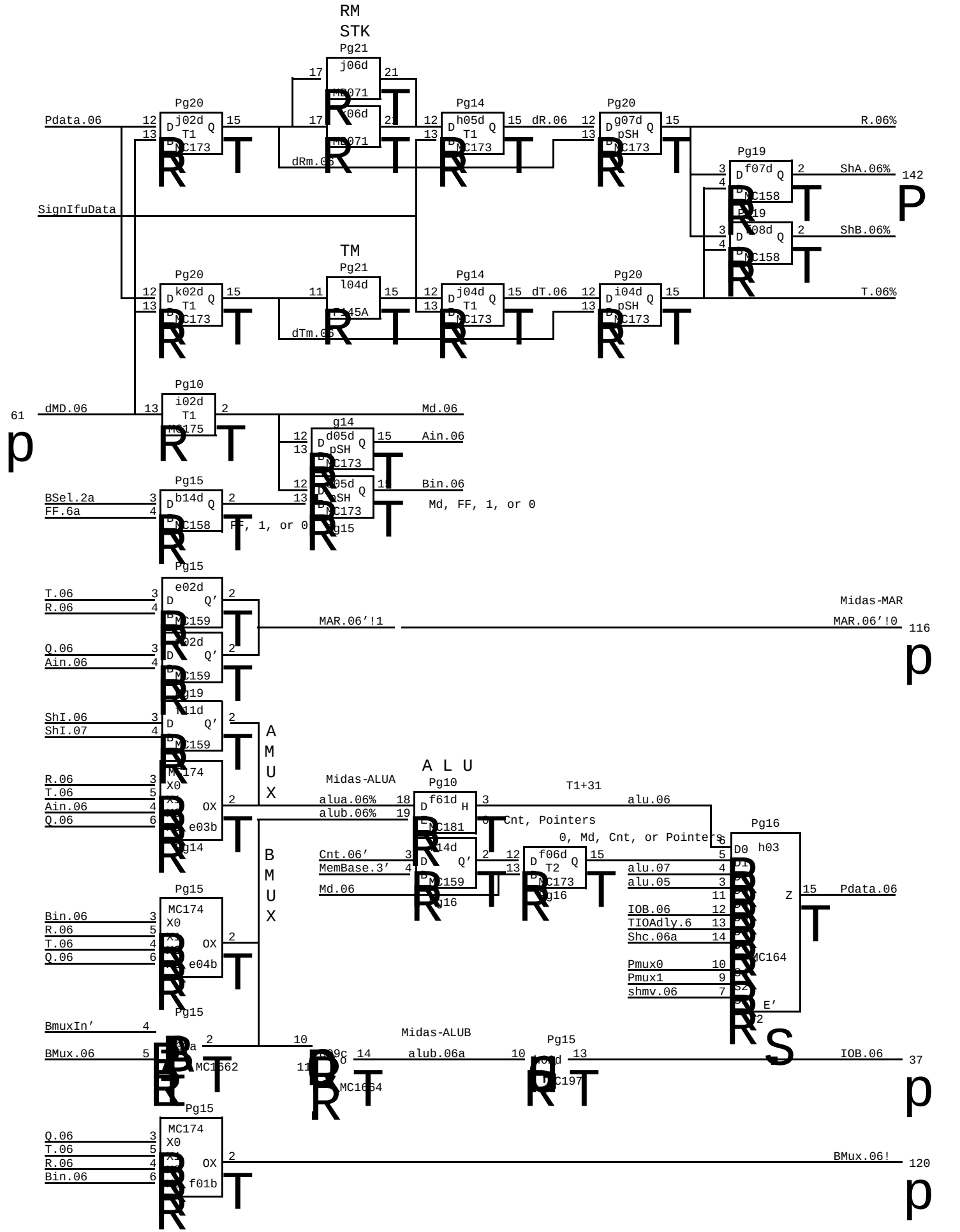
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 03	ProcH05.sil	R Bates	Ce	6/19/79	05



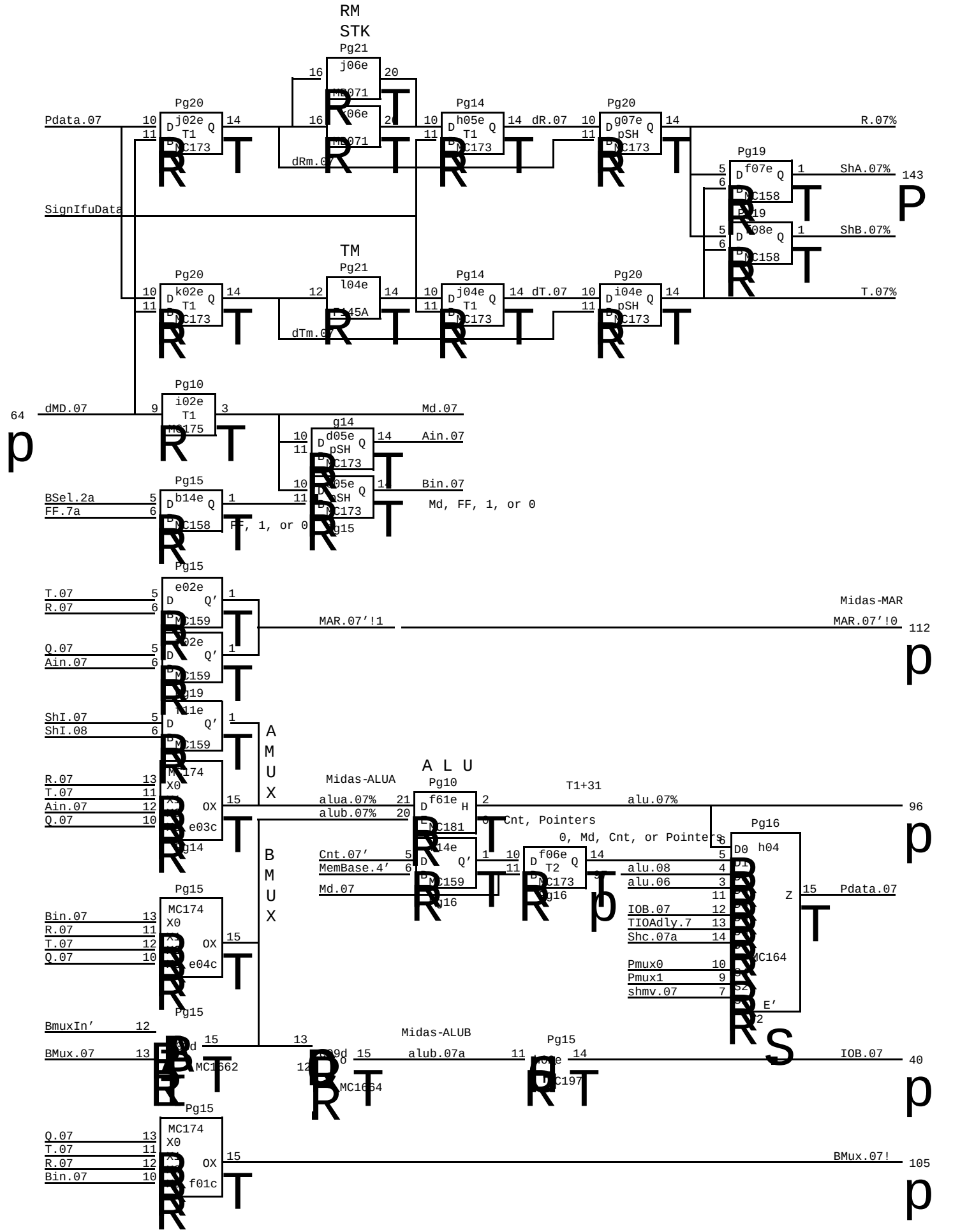
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 04	ProcH06.sil	R Bates	Ce	6/19/79	06



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 05	ProcH07.sil	R Bates	Ce	6/19/79	07



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 06	ProcH08.sil	R Bates	Ce	6/19/79	08


RM
STK
TM
A L U
A
M
U
X
B
M
U
X
Pdata.07
SignIfuData
dRm.07
dTm.07
dR.07
dT.07
R.07%
T.07%
ShA.07%
ShB.07%
dMD.07
Md.07
Ain.07
Bin.07
Md, FF, 1, or 0
FF, 1, or 0
BSel.2a
FF.7a
MAR.07'!1
Midas-MAR
MAR.07'!0
ShI.07
ShI.08
Midas-ALUA
alua.07%
alub.07%
T1+31
alu.07%
Cnt, Pointers
0, Md, Cnt, or Pointers
Cnt.07'
MemBase.4'
Md.07
alu.08
alu.06
IOB.07
TIOAdly.7
Shc.07a
Pmux0
Pmux1
shmv.07
Pdata.07
BmuxIn'
BMux.07
Midas-ALUB
alub.07a
IOB.07
Q.07
T.07
R.07
Bin.07
BMux.07!
XEROX
PARC
Project
Dorado
Drawing
BIT SLICE 07
File
ProcH09.sil
Designer
R Bates
Rev
Ce
Date
6/19/79
Page
09

ALU delays

Logical function to output = 11.9

Arithmetic operation to data = 20.0

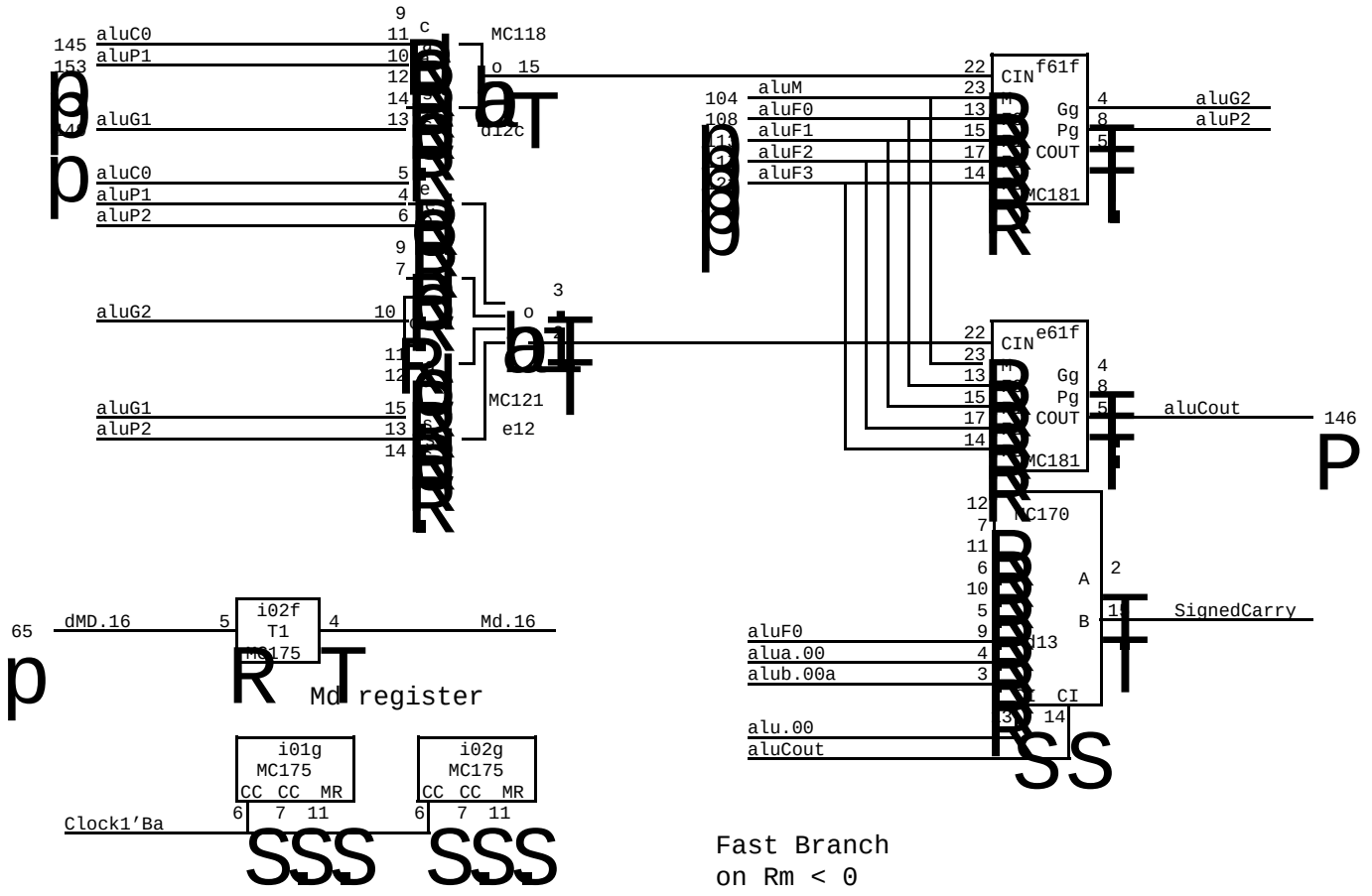
Arithmetic operation to carry = 17.9

ALU output (assuming 10.2 ns to output of BMux)

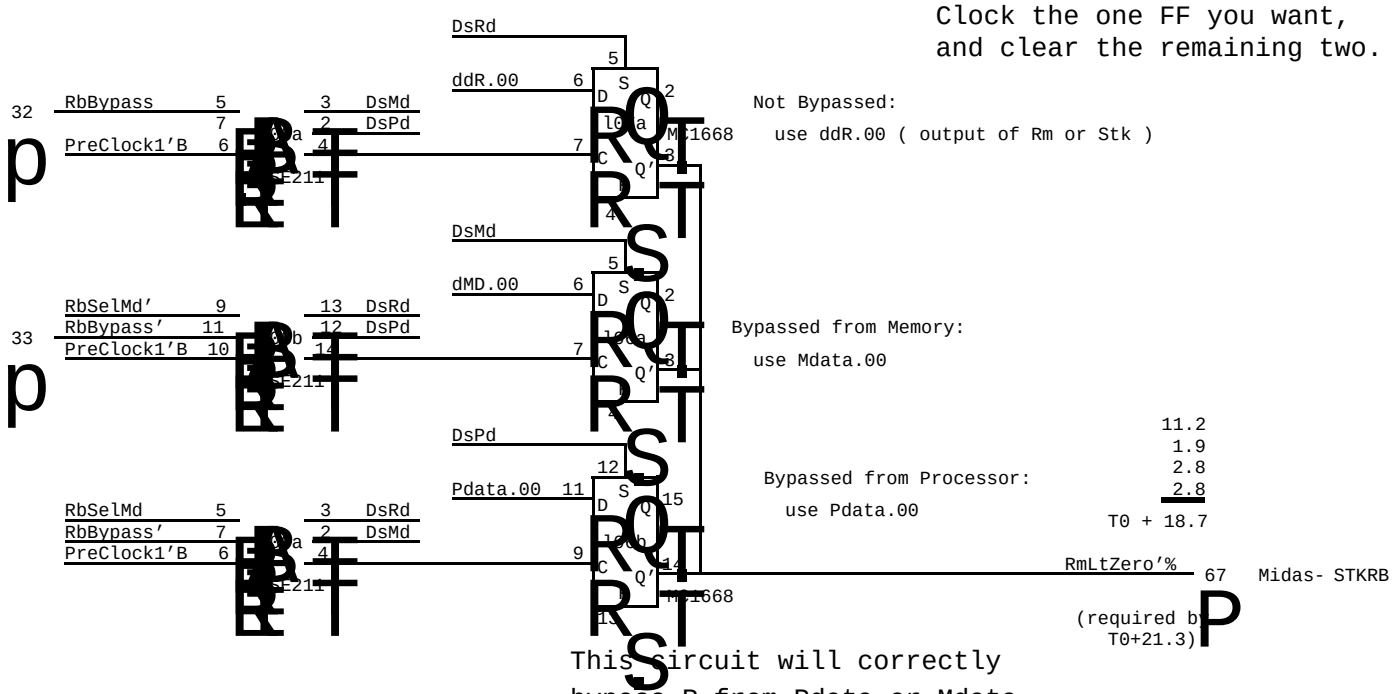
Logical Function = 22.0

Arithmetic operation to data = 30.1

Arthmetic operation to carry = 28.0

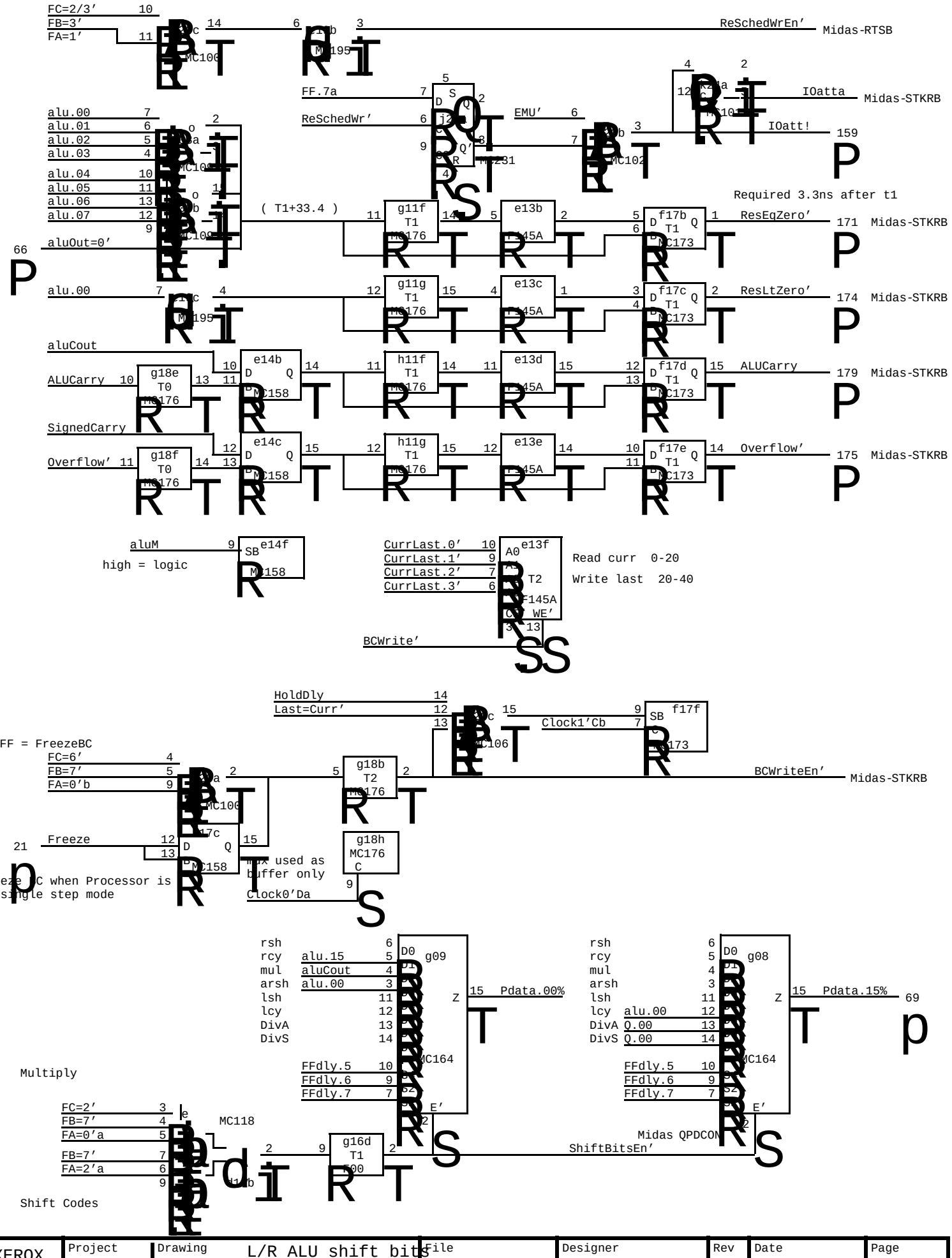


Clock the one FF you want,
and clear the remaining two.

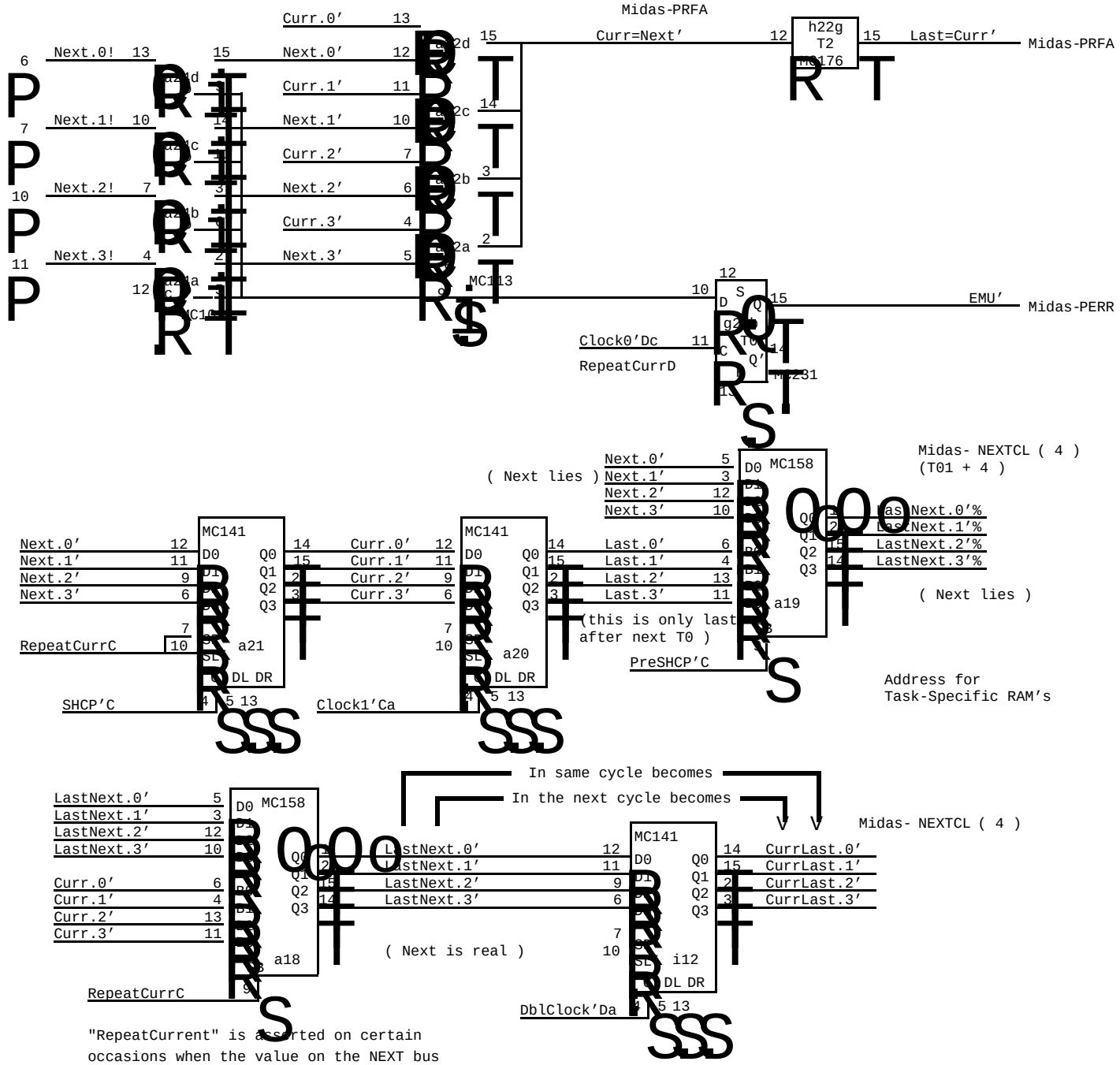


This circuit will correctly
bypass R from Pdata or Mdata
When "RisIfData" is in effect, the fast branch
will be based on the contents of the addressed
RM or STK, bypassed if necessary.

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Atithmetic Logic Unit	ProcH10.sil	R Bates	Ce	6/18/79	10

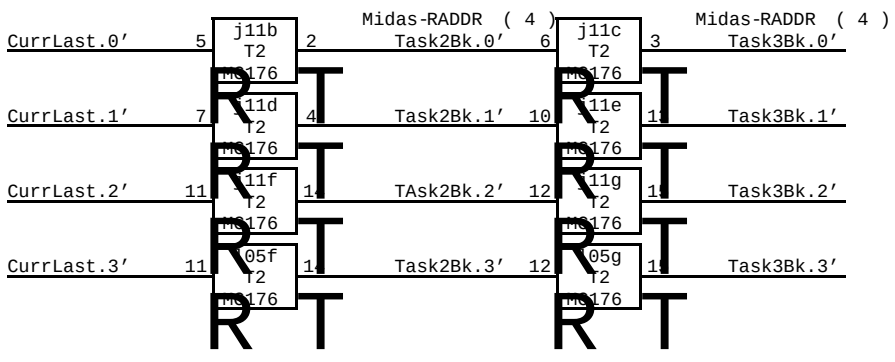


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	L/R ALU shift bits Branch Condition Ram	ProcH11.sil	R. Bates	Ce	6/18/79	11



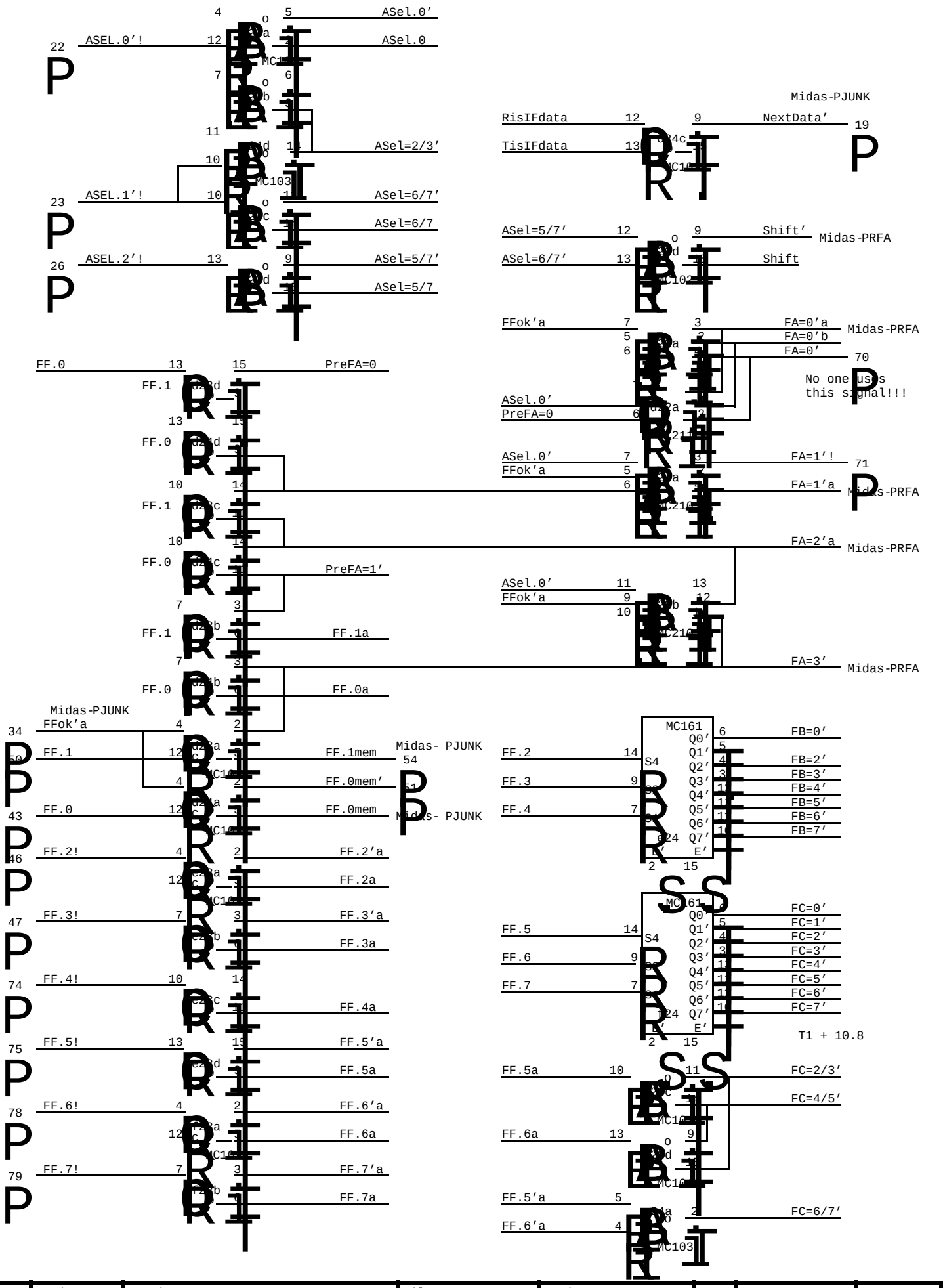
Task number tracking logic

Task number tracking logic (for Midas)



These are saved values of Task number so that Midas can determing the task running whenever a parity error occurs

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Task logic	ProcH12.sil	R. Bates	Ce	7/08/79	12



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Function Field Decoding	ProcH13.sil	R Bates	Ce	6/18/79	13

AMux decoding

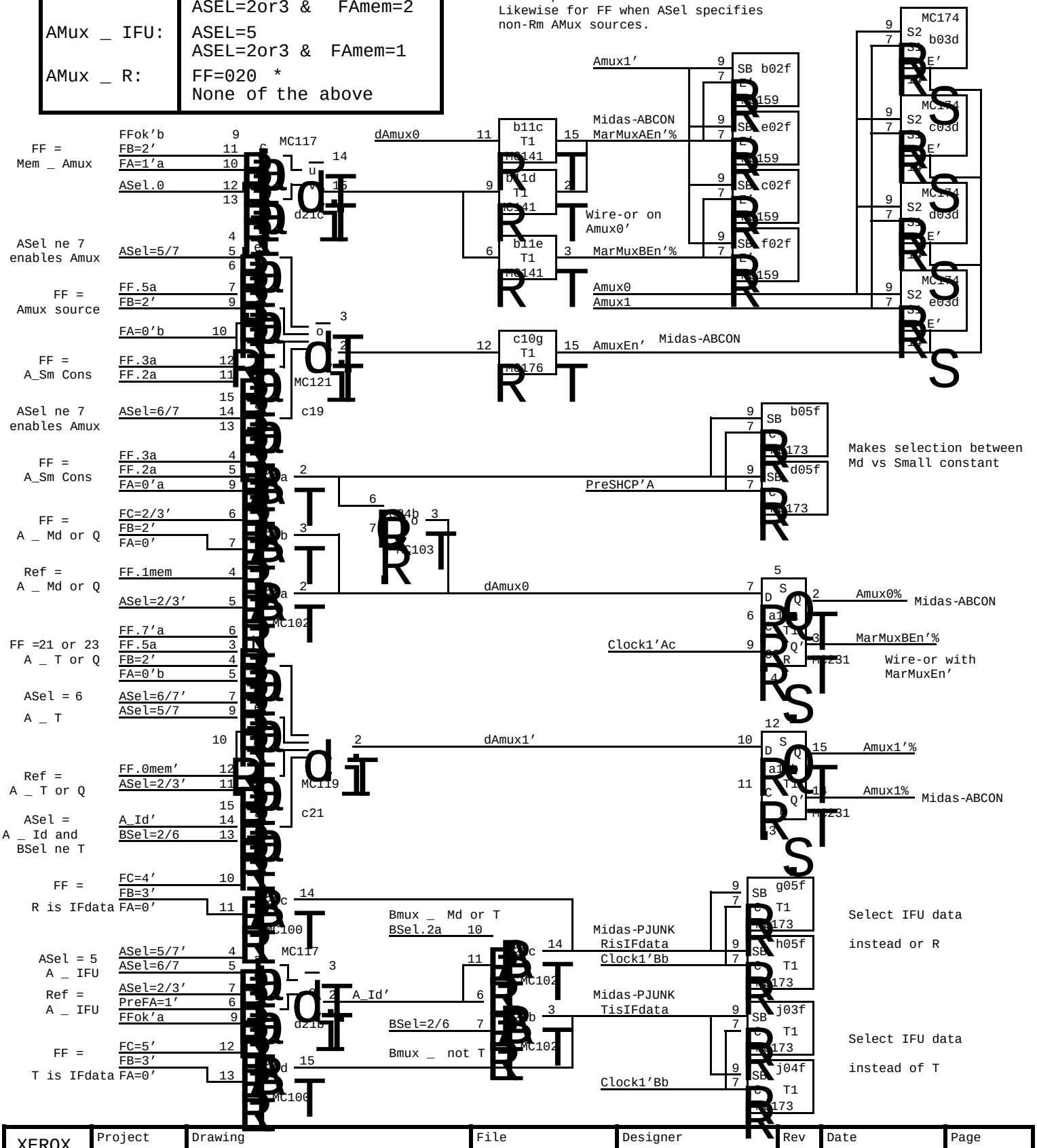
AMux _ FF:	FF=0-17 *
AMux _ T:	FF=021 * ASEL=2or3 & FAmem=3 ASEL=6
AMux _ Md:	FF=022 * ASEL=2or3 & FAmem=0
AMux _ Q:	FF=023 * ASEL=2or3 & FAmem=2
AMux _ IFU:	ASEL=5 ASEL=2or3 & FAmem=1
AMux _ R:	FF=020 * None of the above

* The Amux is disabled by ASEL=7 unless one of these codes are in effect

NOTE: ASel selects and FF selects for the AMux are "OR'd" by this hardware. Thus ASel codes selecting non-Rm sources of Amux must not be used when an FF specifies an ASel source. Likewise for FF when ASel specifies non-Rm AMux sources.

AMux encoding

Mux Input	Source
0	R or IFU data
1	T or IFU data
2	Md or Small Const.
3	Q



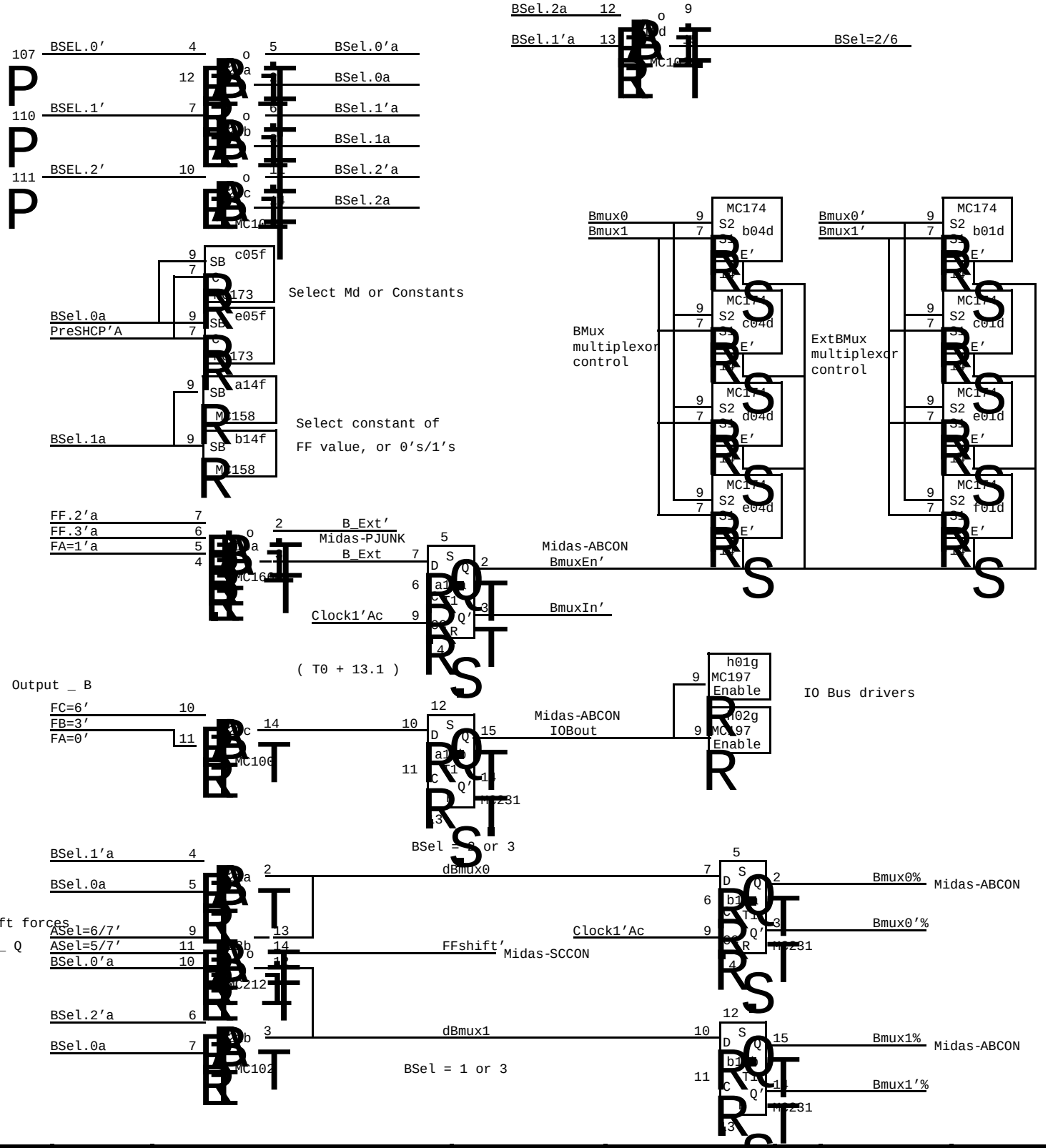
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	"A" Multiplexor Control	ProcH14.sil	R. Bates	Ce	6/18/79	14

BSEL field decoding

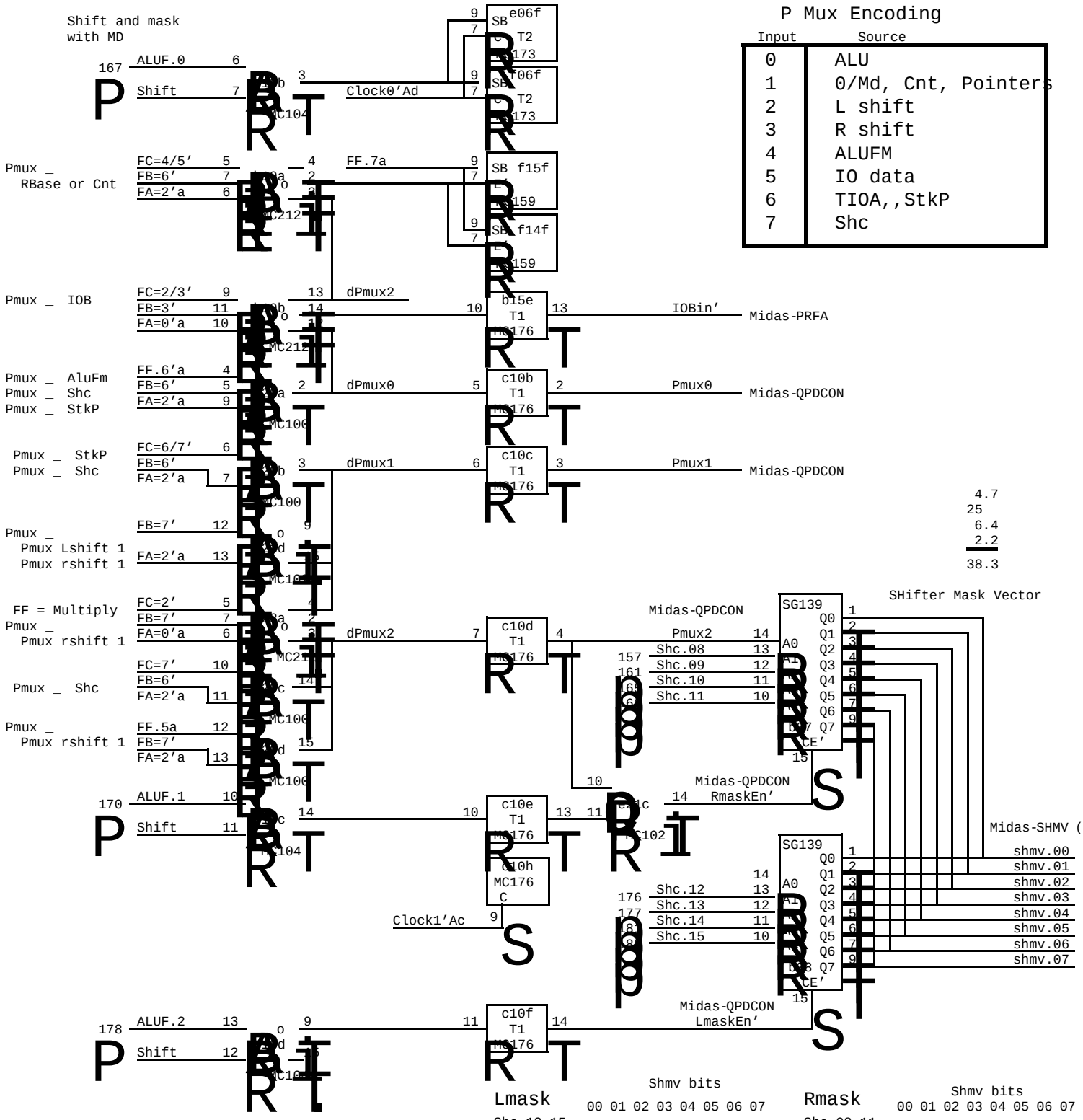
BSEL	INTERNAL	EXTERNAL
0	Md	--
1	R	--
2	T	Hold_B
3	Q	Q _ B
4	0,,FF	--
5	377,FF	--
6	FF,,0	--
7	FF,,377	--

BMux encoding

BMux	
0	Md or Constant
1	R
2	T
3	Q



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	"B" Multiplexor & Cont.	ProcH15.sil	R Bates	Ce	6/20/79	15



NOTE: The prom patterns are designed so that a one into address bit 0 will produce all 1's on the output. This allows the odd address inputs to Pmux to be selected.

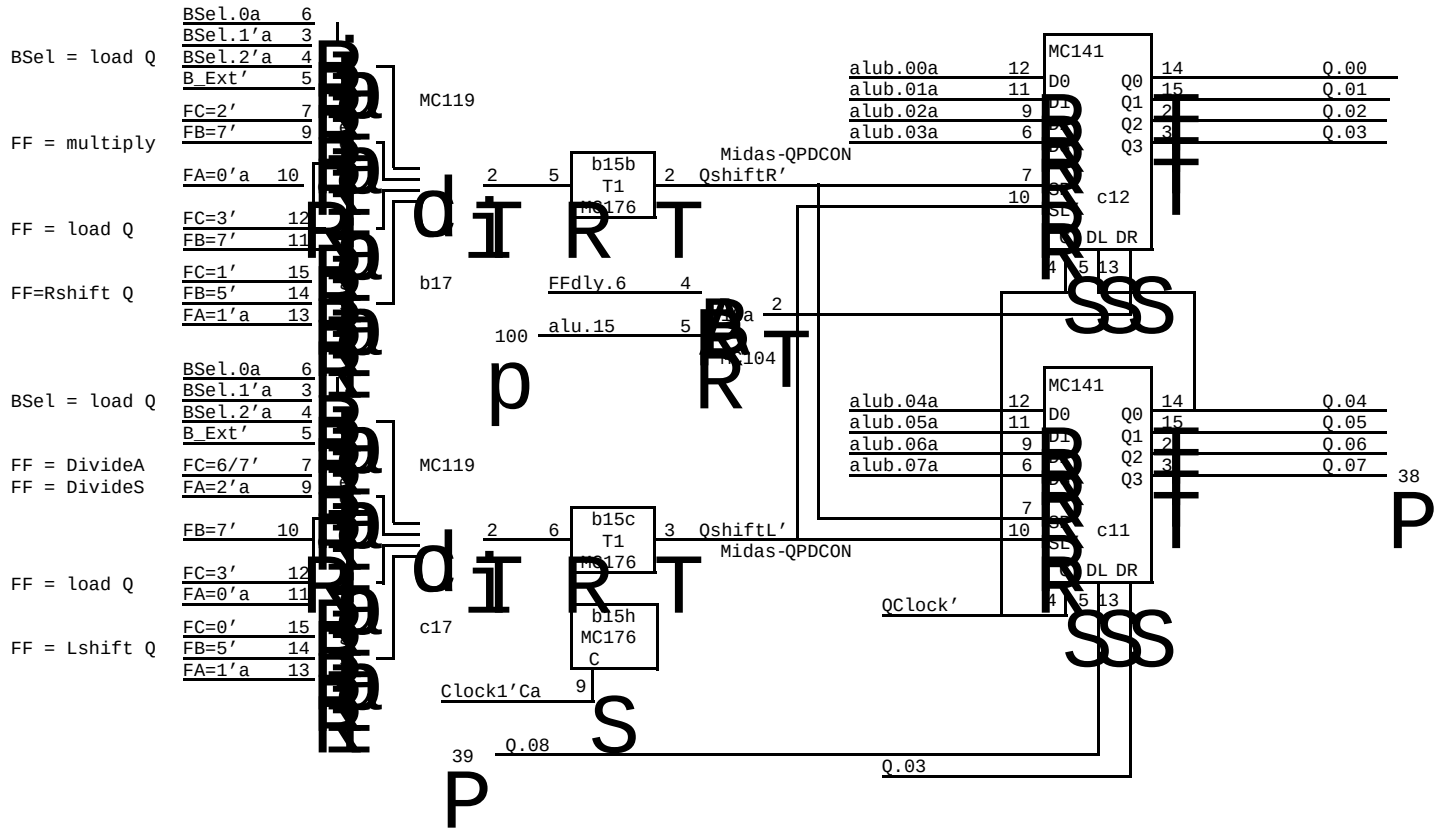
Lmask

Shc.12-15	Shmv bits 00	01	02	03	04	05	06	07
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	1	1	0	0	0
6	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	0
10	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1
12	1	1	1	1	1	1	1	1
13	1	1	1	1	1	1	1	1
14	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1
16	1	1	1	1	1	1	1	1
17	1	1	1	1	1	1	1	1
20- 37	1	1	1	1	1	1	1	1

Rmask

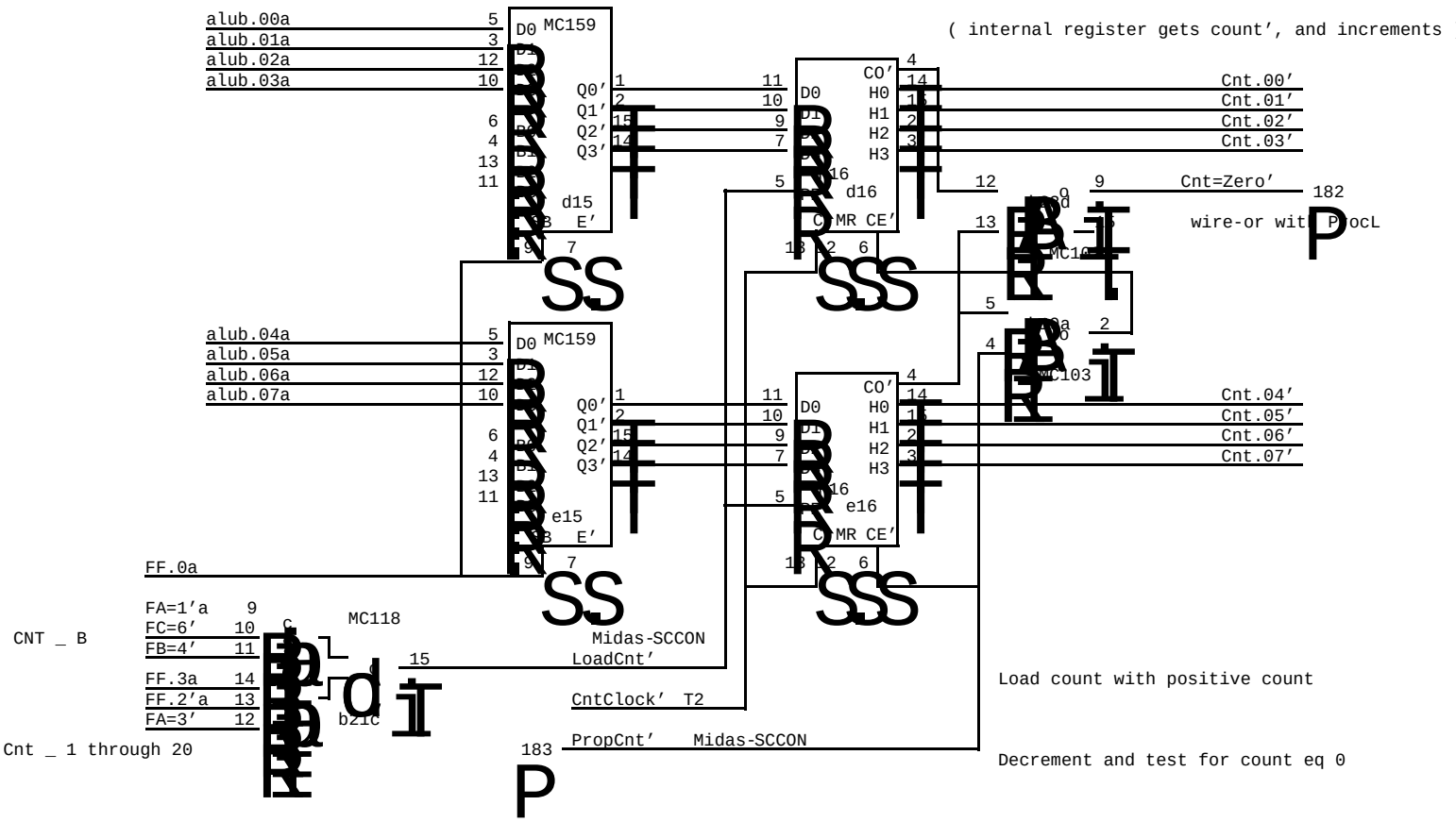
Shc.08-11	Shmv bits 00	01	02	03	04	05	06	07
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	1
12	0	0	0	0	0	0	1	1
13	0	0	0	0	0	1	1	1
14	0	0	0	0	1	1	1	1
15	0	0	0	1	1	1	1	1
16	0	0	1	1	1	1	1	1
17	0	1	1	1	1	1	1	1
20- 37	1	1	1	1	1	1	1	1

XEROX PARC	Project Dorado	Drawing Proc Multiplexor & Shift mask Prom	File ProcH16.sil	Designer R Bates	Rev Ce	Date 6/18/79	Page 16



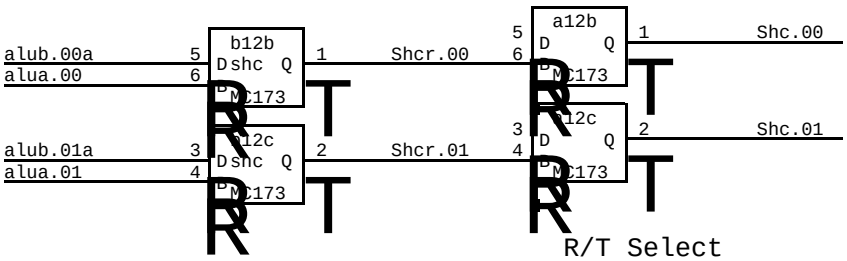
Q Register

Count Register



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Q Register and Count Register	ProcH17.sil	R Bates	Ce	7/08/79	17

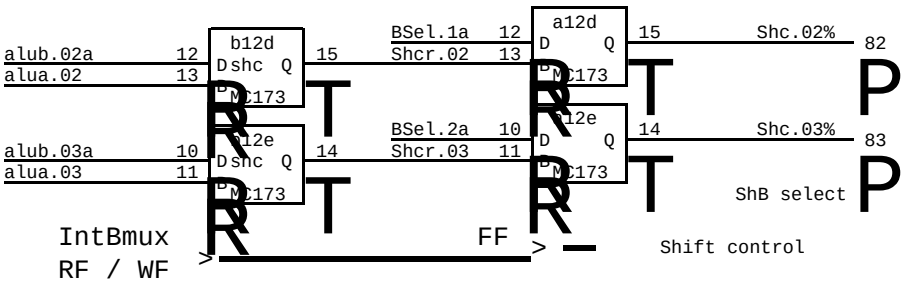
Extra Bits



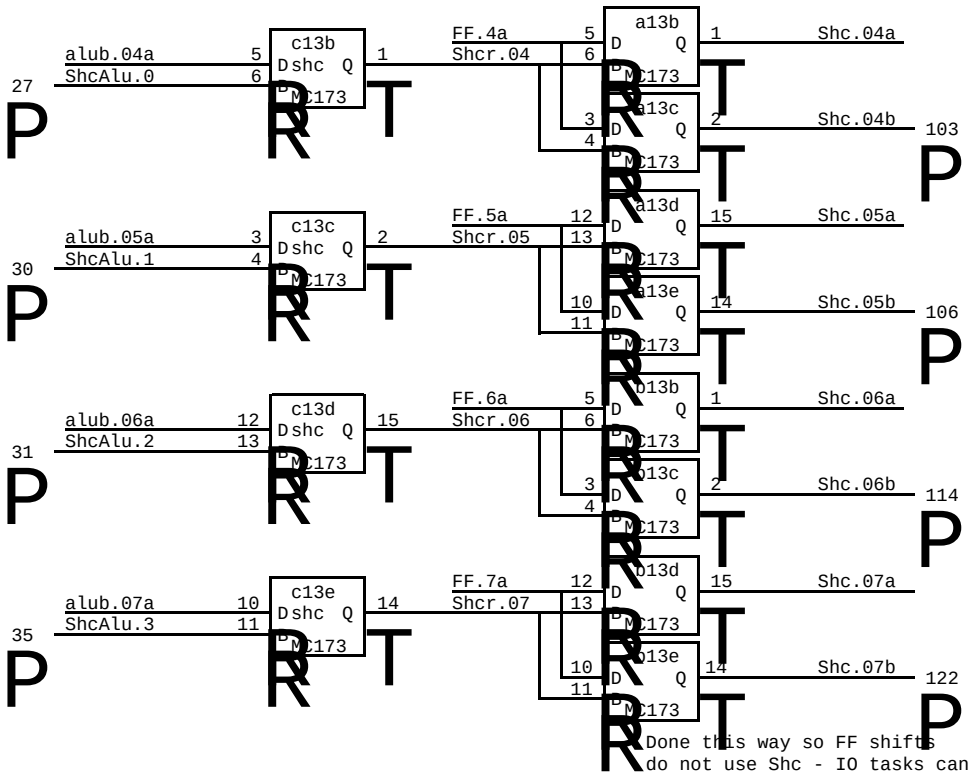
R/T Select

	Shc.02	Shc.03	ProcH ShA	ProcH ShB	ProcL ShA	ProcL ShB
R,,R	0	0	R	R	R	R
R,,T	0	1	R	T	T	R
T,,R	1	0	T	R	R	T
T,,T	1	1	T	T	T	T

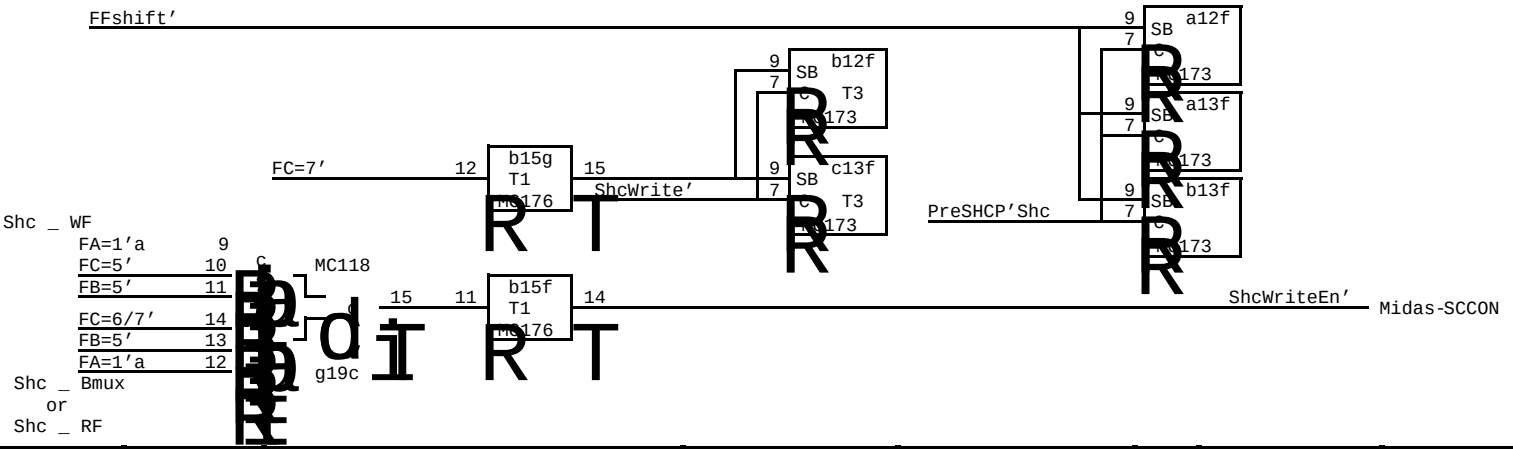
Note R selcted with "0"
T selected with "1"



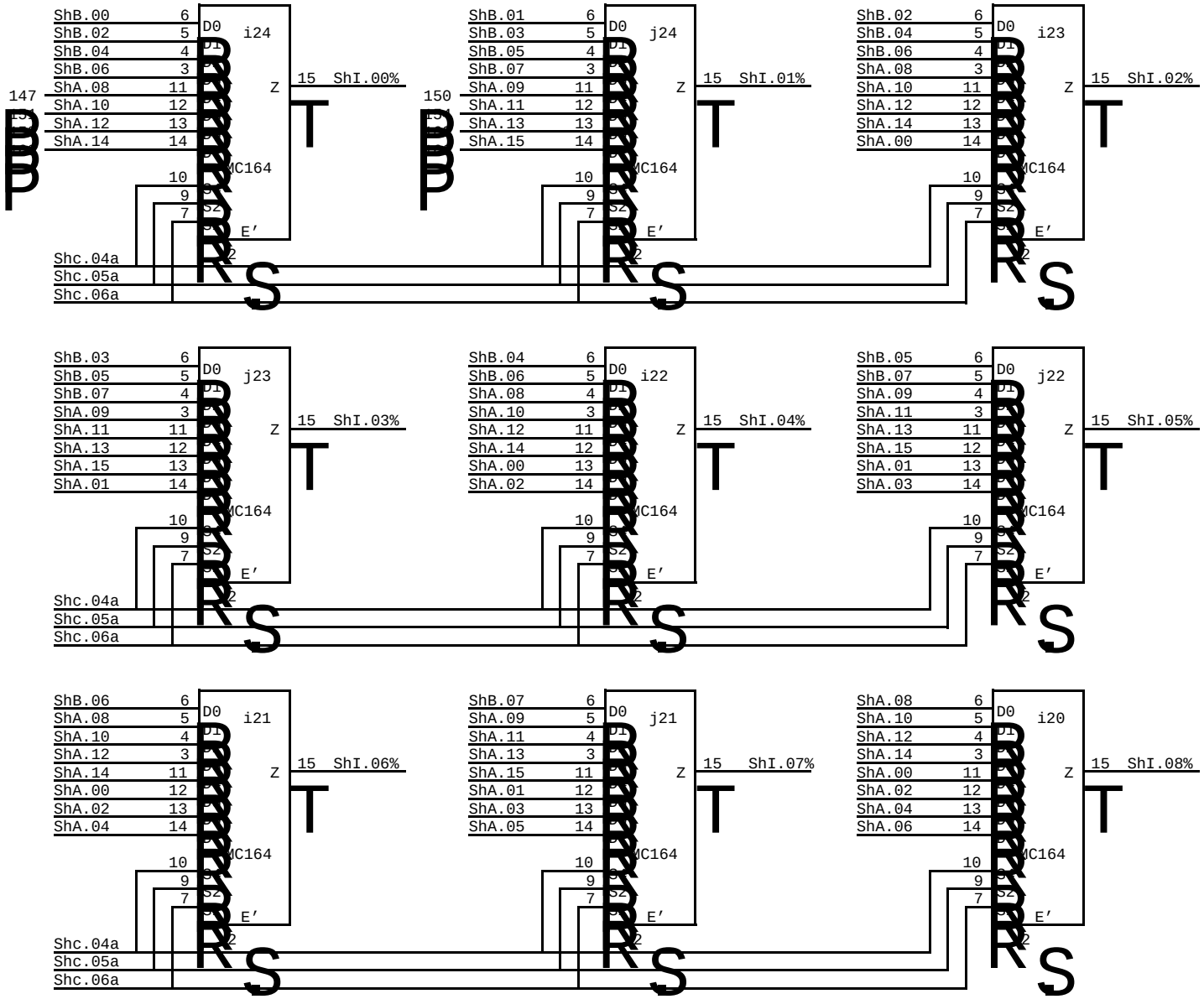
Shift Count

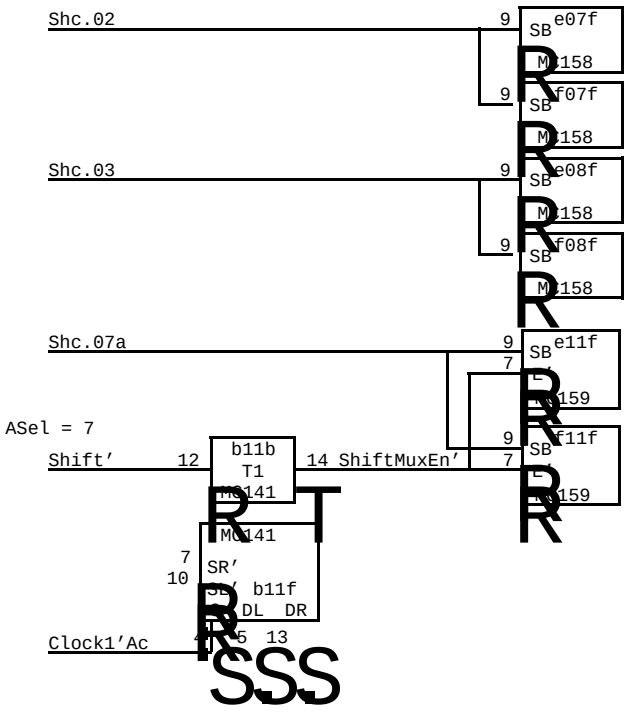


Done this way so FF shifts do not use Shc - IO tasks can use the shifter without saving and restoring Shc.



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Shift Register Control	ProcH18.sil	R Bates	Ce	6/18/79	18





ShA Mux Control

ShB Mux Control

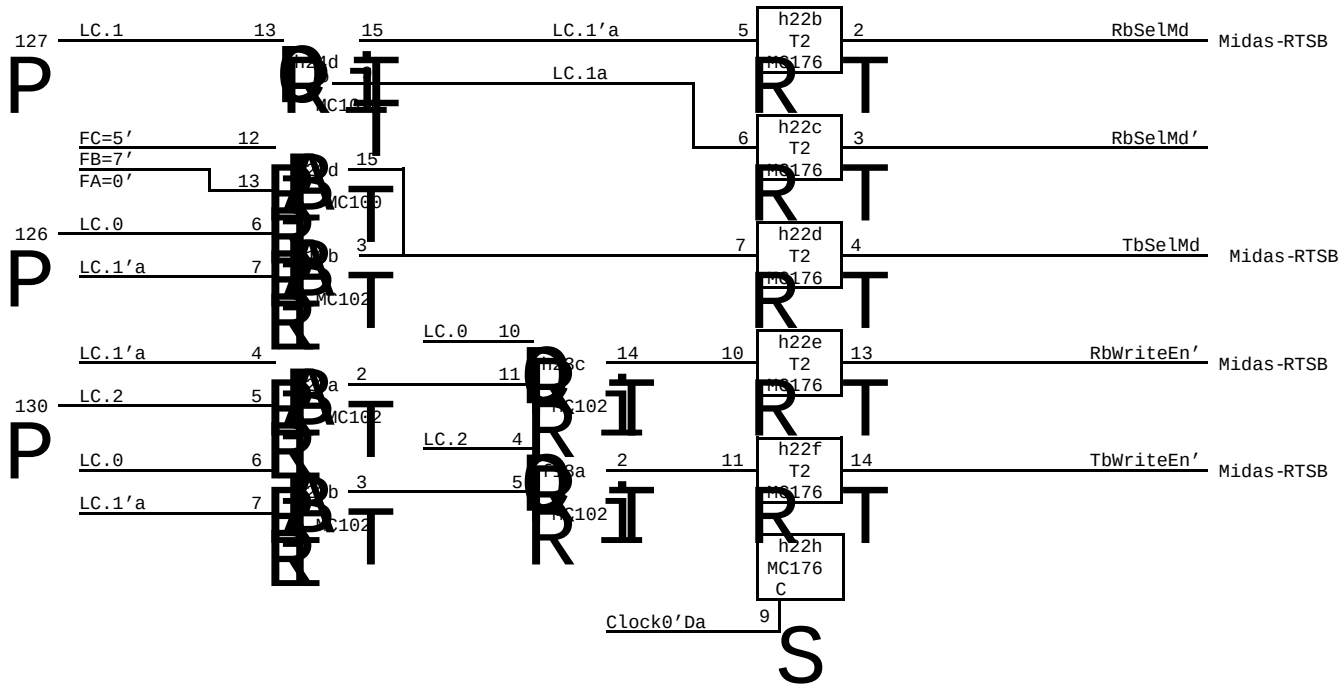
Sh on alua Mux Control

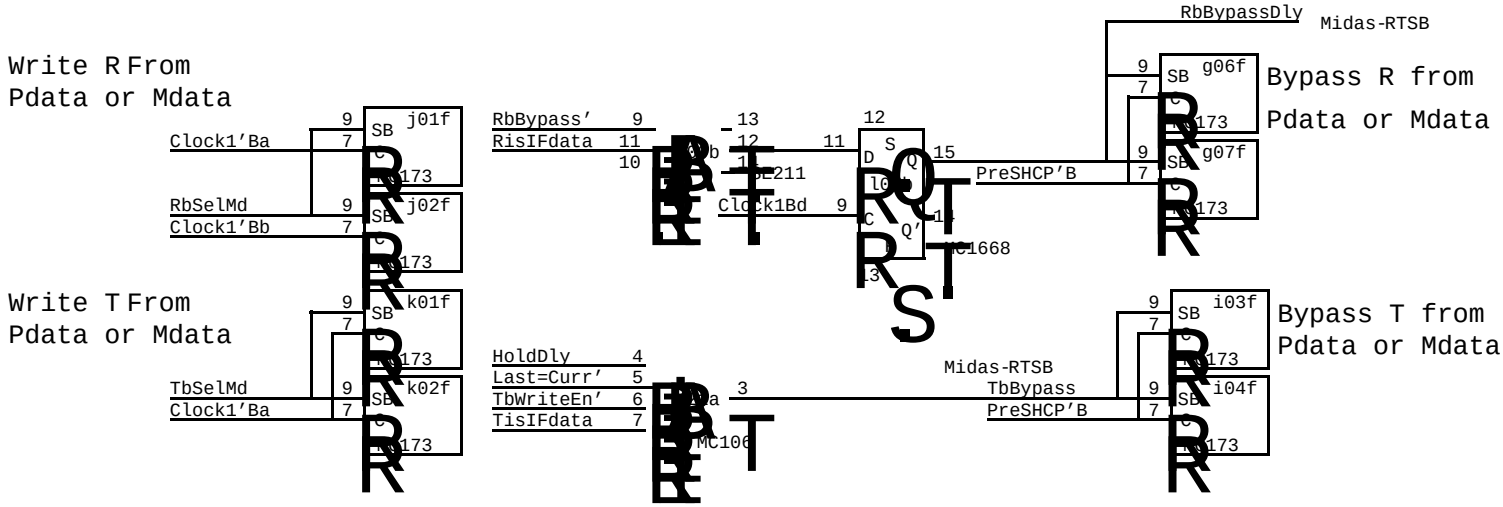
Shc.02	Shc.03	Shc.04 - .07
0	0	16 bit Left cycle o
0	1	16 bit Left cycle, T o
1	0	16 bit Left cycle, R o
1	1	16 bit Left cycle o

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Shifter	ProcH19.sil	R Bates	Ce	6/18/79	19

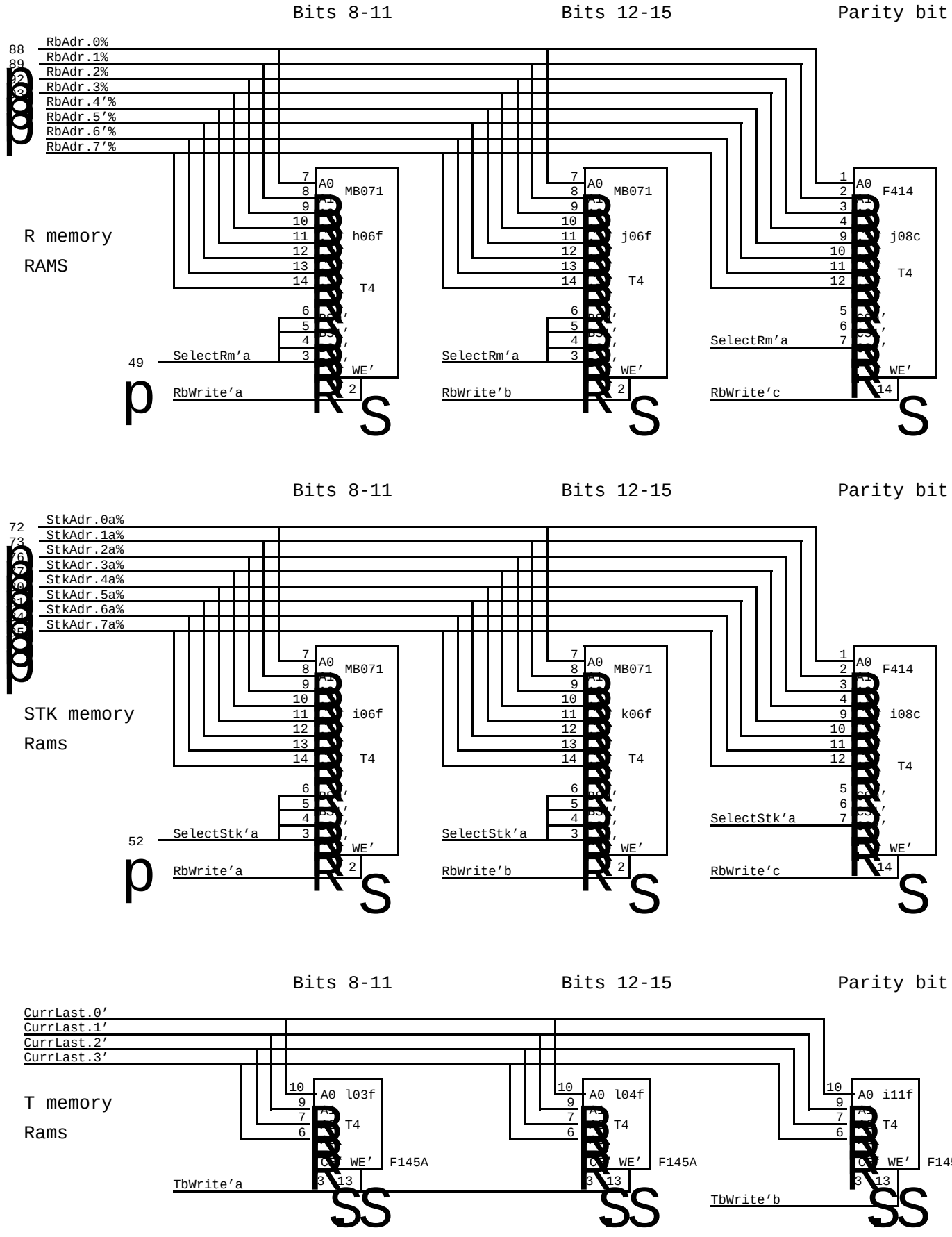
LC 0	LC 1	LC 2	R	T
0	0	0	-	-
0	0	1	-	Pd *
0	1	0	Pd	Md
0	1	1	-	Md
1	0	0	Md	-
1	0	1	Md	Pd *
1	1	0	Pd	-
1	1	1	Pd	Pd *

* Md if used when FF = 075



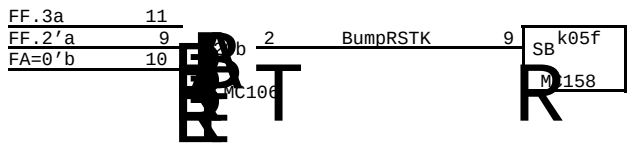


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	LC FIELD RAM ADDRESSES	ProcH20.sil	R Bates	Ce	6/18/79	20



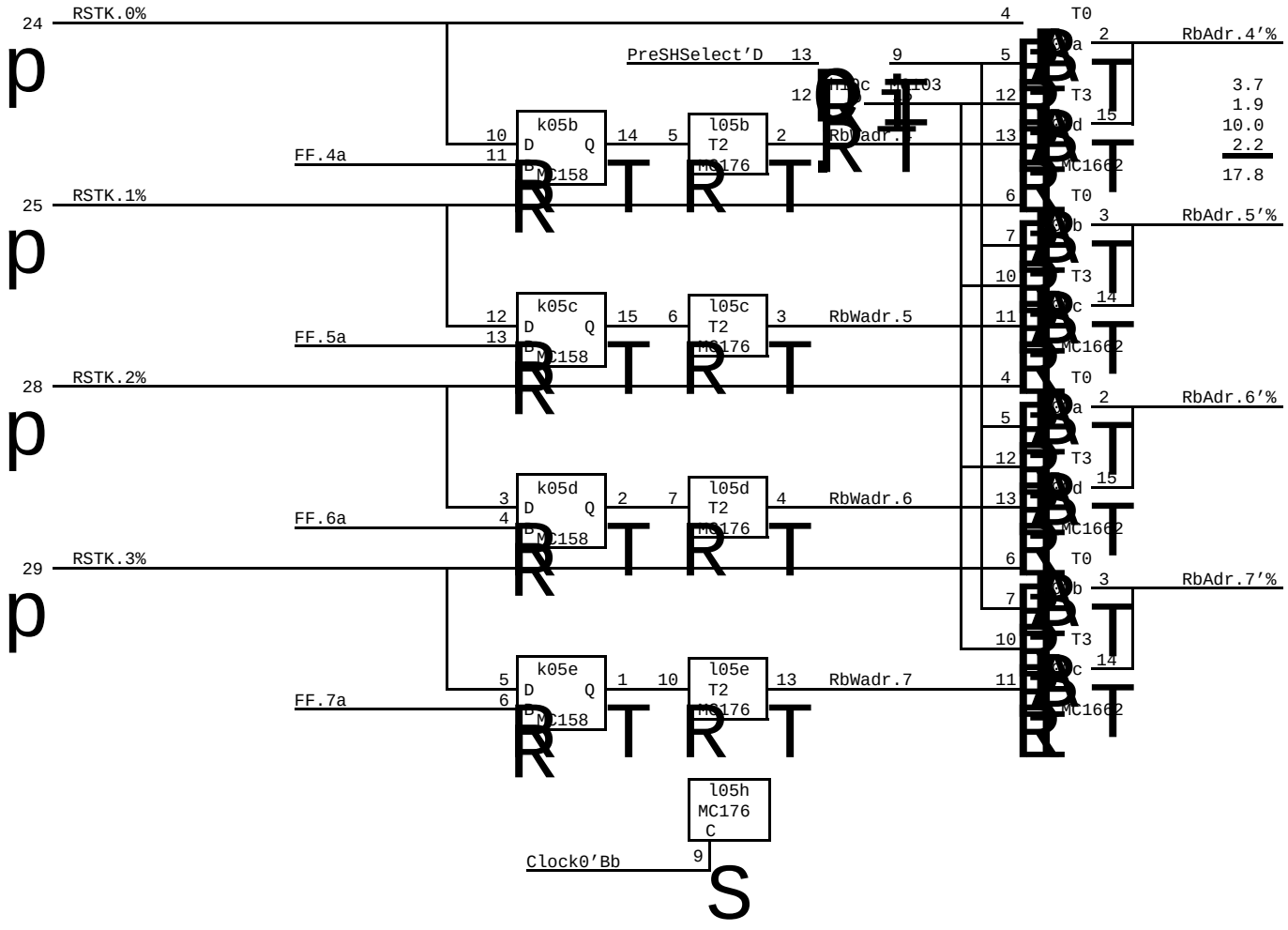
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	RM & STK addressing	ProcH21.sil	R Bates	Ce	6/18/79	21

RbWadr _ RBase,,FF

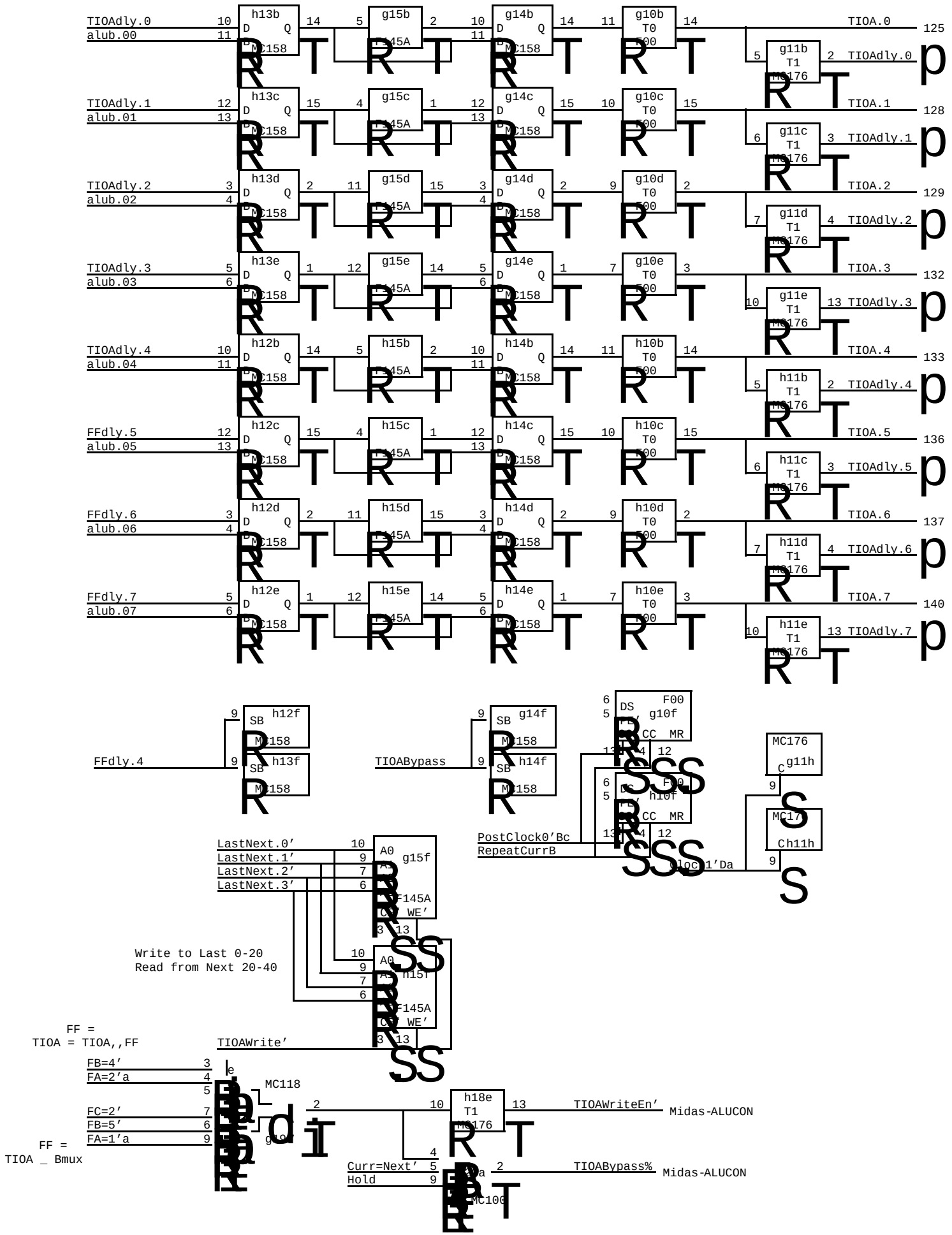


RSTK Control for bits 4 - 7 of the Rm address

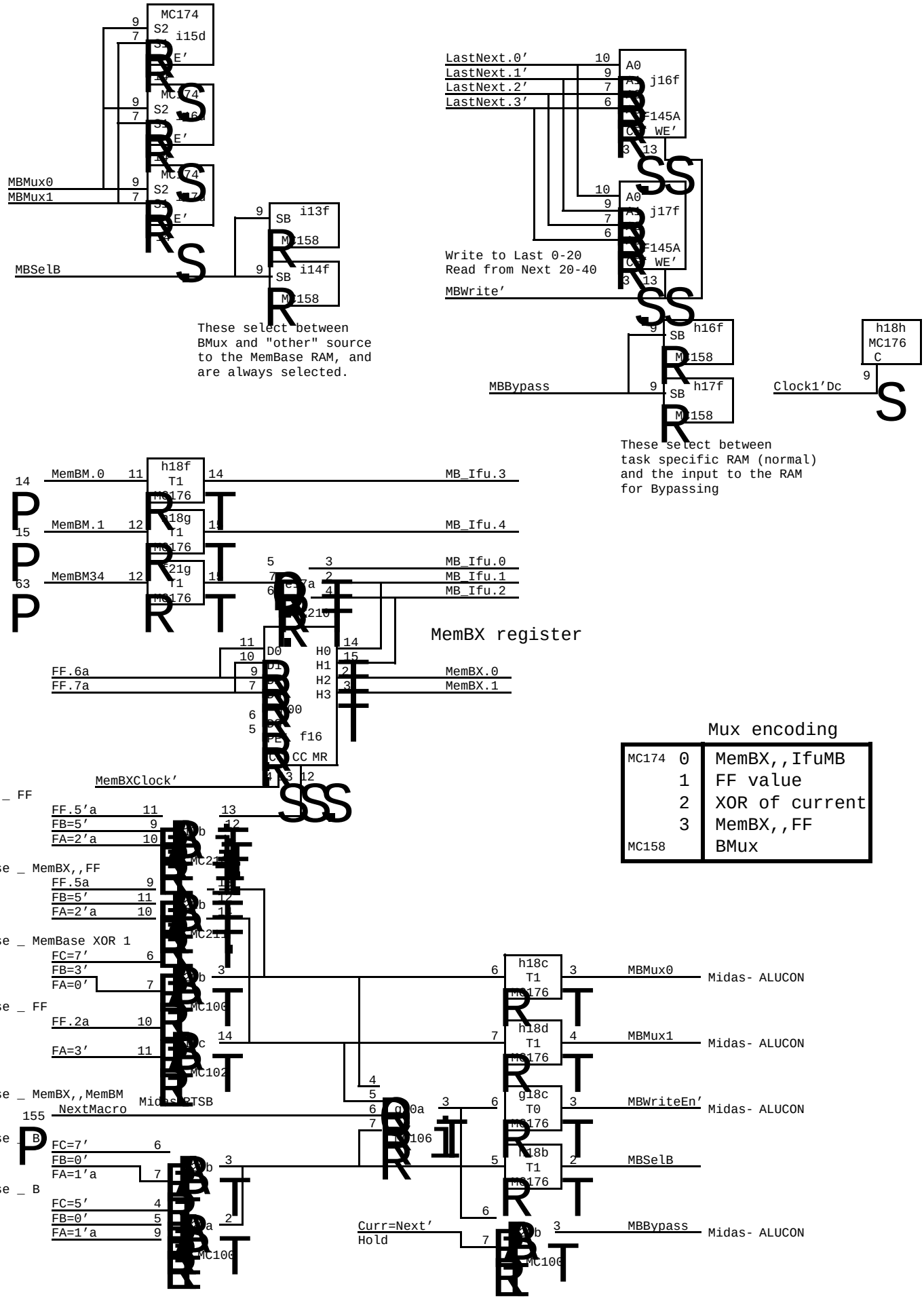
RSTK bits that make up Rm address bits 4-7



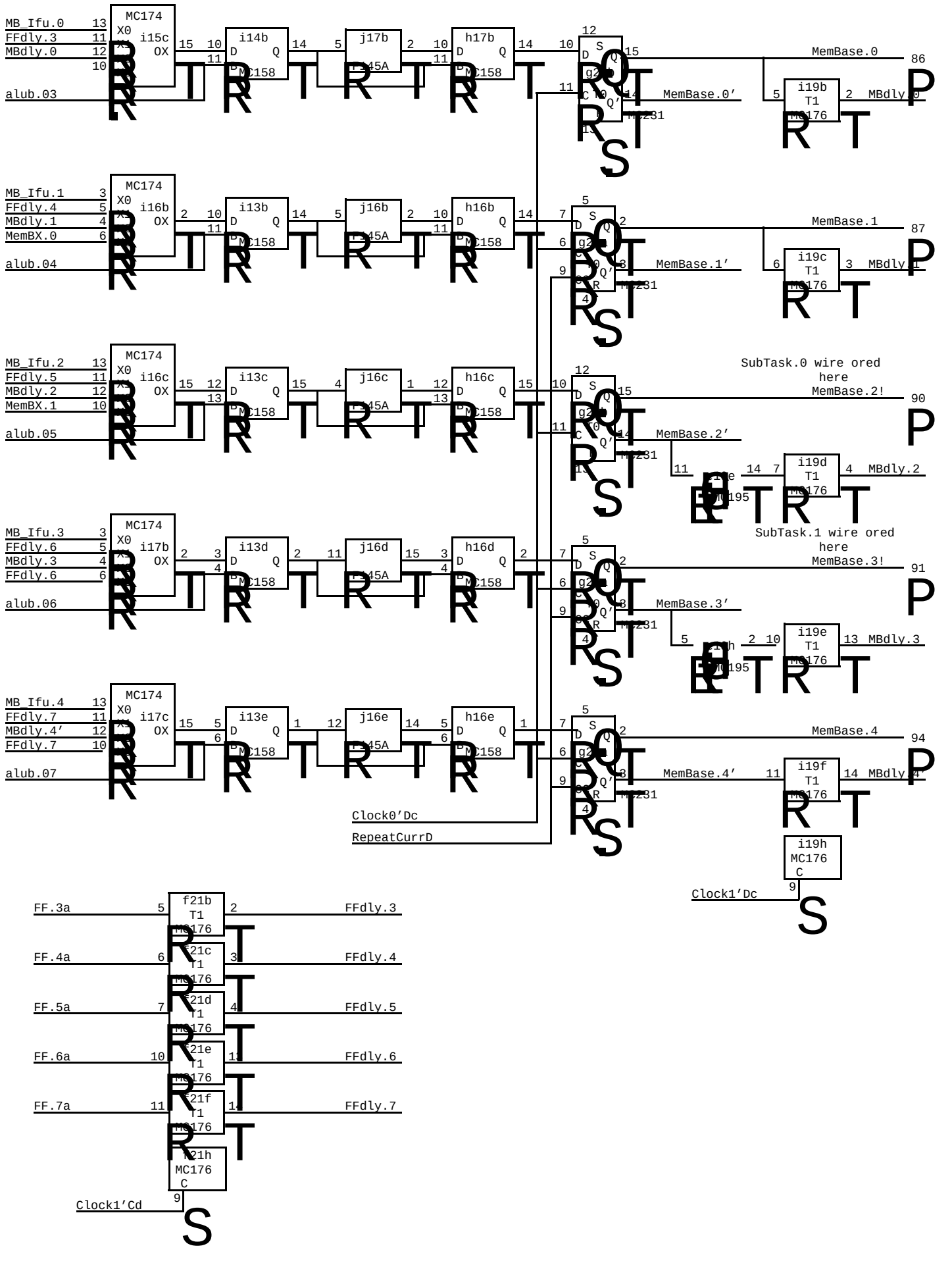
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	R memory Address logic	ProcH22.sil	R Bates	Ce	6/20/79	22



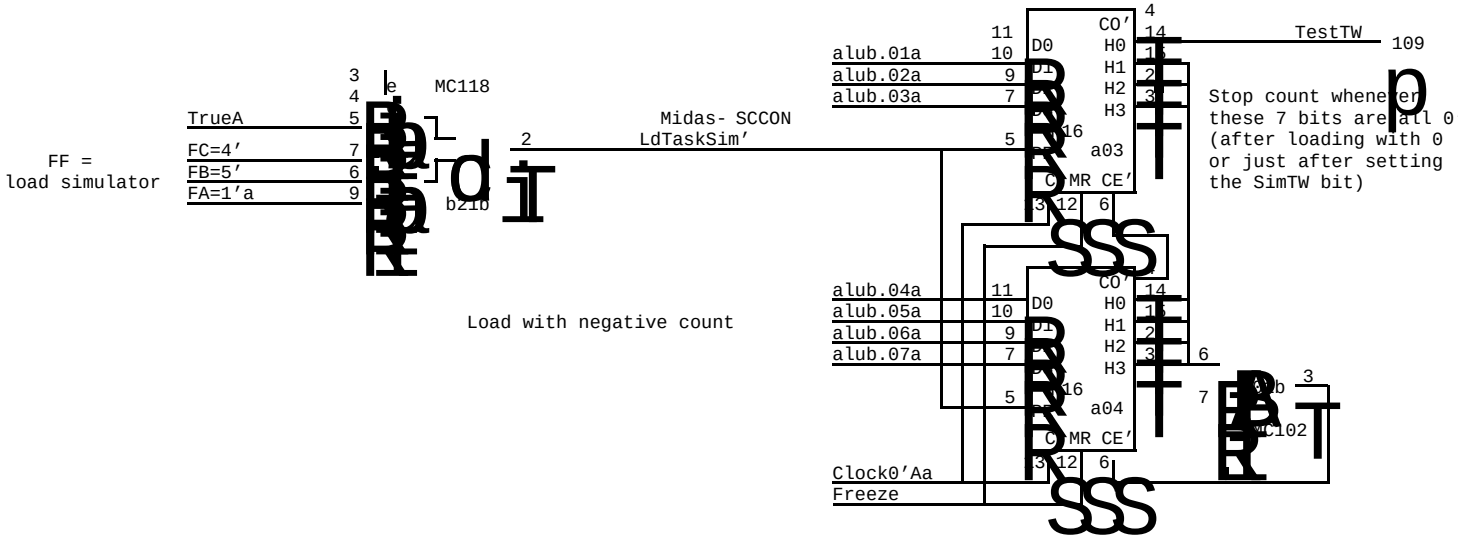
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	I/O ADDRESS RAM	ProcH23.sil	R Bates	Ce	6/18/79	23



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	MemBase Register Cont.	ProcH24.sil	R Bates	Ce	6/18/79	24



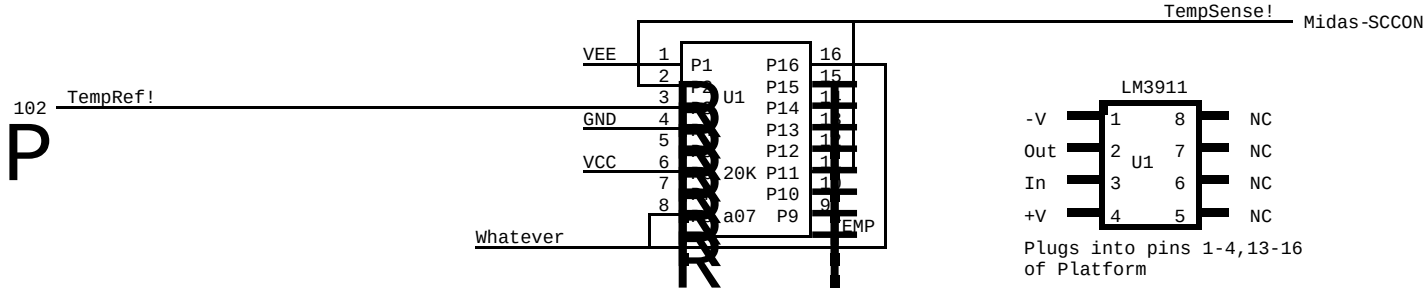
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Map Base Addressing	ProcH25.sil	R Bates	Ce	6/18/79	25



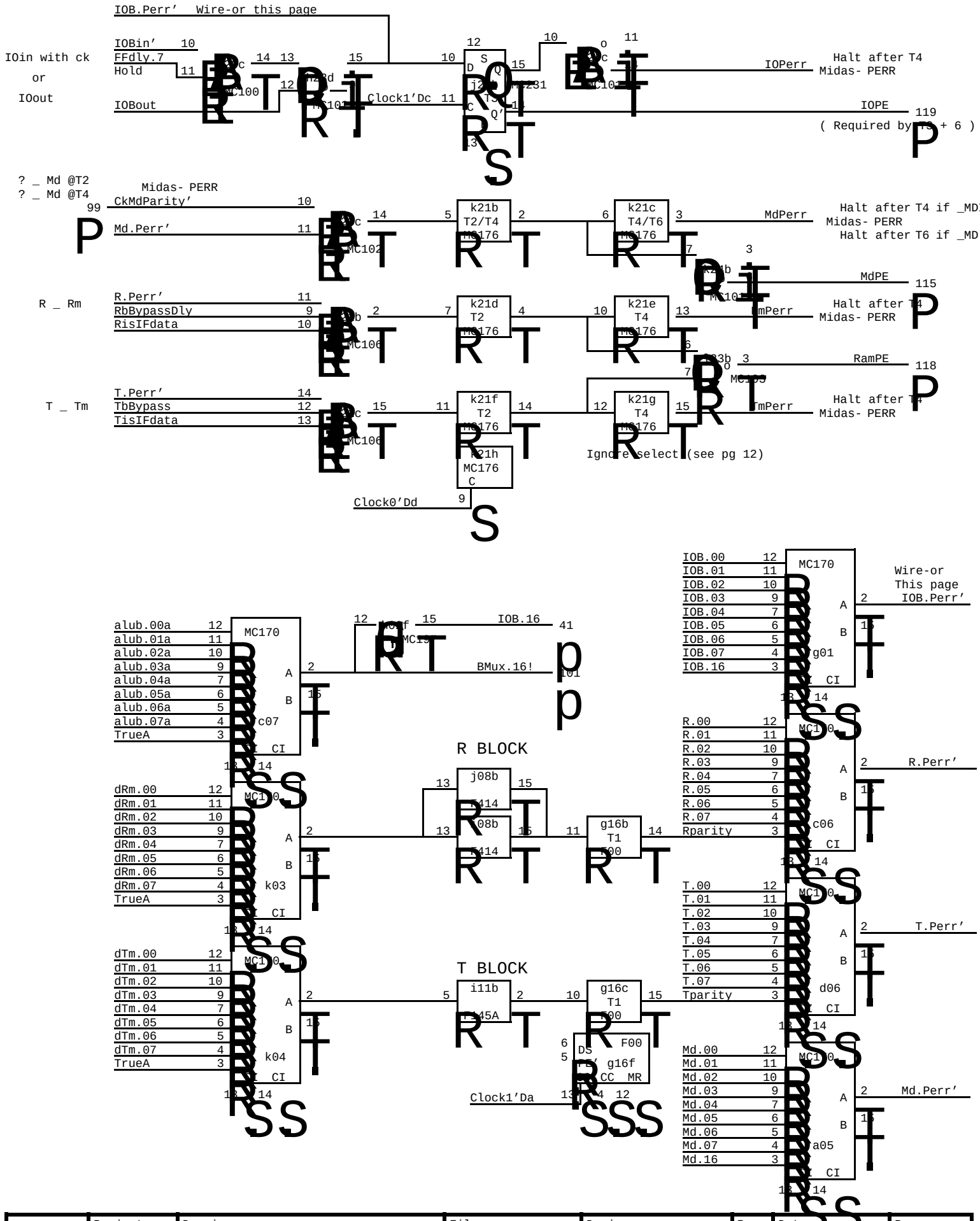
To enable this test circuit be sure there is a jumper
Connect TestTW (<109>) to ContA pin <140>

Task Simulator

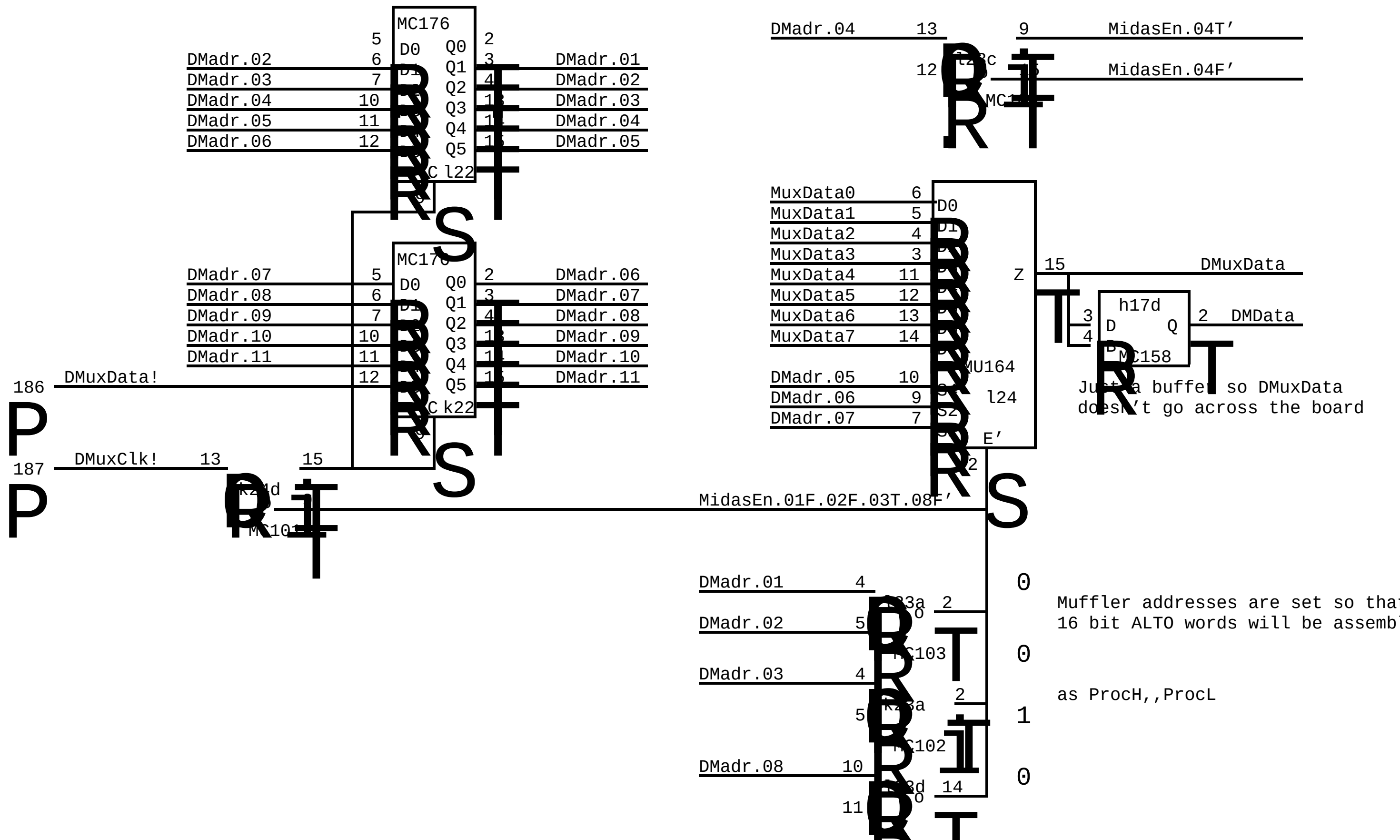
Temperature Sensing Ckt



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Hold Simulator and Temperature Sense	ProcH26.sil	R Bates	Ce	6/19/79	26

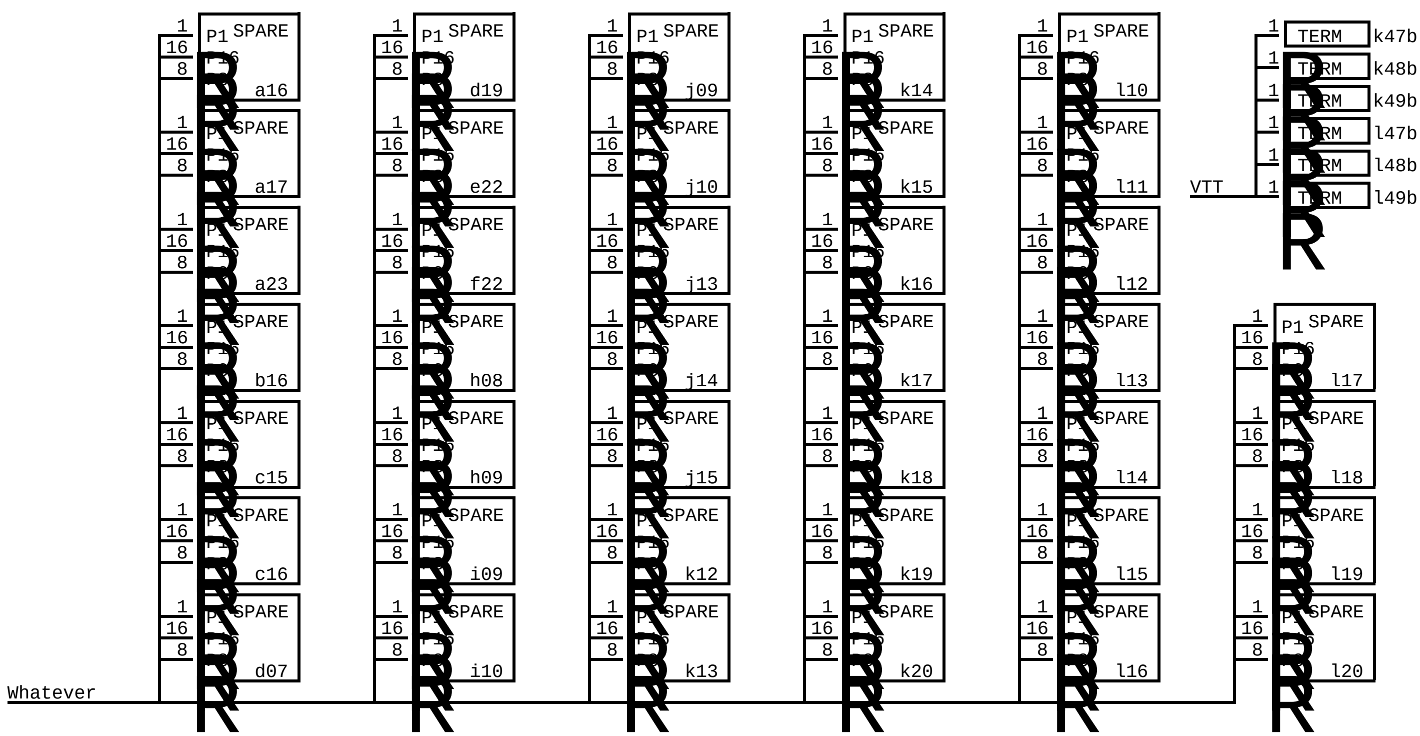


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Parity Logic	ProcH27.sil	R Bates	Ce	6/18/79	27



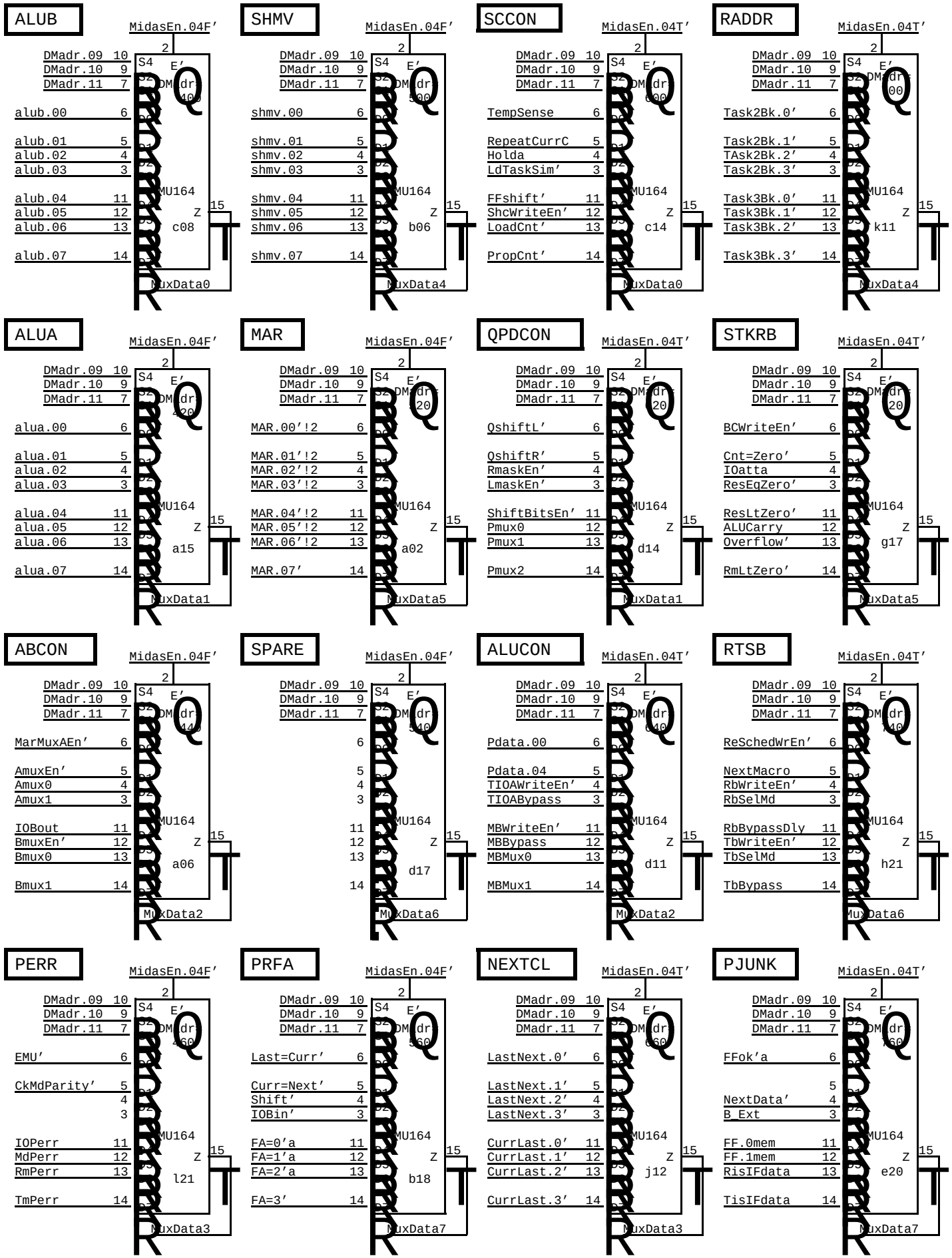
Midas Control

Spare Sockets for Multiwire

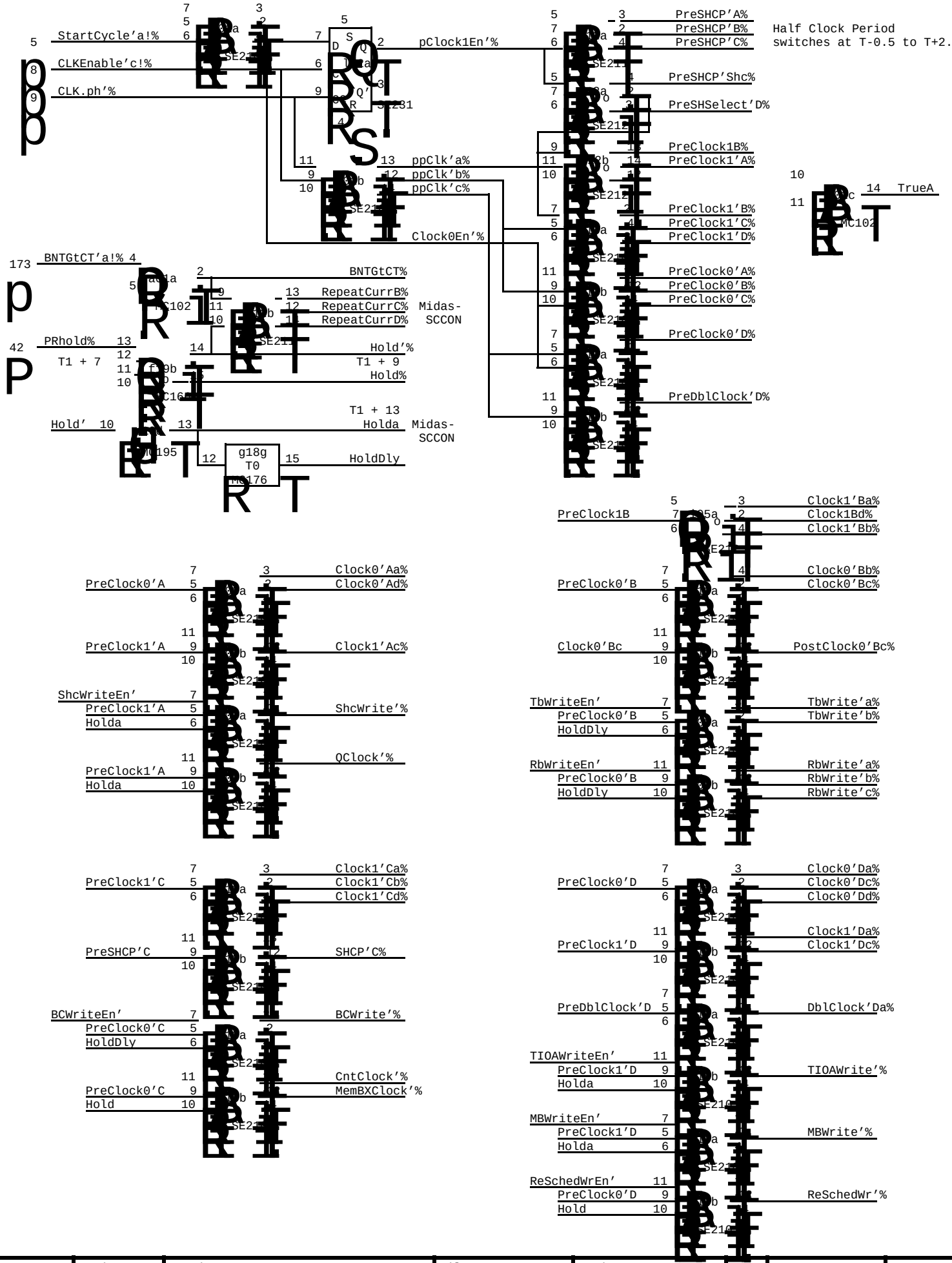


The following Platforms are entered so that route will cause multi-wire drill pattern
to include a number of unused locations just in case they need to be used in some way.

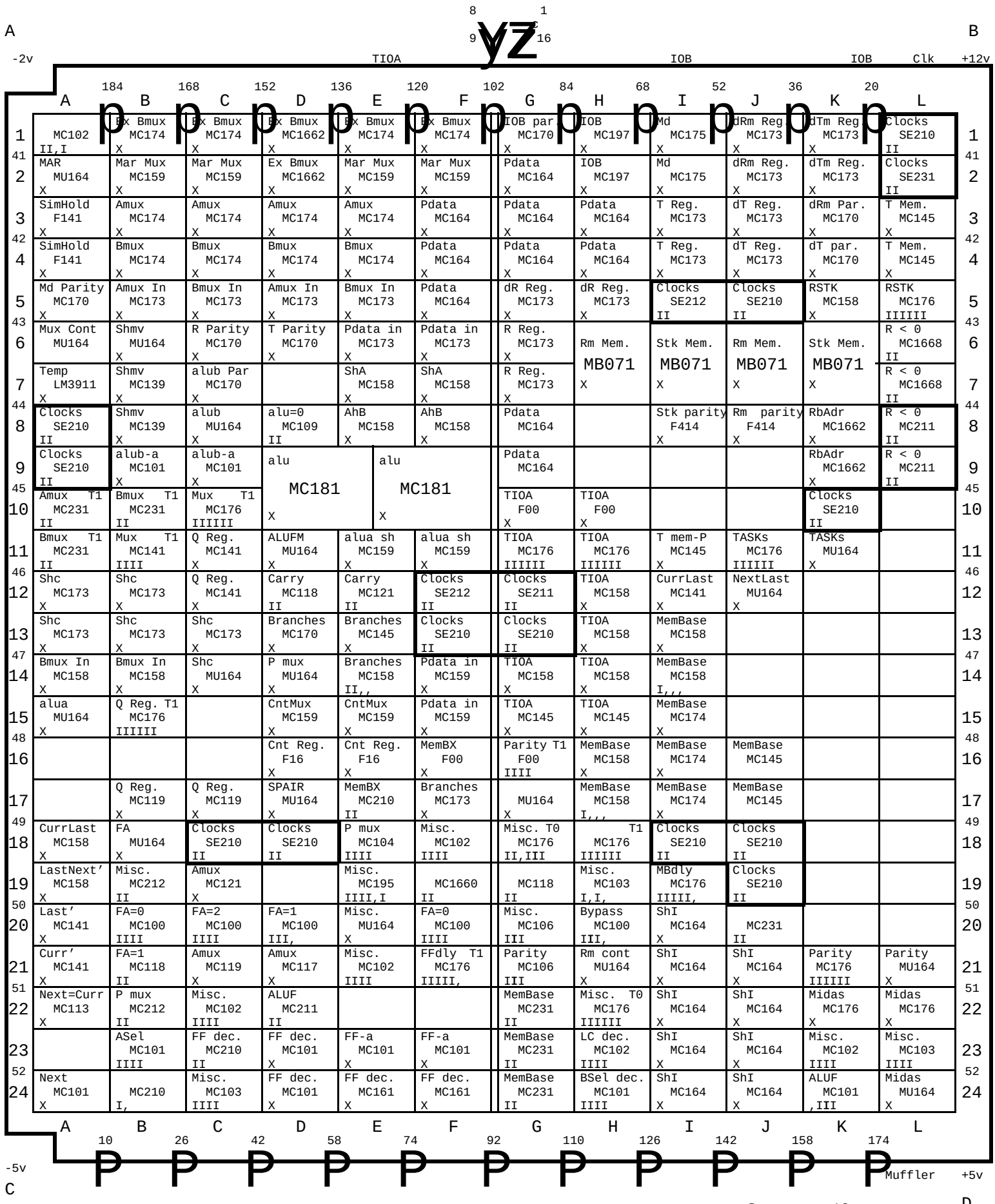
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Midas Control	ProcH28.sil	R Bates	Ce	6/18/79	28



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	DMUX MUFFLERS	ProcH29.sil	R Bates	Ce	6/18/79	29



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CLOCK DRIVERS	ProcH30.sil	R Bates	Ce	6/18/79	30



XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Board Layout	ProcH31.sil	R. Bates	Ce	6/18/79	31

Use Dorado Proms to define the following Proms:

Board Name	Prom Name	location
PorcH	Lmask (High byte)	b07
	Rmask (High byte)	b08