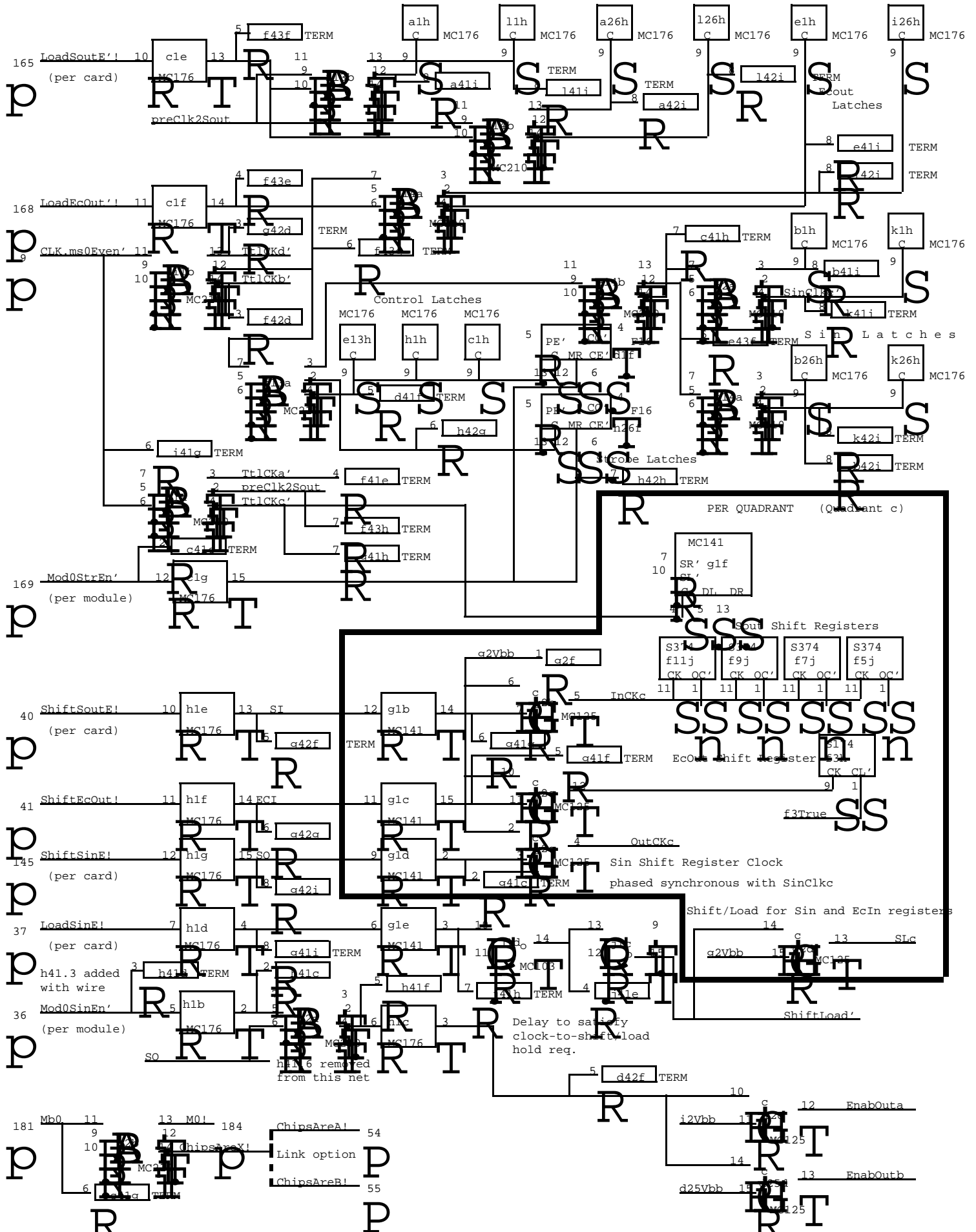


Dorado Printed Circuit Memory Storage Array

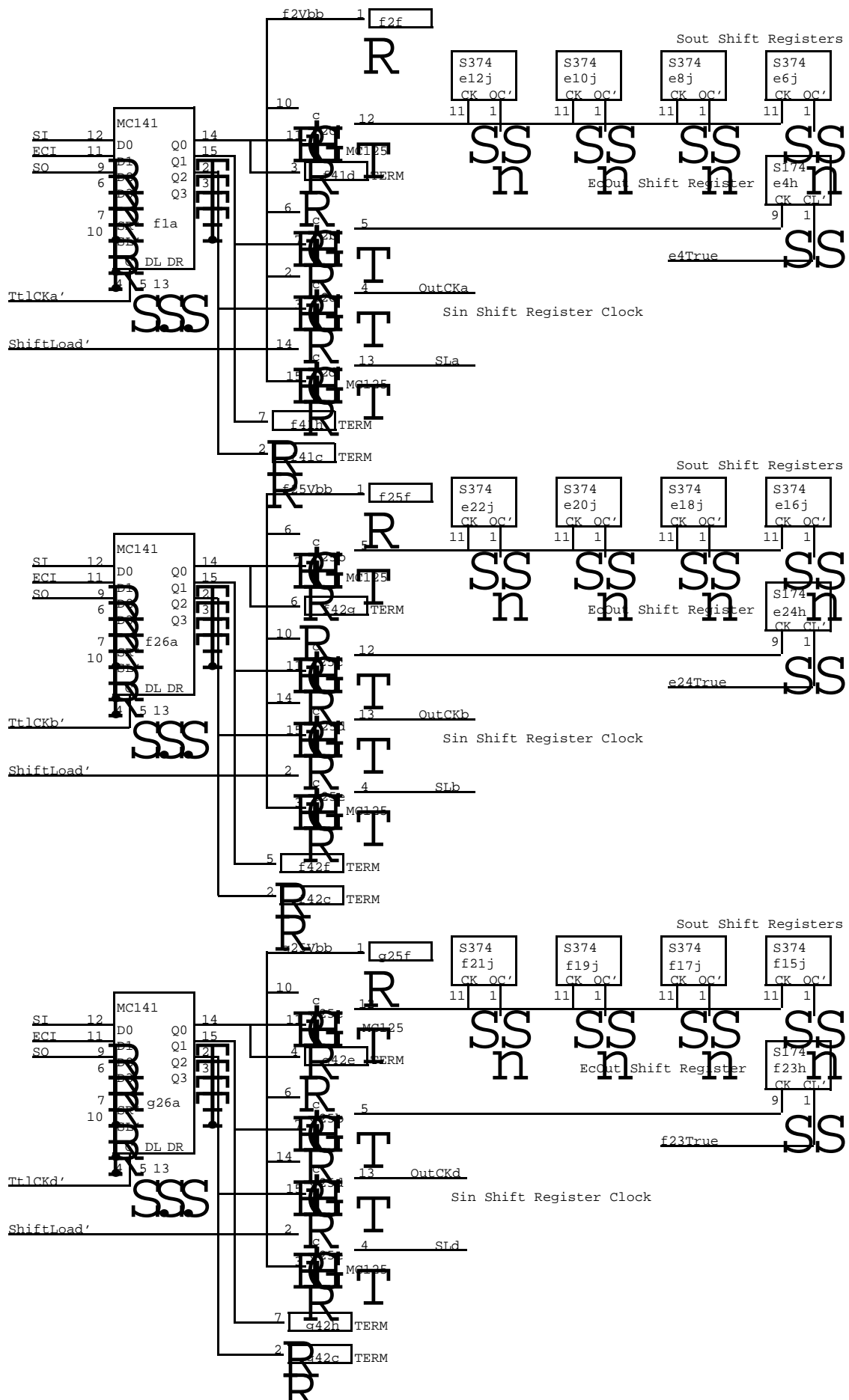
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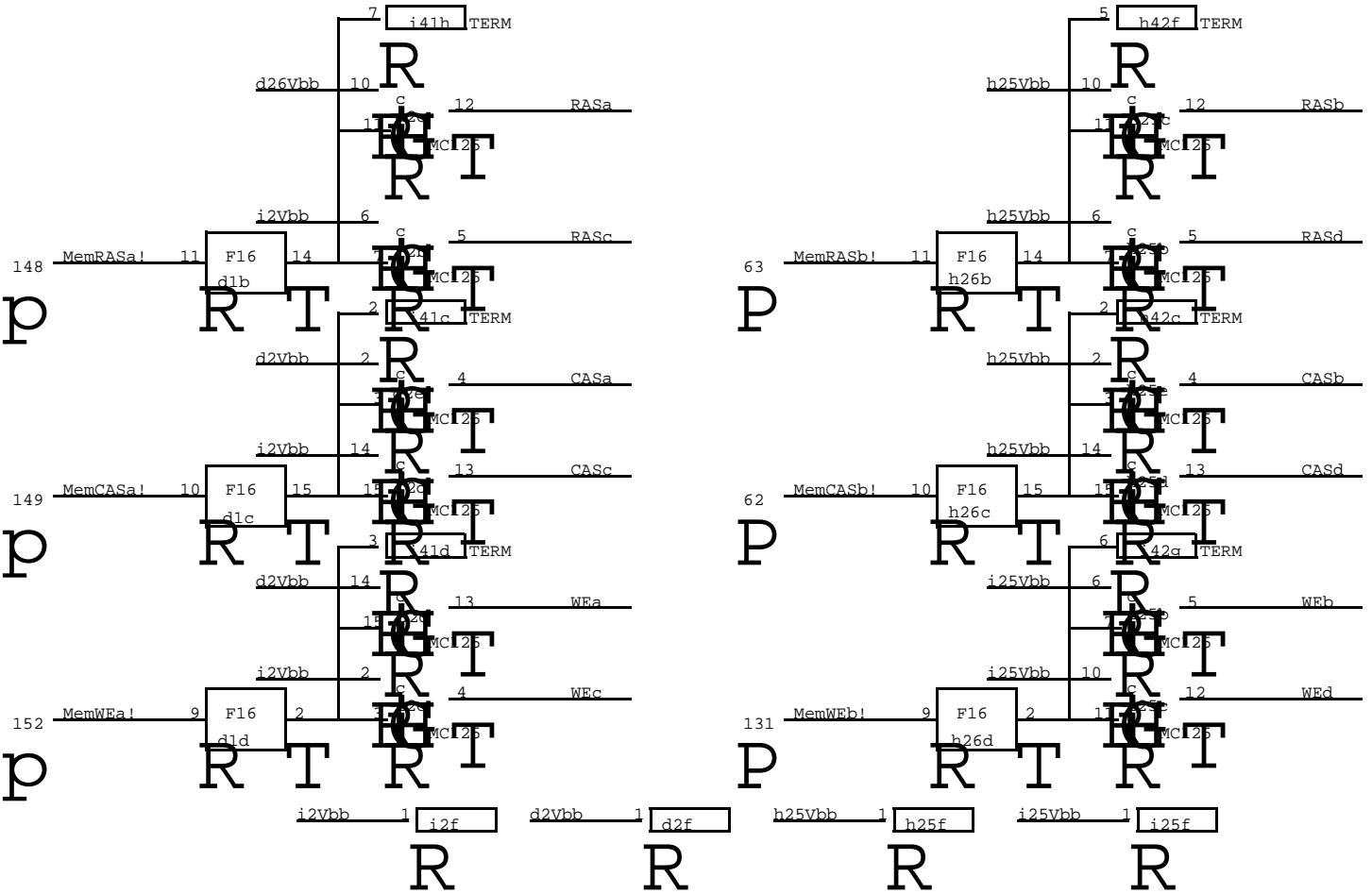
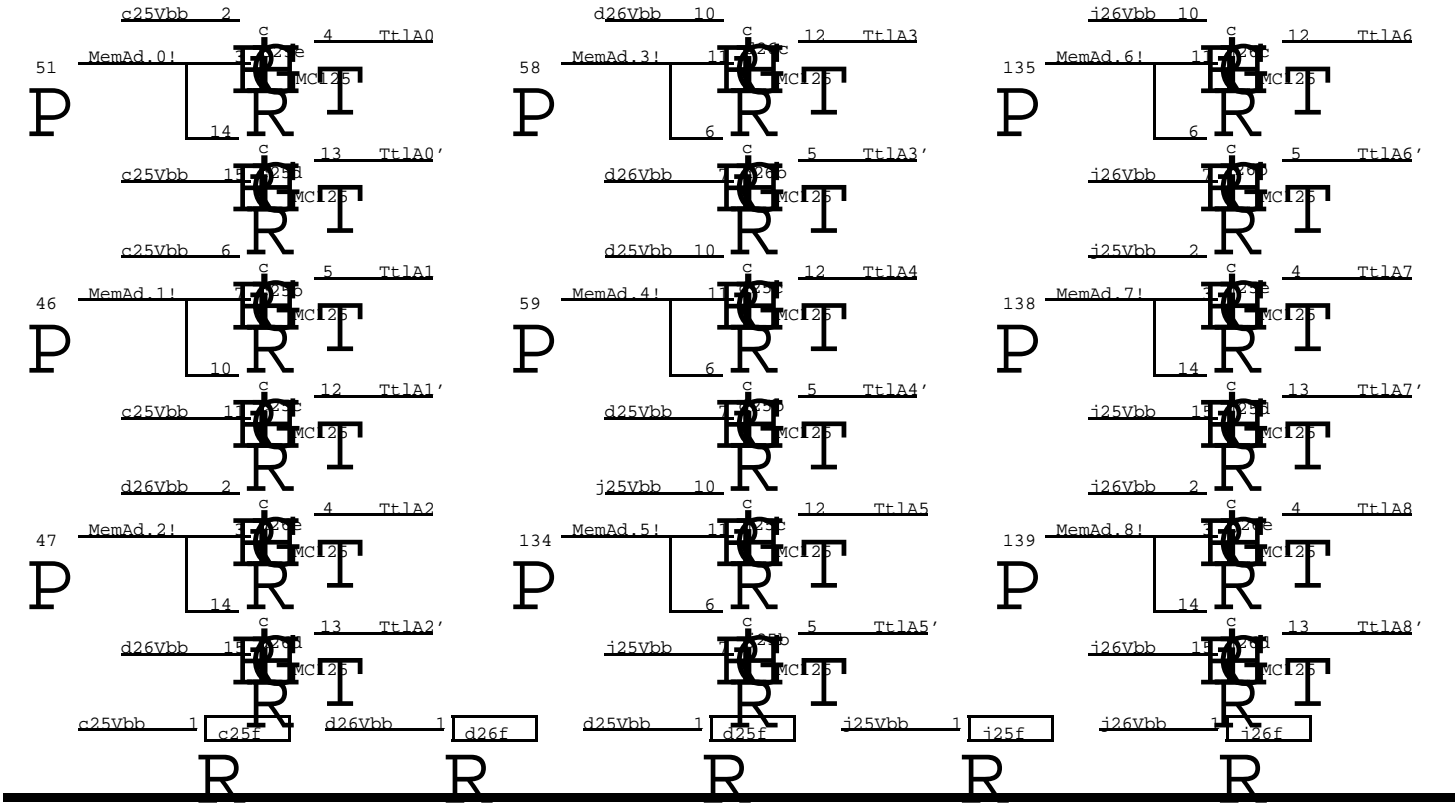
Control_____ 1
TTL Quadrant Clocking_____ 2
Address and Strobe Receivers_____ 3
Data Bit Paths_____ 4-11
Error Correction Bit Paths_____ 12
Address Paths_____ 13-28

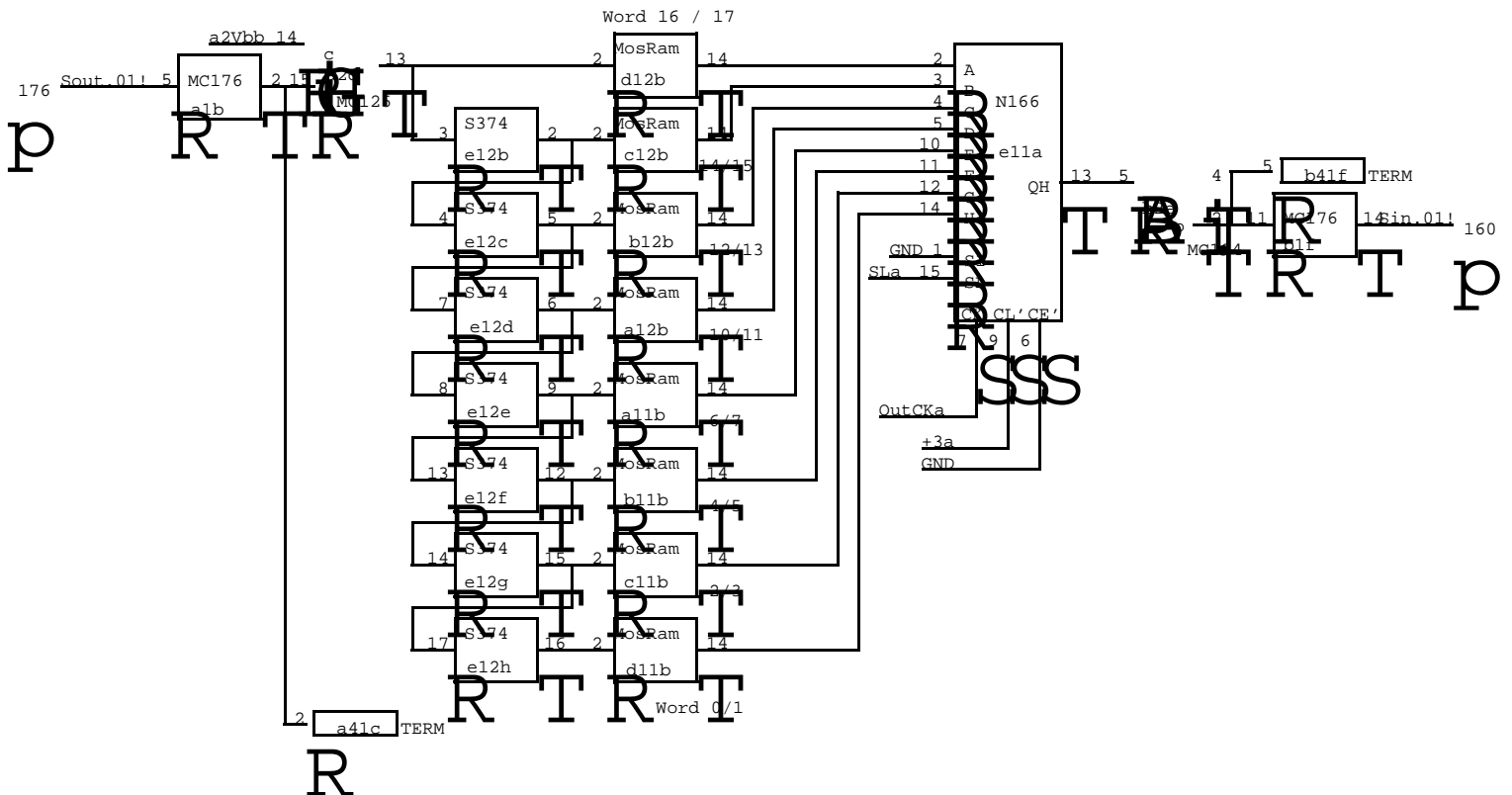
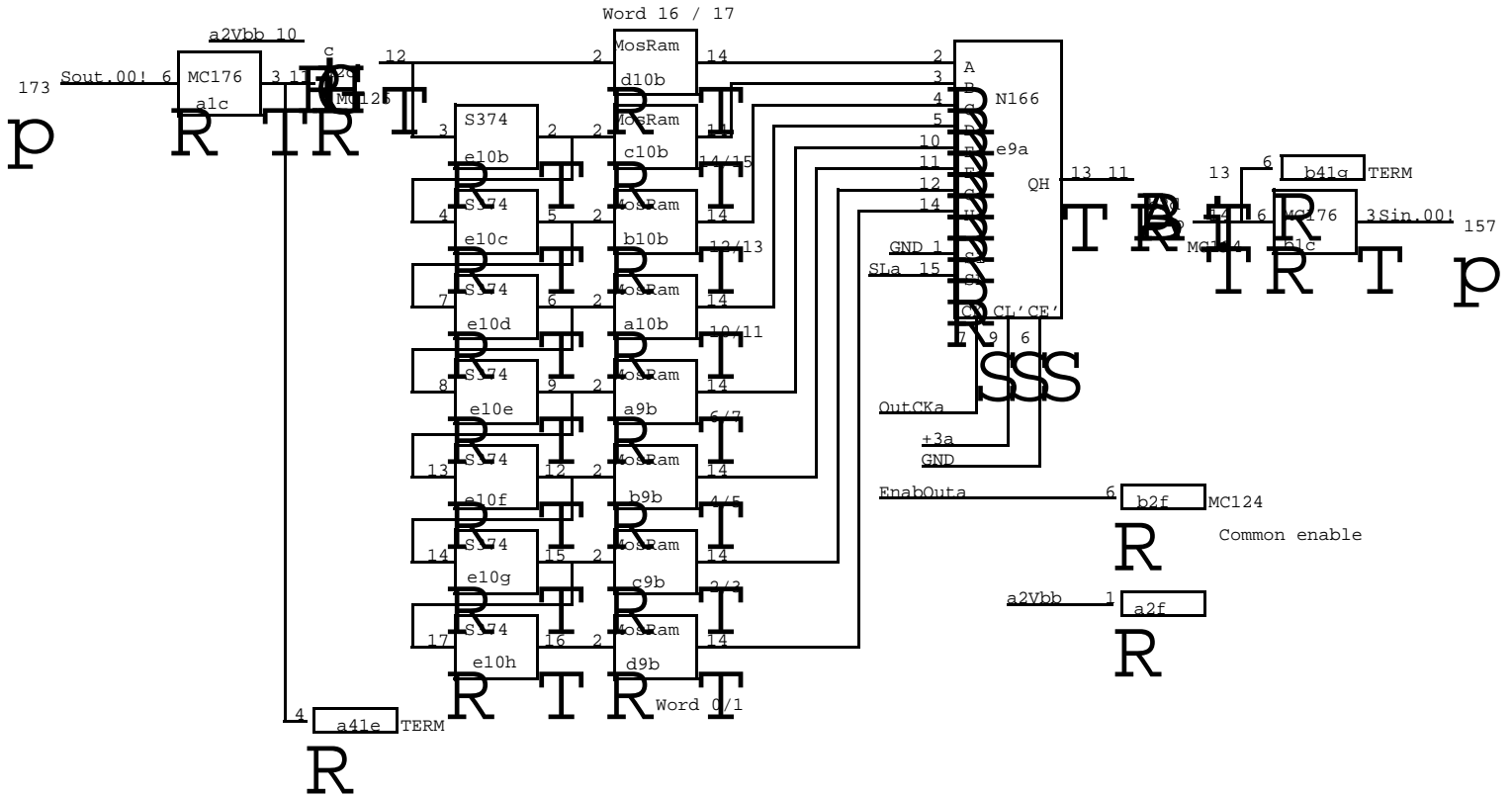
Sout Latches

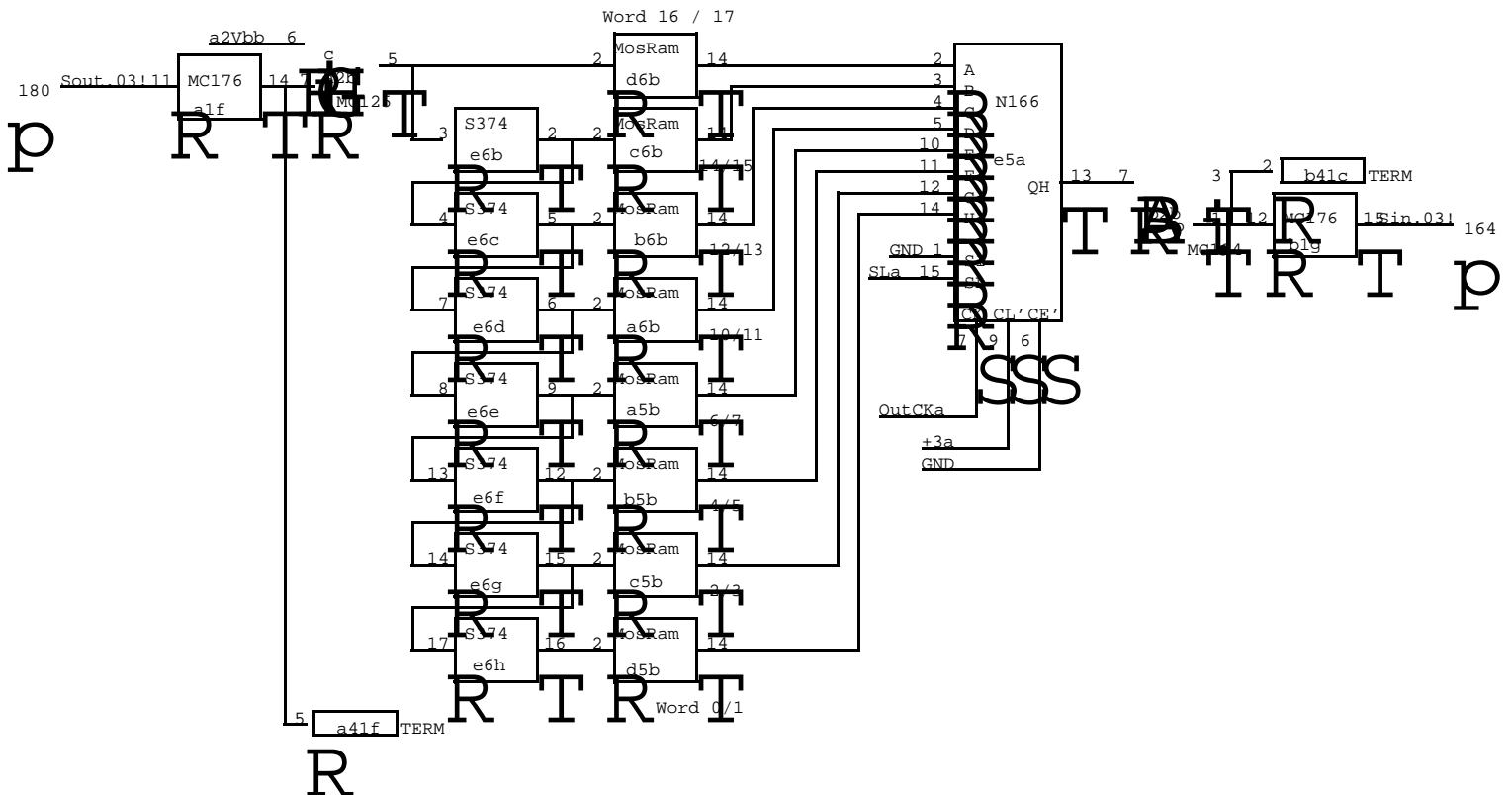
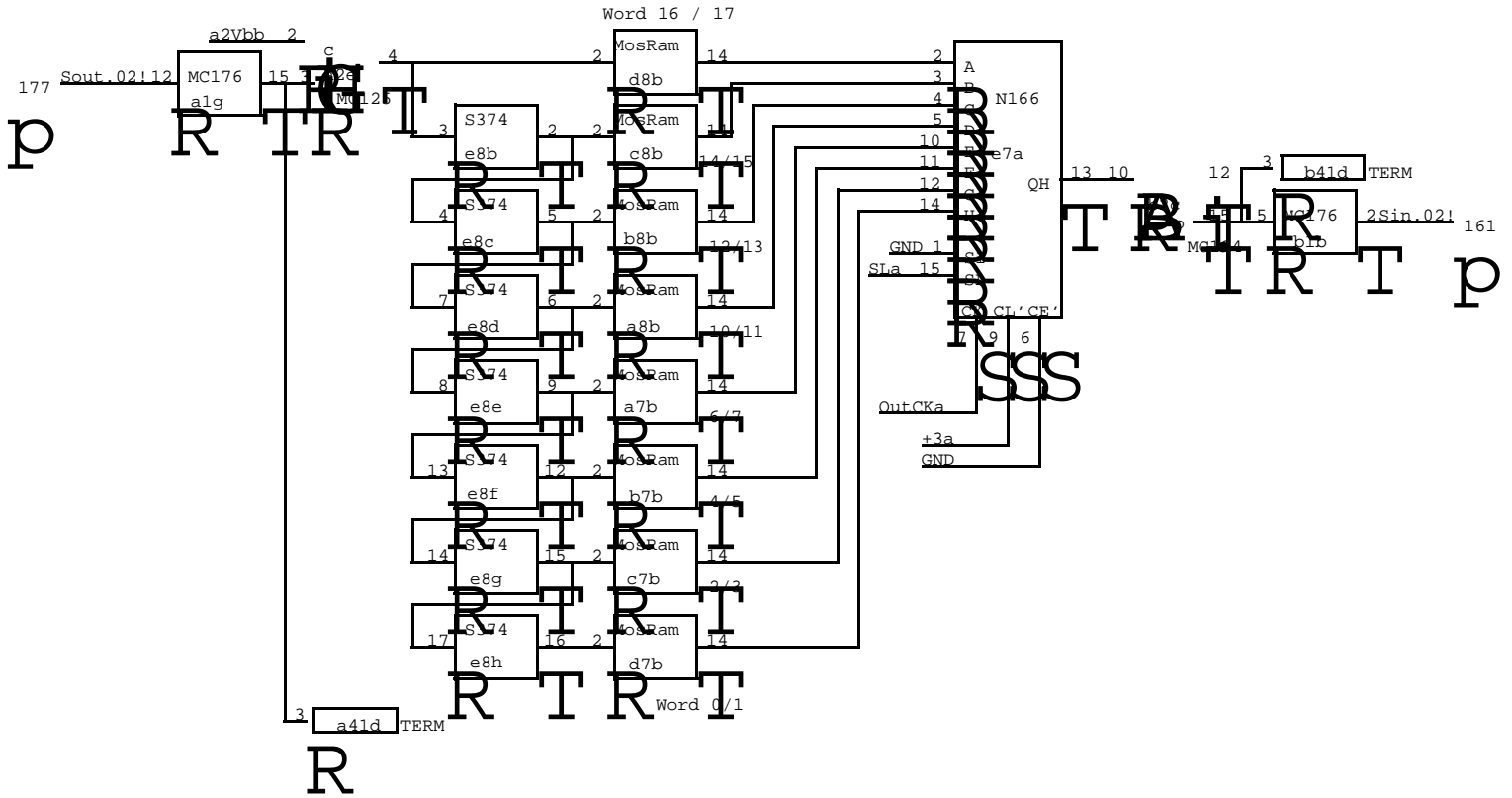


XEROX PARC	Project Dorado	Memory Storage Array Control	File pcmsa01.sil	Designer McCreight	Rev Pa	Date 8/10/84	Page 01
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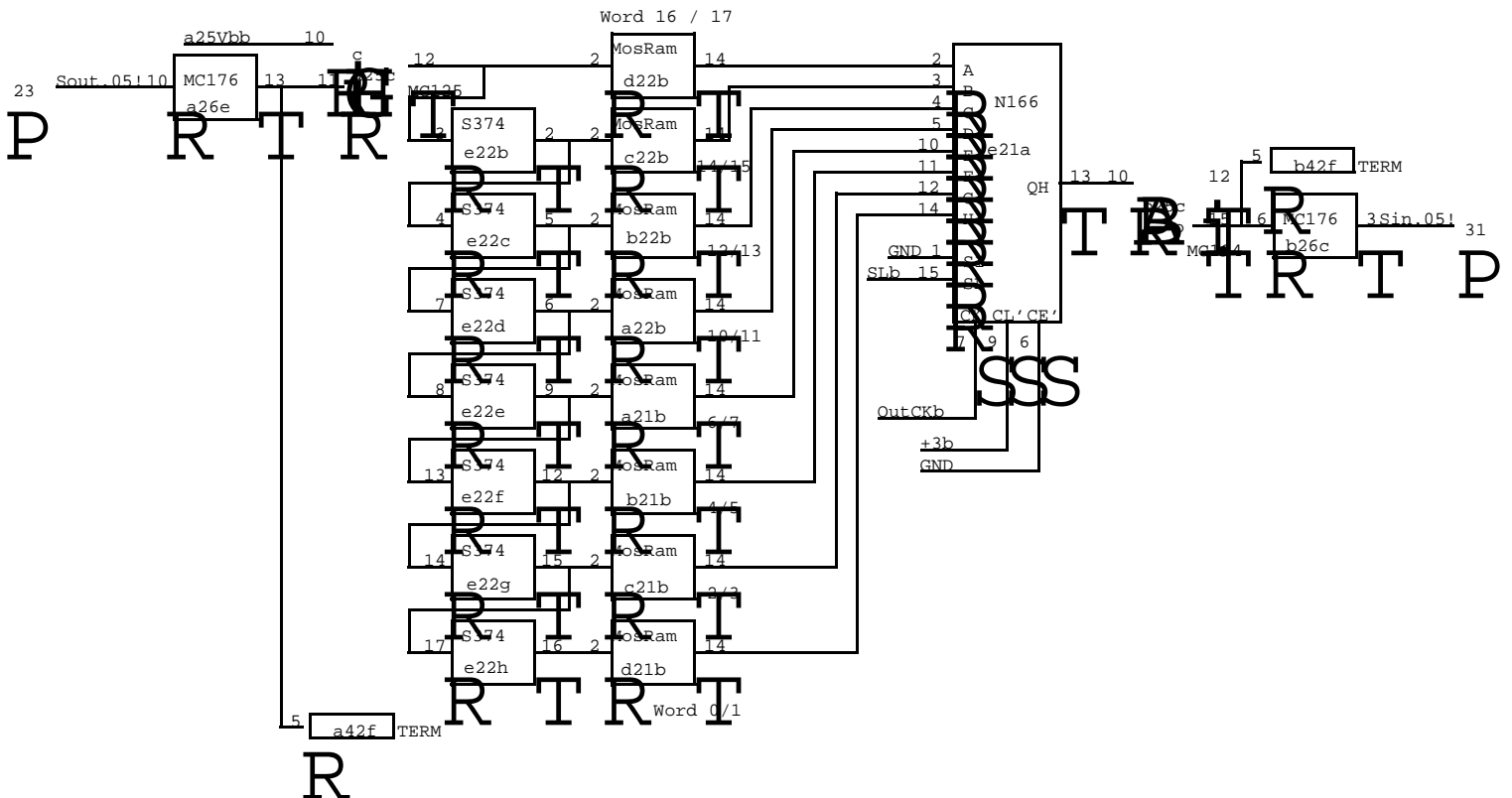
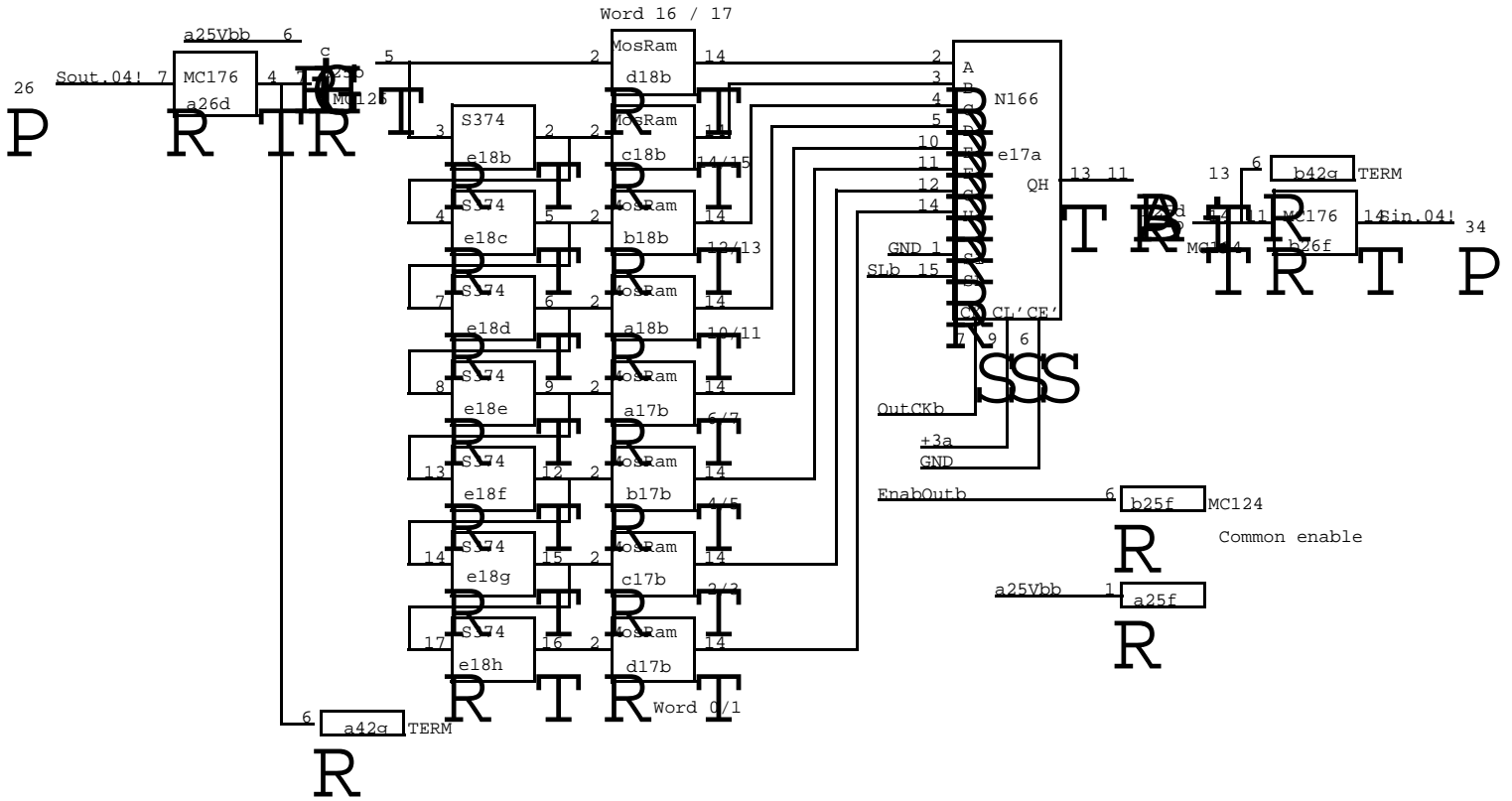


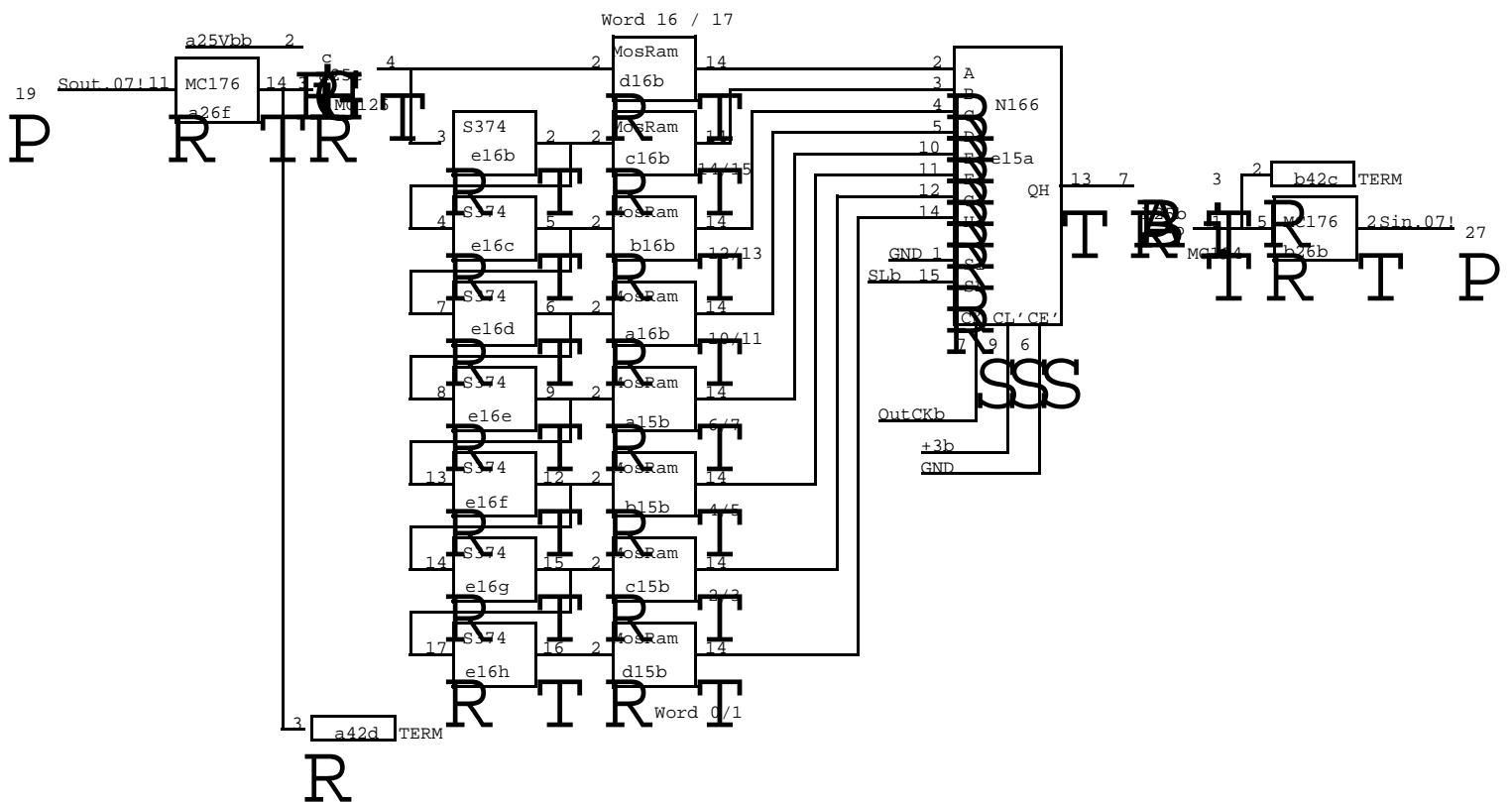
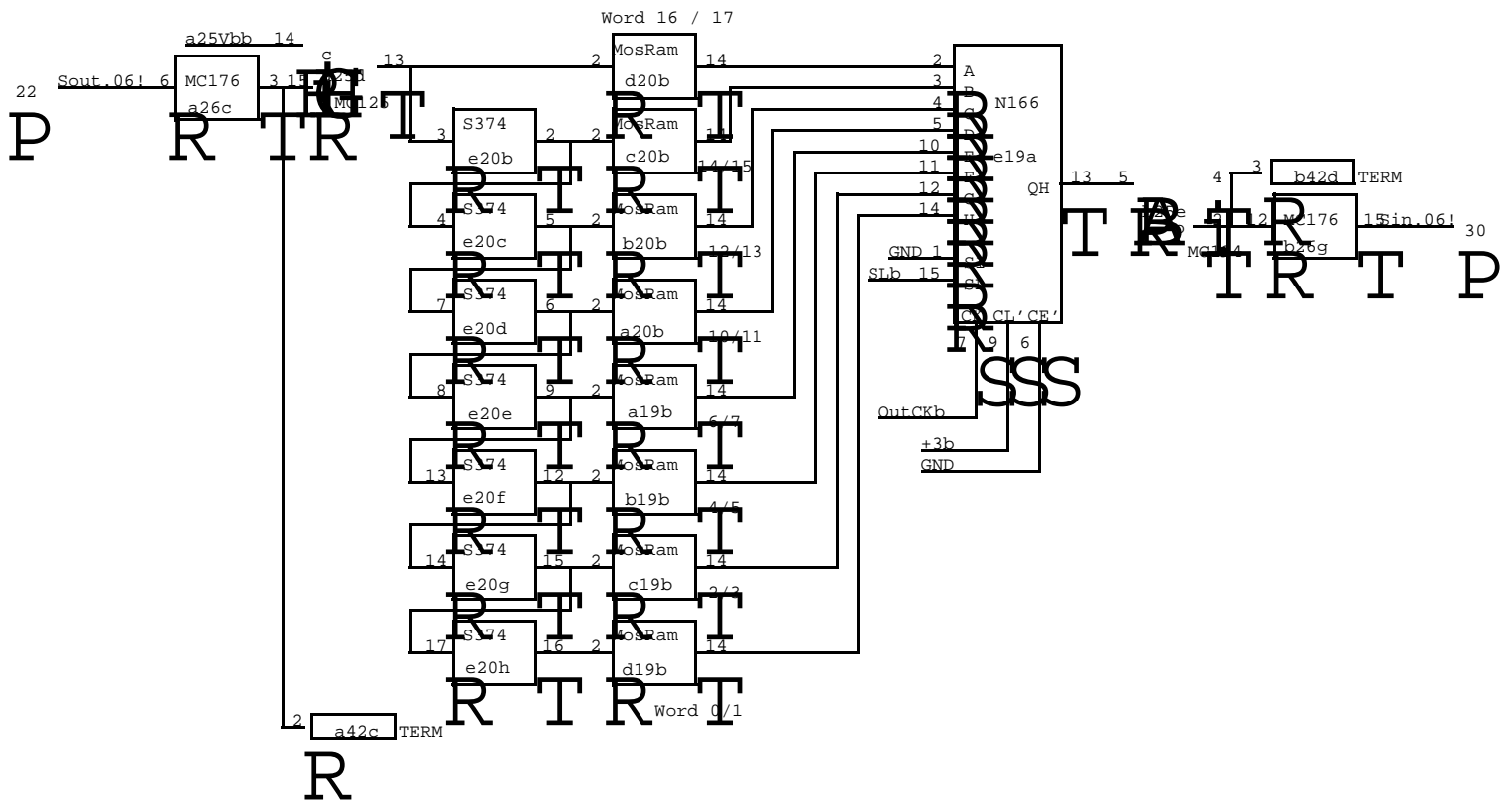




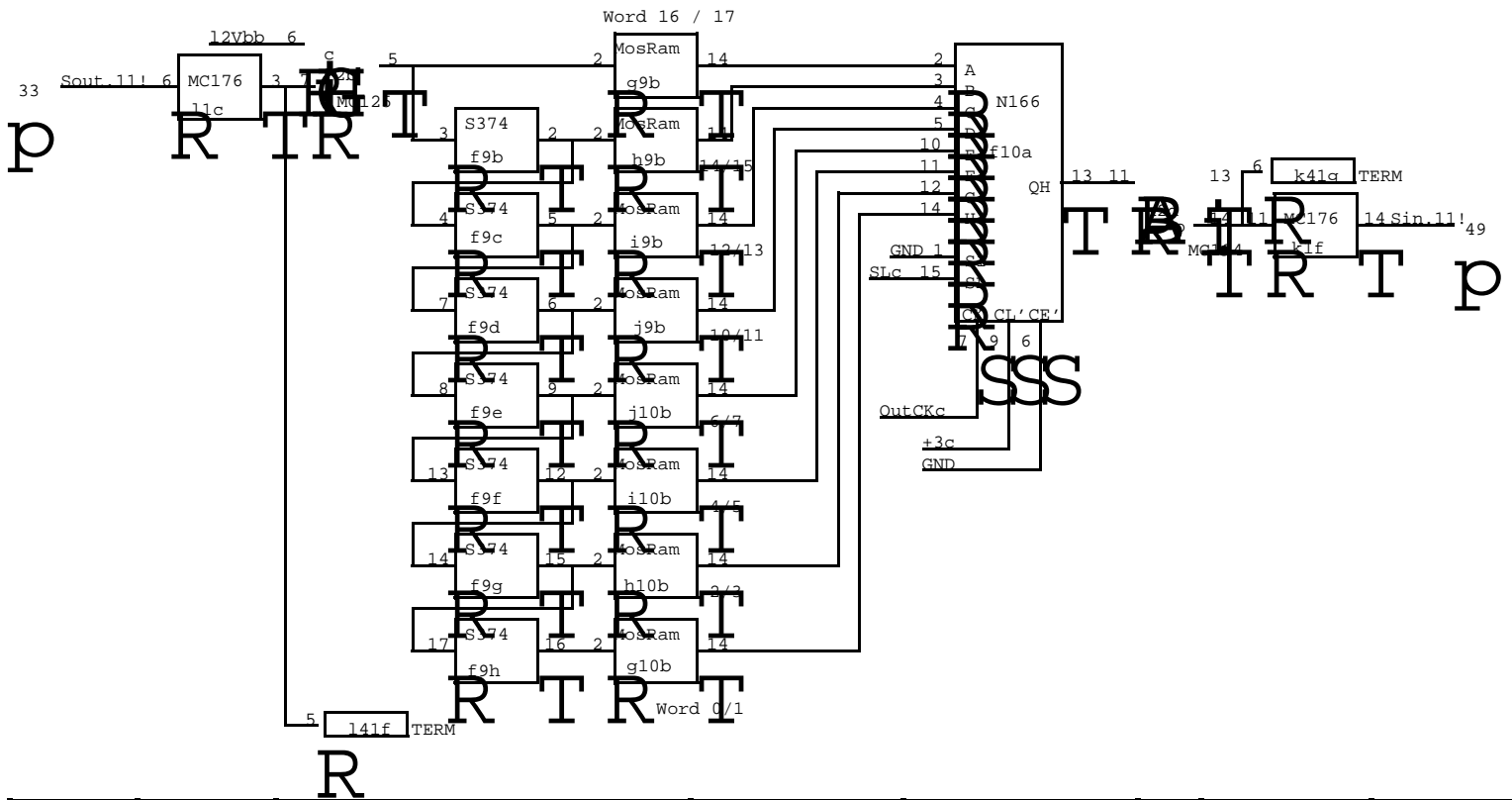
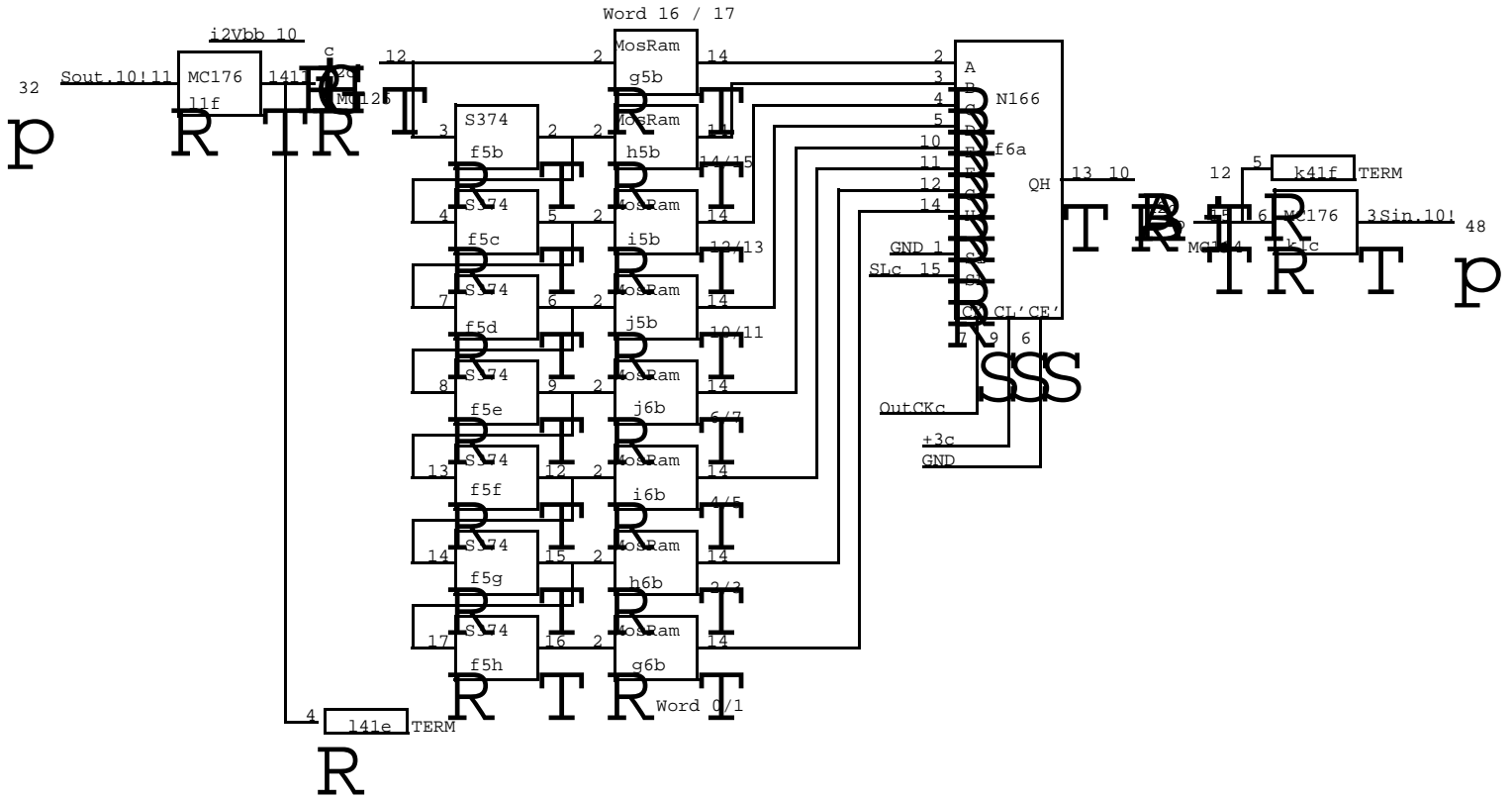


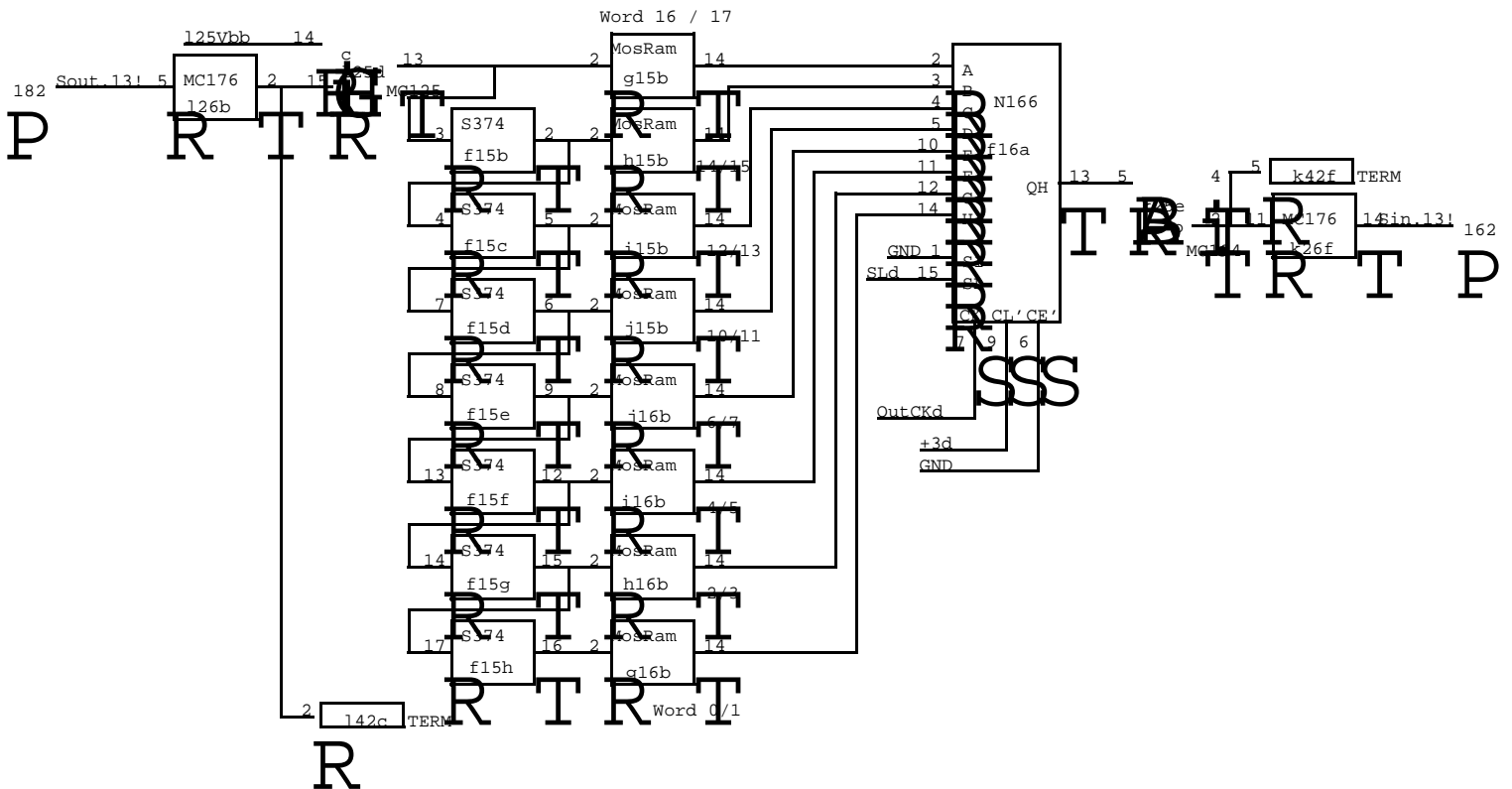
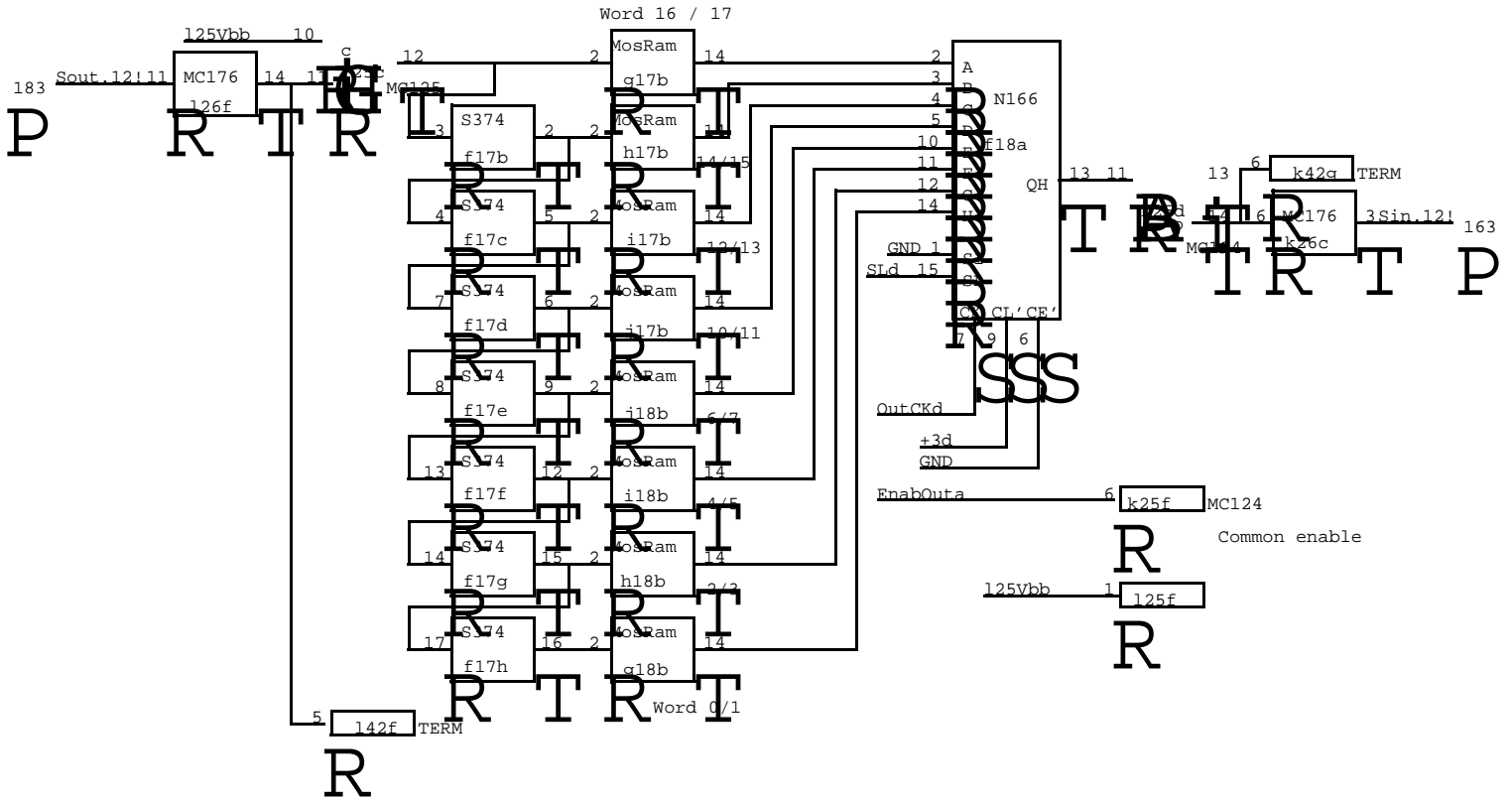
Project	File	Designer	Rev	Date	Page
XEROX PARC	pcmsa05.sil	McCreight	Pa	10/30/79	05

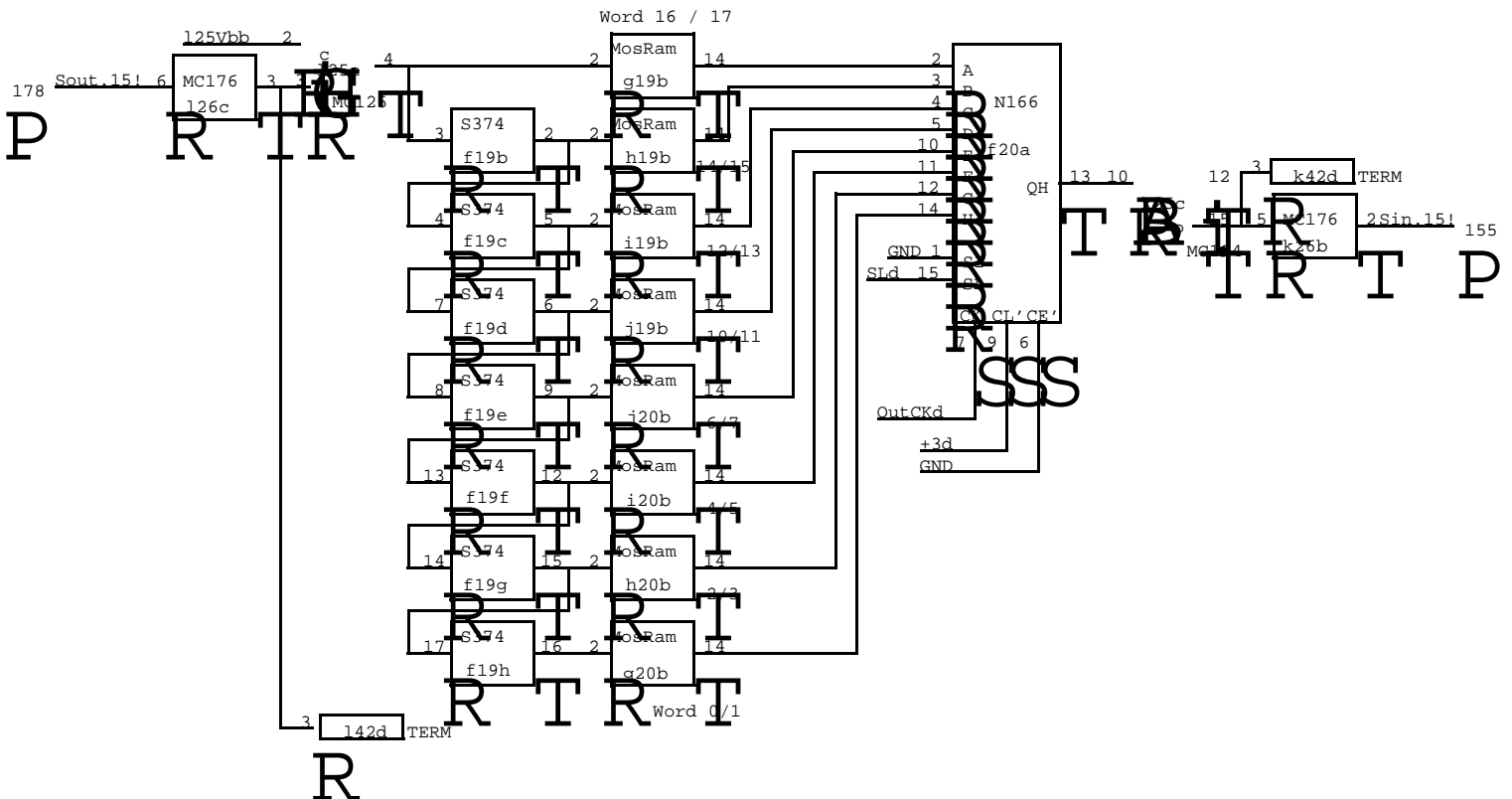
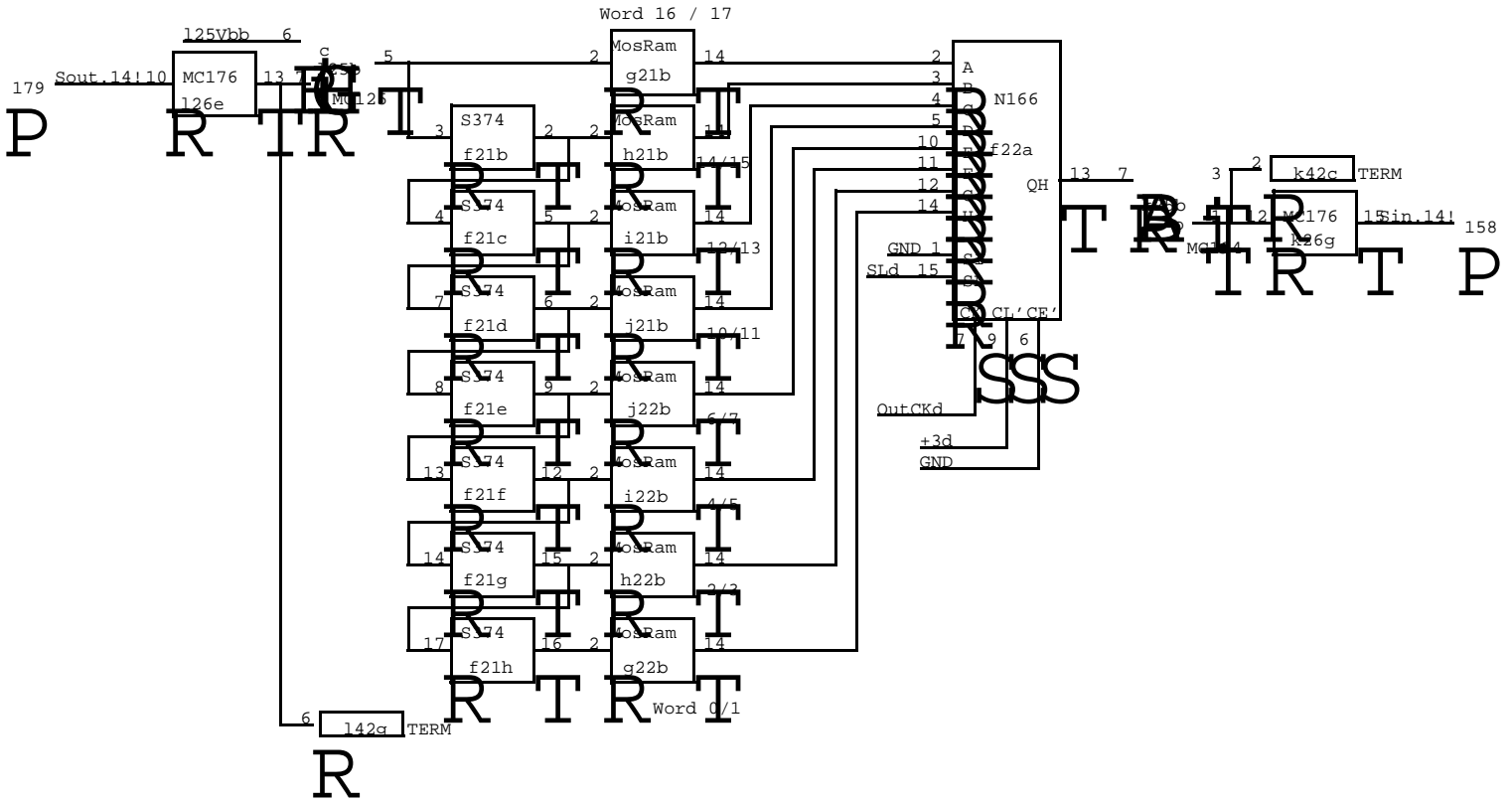


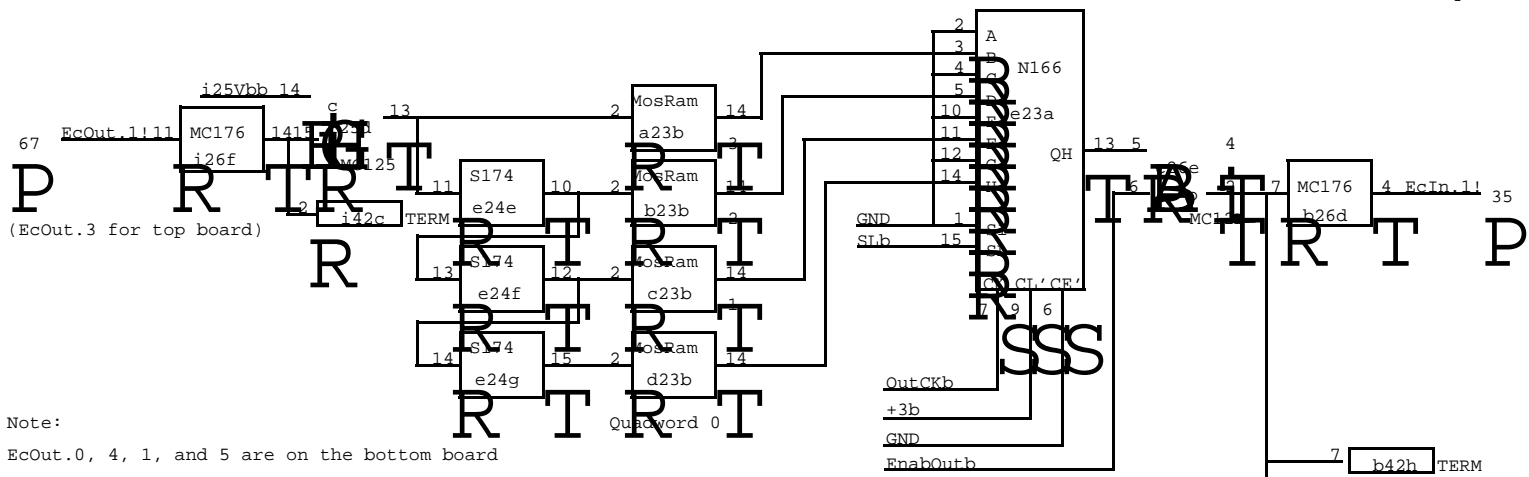
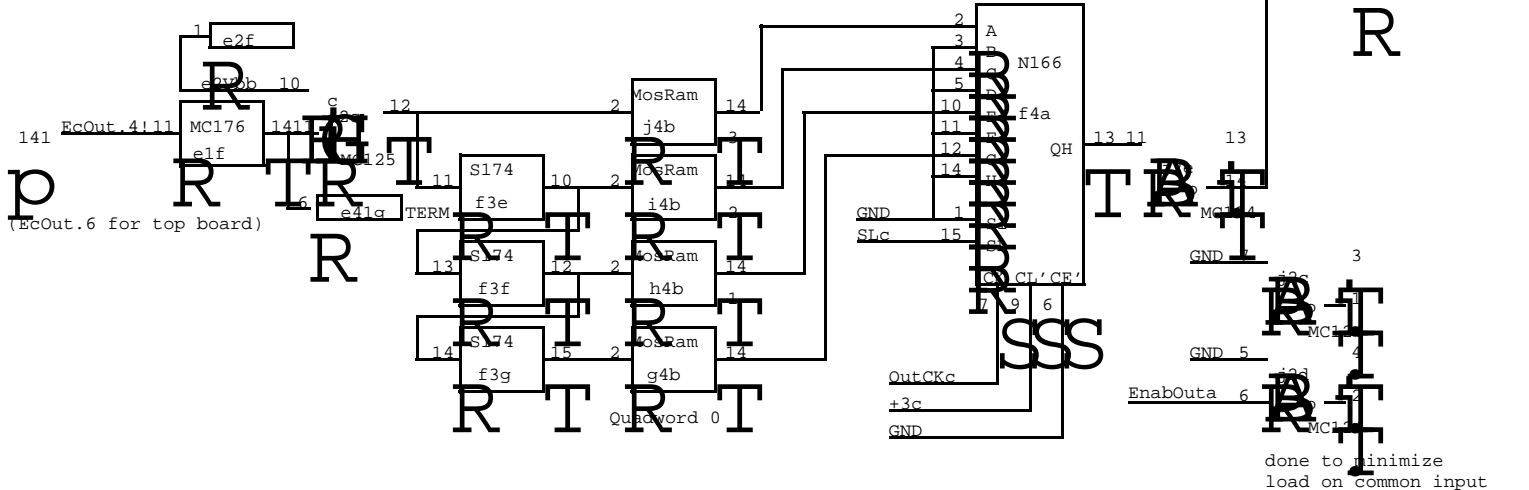
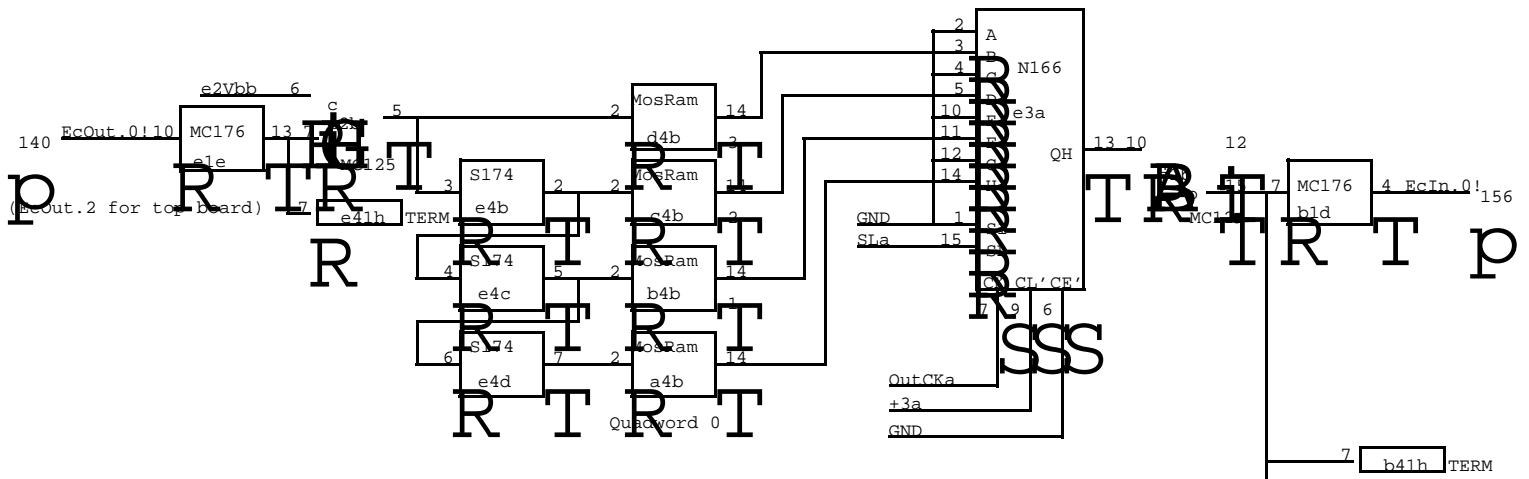


XEROX PARC	Project Dorado	Memory Storage Array Quadrant b / Bits 06:07	File pcmsa07.sil	Designer McCreight	Rev Pa	Date 10/30/79	Page 07
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Note:
 EcOut.0, 4, 1, and 5 are on the bottom board
 EcOut.2, 6, 3, and 7 are on the top board

