D O R A D O S C H E M A T I C S

M e m X

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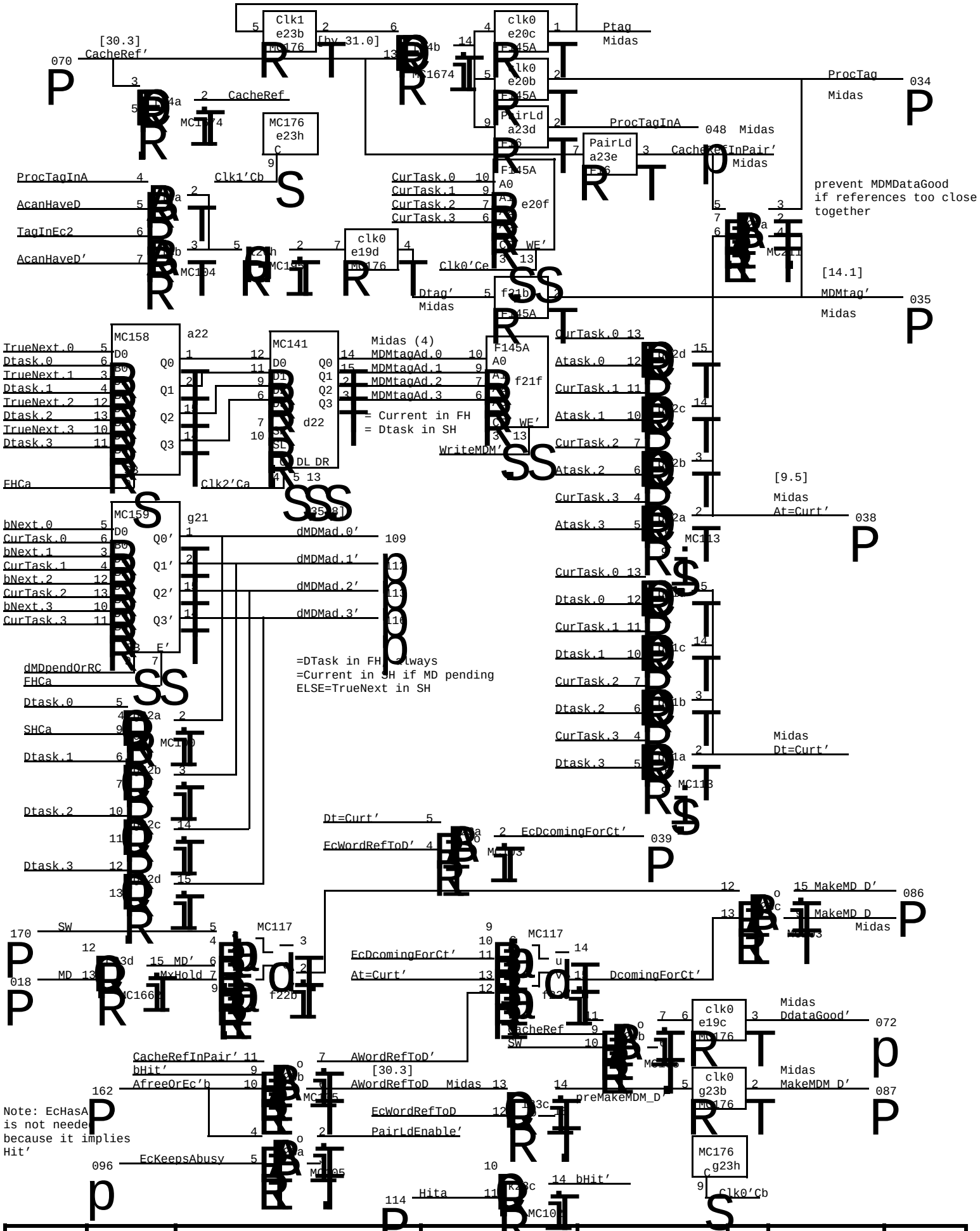
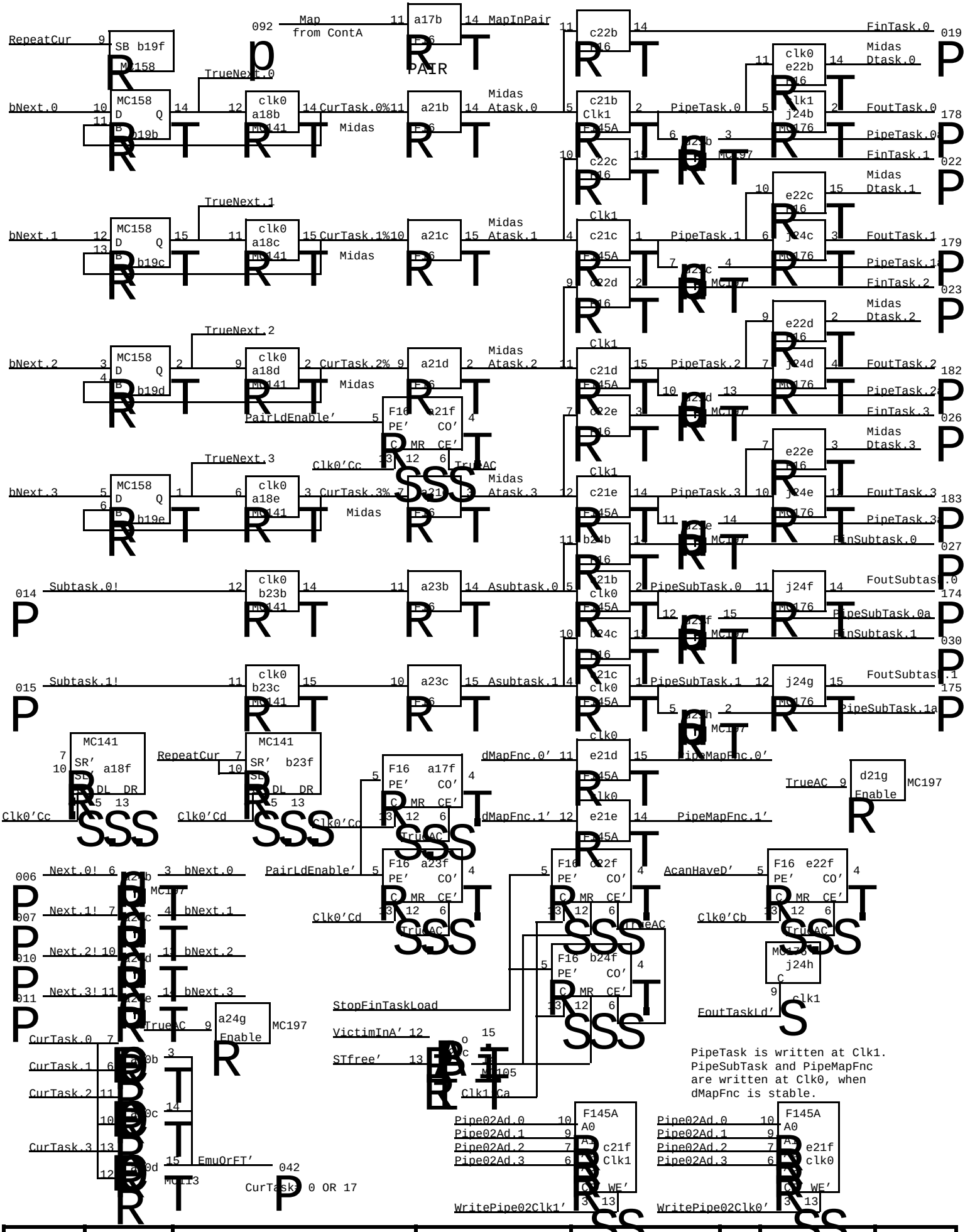
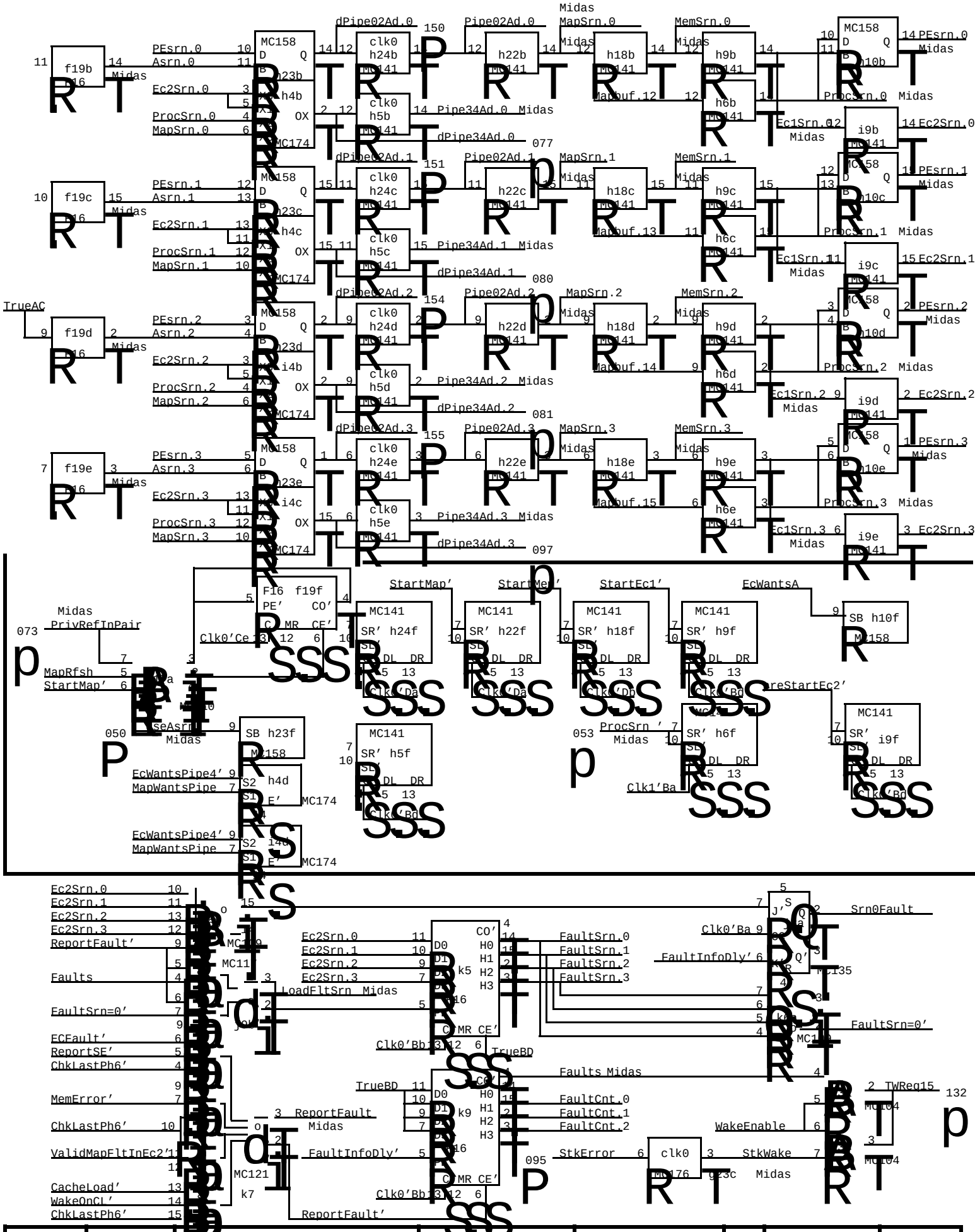


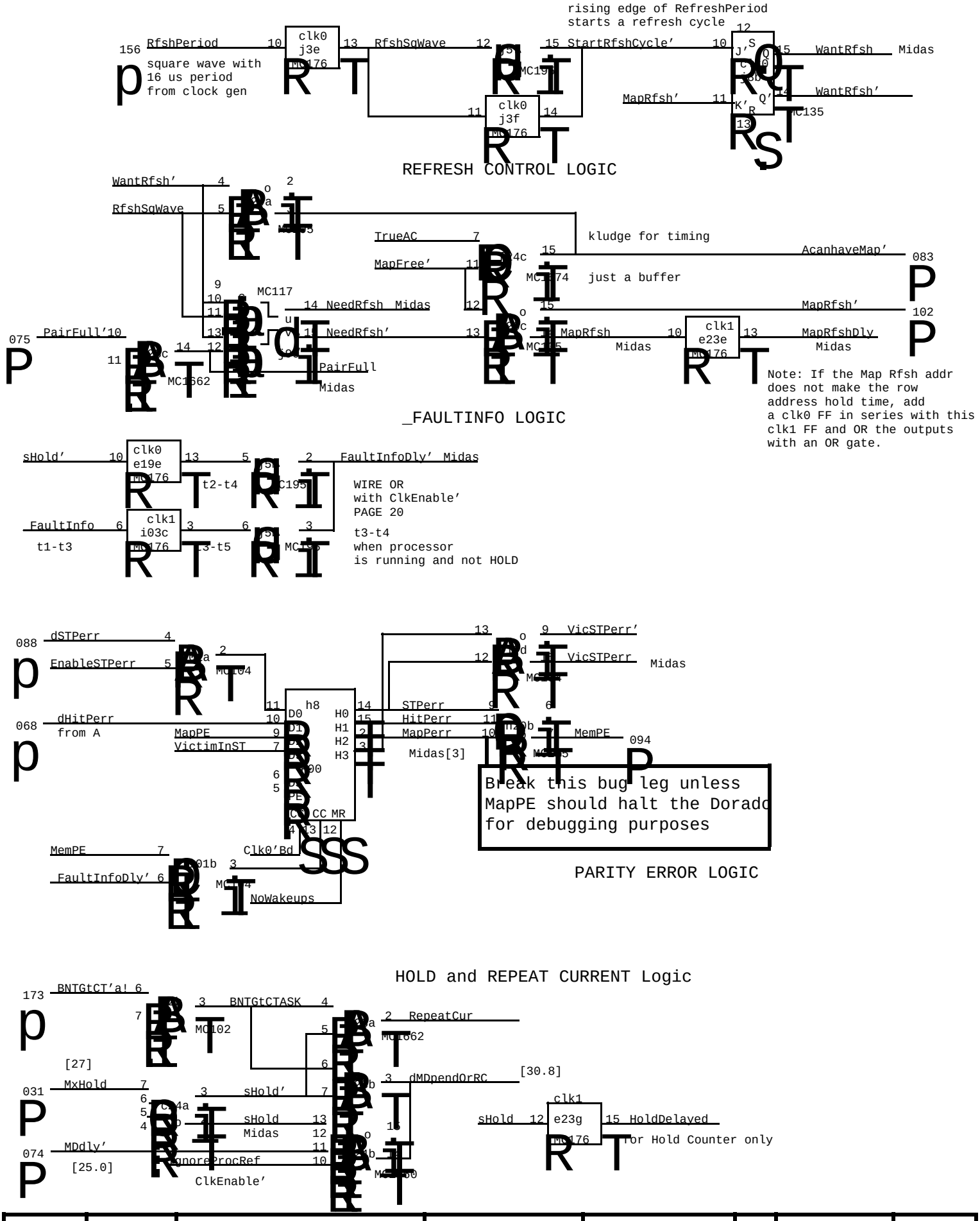
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Tags, Tasks, MD Control	MemX01.sil	K. Pier	Da	7/02/79	01



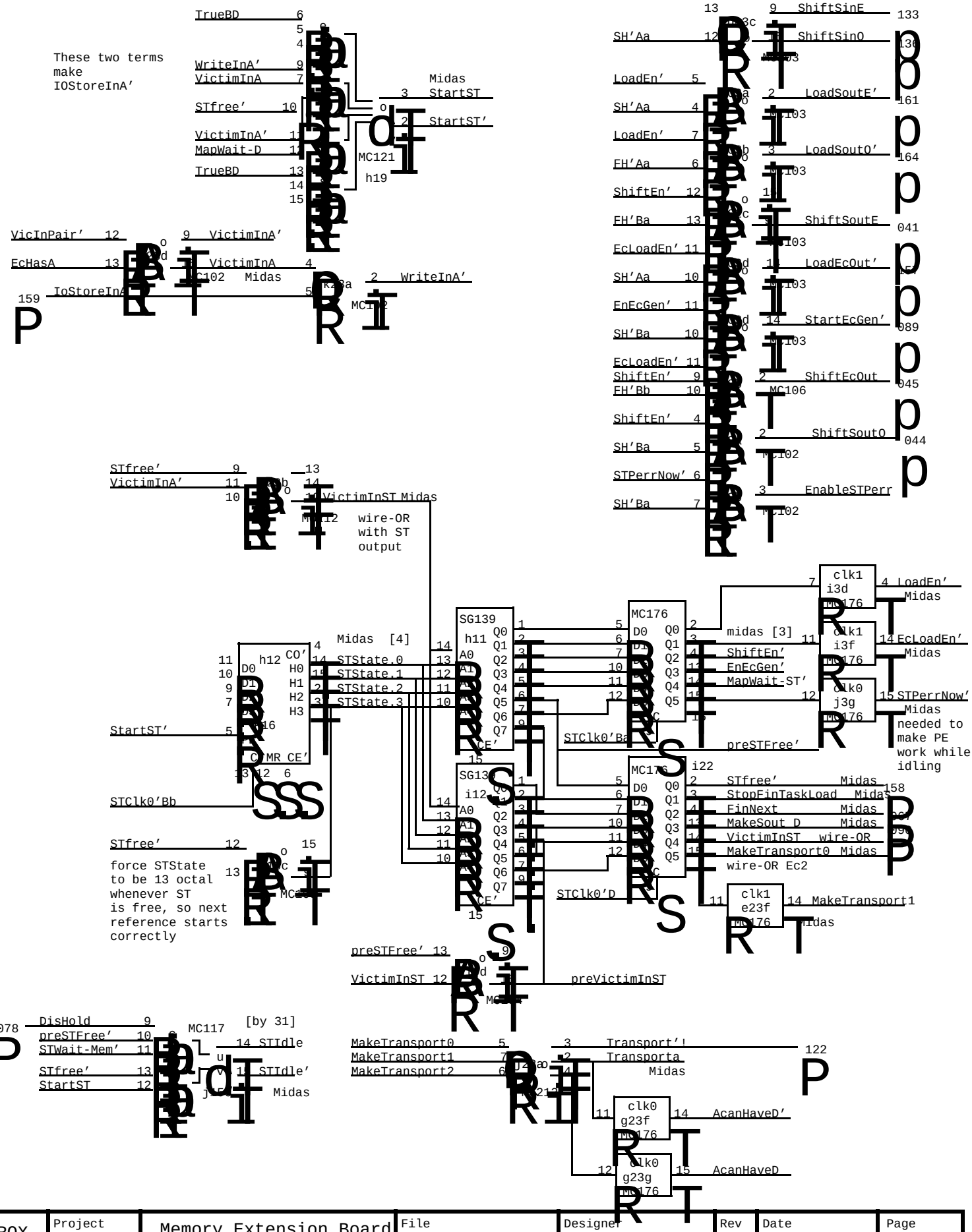
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Next, *Task, Pipe 2	MemX02.sil	K. Pier	Da	6/23/79	02



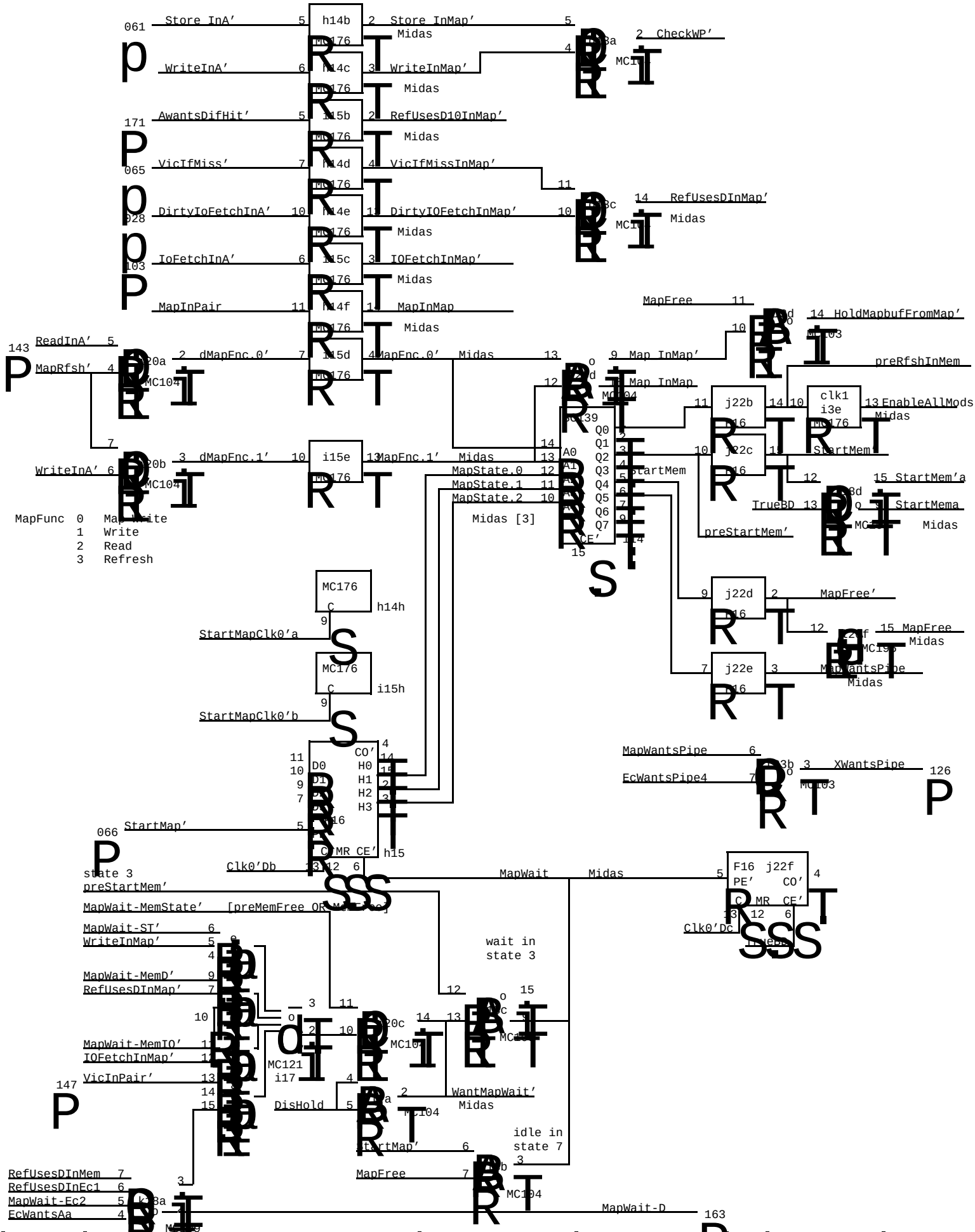
XEROX PARC	Project	Memory Extension Board	File	Designer	Rev	Date	Page
	Dorado	SRNs and Fault Info	MemX03.sil	K. Pier	Da	9/08/79	03



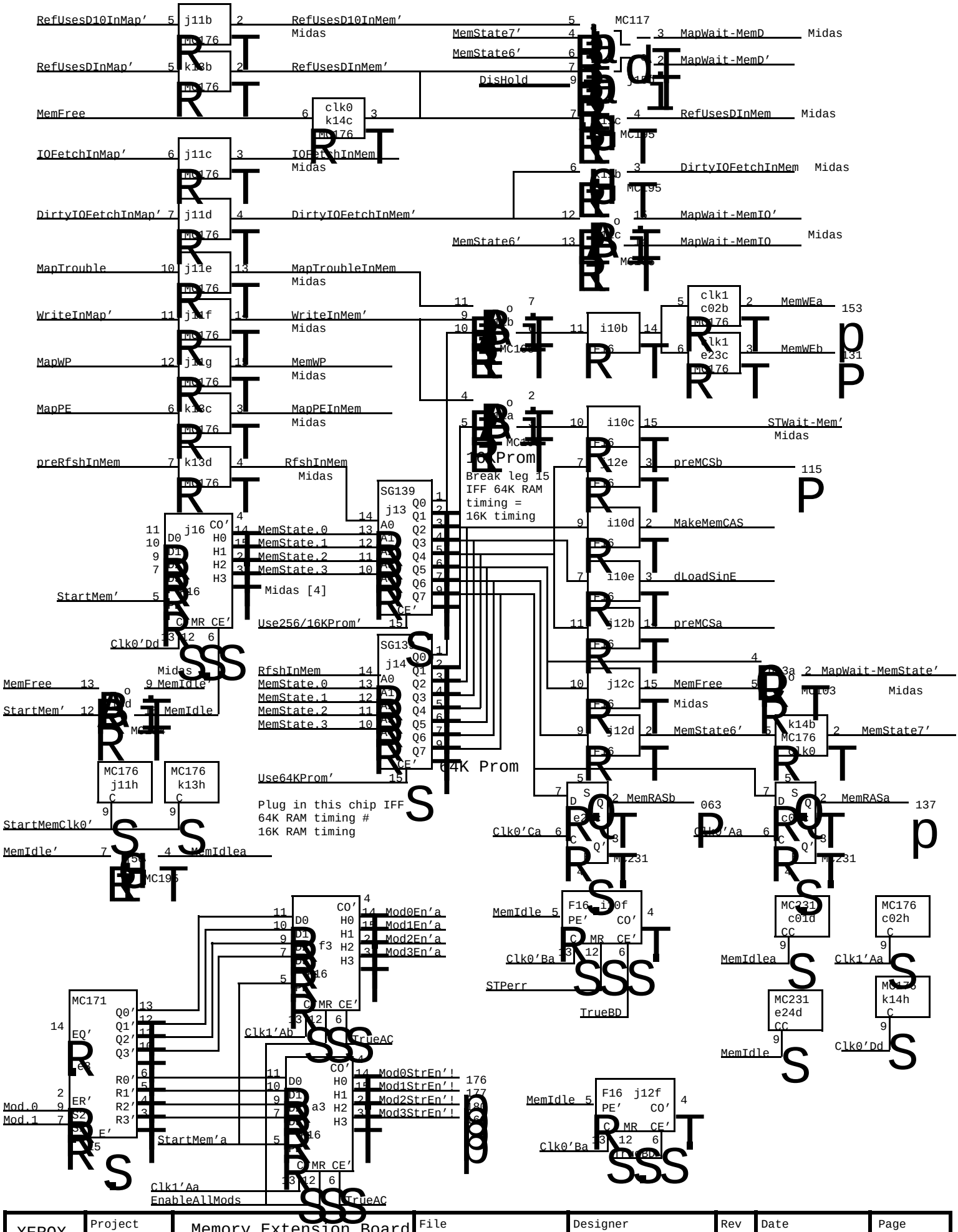
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Refresh Control & PEs	MemX04.sil	K. Pier	Da	7/11/79	04



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Store Transport Automaton MemX05.sil	K. Pier	Da	6/23/79	05



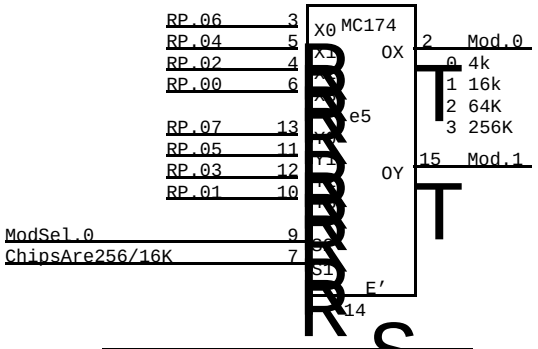
XEROX PARC	Project: Dorado	Memory Extension Board Map Automaton	File: MemX06.sil	Designer: K. Pier	Rev: Da	Date: 6/23/79	Page: 06



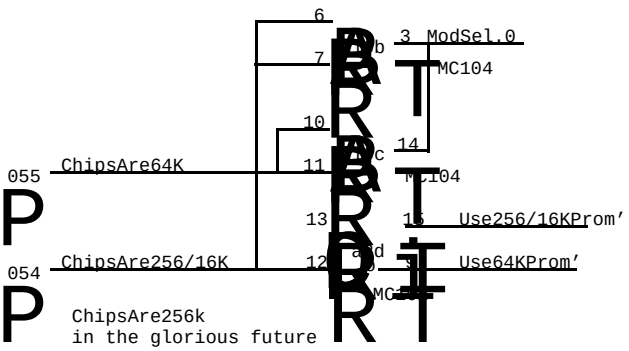
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado Memory Extension Board Memory Automaton	MemX07.sil	K. Pier	Da	10/21/81	07

Note: Chip size options are available:
16K only, 16K or 64K, 64K only, 64K
or 256K, 256K only.

Only one of the ChipsAreXXX signals should
be true at any time.

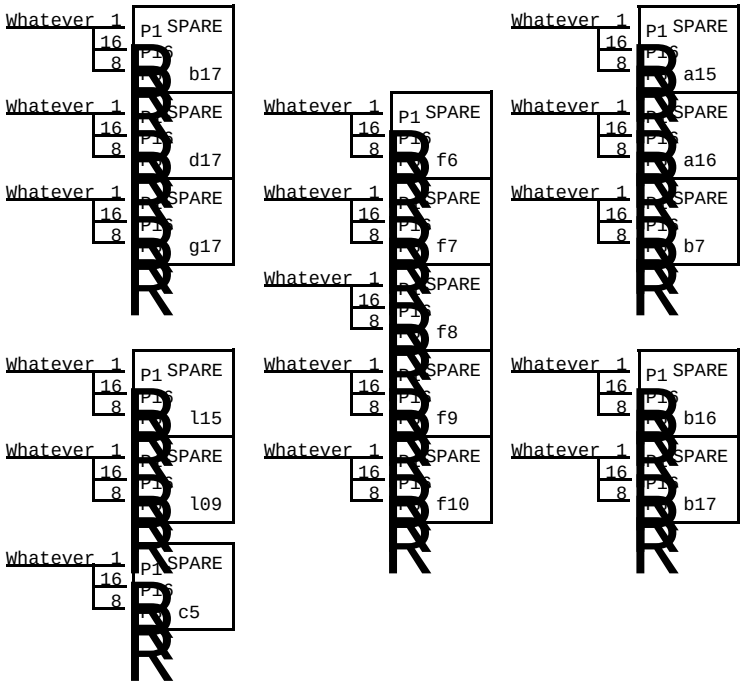


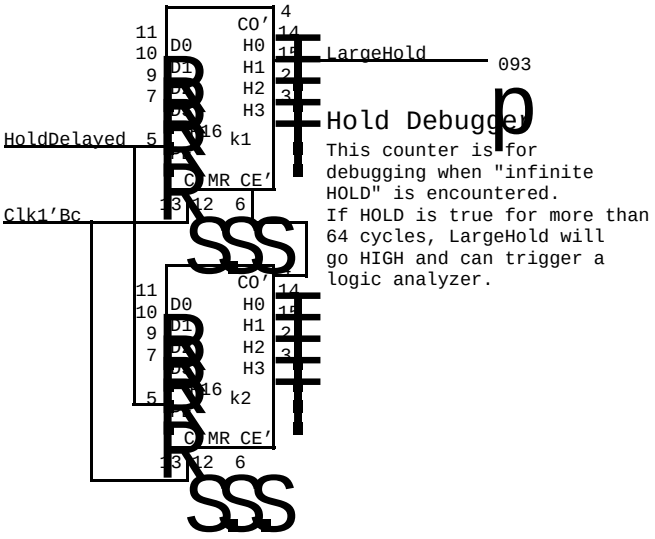
BREAK THIS BUG LEG
UNTIL 256K CHIPS
ARE USED



ChipsAre256k
in the glorious future

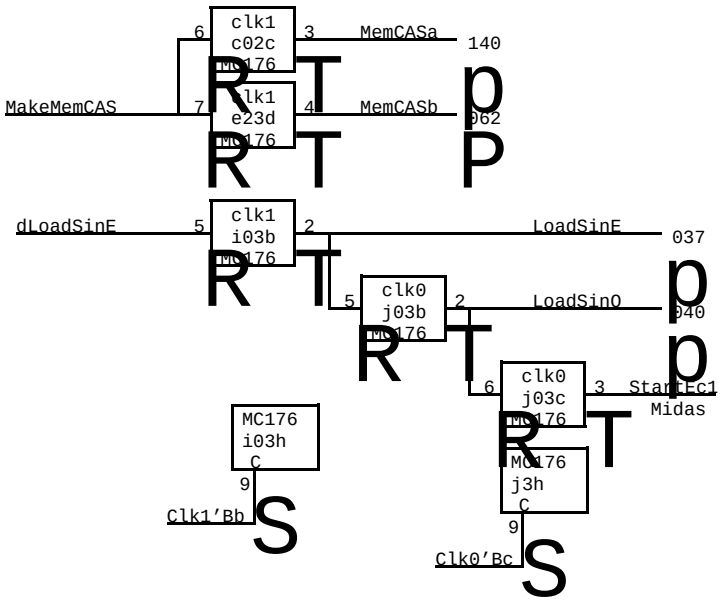
When the only two chip
options for Dorado are
64K or 256K, then interpret
this signal as ChipsAre256K
and enable the upper gate of ModSel.0



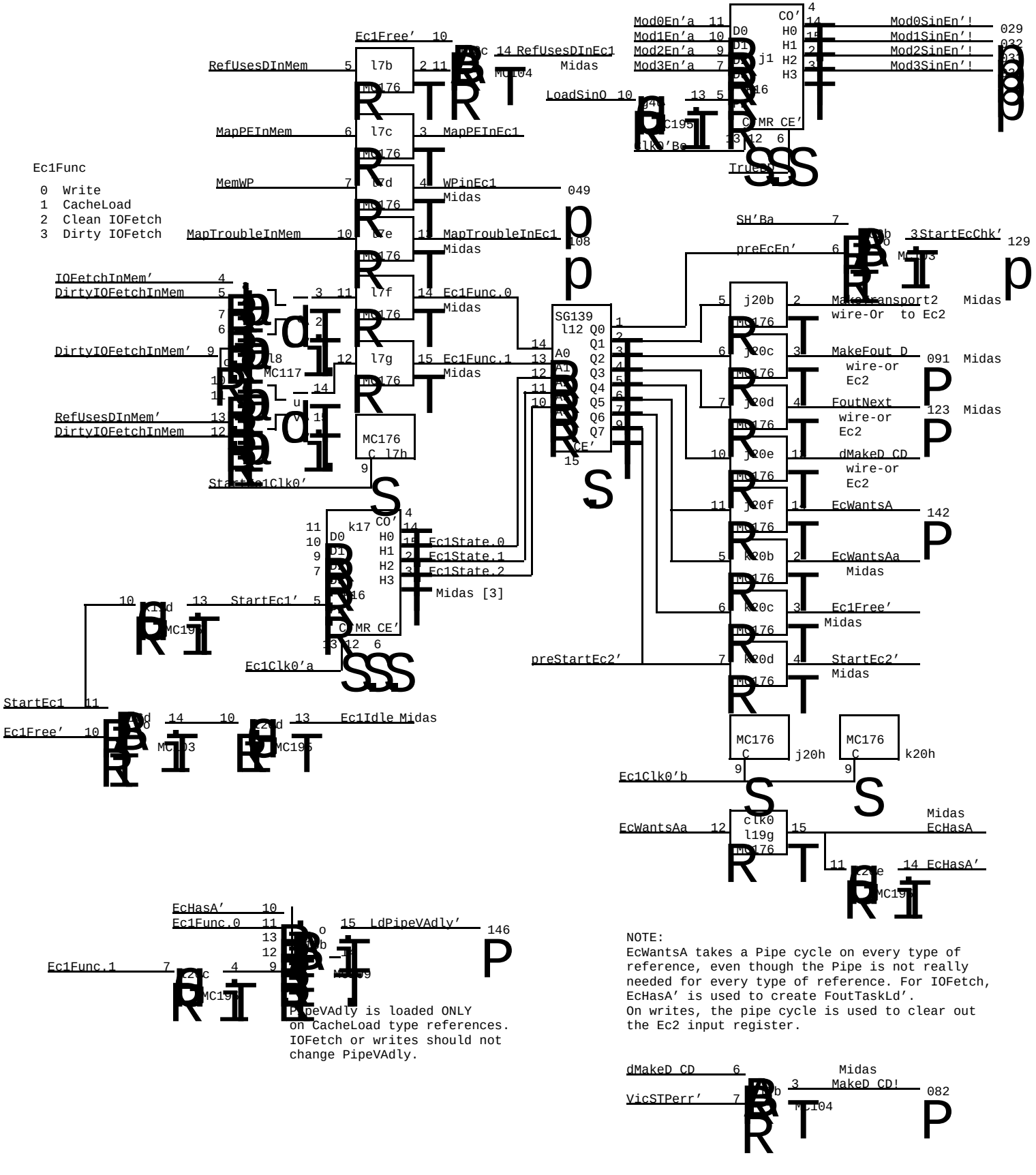


Hold Debugger

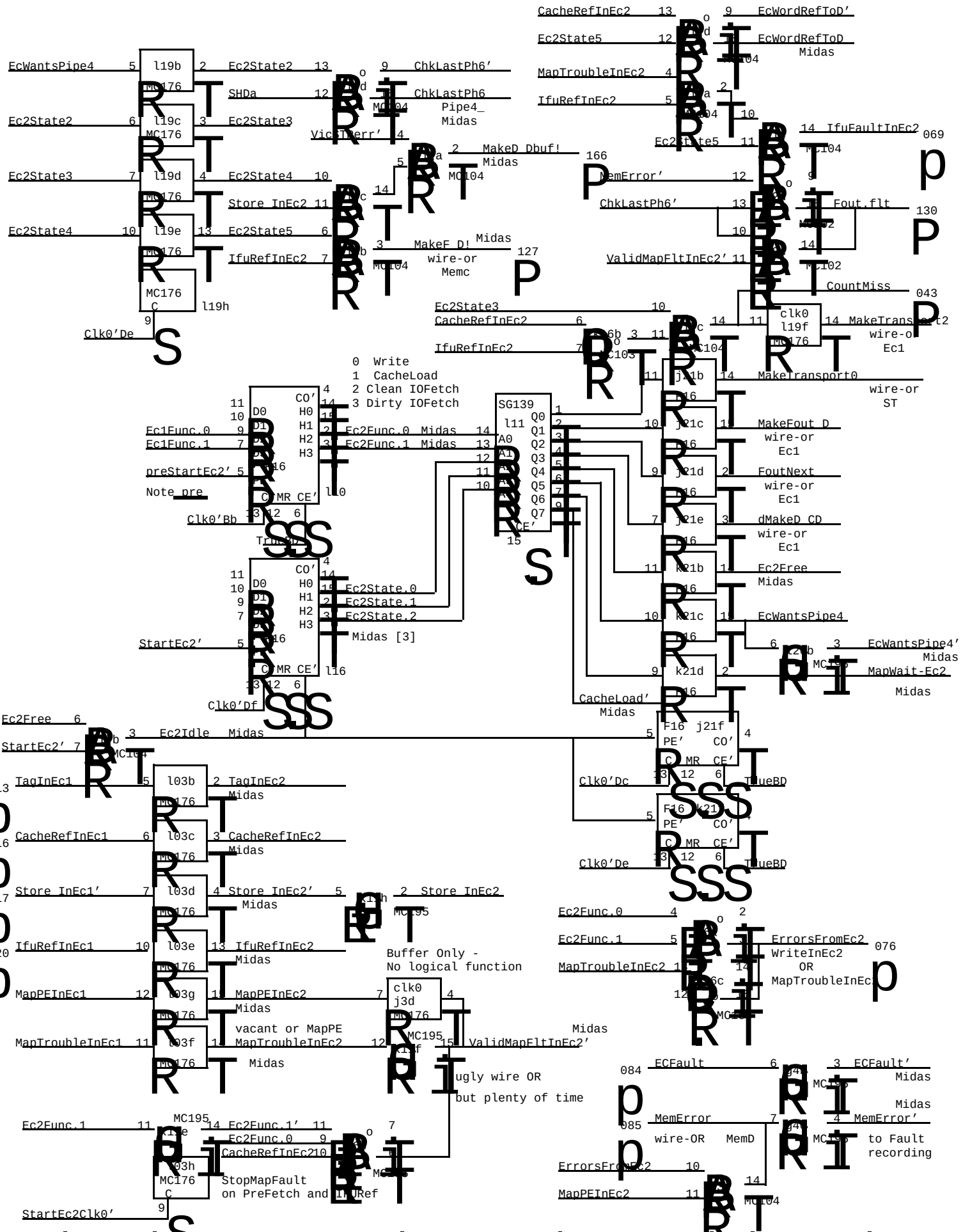
This counter is for
debugging when "infinite
HOLD" is encountered.
If HOLD is true for more than
64 cycles, LargeHold will
go HIGH and can trigger a
logic analyzer.



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado CAS Control RAM size control	MemX08.sil	K. Pier	Da	10/29/79	08



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Ec1 Automaton	MemX09.sil	K. Pier	Da	7/11/79	09


0 Write
1 CacheLoad
2 Clean IOFetch
3 Dirty IOFetch
Buffer Only -
No logical function
vacant or MapPE
Midas
wire-or
Memc
wire-OR
MemD
StopMapFault
on PreFetch and IfuRef
to Fault
recording
Project
Dorado
Memory Extension Board
Ec2 Automaton
File
MemX10.sil
Designer
K. Pier
Rev
Da
Date
9/08/79
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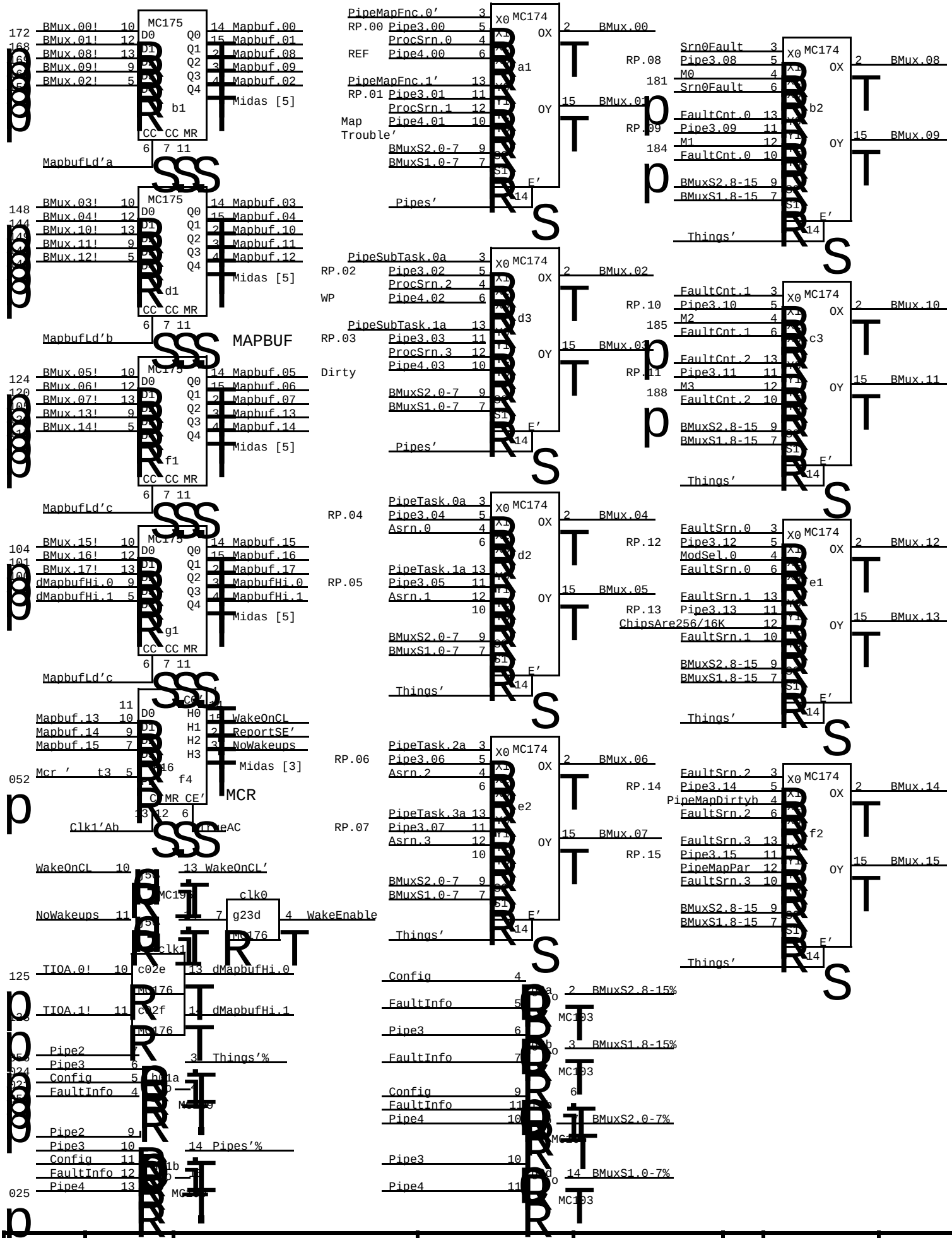
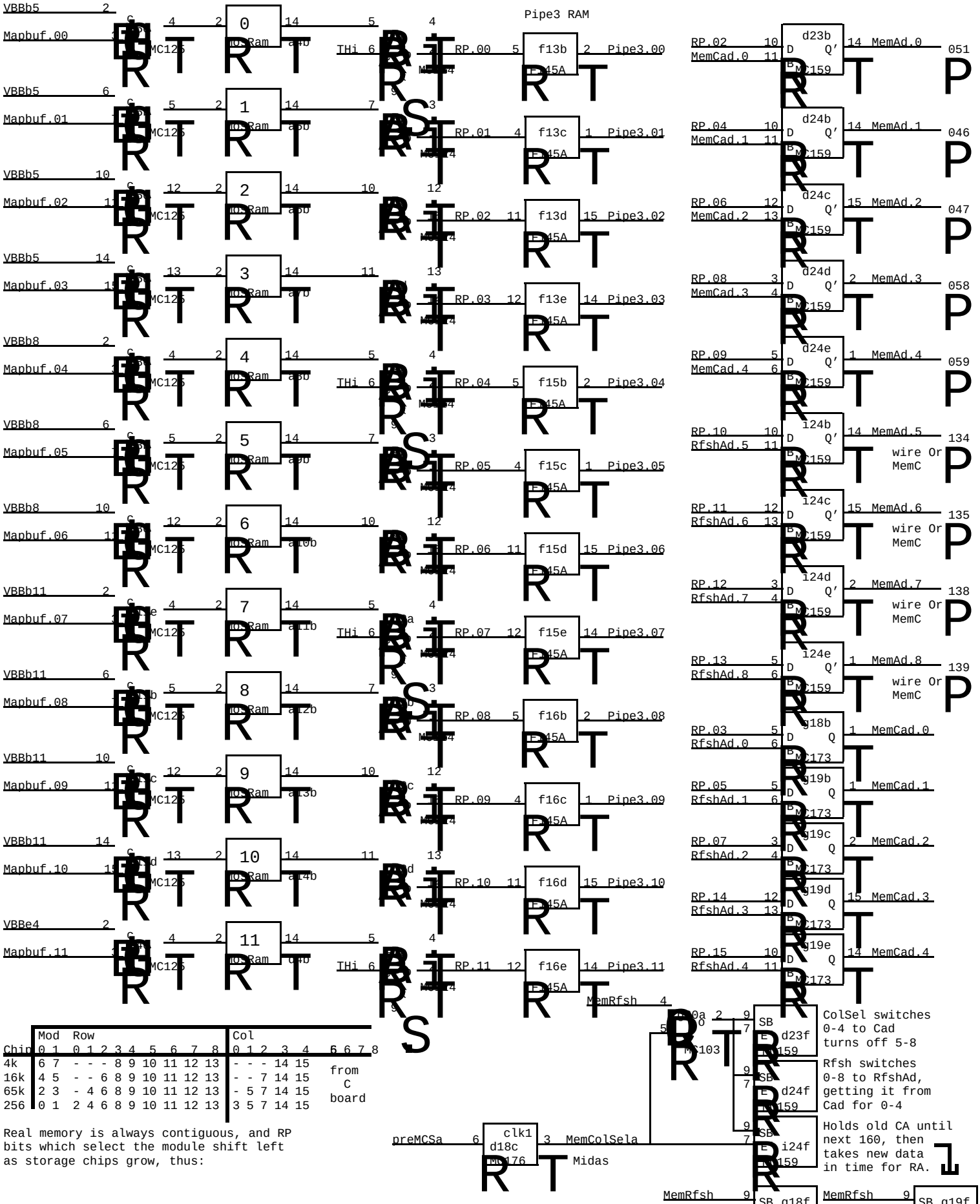
10



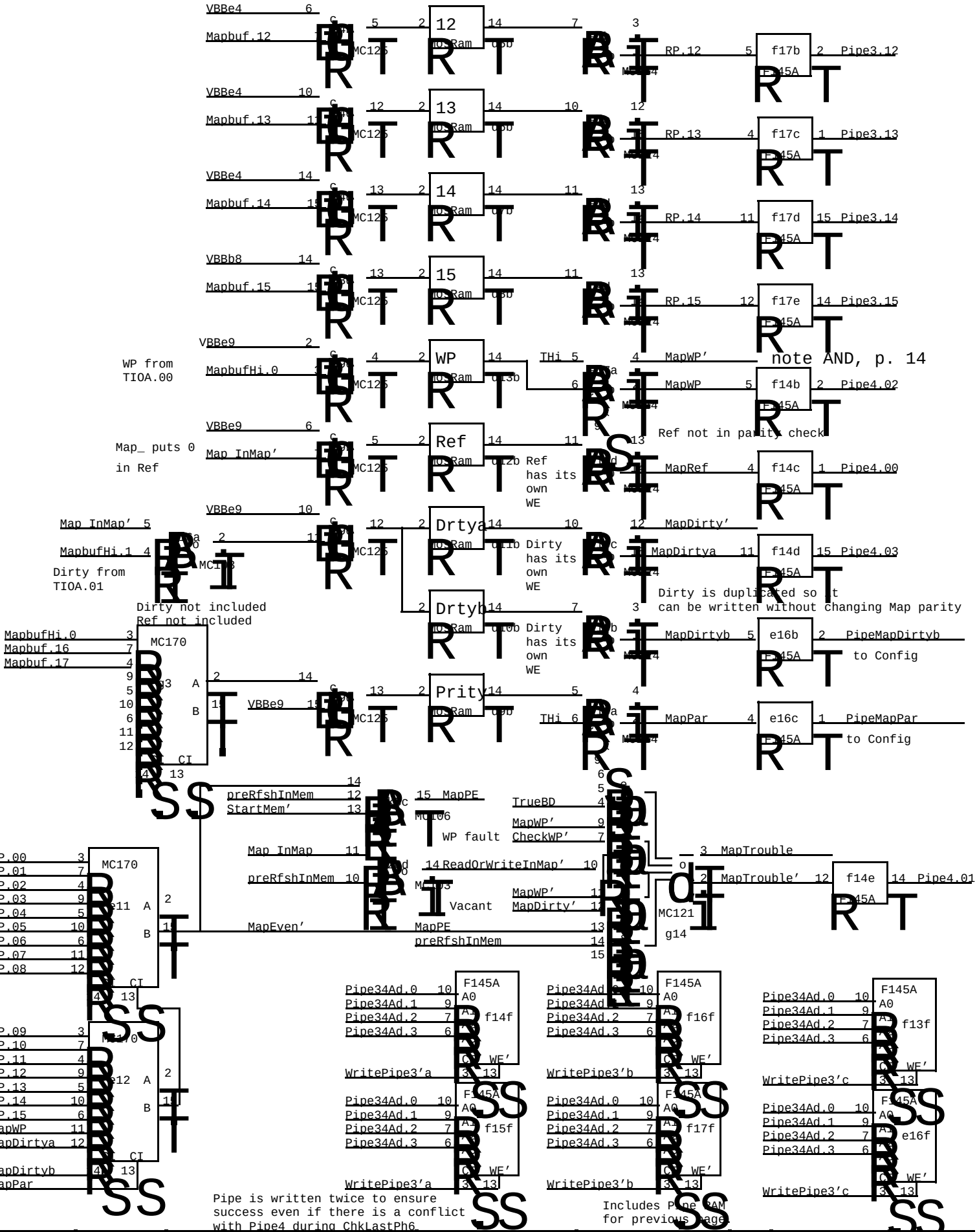
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board BMux drivers and rcvrs	MemX11.sil	K. Pier	Da	9/08/79	11



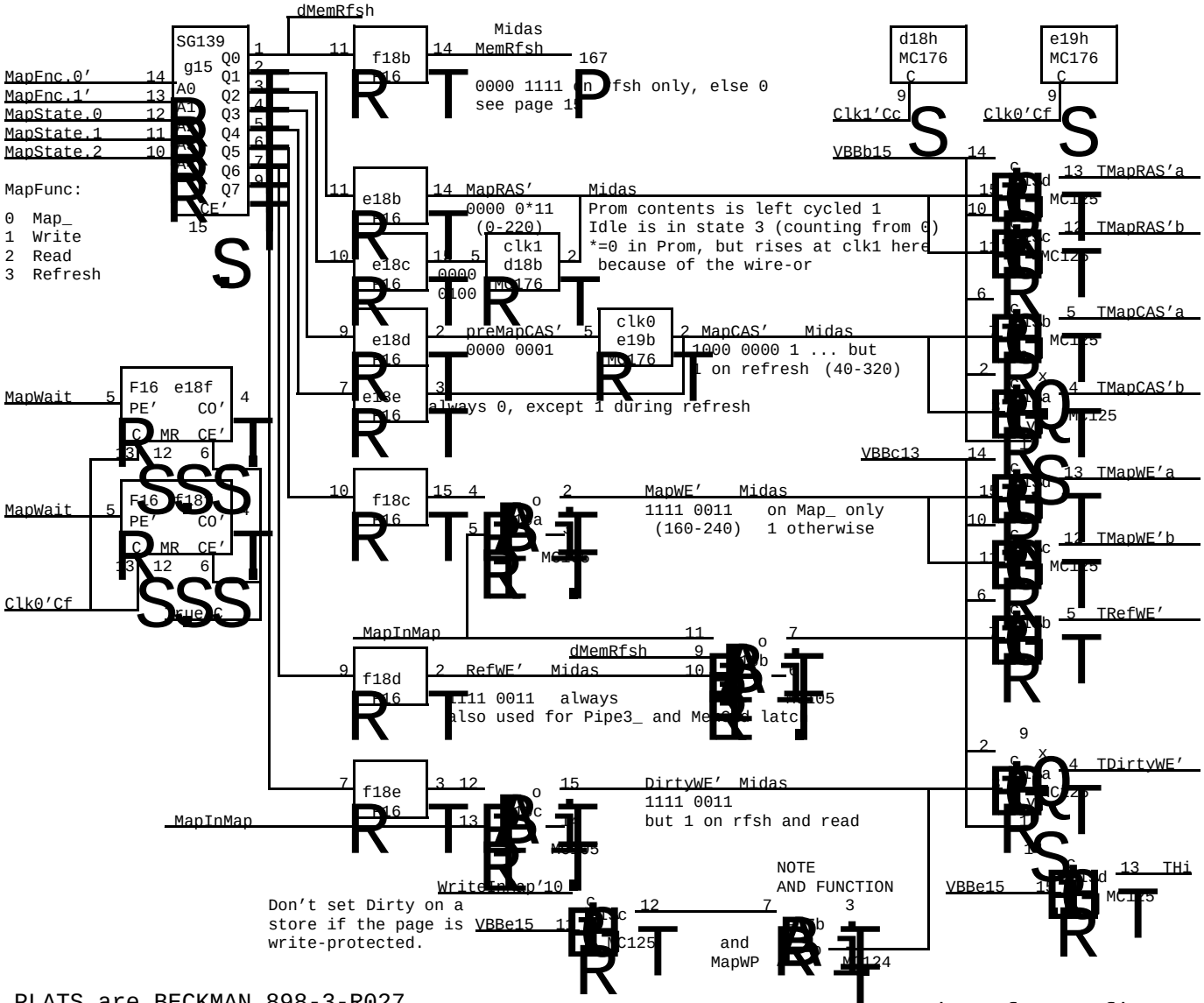
Chip	Mod	Row	Col	6 6 7 8
	0 1	0 1 2 3 4 5 6 7 8	0 1 2 3 4	
4k	6 7	- - - 8 9 10 11 12 13	- - - 14 15	from C board
16k	4 5	- - 6 8 9 10 11 12 13	- - 7 14 15	
65k	2 3	- 4 6 8 9 10 11 12 13	- 5 7 14 15	
256	0 1	2 4 6 8 9 10 11 12 13	3 5 7 14 15	

Real memory is always contiguous, and RP bits which select the module shift left as storage chips grow, thus:

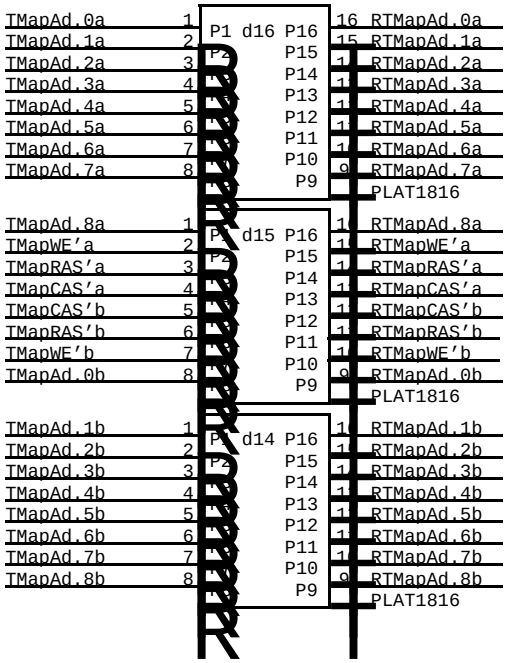
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Map RP 00-11	MemX12.sil	K. Pier	Da	7/03/79	12



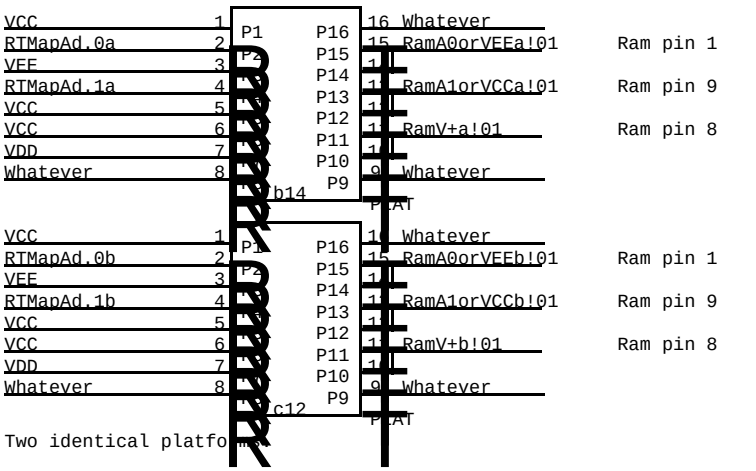
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado Memory Extension Board Map RP12-15 and Other	MemX13.sil	K. Pier	Da	7/03/79	13

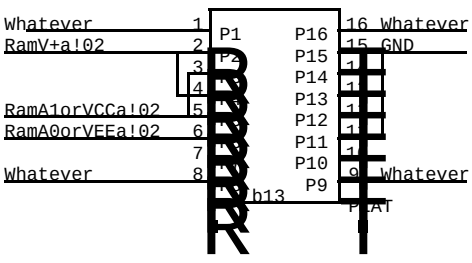


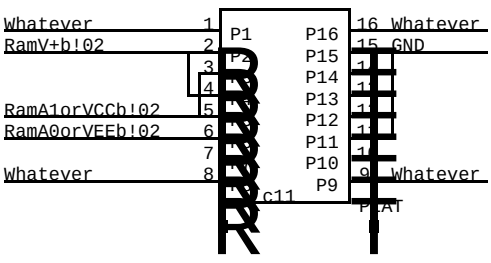
PLATS are BECKMAN 898-3-R027
series resistors 8 per chip



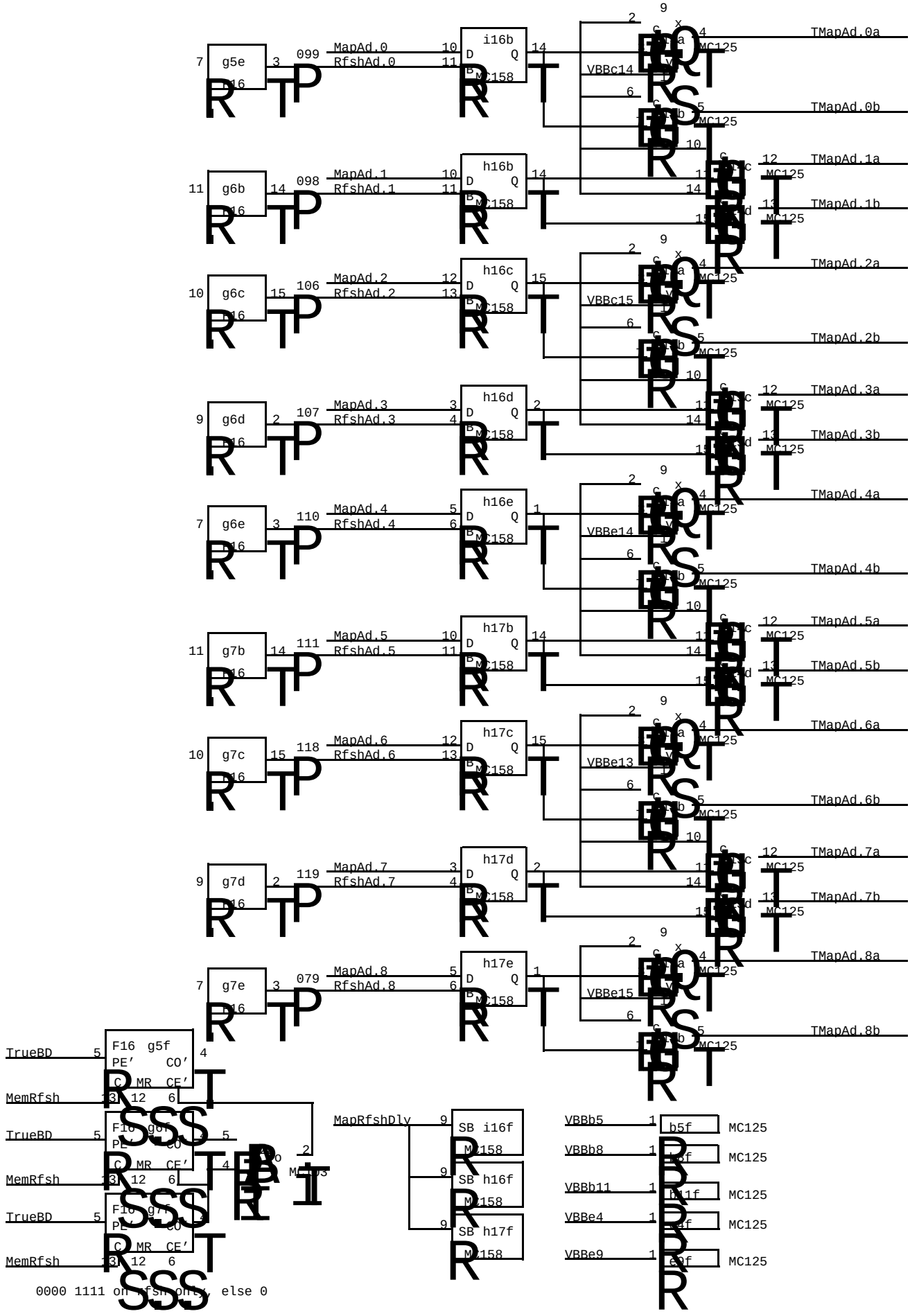
PLATS are Jumper wires for configuration



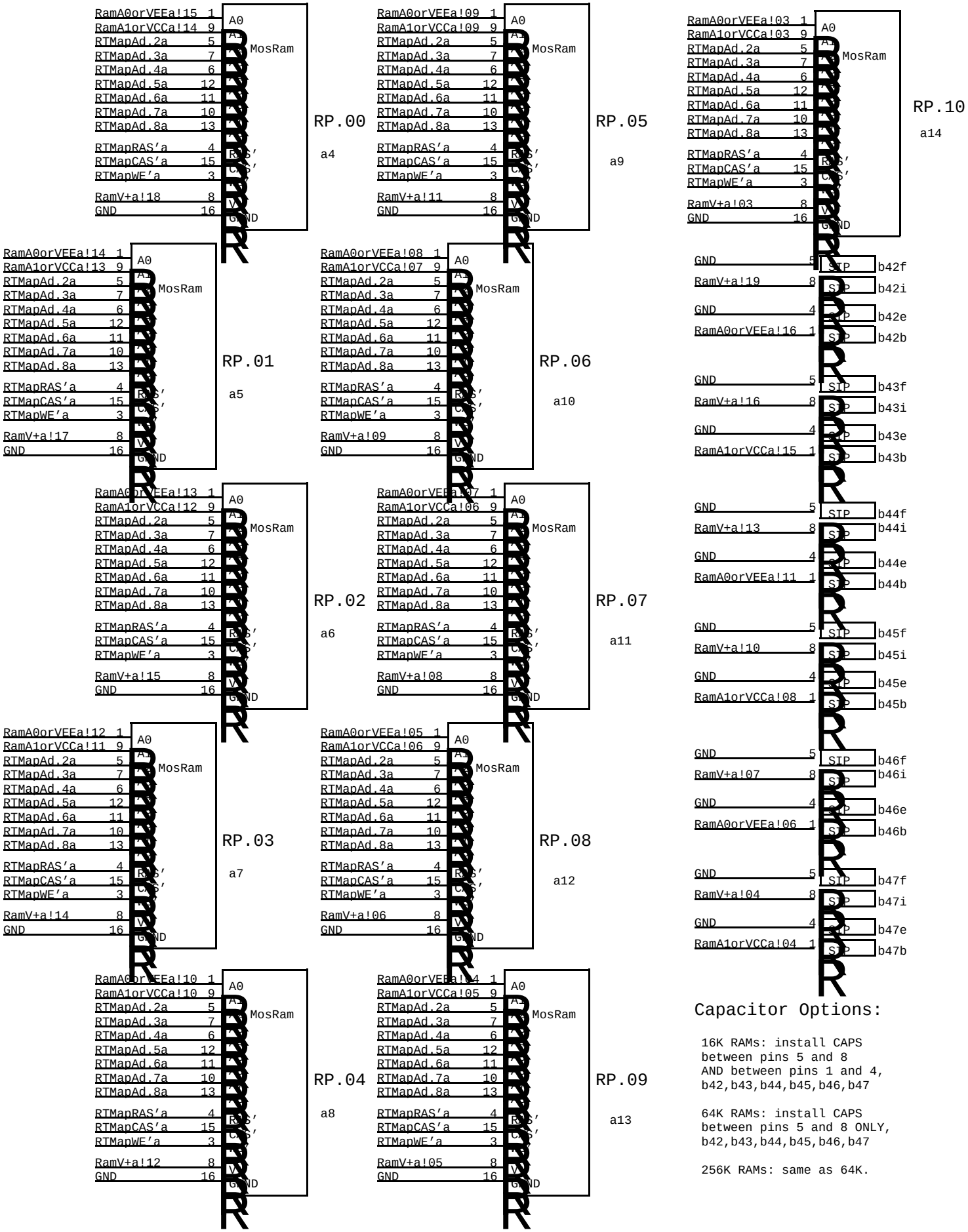




XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Map address and control	MemX14.sil	K. Pier	Da	10/29/79	14



XEROX PARC	Project: Dorado	Memory Extension Board Map address and control	File: MemX15.sil	Designer: K. Pier	Rev: Da	Date: 7/03/79	Page: 15



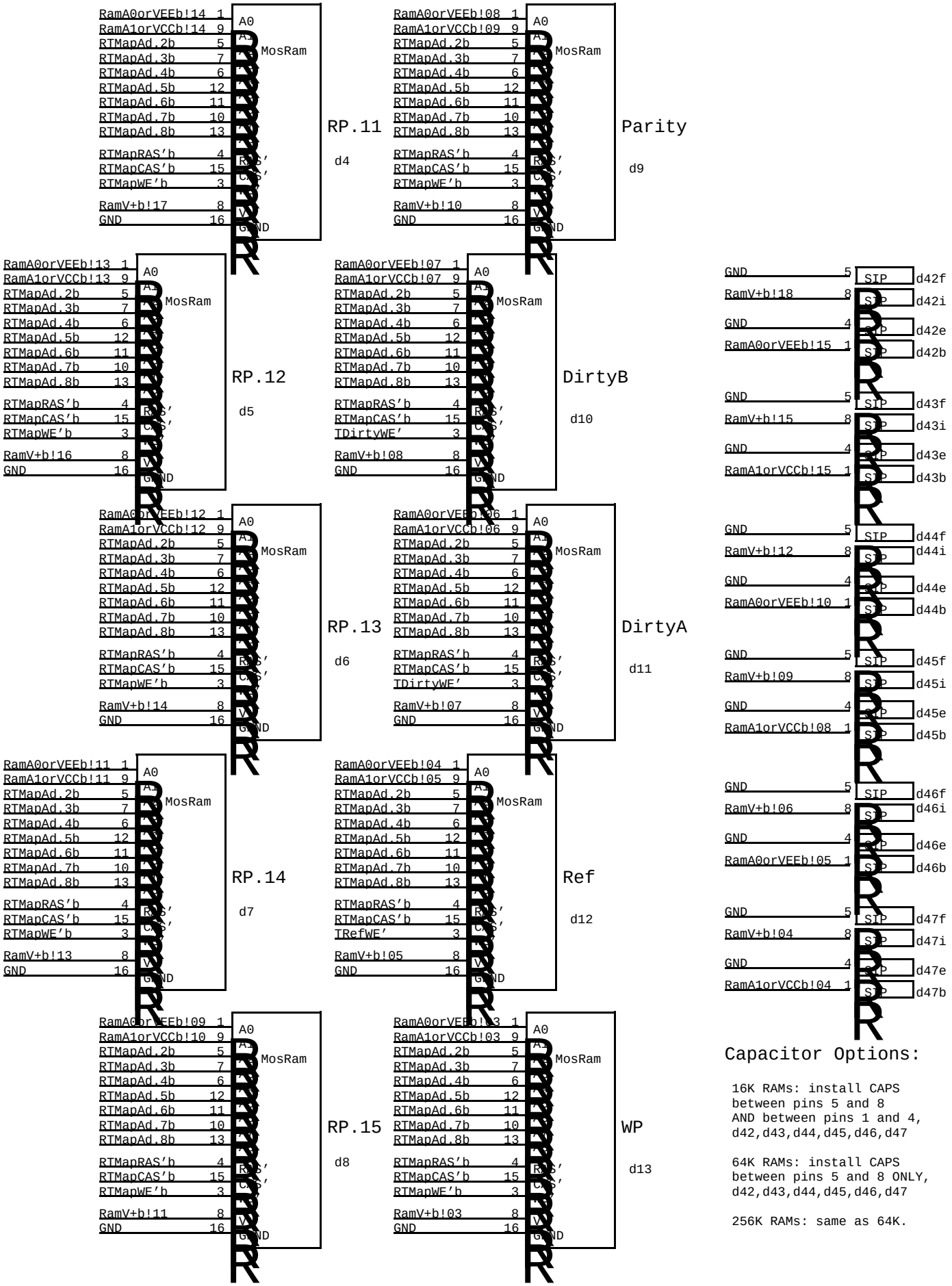
Capacitor Options:

16K RAMs: install CAPS
between pins 5 and 8
AND between pins 1 and 4,
b42,b43,b44,b45,b46,b47

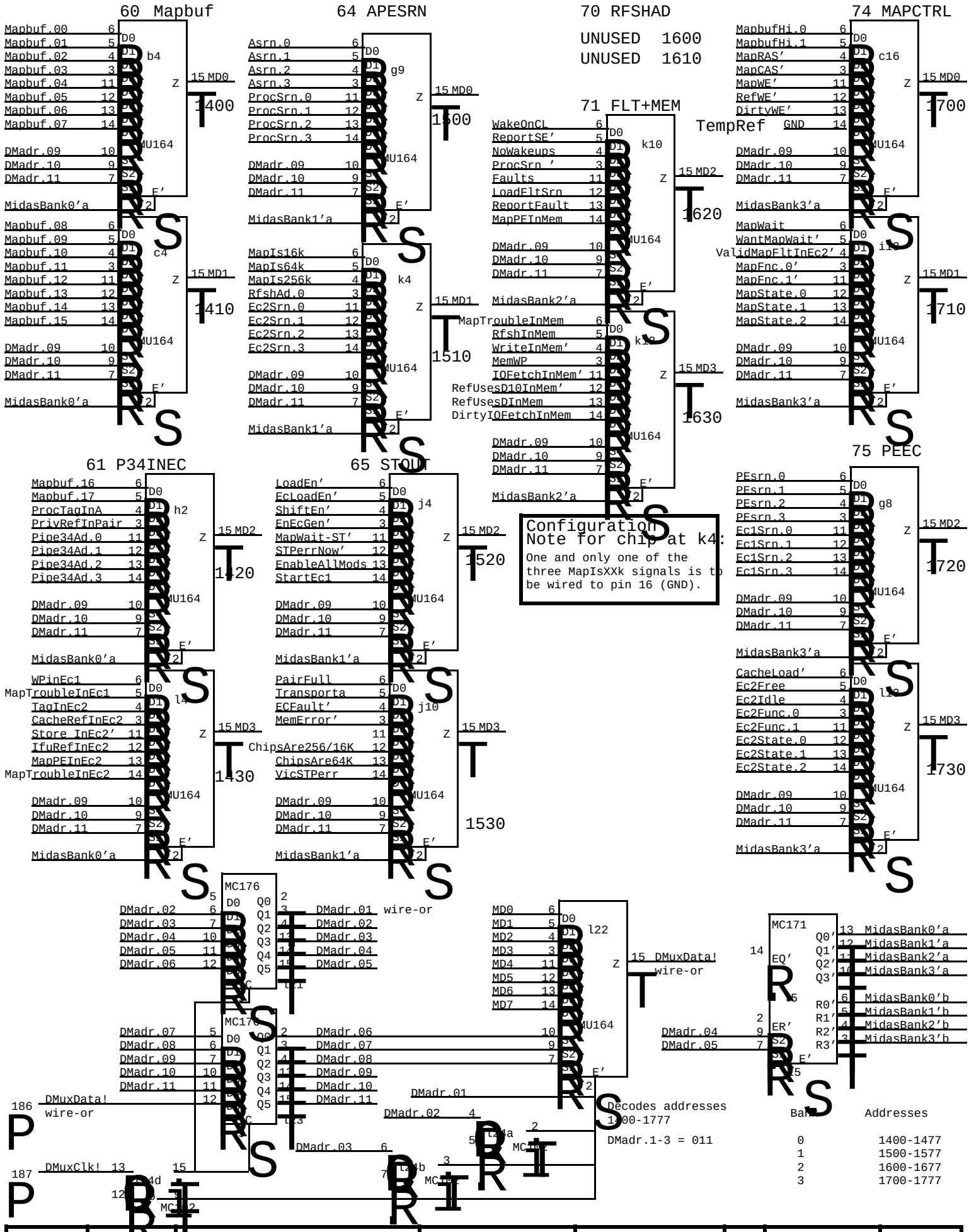
64K RAMs: install CAPS
between pins 5 and 8 ONLY,
b42,b43,b44,b45,b46,b47

256K RAMs: same as 64K.

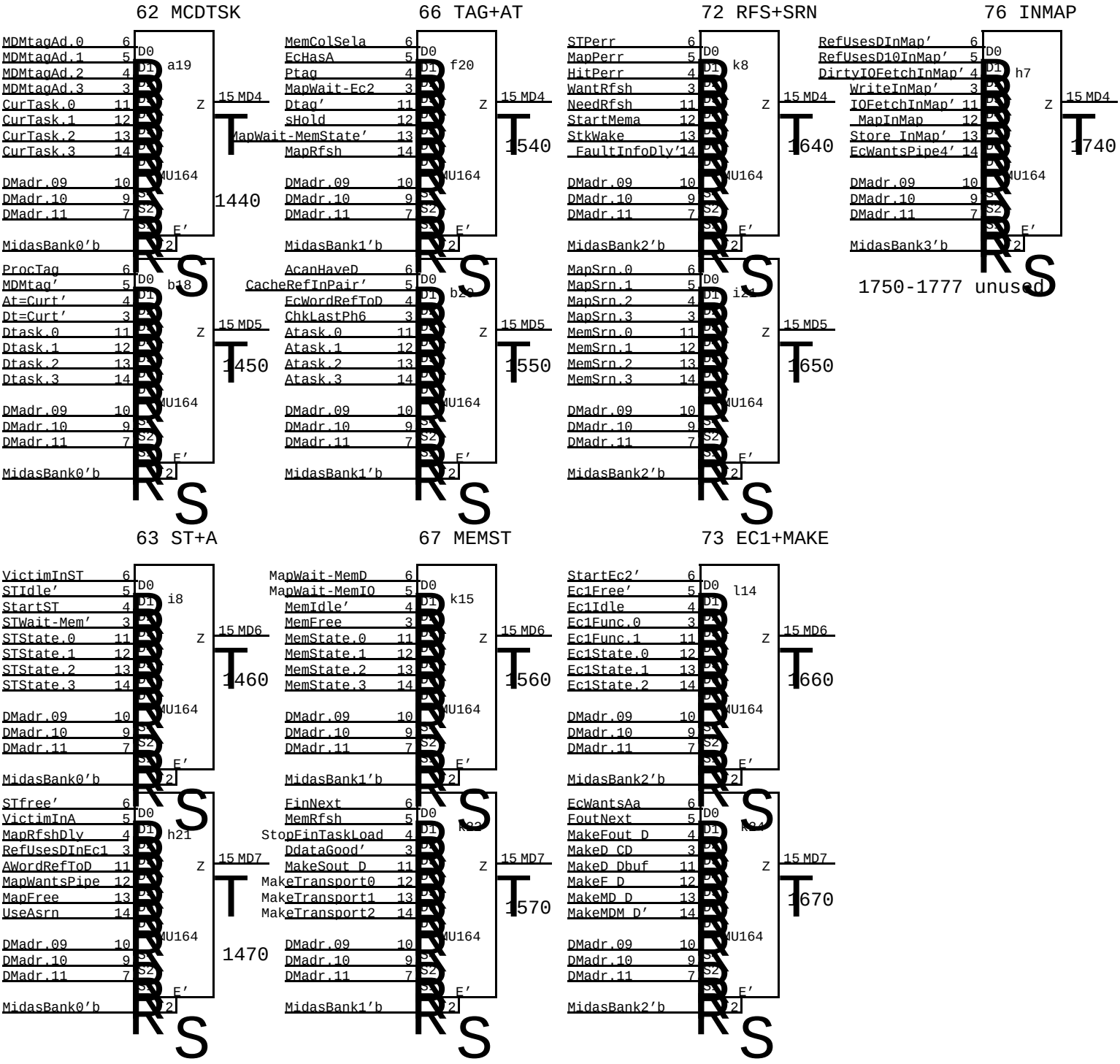
XEROX PARC	Project	Memory Extension Board	File	Designer	Rev	Date	Page
	Dorado	Map RAM chips	MemX16.sil	K. Pier	Da	10/29/79	16



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Map RAM chips	MemX17.sil	K. Pier	Da	10/29/79	17

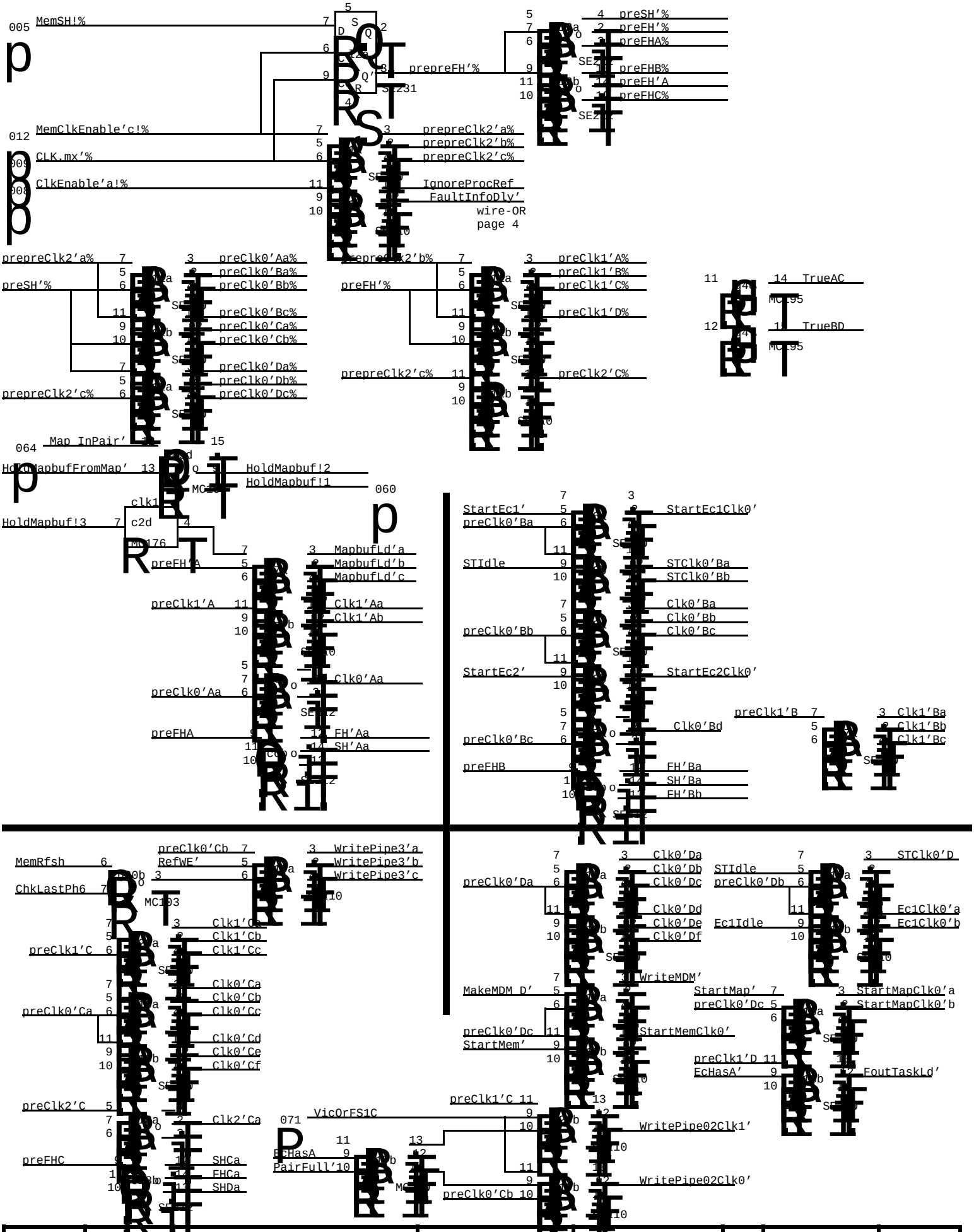


XEROX PARC	Project: Dorado	Memory Extension Board Midas Interface	File: MemX18.sil	Designer: K. Pier	Rev: Da	Date: 7/19/79	Page: 18

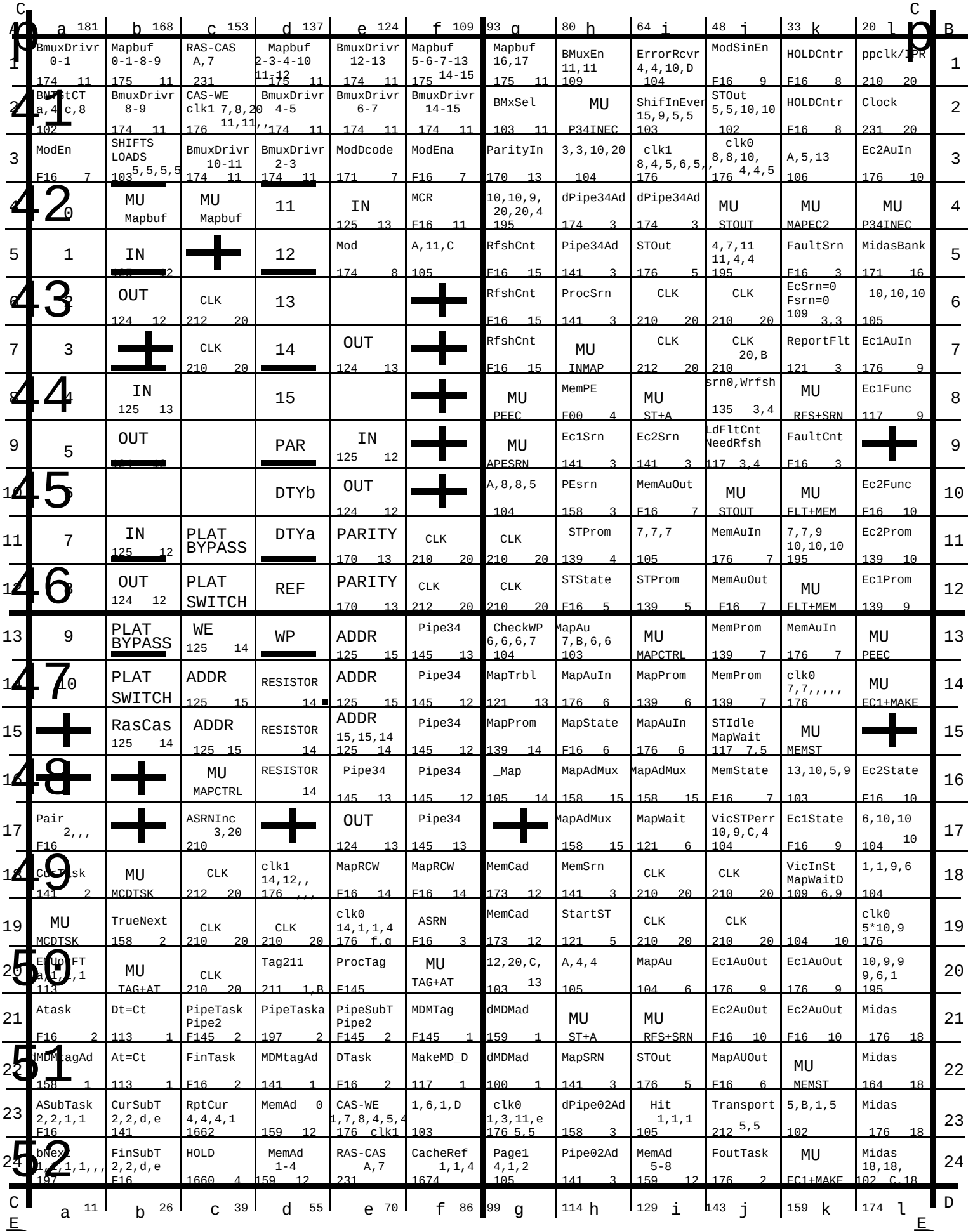


Bank	Addresses
0	1400-1477
1	1500-1577
2	1600-1677
3	1700-1777

XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado Memory Extension Board Midas Interface	MemX19.sil	K. Pier	Da	7/03/79	19



XEROX PARC	Project: Dorado	Memory Extension Board Clock Logic	File: MemX20.sil	Designer: K. Pier	Rev: Da	Date: 7/03/79	Page: 20



XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	MemX Board Layout	MemX21.sil	K. Pier	Da	10/29/79	21

Location h11

ST

Q	ADDR STATE	11 cycles IO Store 0-13 012345678910	14-17 11	12 cycles VictimStore 20- 33 01234567891011	34-37
0	prepreLoadEn’	00000001110	0 1	00000000111 1	1
1	preEcLoadEn’	10101010111	1 1	11010101011 1	1
2	preShiftEn’	00000001111	1 1	10000000111 1	1
3	preEnEcGen’	11111111110	0 1	01111111111 1	1
4	preMapWait-ST’	00001111110	0 1	00000111111 0	1
5	preSTfree’	11111111101	1 1	11111111110 1	1
6	prepreSTPerrNow’	00000000111	1 1	10000000011 1	1
7	preStopFinTaskLd	11111100001	1 0	11111111000 0	0
Location i12					
0	preFinNext	11111110001	1 0	00000000000 0	0
5	preMakeSout_D	00000000000	0 0	11111111000 0	0
6	PreMakeTrnspt0	00000000000	0 0	11111110000 1	0

Location l12

EC1

Q	ADDR STATE	Write 0 - 7 01234567	CacheLoad 10 - 17 01234567	Clean or Miss IOfetch 20 - 27 01234567	Dirty Hit IOfetch 30 - 37 01234567
0	preEcEn’	01111111	01111111	01111111	01111111
1	preMakeTrspt2	00000000	00111100	00000000	00111100
2	preMakeFout_D	00000000	00000000	00000000	00011100
3	preFoutNext	00000000	00000000	00011100	00001100
4	preMakeD_CD	00000000	00111100	00000000	00000000
5	preEcWantsA	01000000	01000000	01000000	01000000
6	preEc1Free’	11111101	11111101	11111101	11111101
7	preStartEc2’	11111011	11111011	11111011	11111011

Location l11

EC2

Q	ADDR STATE	Write 0 - 7 01234567	CacheLoad 10 - 17 01234567	CLEAN or Miss IOfetch 20 - 27 01234567	Dirty Hit IOfetch 30 - 37 01234567
0	prepreMakeTnspt1	00000000	11100001	00000000	11100001
1	preMakeFout_D	00000000	00000000	00000000	11110001
2	preFoutNext	00000000	00000000	11110001	11111001
3	preMakeD_CD	00000000	11100001	00000000	00000000
4	preEc2Free	00000010	00000010	00000010	00000010
5	preEcWantsPipe4	10000000	10000000	10000000	10000000
6	preMapWait-Ec2	00000000	11110001	00000000	11110001
7	CacheLoad’	11111111	00000010	11111111	11111111

Location i14

MAP

Q	ADDR STATE	Refresh 0 - 7 01234567	Read 10 - 17 01234567	Write 20 - 27 01234567	Map write 30 - 37 01234567
0	prepreRfshInMem	00010000	00000000	00000000	00000000
1	UNUSED				
2	preStartMem’	11101111	11101111	11101111	11111111
3	preStartMem	00010000	00010000	00010000	00000000
4	preMapFree’	11111101	11111101	11111101	11111101
5	preMapWantsPipe	00000000	00110000	00110000	00110000

IDENTICAL

Location g15

MAP

Q	ADDR STATE	Refresh 0 - 7 01234567	Read 10 - 17 01234567	Write 20 - 27 01234567	Map Write 30 - 37 01234567
0	preMemRfsh	00011110	00000000	00000000	00000000
1	preRAS1’	00000110	00000110	00000110	00000110
2	preRAS2’	00001000	00001000	00001000	00001000
3	prepreCAS1’	11111110	00000010	00000010	00000010
4	prepreCAS2’	11111100	00000000	00000000	00000000
5	preMapWE’	11111111	11111111	11111111	11100111
6	preRefWE’	11100111	11100111	11100111	11100111
7	preDirtyWE’	11111111	11111111	11100111	11100111

Location j13

MEM 16K chips

Q	ADDR STATE	READ 0 - 7 01234567	WRITE 0 - 7 01234567	10-17	REFRESH 20 - 27 01234567	30-37
0	prepreMemWE’	10011111	10011111	1	11111111	1
1	preSTWait-Mem’	10111111	10111111	1	11111111	1
2	prepreMemCAS	11111100	11111100	0	00000000	0
3	prepreShiftLoadEven	00010000	00010000	0	00000000	0
4	prepreMCS	11111000	11111000	0	00000000	0
5	preMemFree	00000010	00000010	0	00000010	0
6	preMemState6’	11111011	11111011	1	11111011	1
7	preMemRAS	11110001	11110001	1	11110001	1

IDENTICAL

Location j14

MEM 4K chips

Q	ADDR STATE	READ 0 - 14 0123456789	10	11	12	15-17 13-15	WRITE 0123456789	10	11	12	13-15	REFRESH 20 - 34 0123456789	10	11	12	35-37 13-15
0	prepreMemWE’	1100000111	1	1	1	1	1100000111	1	1	1	1	1111111111	1	1	1	1
1	preSTWait-Mem’	1111101111	1	1	1	1	1111101111	1	1	1	1	1111111111	1	1	1	1
2	prepreMemCAS	0001111100	0	0	0	0	0001111100	0	0	0	0	0001111100	0	0	0	0
3	prepreShiftLoadEven	0000000100	0	0	0	0	0000000100	0	0	0	0	0000000000	0	0	0	0
4	prepreMCS	0111111000	0	0	0	0	0111111000	0	0	0	0	0000000000	0	0	0	0
5	preMemFree	0000000000	0	1	0	1	0000000000	0	1	0	1	0000000000	0	1	0	1
6	prepreState7’	1111111111	1	1	1	1	1111111111	1	1	1	1	1111111111	1	1	1	1
7	preMemRAS	1111111100	0	0	1	0	1111111100	0	0	1	0	1111111100	0	0	1	0

OBSOLETE

IDENTICAL

XEROX PARC	Project Dorado	Reference Automata program tables	File Memx22.sil	Designer K. Pier	Rev Da	Date 9/08/79	Page 22

Dorado Memory Extension Board
Stuffing and Configuration Instructions

1. If 256 chips are NOT installed in the Memory Storage Arrays (MSA), then

   a. Break g10.6 (MC104) before stuffing. Label this chip as MemX-g10.

2. Break h20.10 before stuffing. Label this chip as MemX-h20.
   All SG10139 chips are PROMS which must be blown and labeled before stuffing.
   Stuff all PLAT1816 with Beckman type 898-3-R27 resistor packs or equivalent.

3. Do all the actions in one of the following three columns:

Action	16K Map Chips	64K Map Chips	256K Map Chips
Blue Wire	k4.6 to k4.16	k4.5 to k4.16	k4.4 to k4.16
Stuff into MosRam sockets	MK4116-2 or equivalent	TMS4156 or equivalent	256K Ram or equivalent
Jumper wires in socket b14	3 to 14 5 to 12 7 to 10	6 to 11 4 to 13	6 to 11 4 to 13 2 to 15
Jumper wires in socket c12	3 to 14 5 to 12 7 to 10	6 to 11 4 to 13	6 to 11 4 to 13 2 to 15
capacitors in SIP sockets b42,b43,b44,b45,b46,b47 d42,d43,d44,d45,d46,d47	0.1 mmf pins 5 to 8 each socket AND 0.1 mmf pins 1 to 4 each socket	0.1 mmf pins 5 to 8 each socket	0.1 mmf pins 5 to 8 each socket
1 KOhm resistor in socket b14 and 1 KOhm resistor in socket c12	NO	1 to 15 IF Ram has self refresh feature-Motorola or equivalent	NO
22 uf Cap in PLAT c11 & b13	+ 2 to 15 +4 to 14 +11 to 6	+ 3 to 14 + 5 to 12	+ 3 to 14 + 5 to 12