

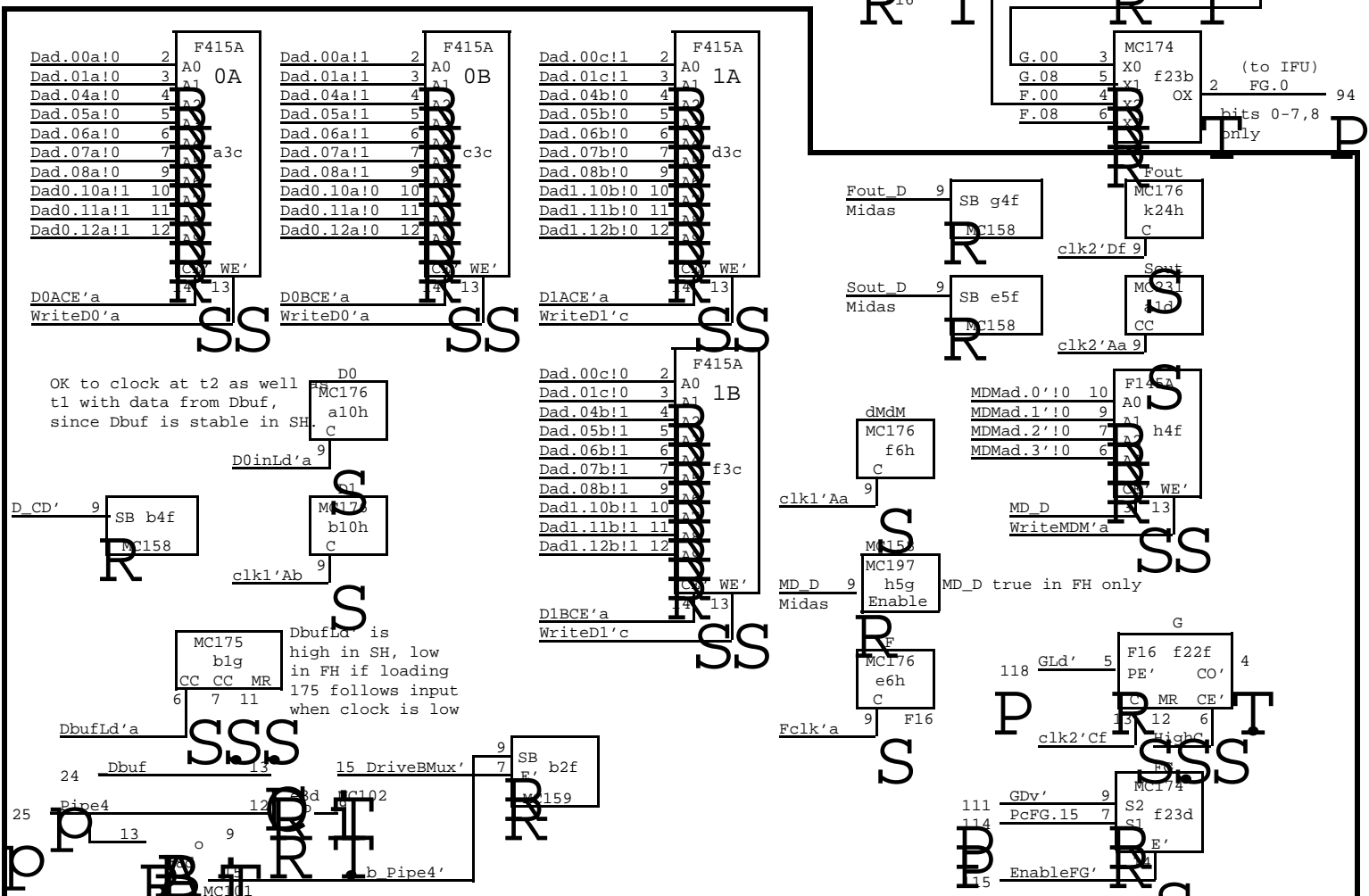
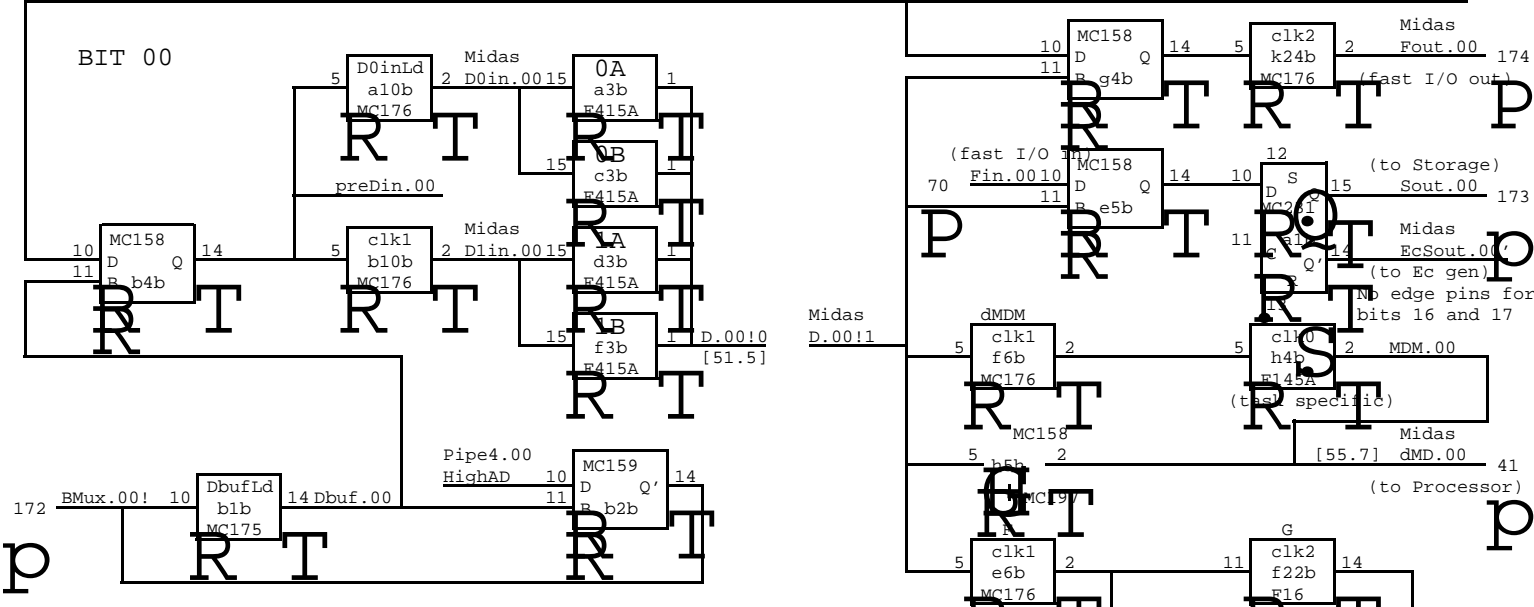
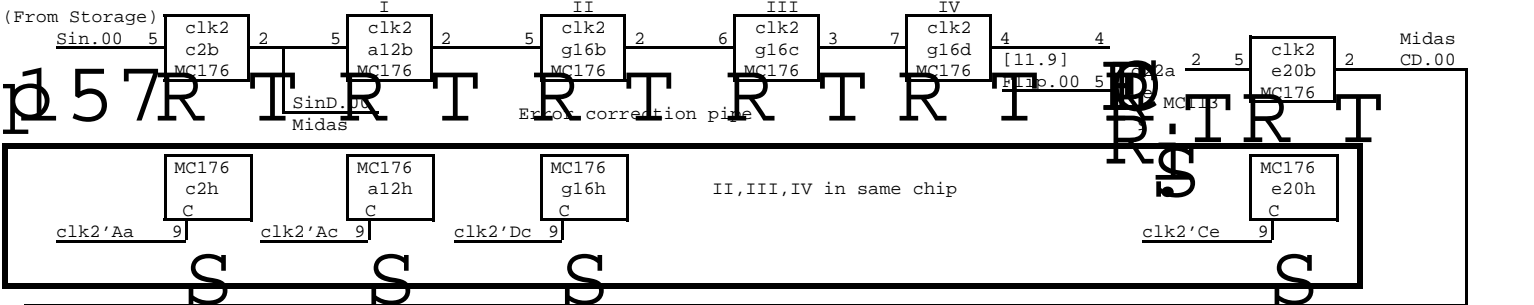
D O R A D O S C H E M A T I C S

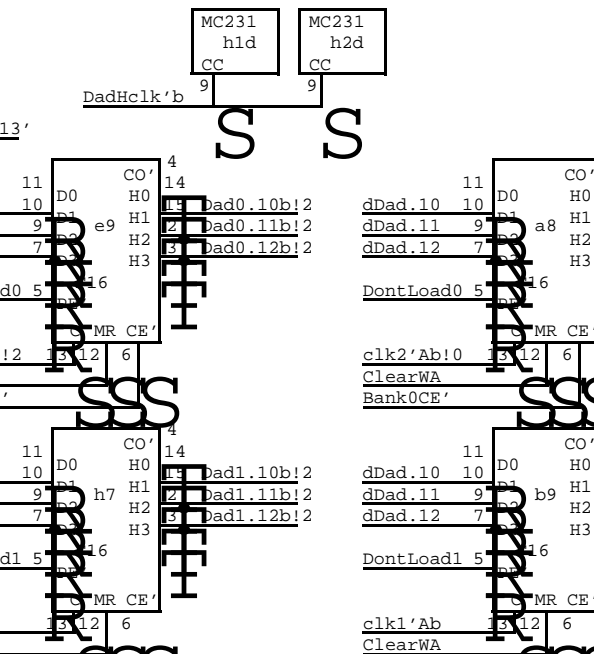
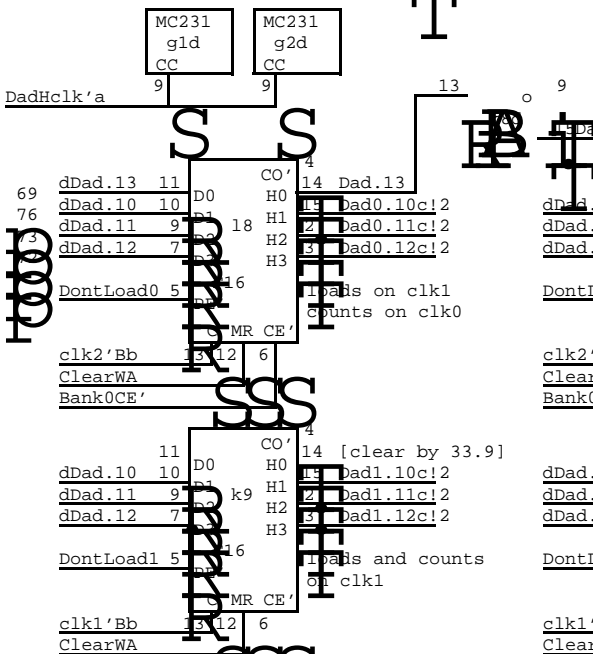
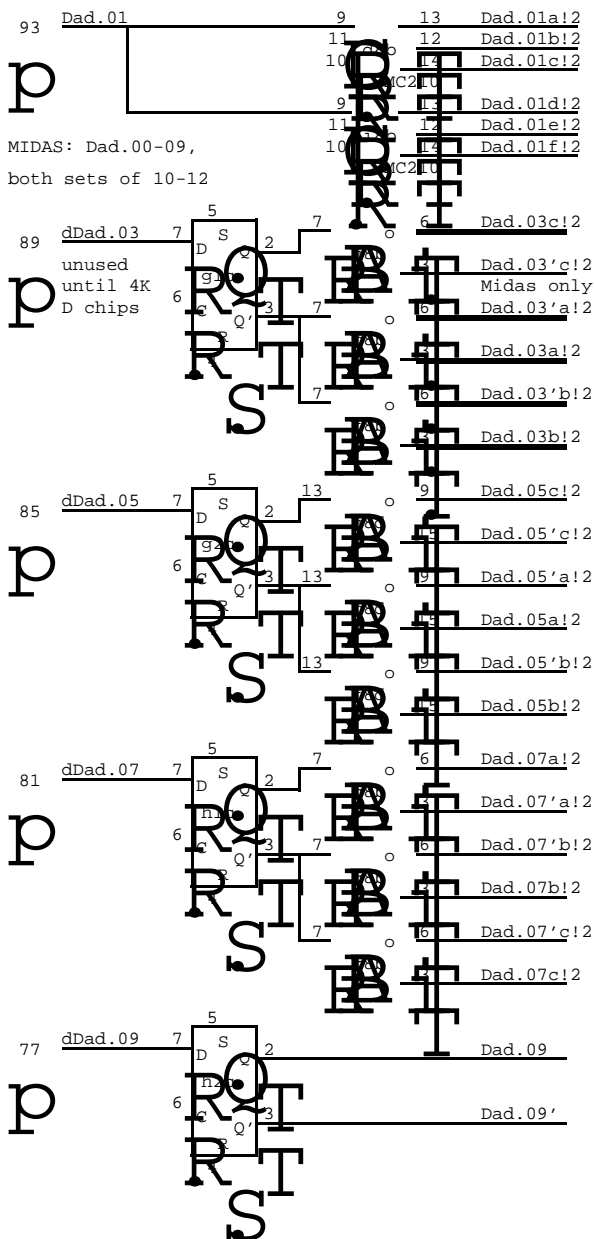
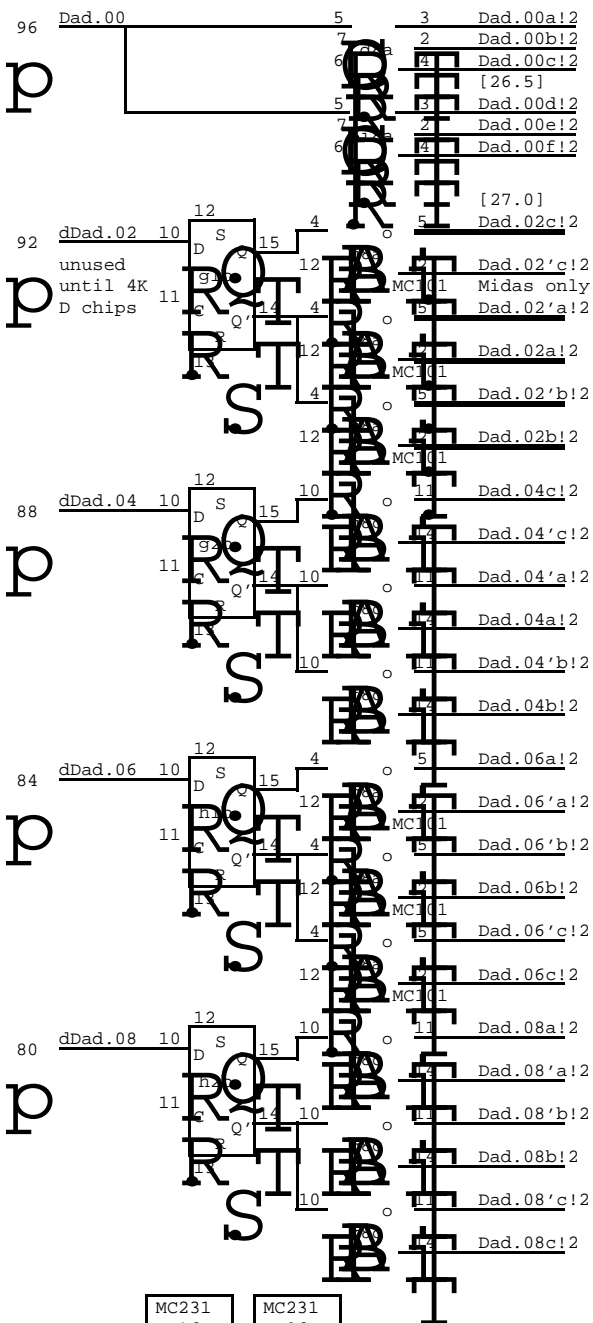
M e m o r y D a t a B o a r d

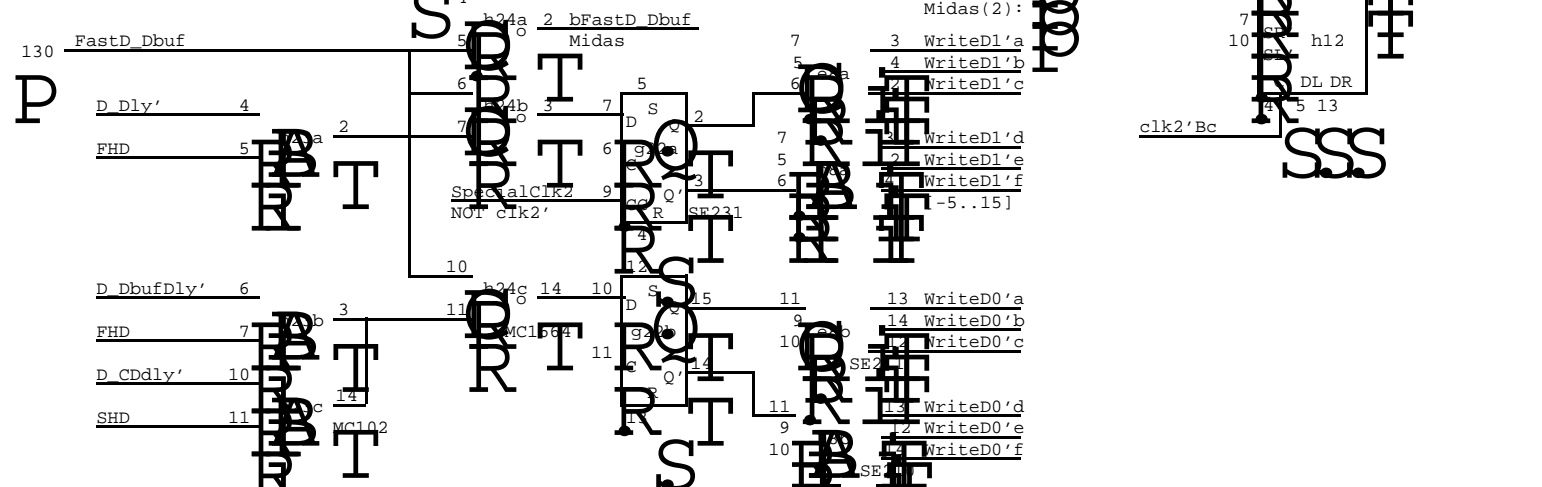
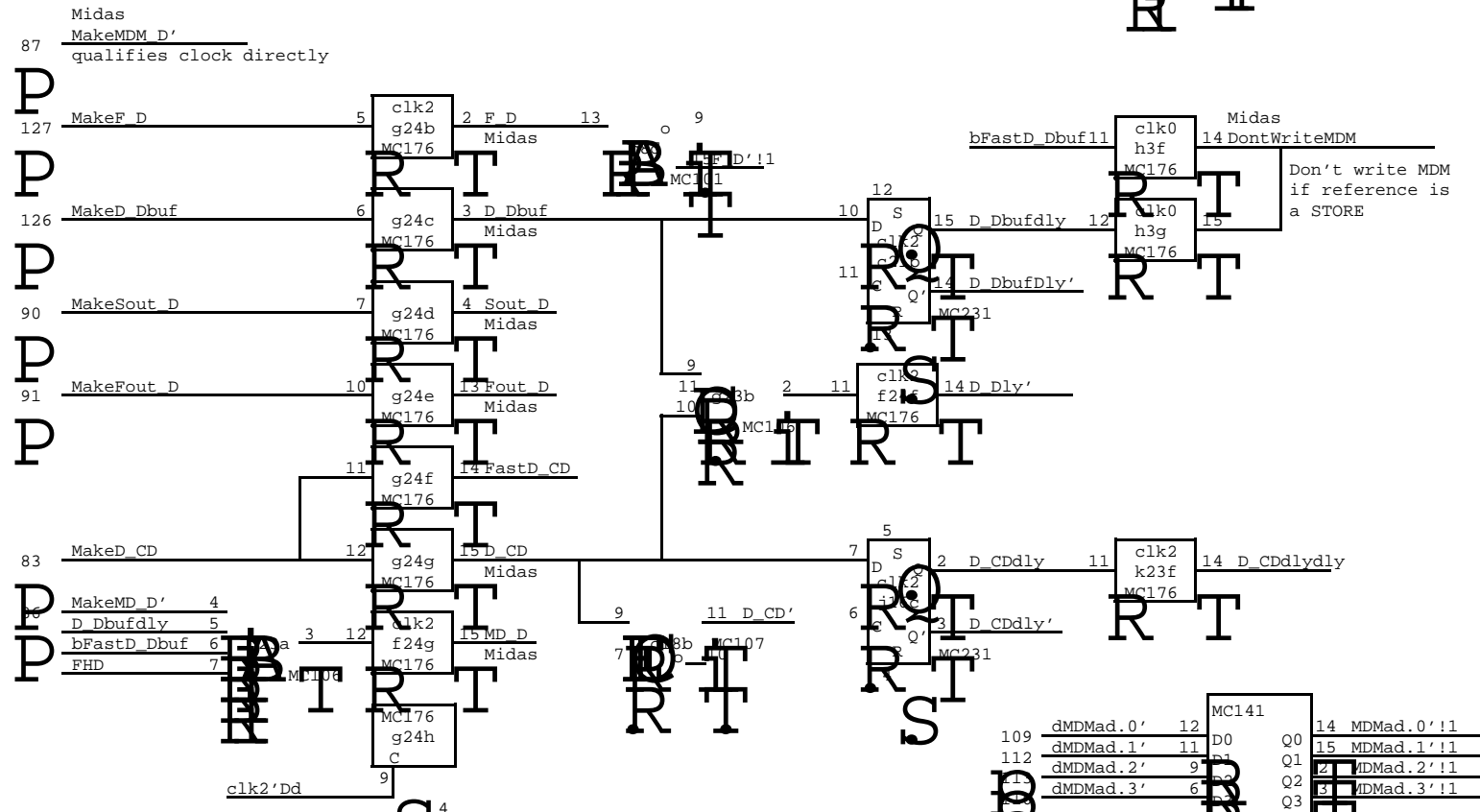
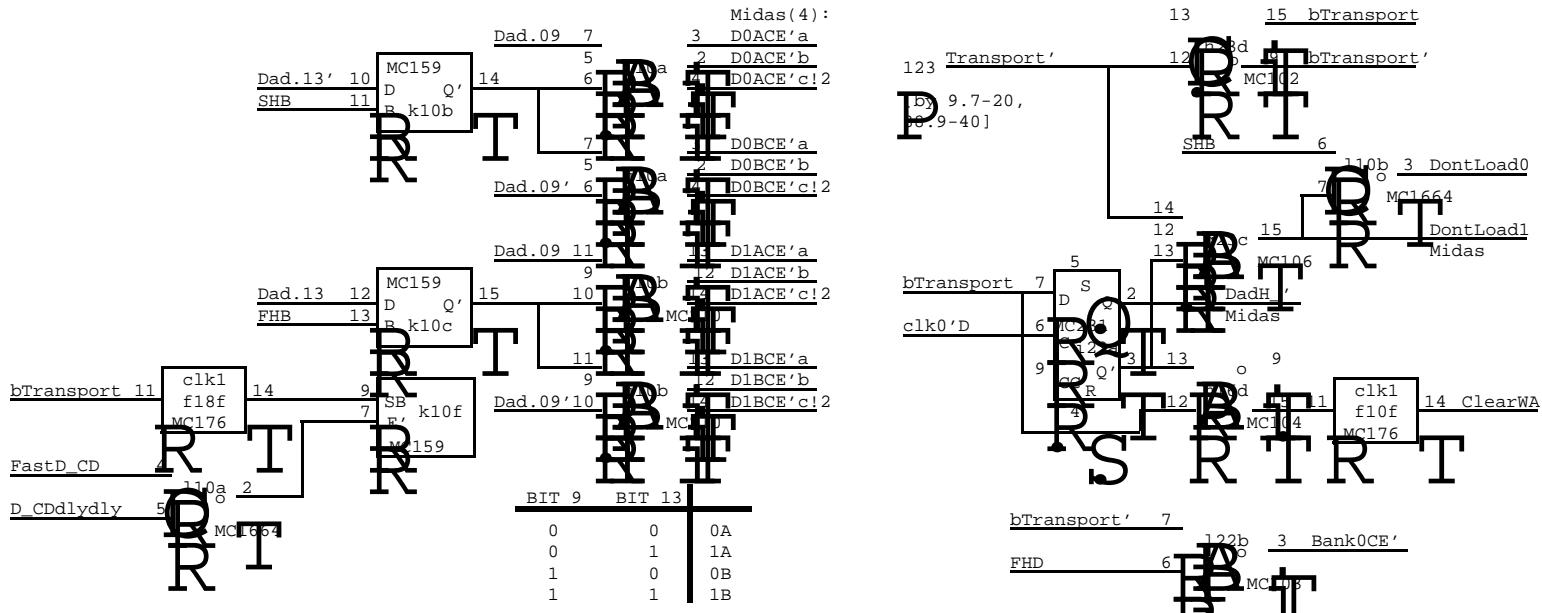
(1k chip version)

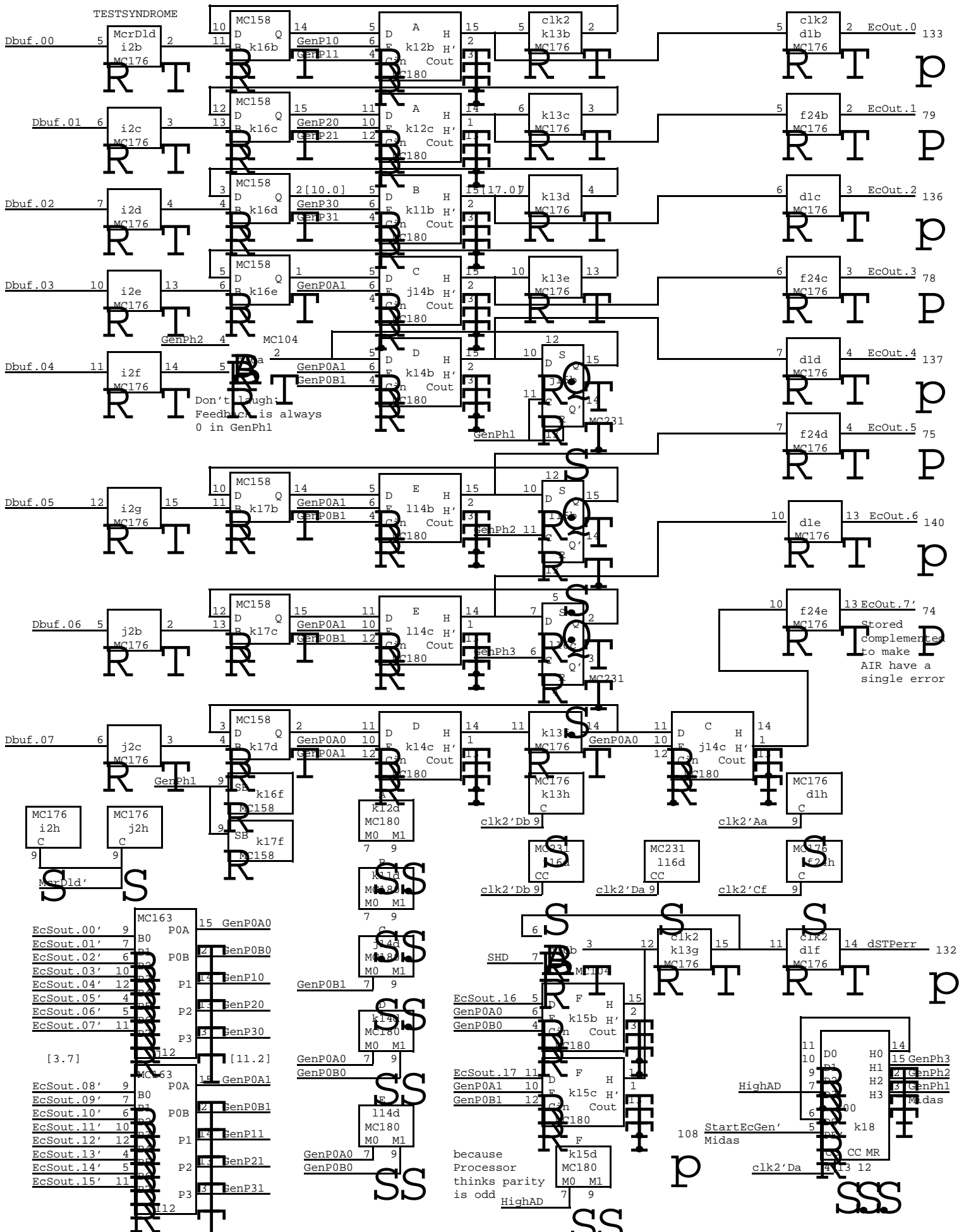
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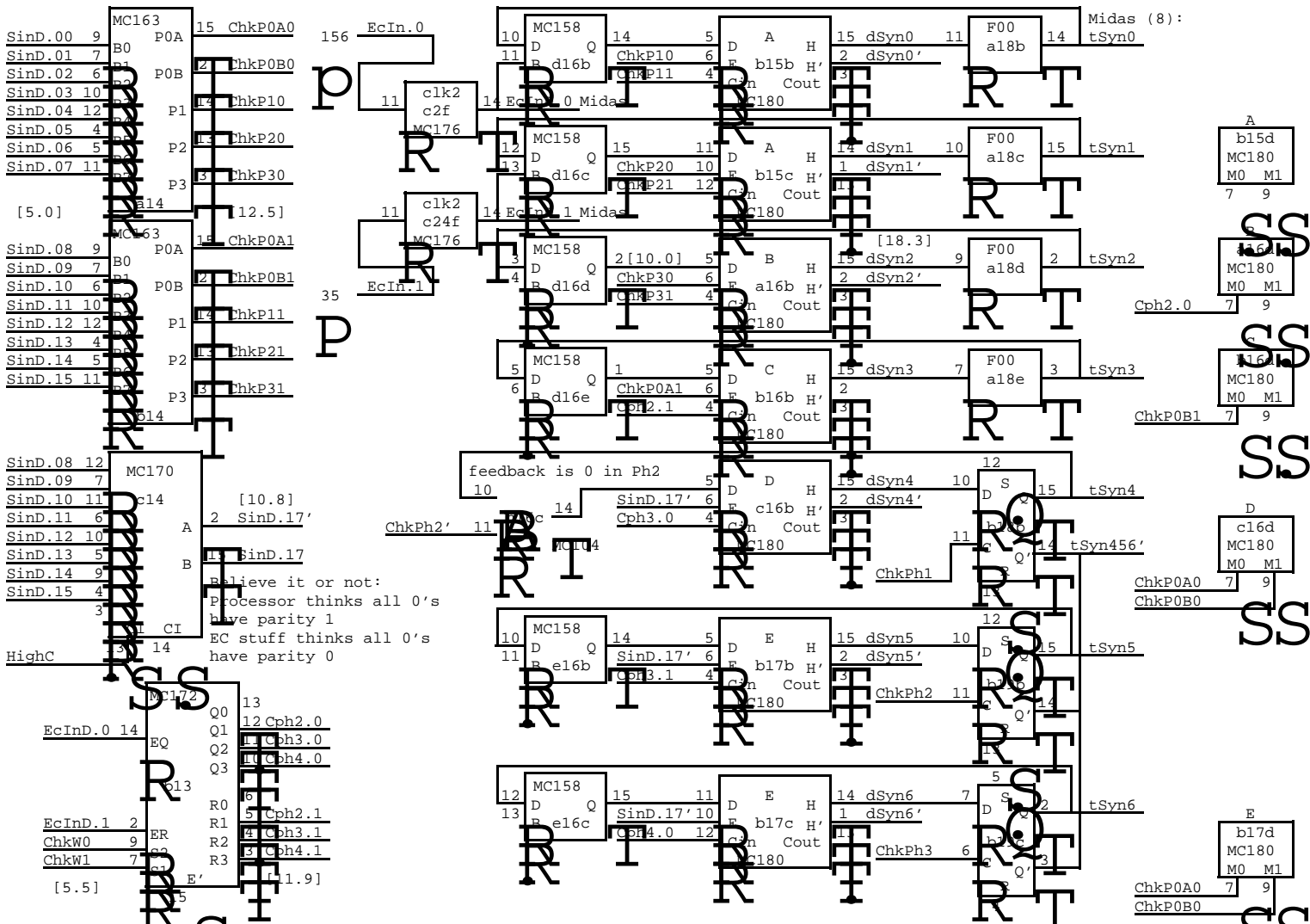
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Note: the MC180 is a dual 5-input xor gate, in which the M0 and M1 inputs are common.

Stored Ci are retrieved two at a time, and xored into the syndrome as they arrive. The Cph1.0/1 signals are the arriving Ci in the proper phase, 0 otherwise

MC163 operation

	0	1	2	3	4	5	6	7
P1		x	x		x		x	
P2			x	x		x	x	
P3					x	x		x
P0A	x	x		x				
P0B	x			x	x			

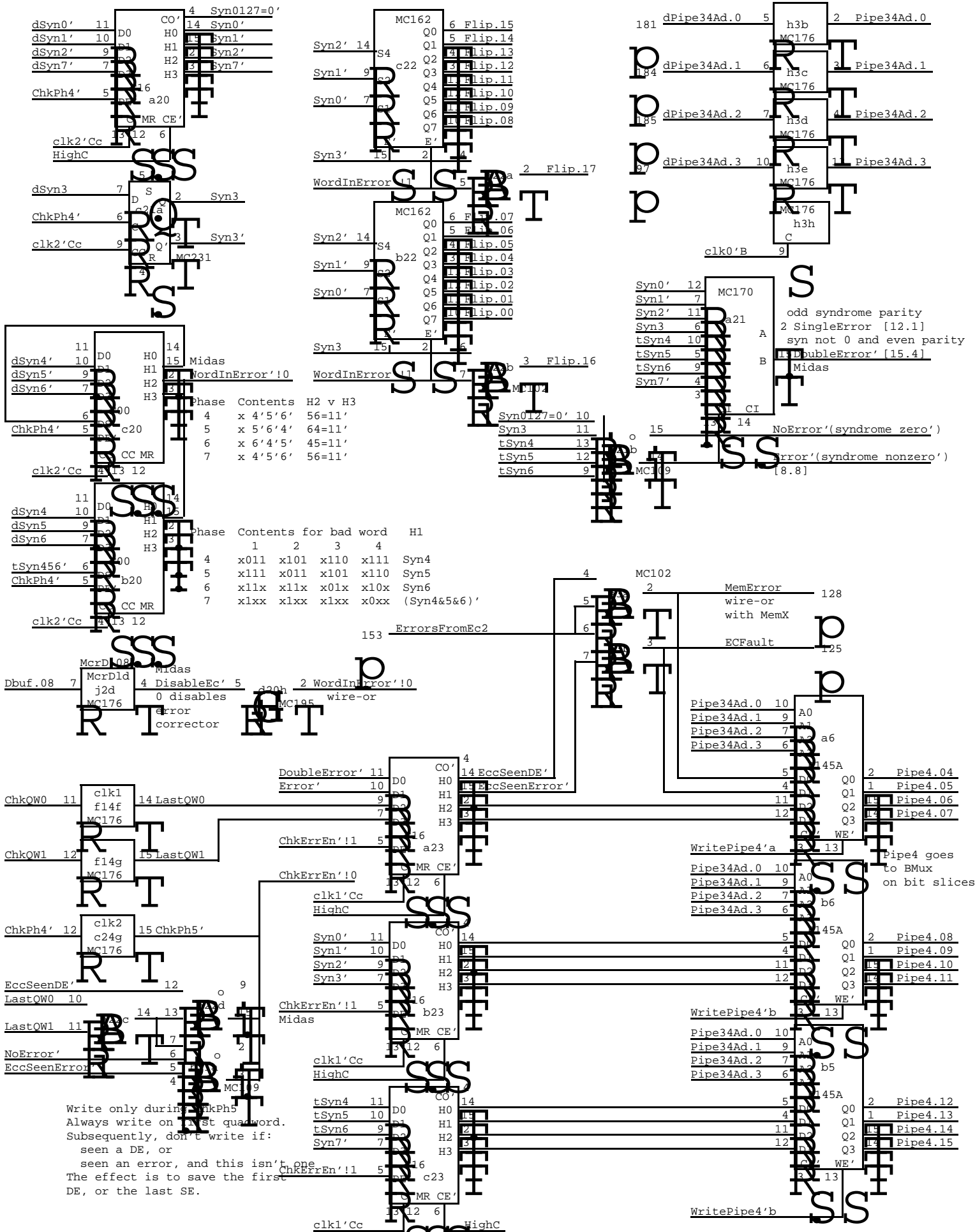
EC code being used:

	0	1	2	3	4	5	6	7
C0		x		x		x		
C1			x	x				
C2					x			
C3						x		
C4							x	
C5	x	x	x	x	x	x	x	
C6	x	x	x	x	x	x	x	
C7	x							

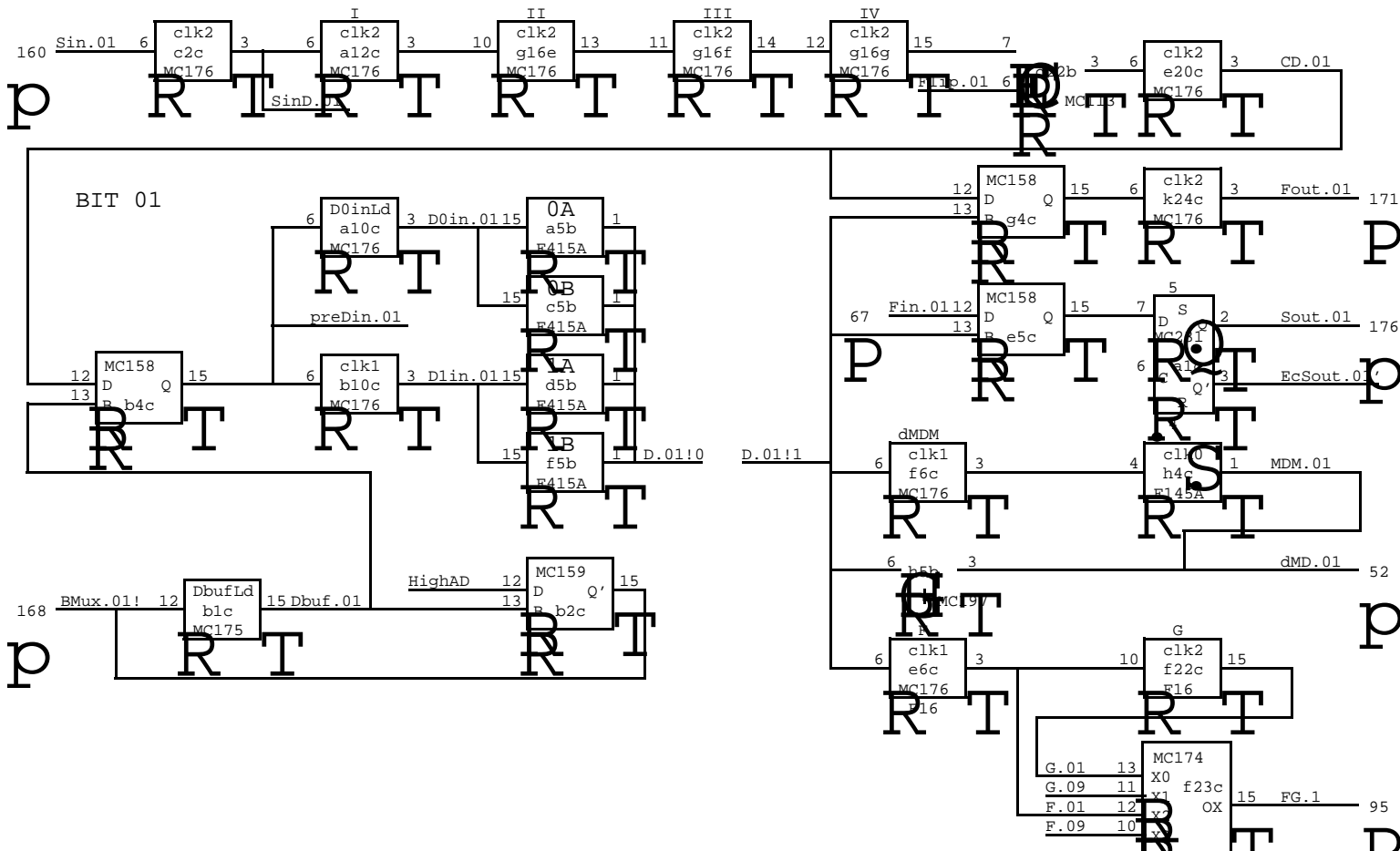
Syndrome is xor of retrieved Ci and Ci computed on retrieved data. Hence it is the Ci for the error pattern, and the following facts follow from looking at the pictures, which show the Ci for single-bit patterns. Syn0-3 point to erroneous bit. Syn4-6 point to bad word with a 2-out-of-3 code:

word	1	011
word 2	101	
word 3	110	
word 4	111	

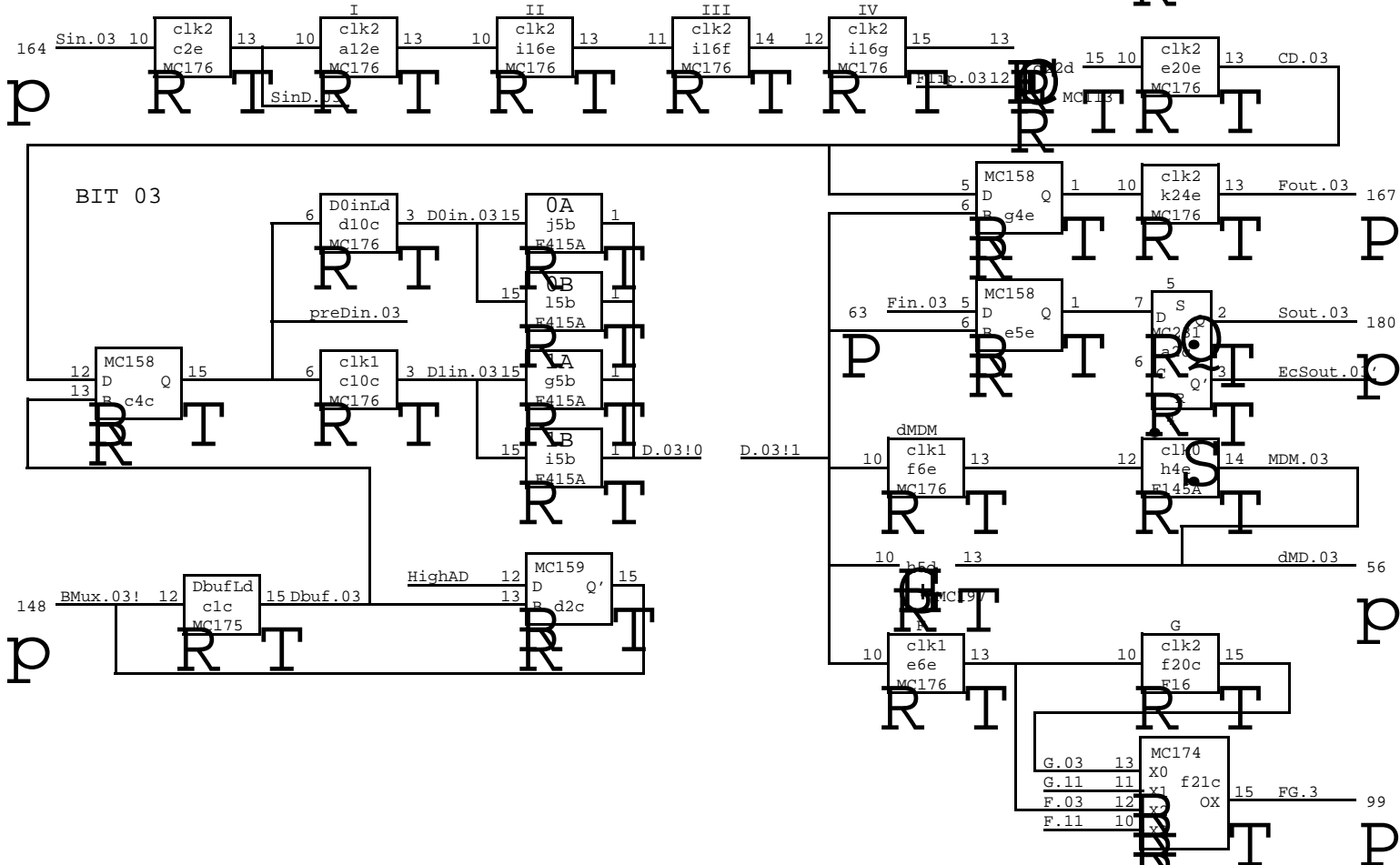
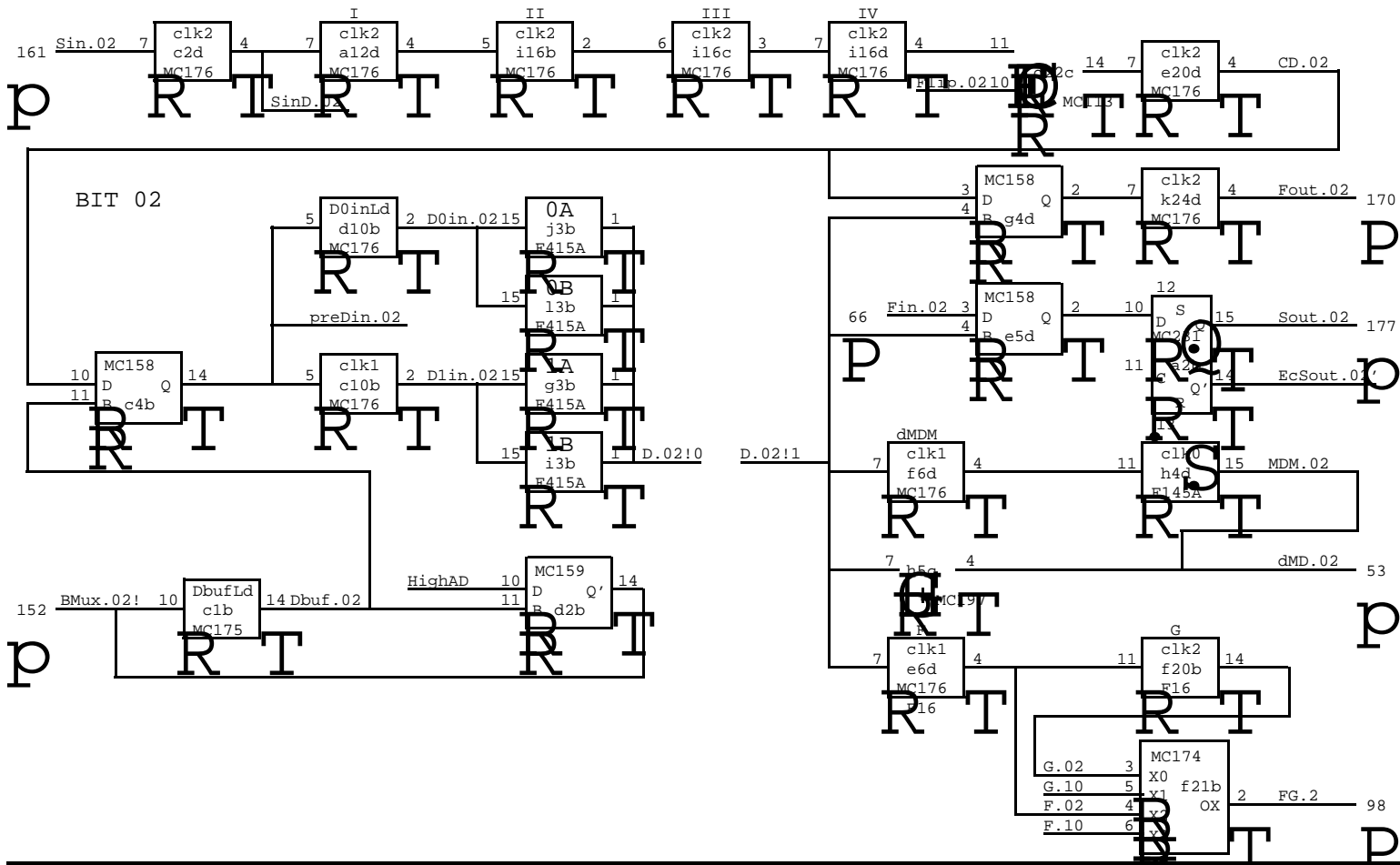
A single-bit error in Ci cannot yield two 1's in C456. C7 is computed so that parity of C0-7 is odd for any data with exactly one 1. Hence parity of Syn0-7 will be odd for any single bit error.

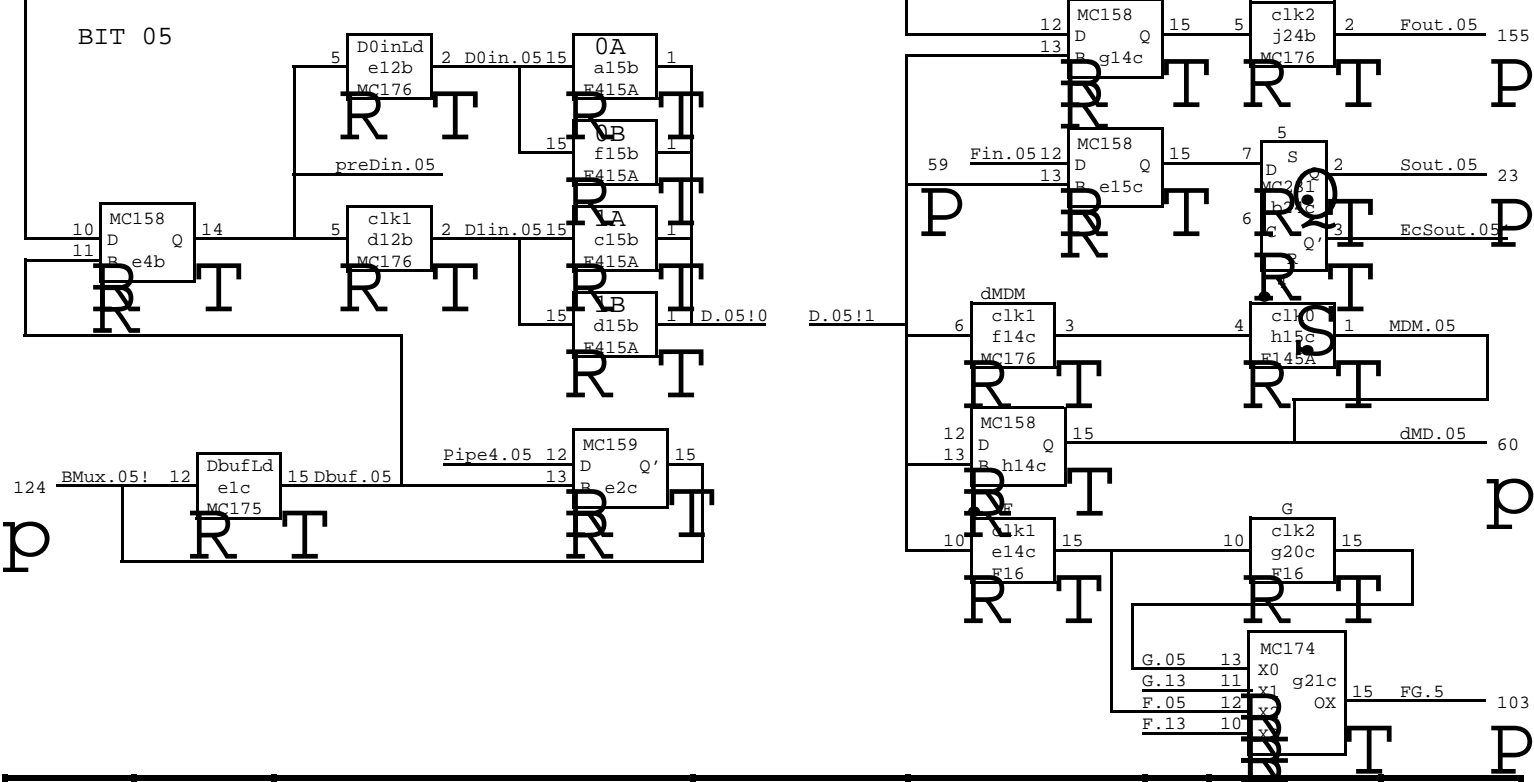
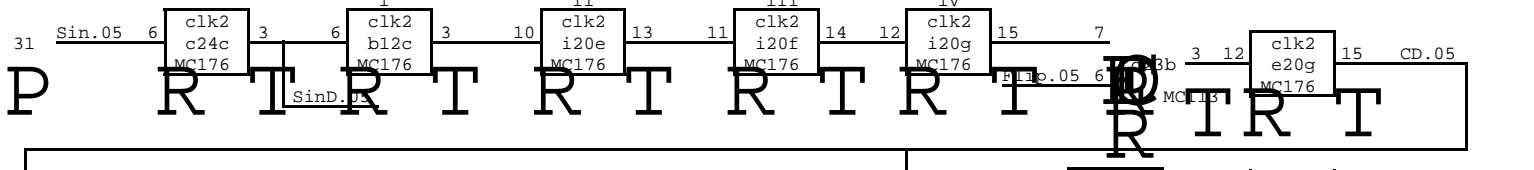
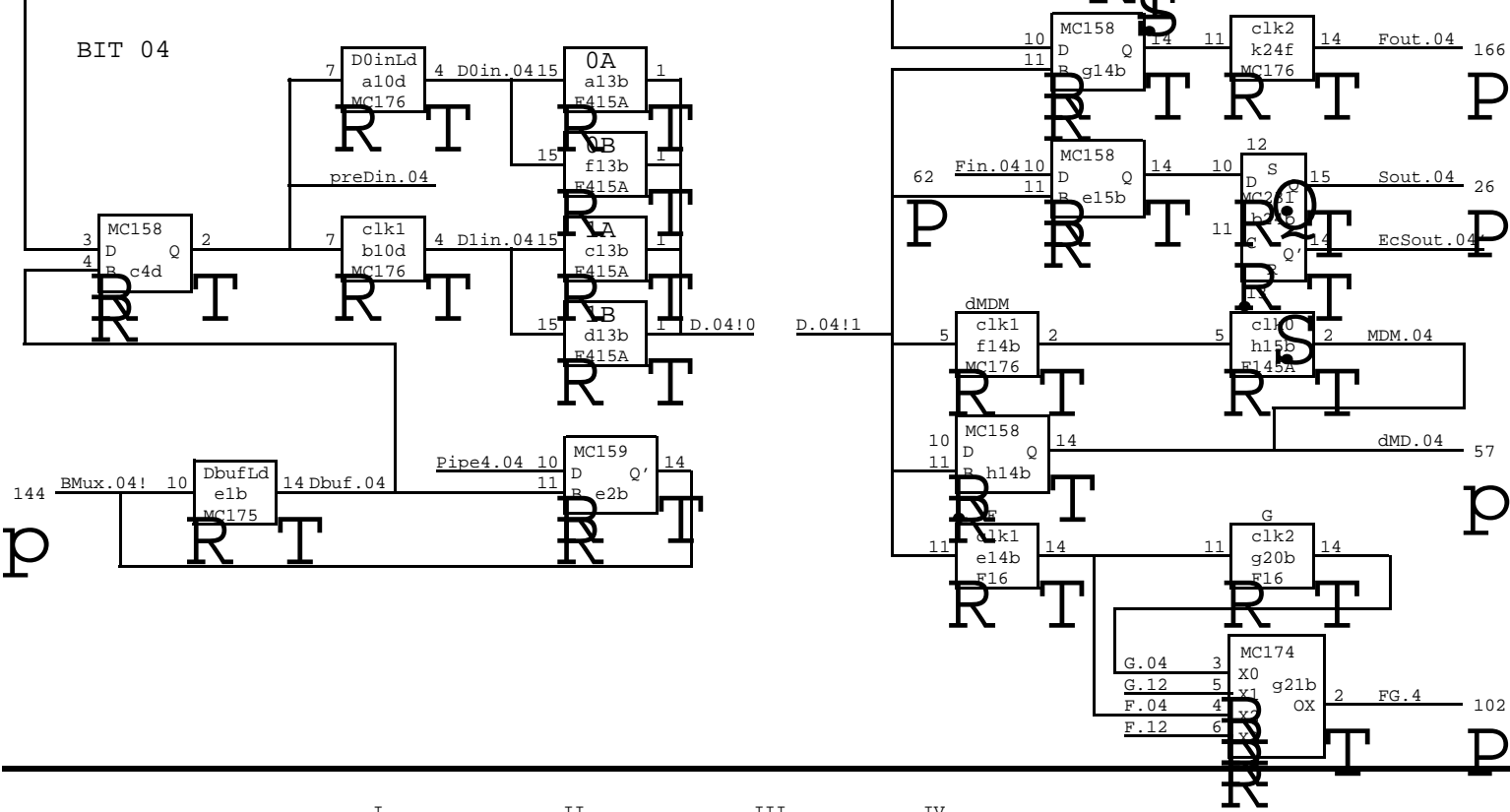
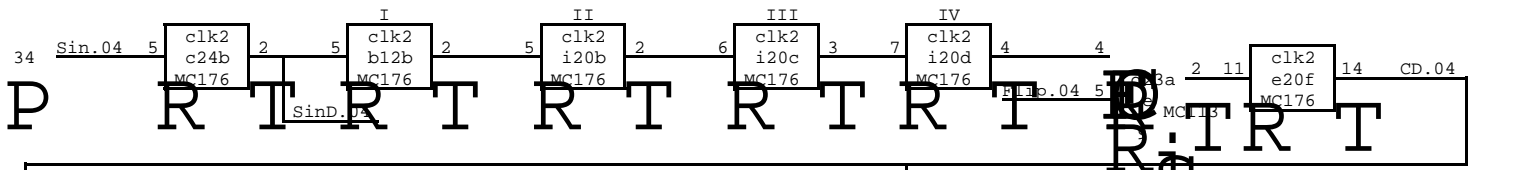


Bit 00 is on page 2

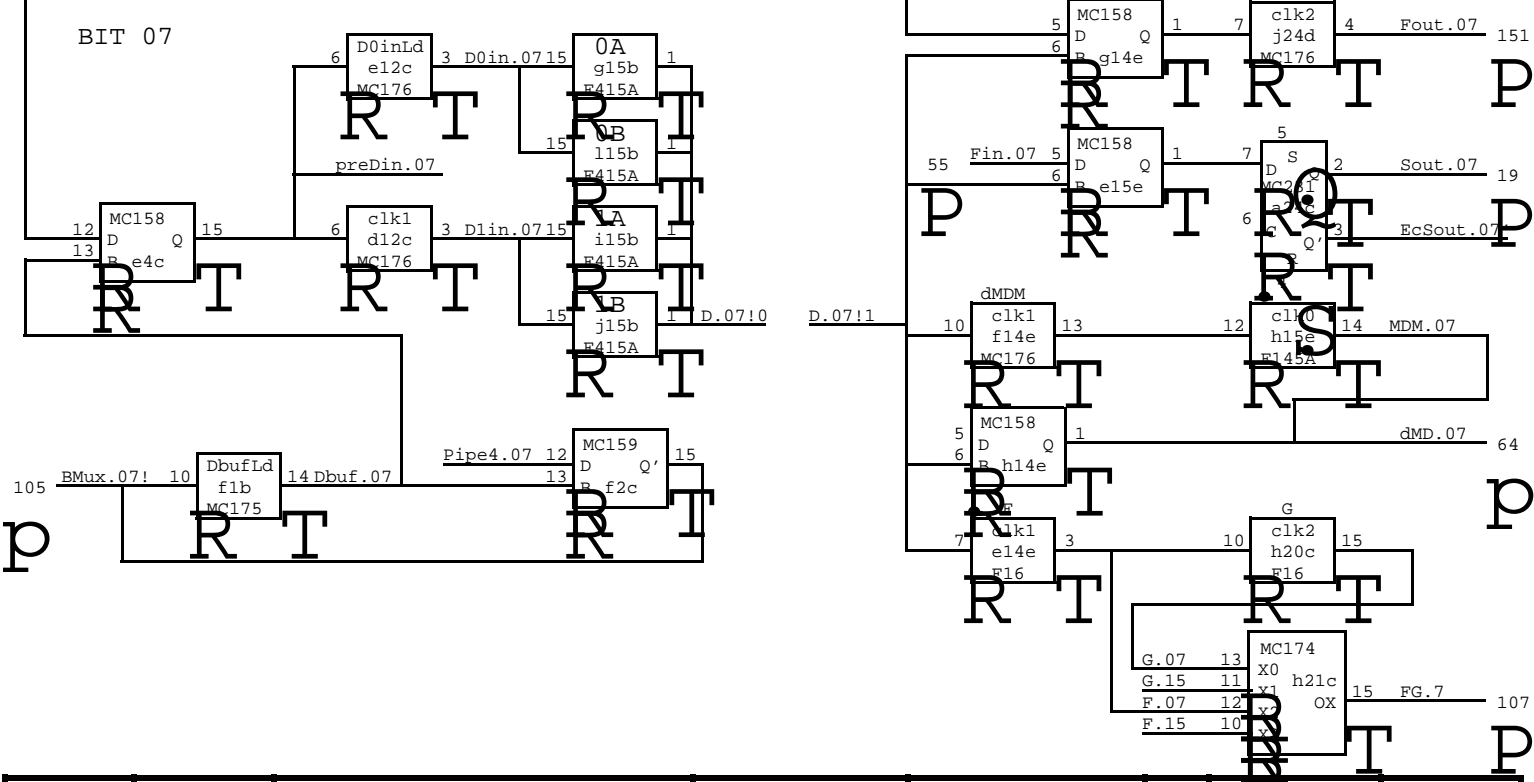
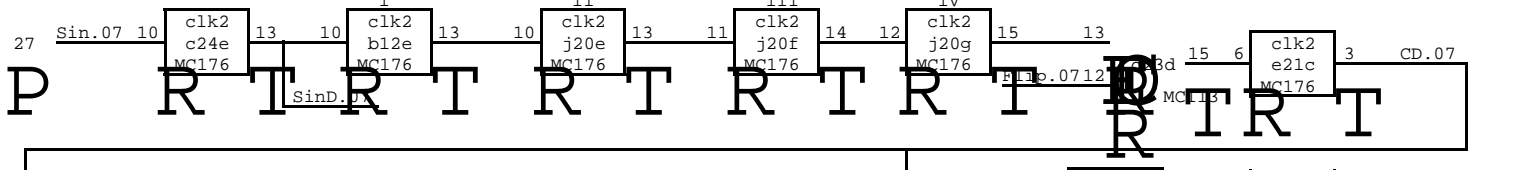
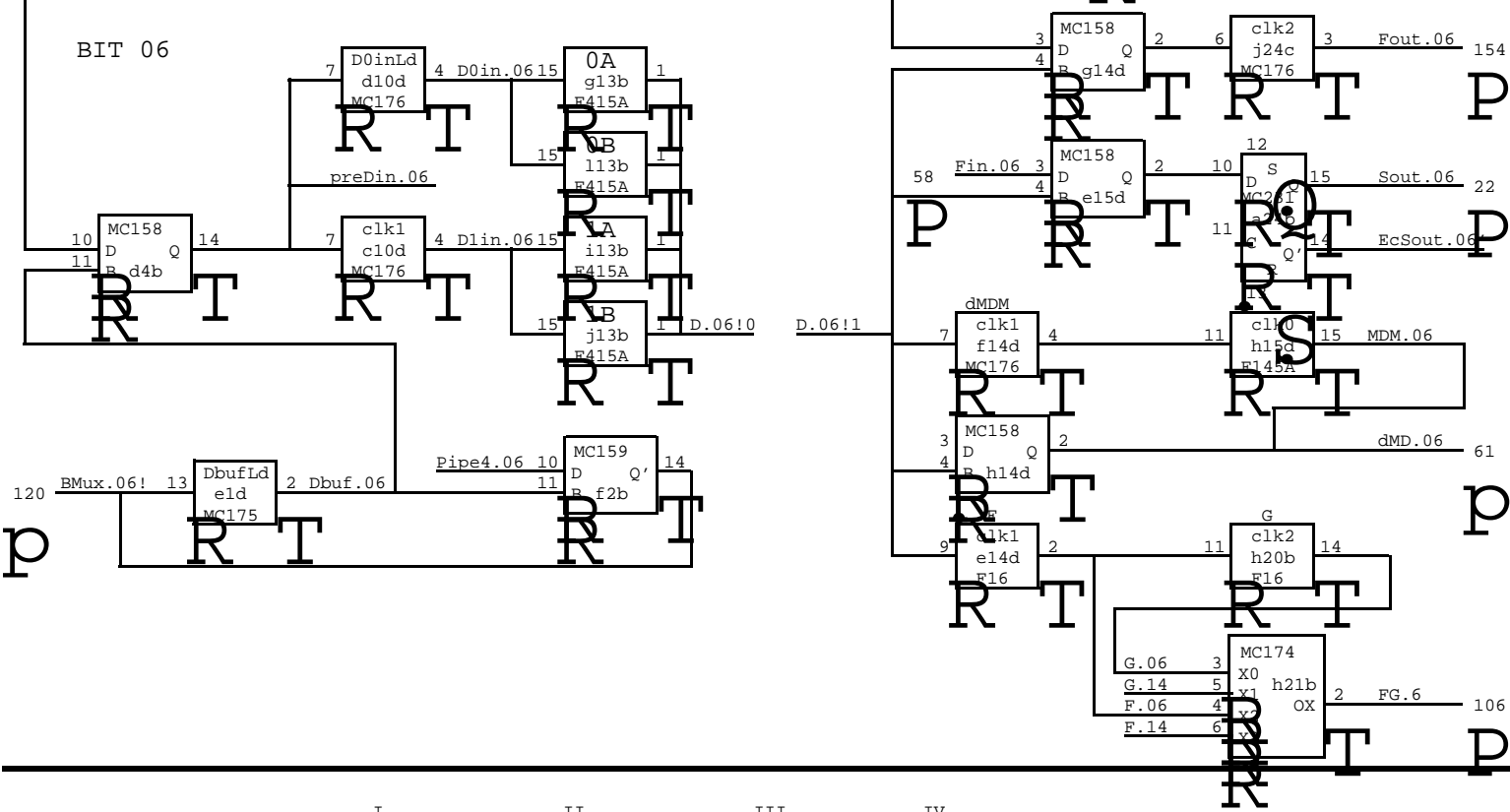
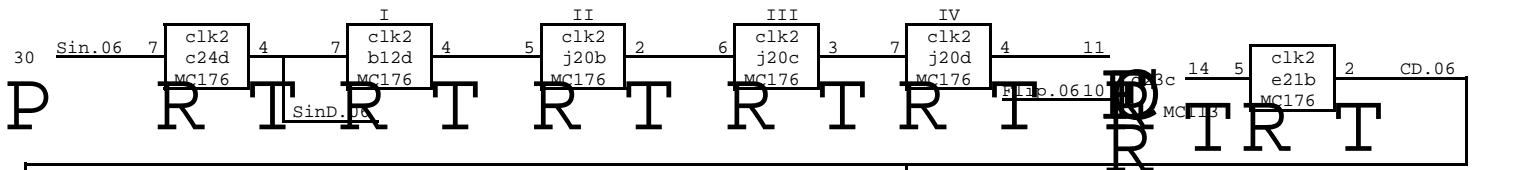


XEROX PARC/CSL	Project Dorado	Memory data board Bit slice 01	File MemD07.sil	Designer D. Clark	Rev Be	Date 7/09/79	Page 07
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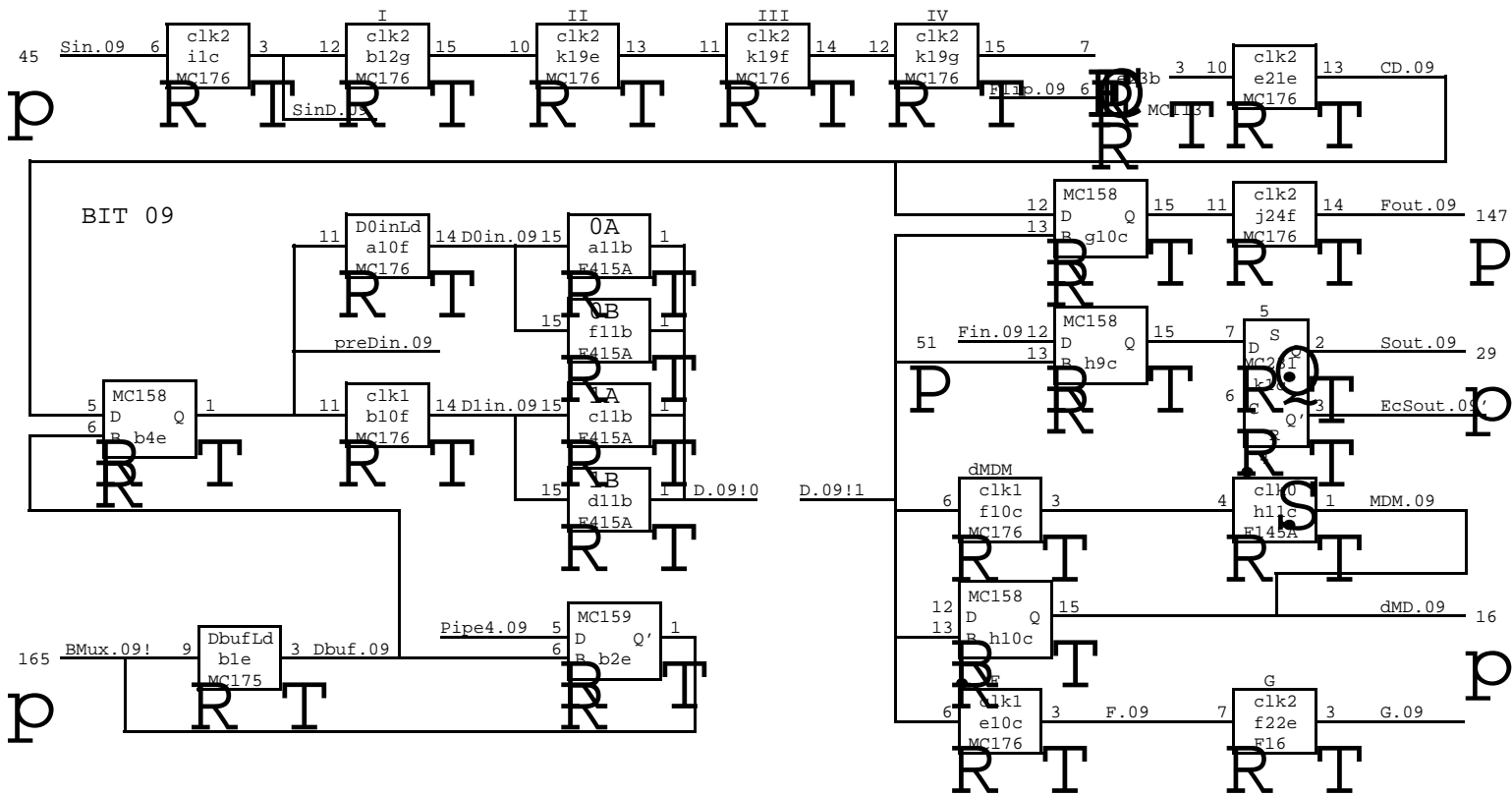
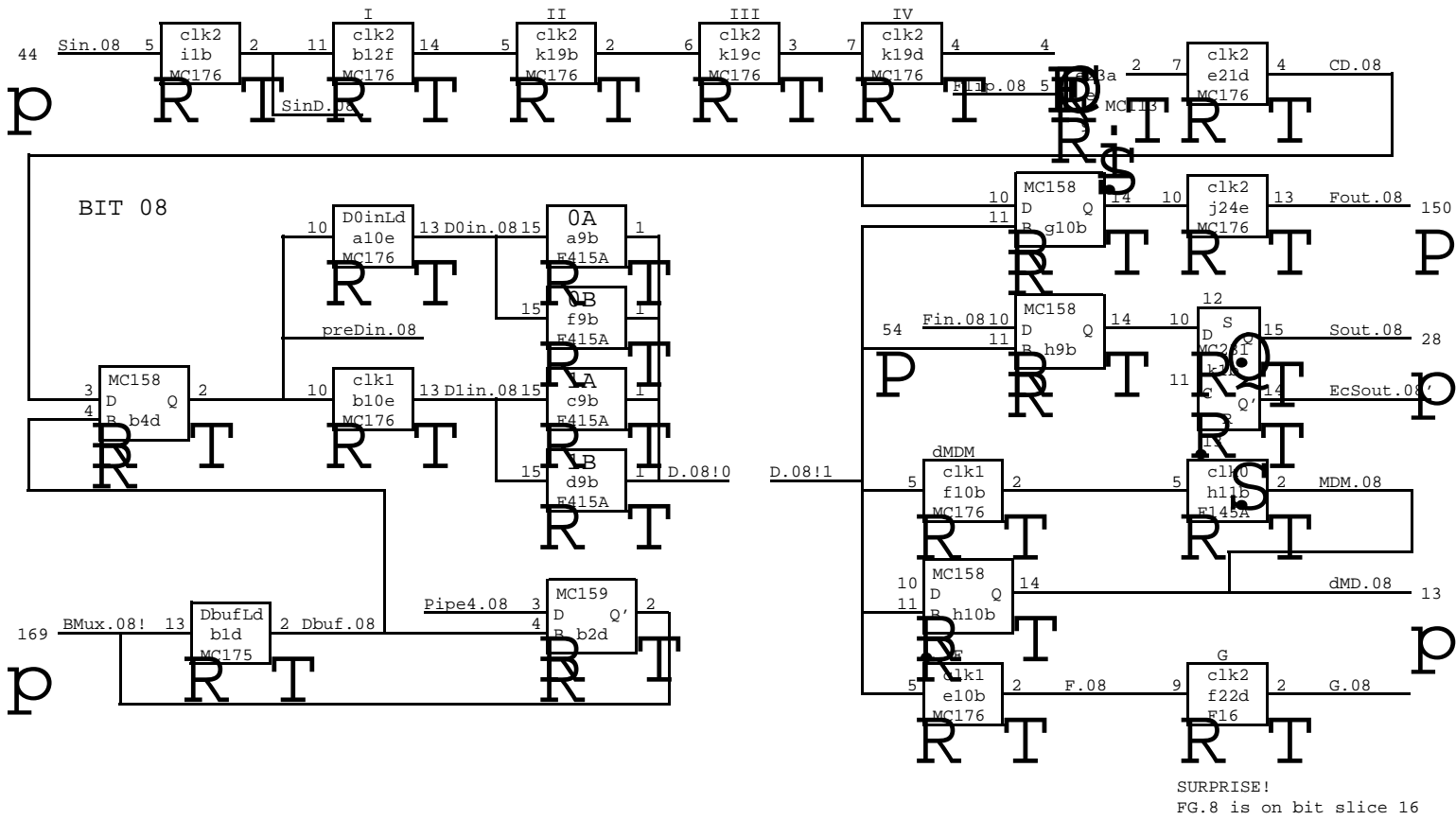




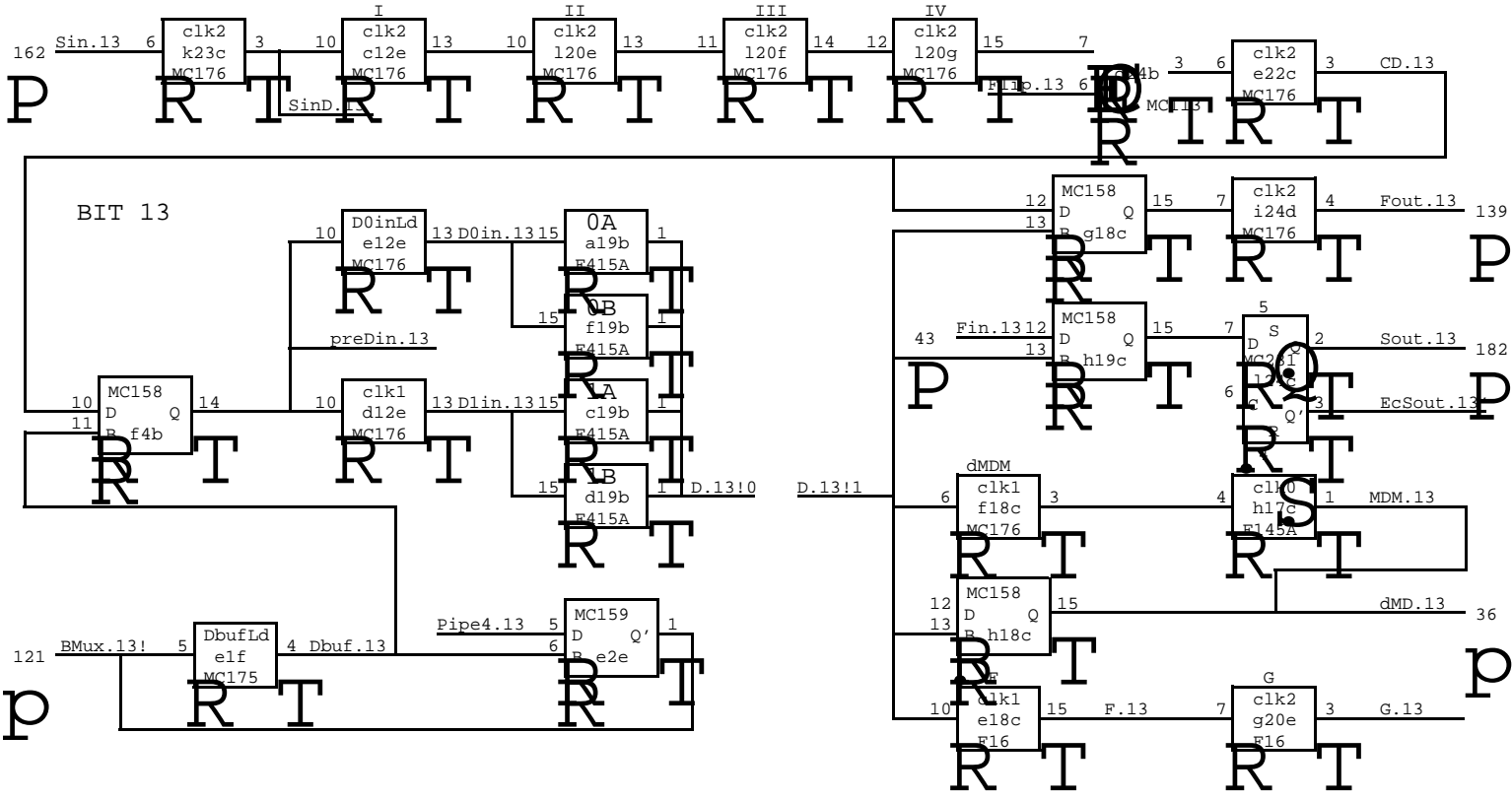
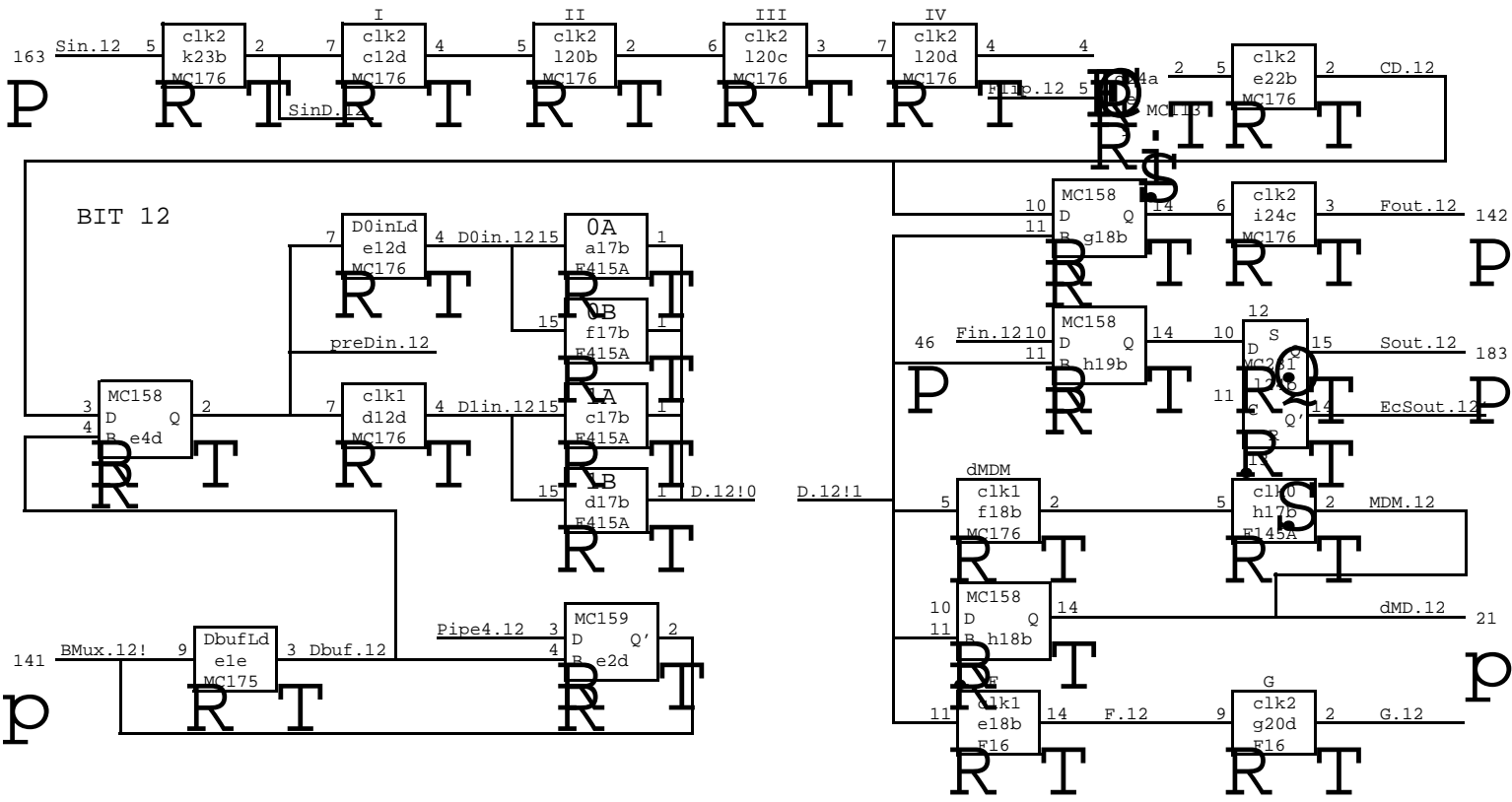
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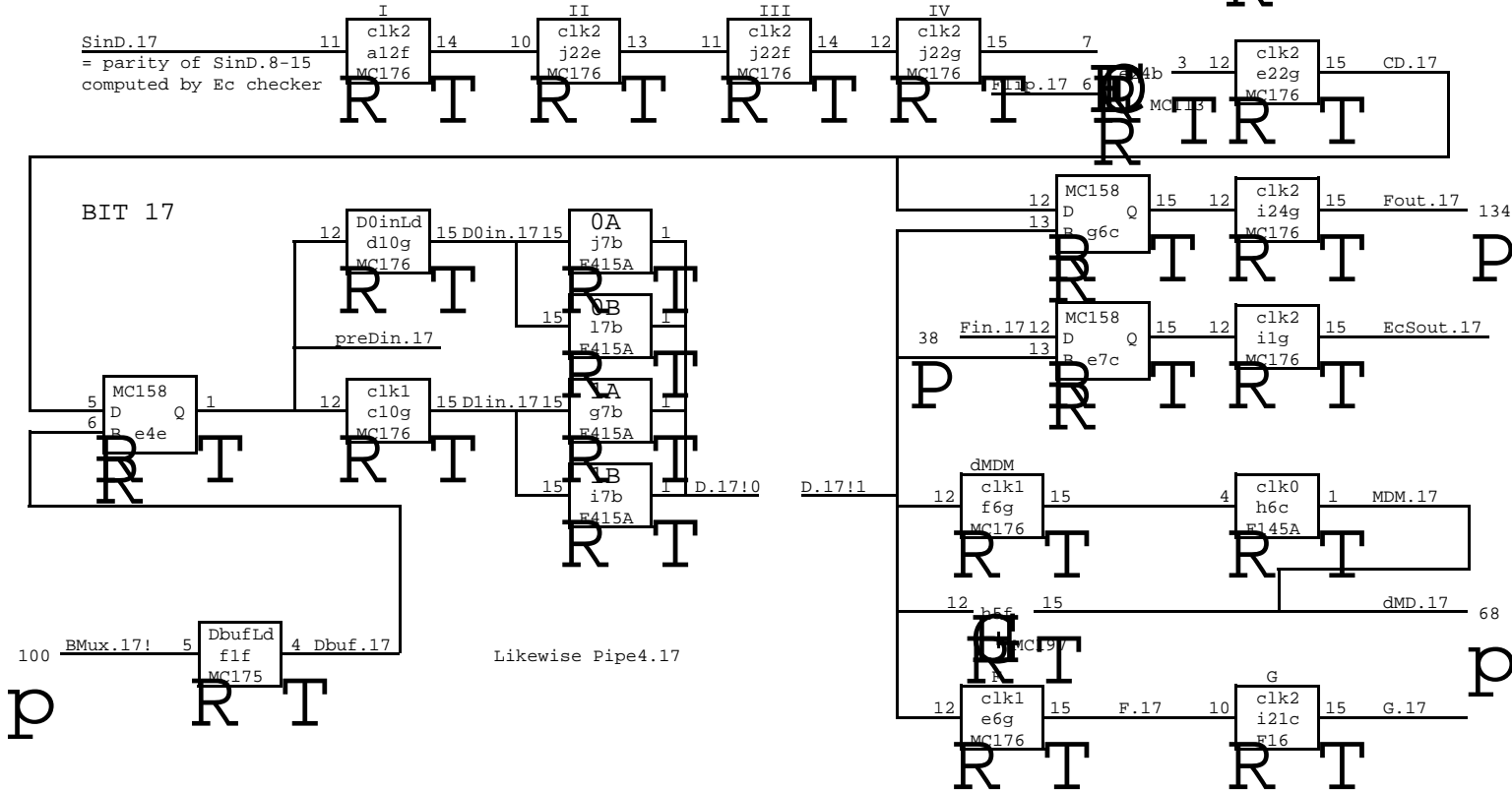
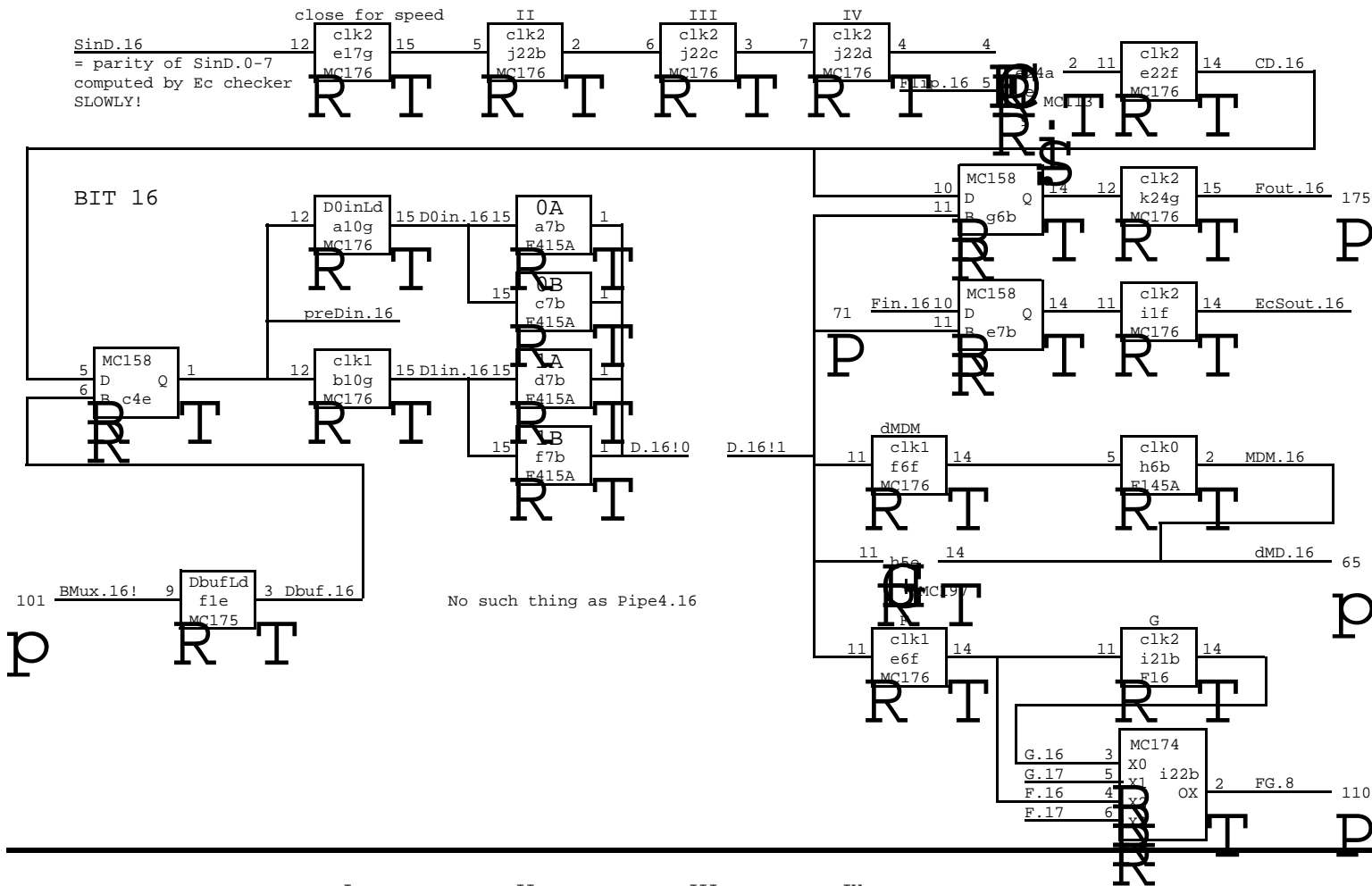


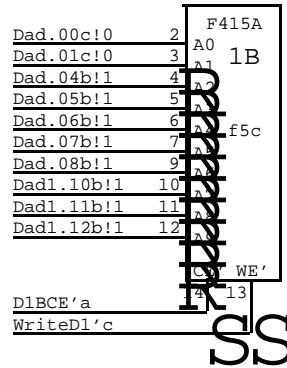
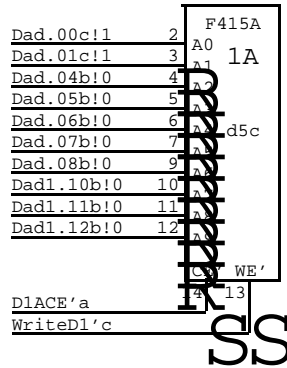
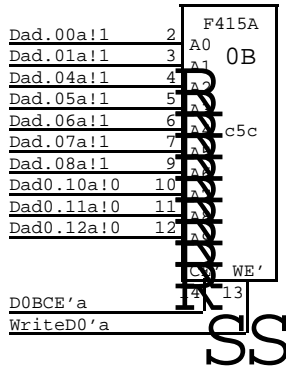
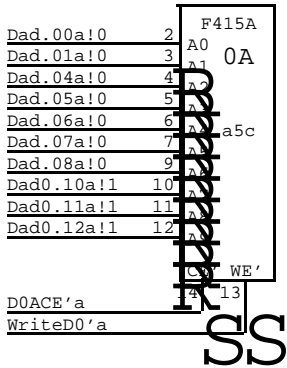
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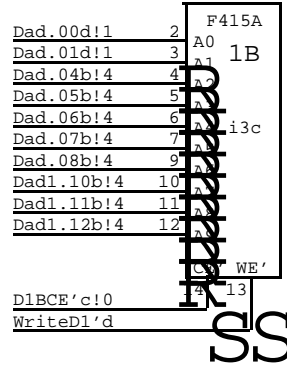
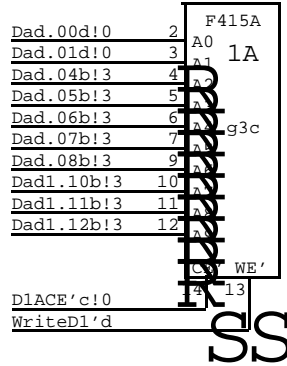
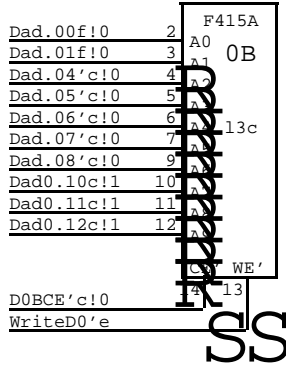
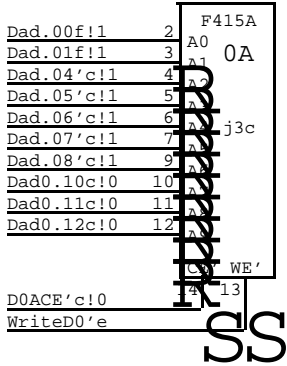
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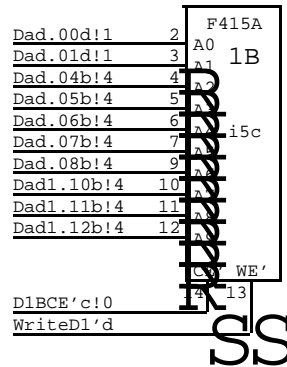
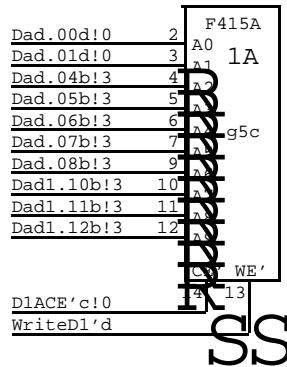
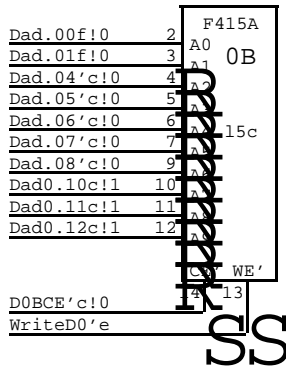
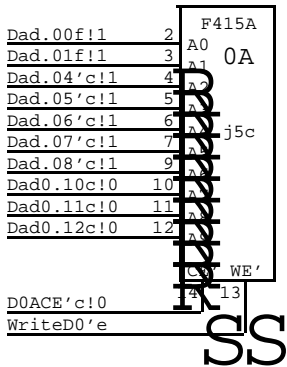




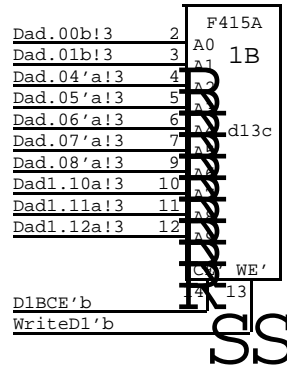
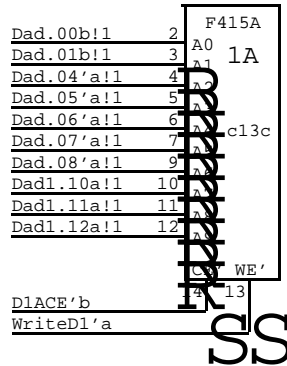
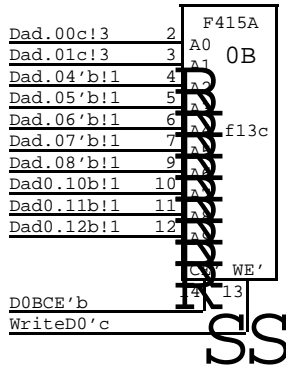
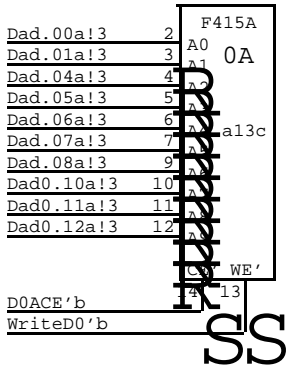
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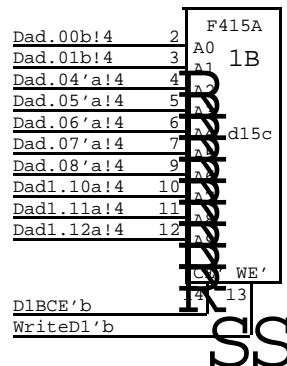
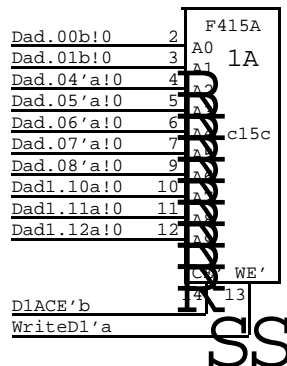
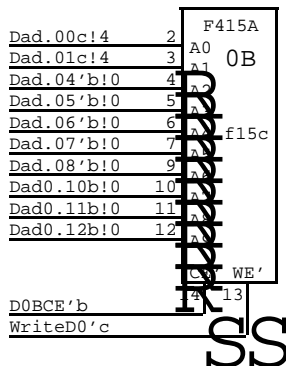
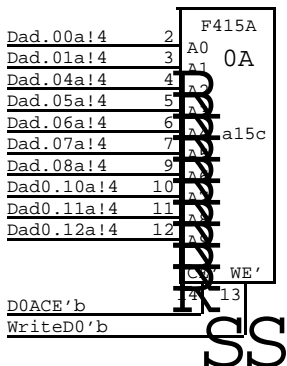
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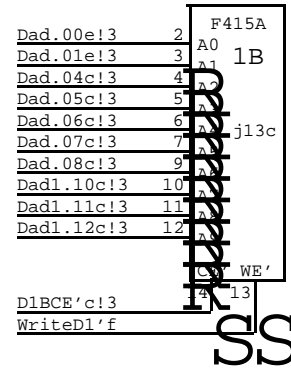
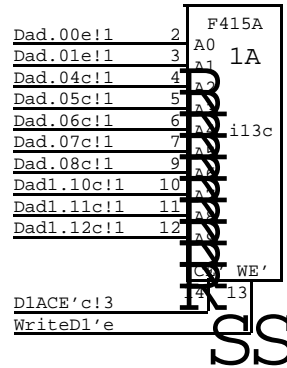
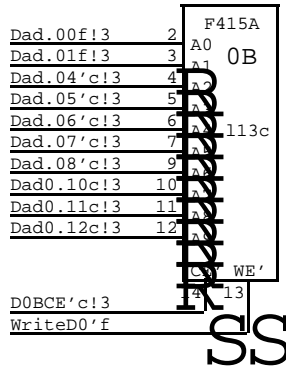
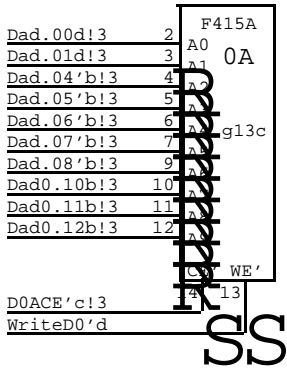
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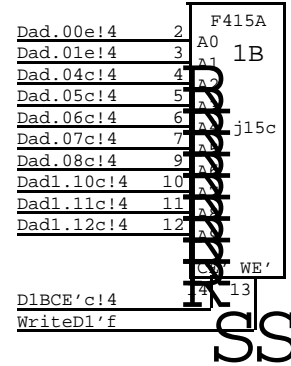
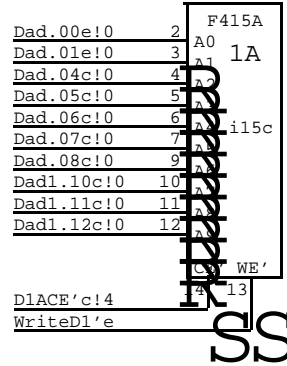
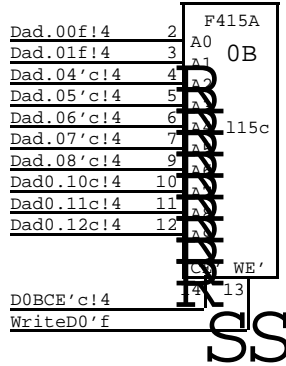
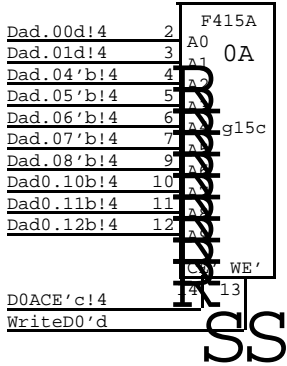
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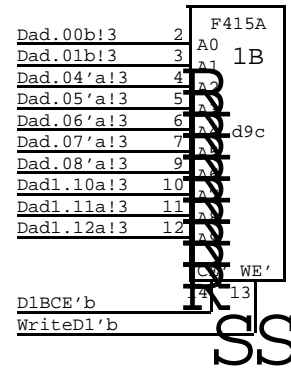
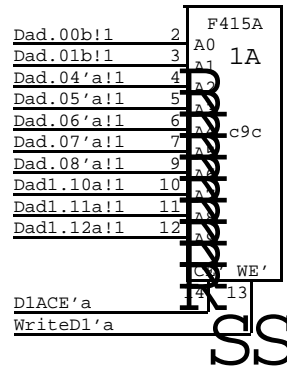
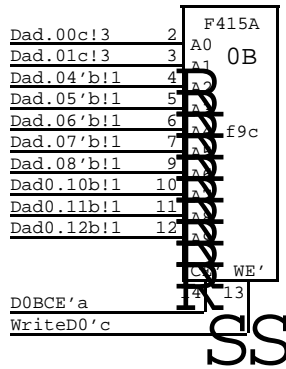
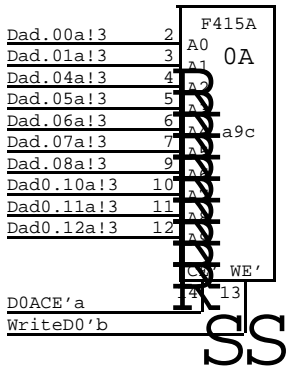
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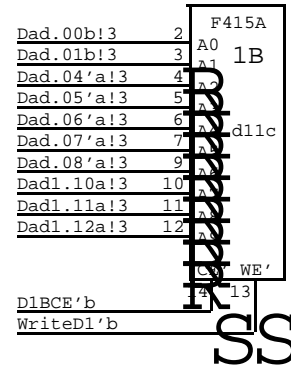
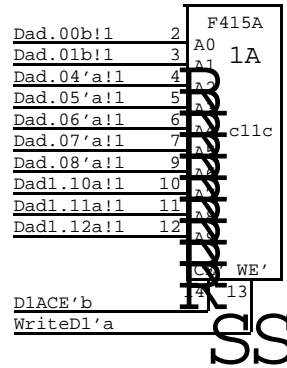
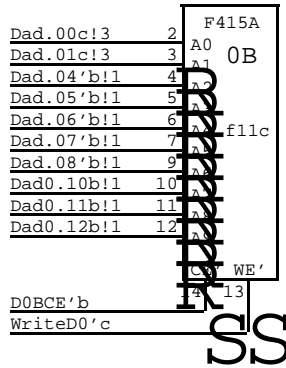
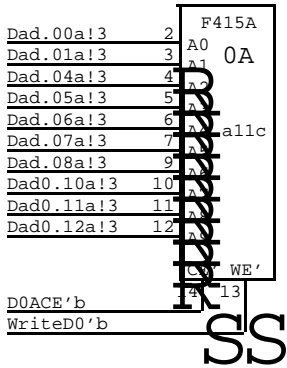
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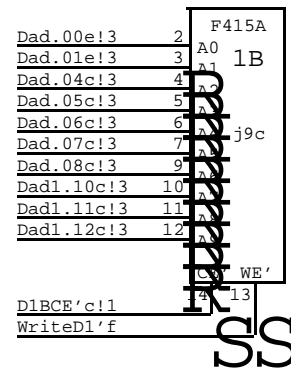
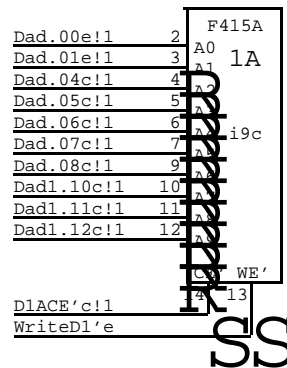
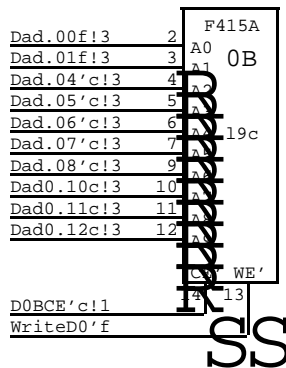
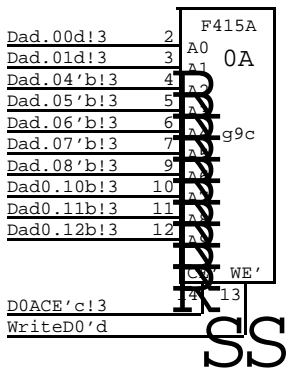
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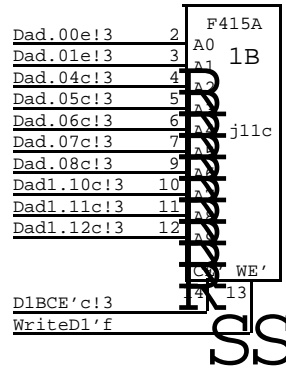
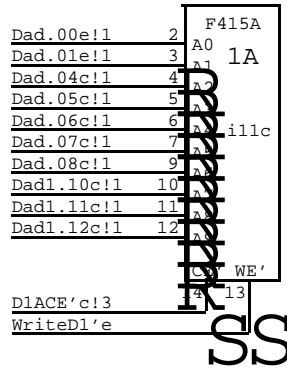
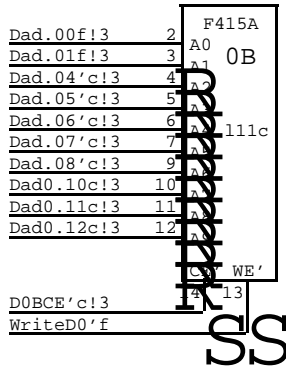
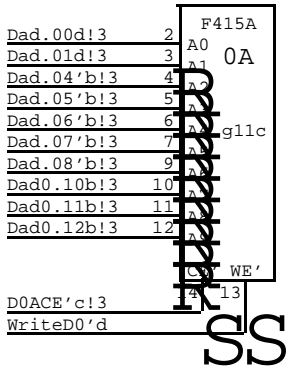
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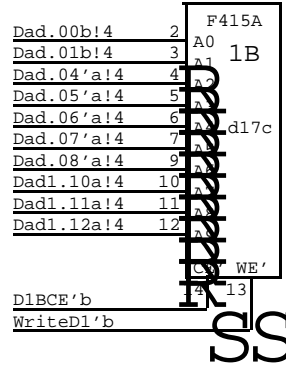
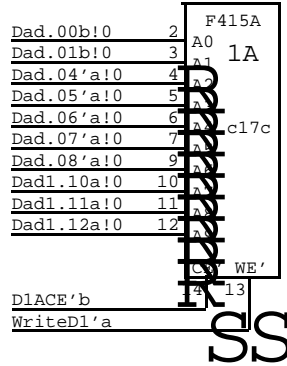
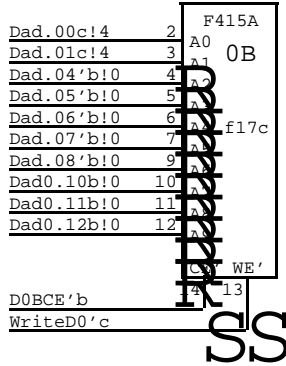
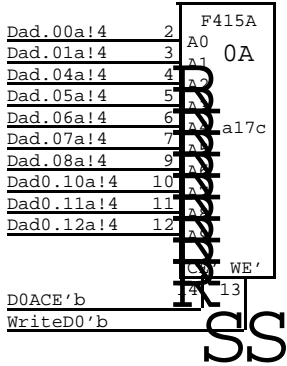
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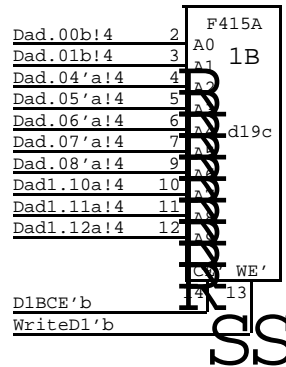
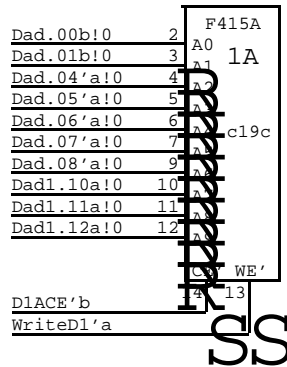
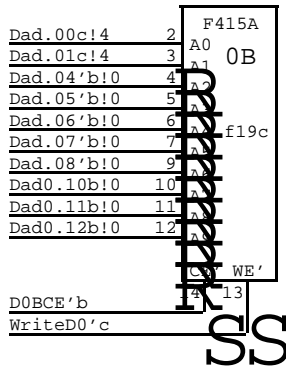
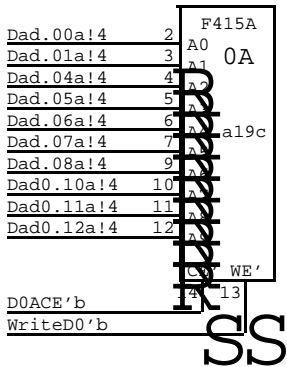
BIT 10



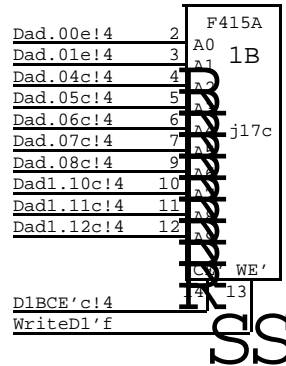
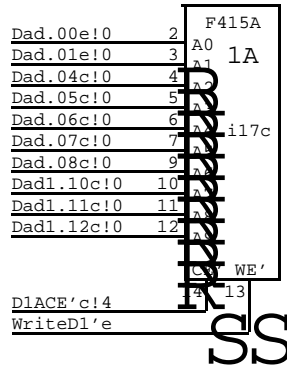
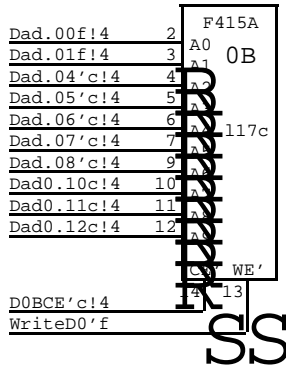
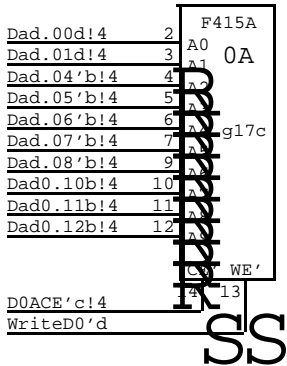
BIT 11



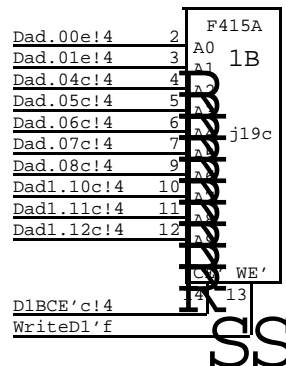
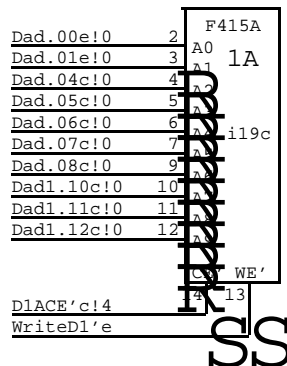
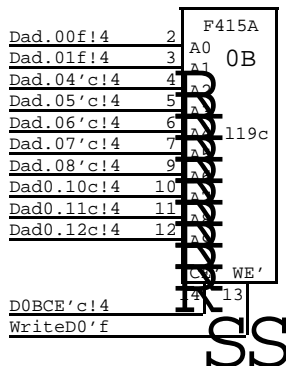
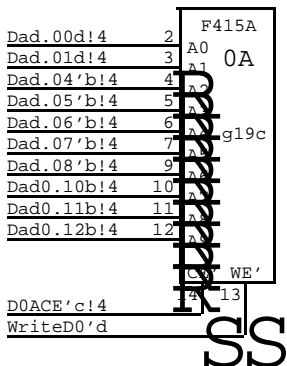
BIT 12



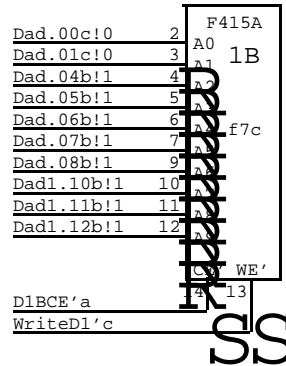
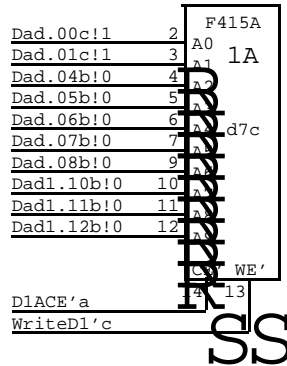
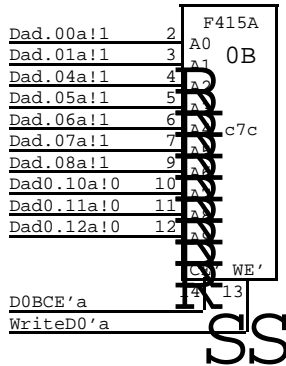
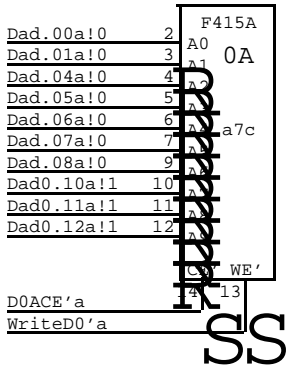
BIT 13



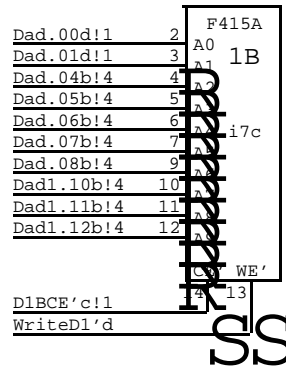
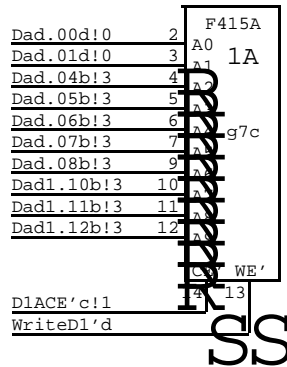
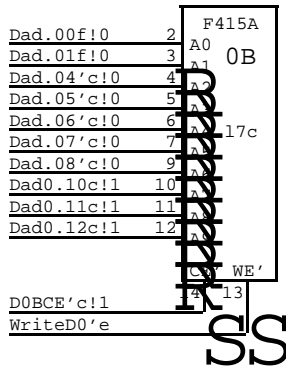
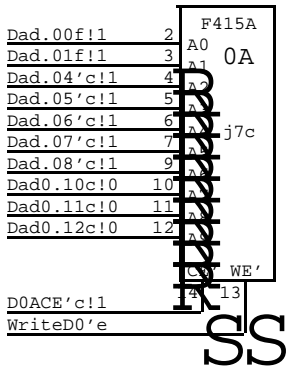
BIT 14



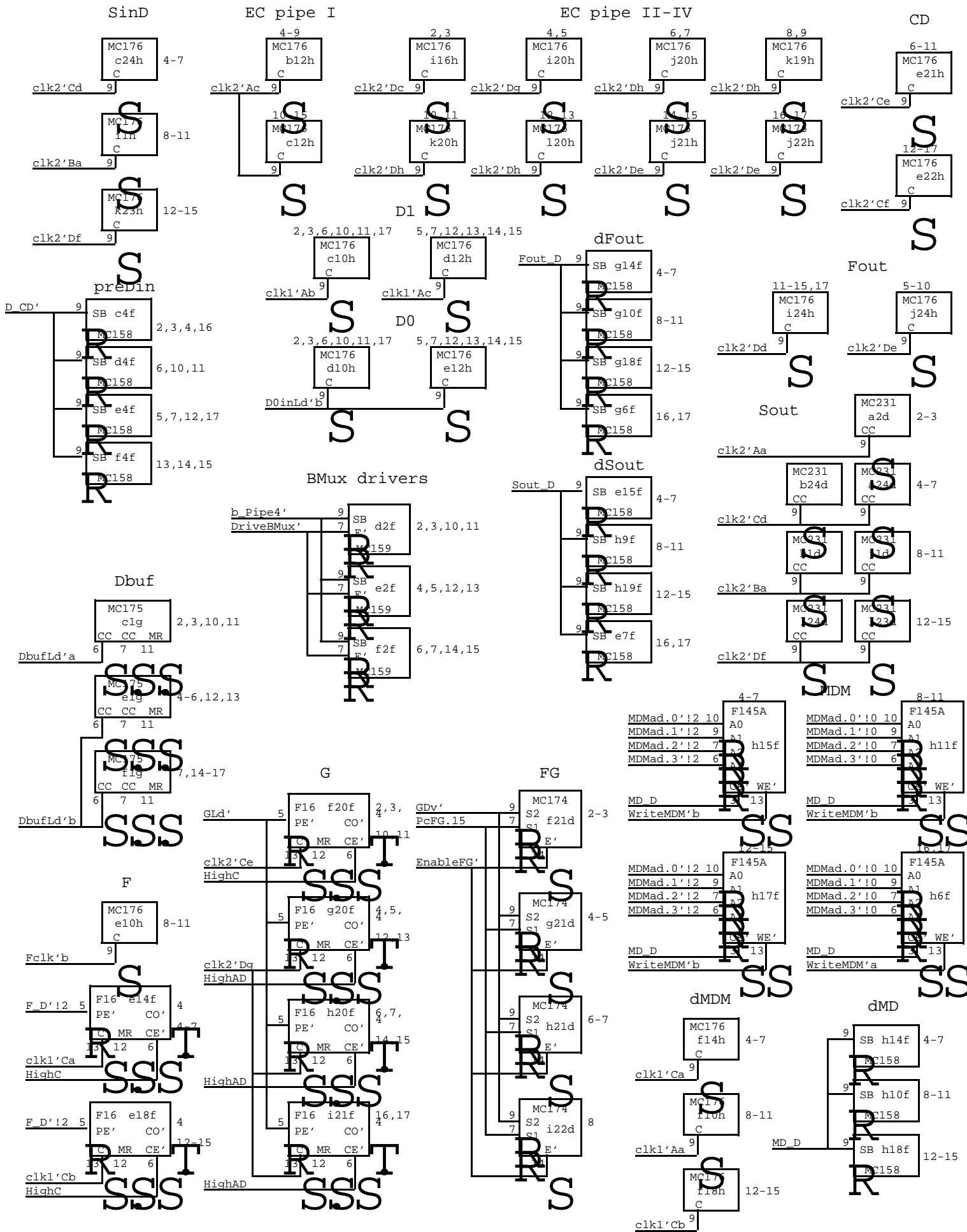
BIT 15



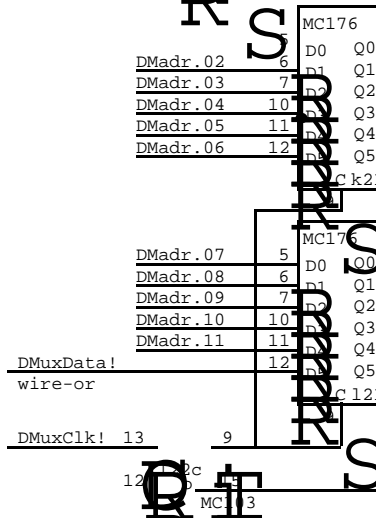
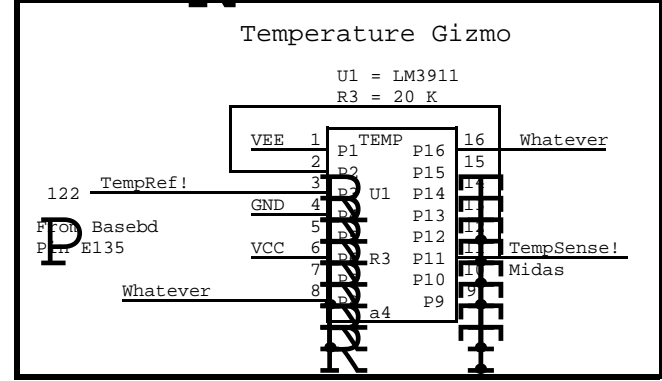
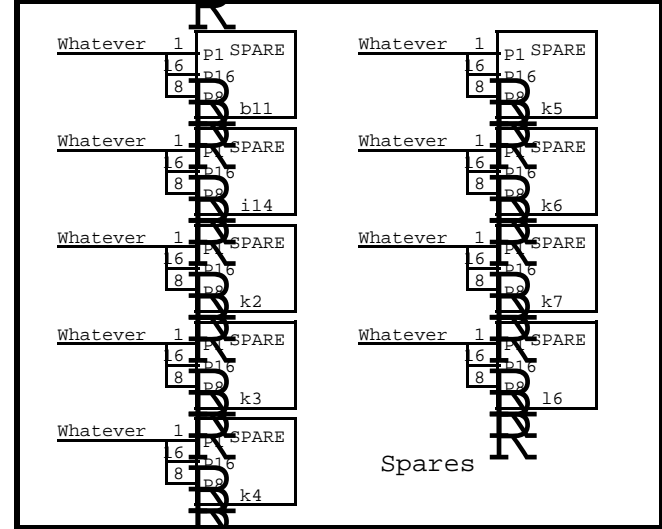
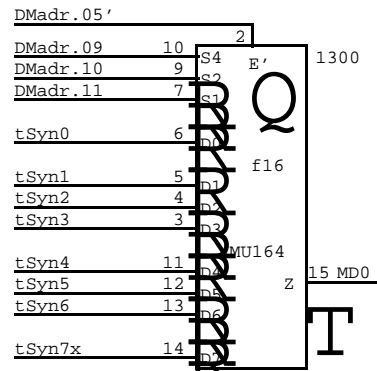
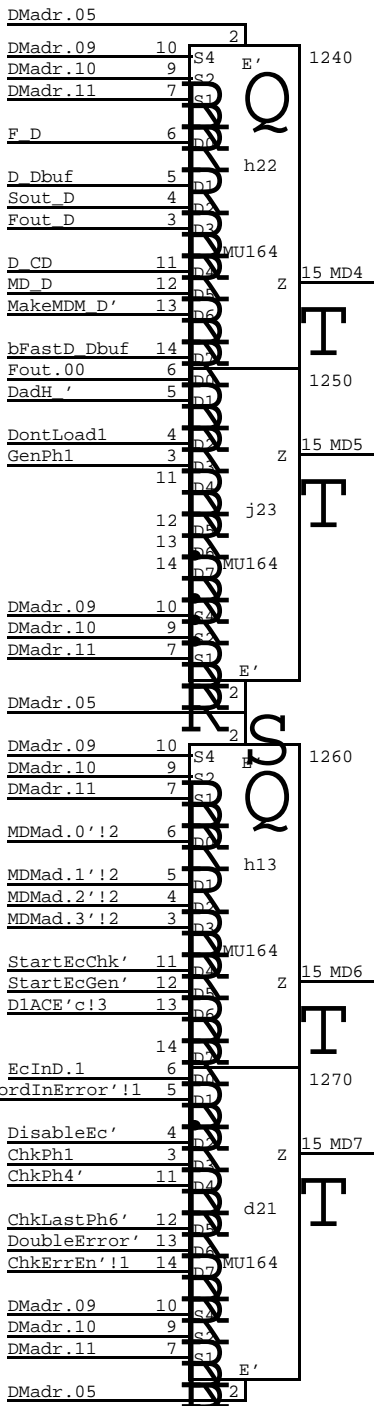
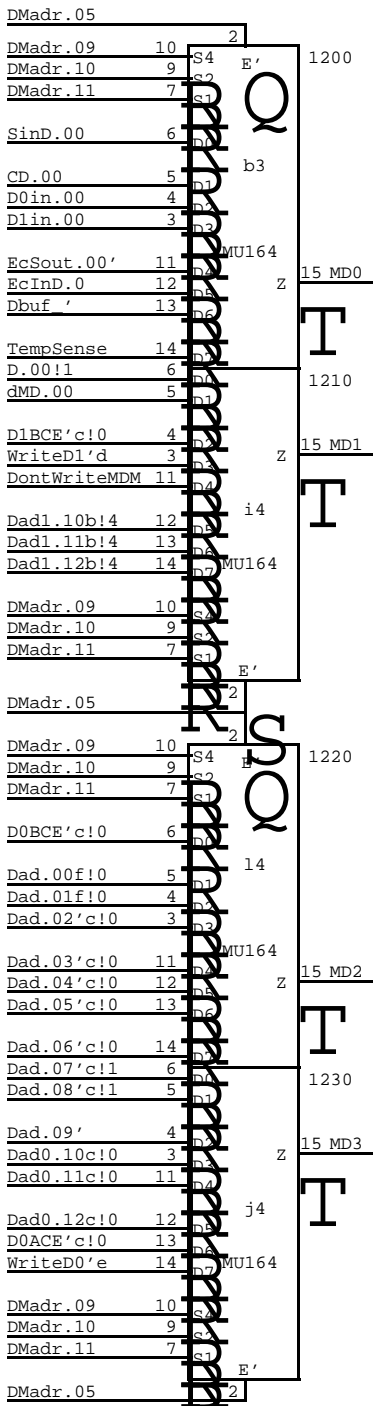
BIT 16

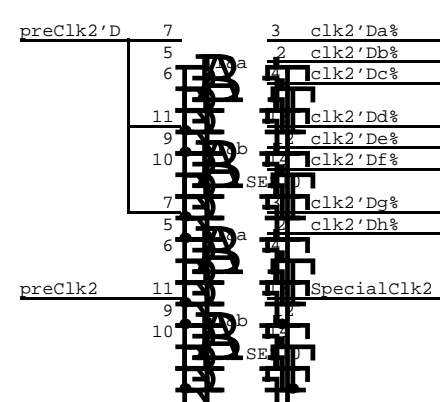
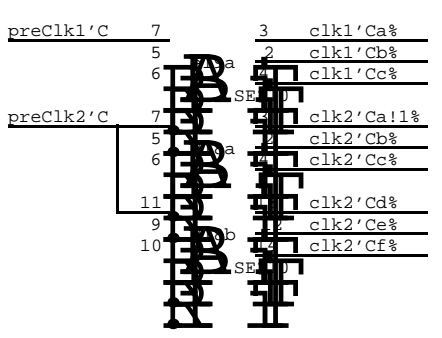
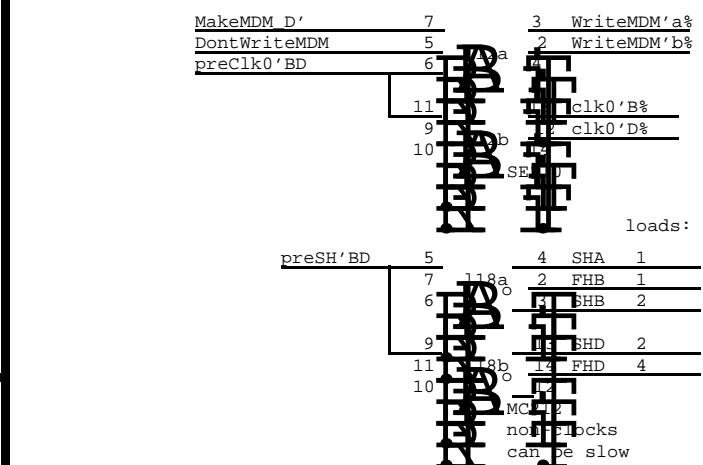
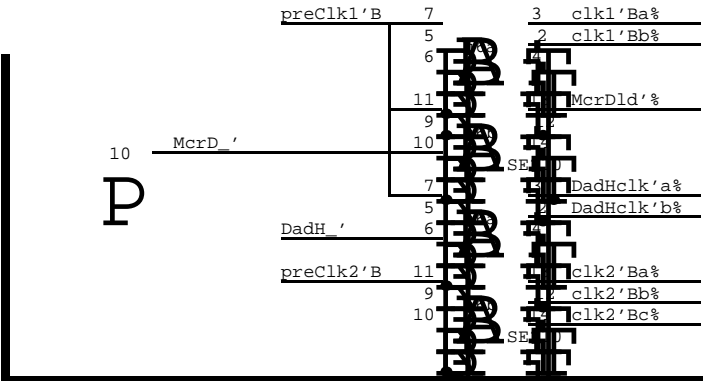
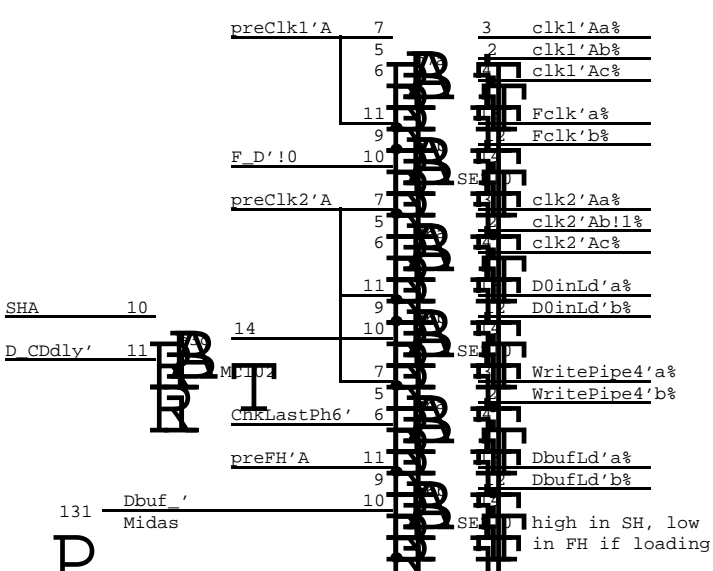
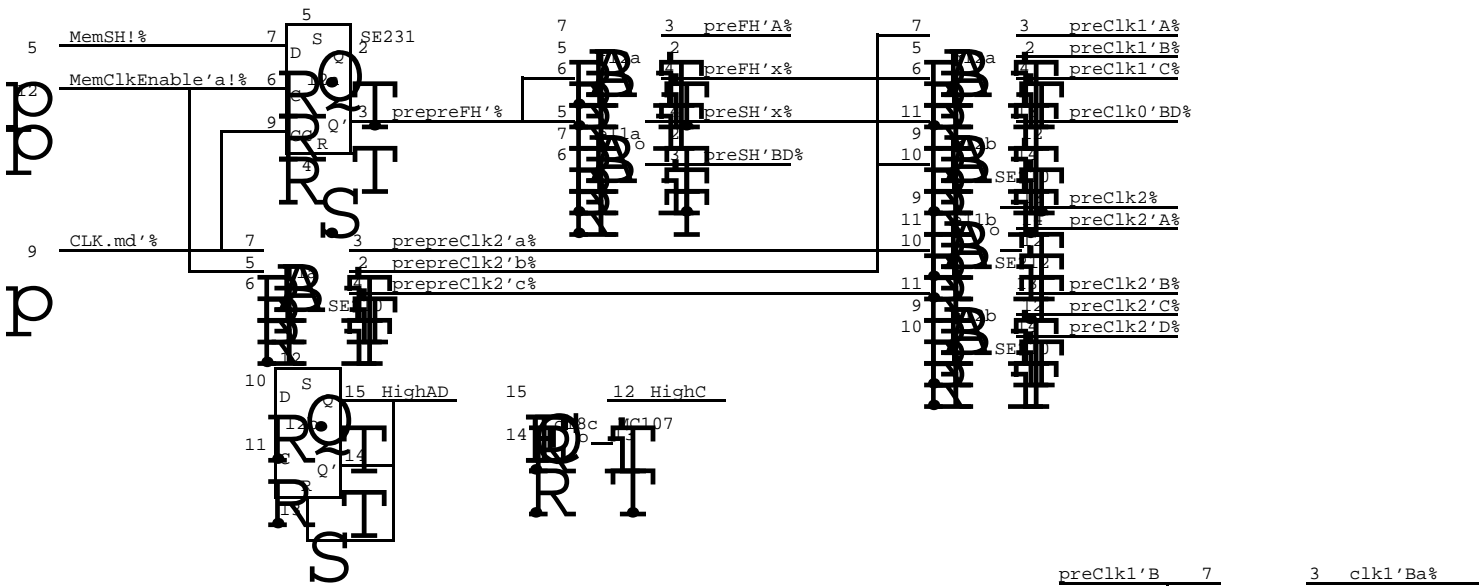


BIT 17



XEROX PARC/CSL	Project Dorado	Memory data board Bit slice control	File MemD20.sil	Designer D. Clark	Rev Be	Date 7/09/79	Page 20
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Cxxx	a 181	b 168	c 153	d 137	e 124	f 109	93 g	80 h	64 i	48 j	33 k	20 l	B
1	Sout drvvr 0-1 231 2a	BMux rcvvr 0,1,8,9 175 *a	BMux rcvvr 2,3,10,11 175 *a	EcOut 0,2,4,6 dSTPerr 176 2a	BMux rcvvr 4-6,12,13 175 *b	BMux rcvvr 7,14-17 175 *b	Dad 2,3 231 *a	rcvvr 6,7 231 *b	SinD.8-11 EcSt.16,17 176 2a	Sout drvvr 10-11 231 2a	Sout drvvr 8-9 231 2a	Clock 210	1
2	Sout drvvr 2-3 231 2a	BMux drvvr 0,1,8,9 159	SinD.0-3 EcInD.0 176 2a	BMux drvvr 2,3,10,11 159	BMux drvvr 4,5,12,13 159	BMux drvvr 6,7,14,15 159	4,5 231 *a	8,9 231 *b	0-5 Test 176 *	Syn 6-8 176 *		231	2
3	DOA.00 a,a,a,a,a 415A	SinD.0 CD.0 DntLd1 EcSout.0 EcInD.0	DOB.00 a,a,a,a,a	D1A.00 c,b,b,a,c	MemError ECFault preDntLd DriveBMux 102	D1B.00 c,b,b,a,c	D1A.02 d,b,b,c,d	Pipe34Ad DntWrMMDM 176 0	D1B.02 d,b,b,c,d	DOA.02 f,'c,c,c,e 415A		DOB.02 f,'c,c,c,e 415A	3
4	TempSense Gizmo PLAT	0,1,8,9 158	2,3,4,16 158	preDin 6,10,11 158	5,7,12,17 158	13,14,15 158	dFout 0-3 158	MdM 0-3 145 *a	CE1B.D.0 10-12(11) Write1 DWrMMDM GMD.0	Dad.7-9 CEOA, 10-12(0) Write0		Dad.0-6 CEOB MU164	4
5	DOA.01 a,a,a,a,a 415A	12-15 145	DOB.01 a,a,a,a,a 415A	D1A.01 c,b,b,a,c 415A	dSout 0-3 158	D1B.01 c,b,b,a,c 415A	D1A.03 d,b,b,c,d 415A	dMd 0-3,16,17 197	D1B.03 d,b,b,c,d 415A	DOA.03 f,'c,c,c,e 415A		DOB.03 f,'c,c,c,e 415A	5
6	4-7 Pipe4 145	4-8-11 145	clks 210	clks 210	F 0-3,16,17 176 *a	dMdM 0-3,16,17 176 1a	dFout 16,17 158	MdM 16,17 145 *a	clks 210	clks 210			6
7	DOA.16 a,a,a,a,a 415A	clks 210	DOB.16 a,a,a,a,a 415A	D1A.16 c,b,b,a,c 415A	dSout 16,17 158	D1B.16 c,b,b,a,c 415A	D1A.17 d,b,b,c,d 415A	Dad1 10-12 b F16 1a	D1B.17 d,b,b,c,d 415A	DOA.17 f,'c,c,c,e 415A		DOB.17 f,'c,c,c,e 415A	7
8	Dad0 10-12 a F16 2b0	Dad.2-5 a, 'a 101	Dad.6-8 a, 'a F_D' 101	Dad.0-1 a,b,c 210	Writes a,b,c 211	Dad.2-5 b, 'b 101	Dad.6-8 b, 'b b_Pipe4' 101	Writes d,e,f 210	Dad.0-1 d,e,f 210	Dad.2-5 c, 'c 101	Dad.6-8 c, 'c Dad.13' 101	Dad0 13 10-12 c F16 2b	8
9	DOA.08 a,a,a,a,b 415A	Dad1 10-12 a F16 1b	D1A.08 b,'a,a,b 415A	D1B.08 b,'a,a,b,b 415A	Dad0 10-12 b F16 2b2	DOB.08 c,'b,b,a,c 415A	DOA.10 d,'b,b,c,d 415A	dSout 8-11 158	D1A.10 e,c,c,c,e 415A	D1B.10 e,c,c,c,f 415A	Dad1 10-12 c F16 1b	DOB.10 f,'c,c,c,f 415A	9
10	D0in0,1,4 8,9,16 176 *a	D1in 0,1,4 8,9,16 176 1b	D2in 2,3,6, 10,11,17 176 1b	D0in 2,3,6, 10,11,17 176 *b	F 8-11 176 *b	dMdM 8-11 ClearWA 176 1a	dFout 8-11 158	dMd 8-11 158	CE's 0A, 1A 210	CE's 0B, 1B 176 1a	preCE 159	preCE DntLoad0 1664	10
11	DOA.09 a,a,a,b,b 415A		D1A.09 b,'a,a,b,a 415A	D1B.09 b,'a,a,b,b 415A	preclks 212	DOB.09 c,'b,b,b,c 415A	DOA.11 d,'b,b,c,d 415A	MdM 8-11 145 *b	D1A.11 e,c,c,c,e 415A	D1B.11 e,c,c,c,f 415A	B 180	DOB.11 f,'c,c,c,f 415A	11
12	0-3,17 176 2c	Ec pipe 4-9 176 2c	I10-15 176 2c	D1in 5,7,12 13,14,15 176 1c	D0in 5,7,12 13,14,15 176 *b	preclks 210	preclks 210	MDMad 141 2c	WriteMDM clk0'B,D 210		Generator A 180	163	12
13	DOA.04 a,a,a,b,b 415A	Cphi 172	D1A.04 b,'a,a,b,a 415A	D1B.04 b,'a,a,b,b 415A	ChkPhi F00 2a0	DOB.04 c,'b,b,b,c 415A	DOA.06 d,'b,b,c,d 415A	MDMad(4) CE1A StartEcChk StartEcGen	D1A.06 e,c,c,c,e 415A	D1B.06 e,c,c,c,f 415A		DOB.06 f,'c,c,c,f 415A	13
14	0-7 163	8-15 163	SinD.17 170	ChkQWi Chkwi F16 2a0	F 4-7 F16 1a	dMMD.4-7 LastQWi 176 1a	dFout 4-7 158	dMd 4-7 158		C 180	D 180	E 180	14
15	DOA.05 a,a,a,b,b 415A	A 180	D1A.05 b,'a,a,b,a 415A	D1B.05 b,'a,a,b,b 415A	dSout 4-7 158	DOB.05 c,'b,b,b,c 415A	DOA.07 d,'b,b,c,d 415A	MdM 4-7 145 *b	D1A.07 e,c,c,c,e 415A	D1B.07 e,c,c,c,f 415A	F 180	DOB.07 f,'c,c,c,f 415A	15
16	B 180	Checker C 180	D 180	A-C 158	D-E 158	tSyni MU164	PipeII- 1V/Gen 3 0,1 176 2c	1V/Gen 3 dClearWA 104	PipeII- 1V 2,3 176 2c	D_CDDly 231 2b	A-C 158	(E) 231 2a	16
17	DOA.12 a,a,a,b,b 415A	E 180	D1A.12 b,'a,a,b,a 415A	D1B.12 b,'a,a,b,b 415A	ChkPh,etc SinD.16dly 176 2a2	DOB.12 c,'b,b,b,c 415A	DOA.14 d,'b,b,c,d 415A	MdM 12-15 145 *b	D1A.14 e,c,c,c,e 415A	D1B.14 e,c,c,c,f 415A	D-E 158	DOB.14 f,'c,c,c,f 415A	17
18	tSyn0-3 F00 2b	tSyn4,7 231 2b	SinD.16 D_CD' HighC 107	clks 210	F 12-15 F16 1b	dMdM 12-15 TickTockCE ChkLstPh6 176 1b	dFout 12-15 158	dMd 12-15 158	clks 210	clks 210	GenPhi F00 2a	FH, SH 212	18
19	DOA.13 a,a,a,b,b 415A	tSyn5,6 231 2b	D1A.13 b,'a,a,b,a 415A	D1B.13 b,'a,a,b,b 415A	clks 210	DOB.13 c,'b,b,b,c 415A	DOA.15 d,'b,b,c,d 415A	dSout 12-15 158	D1A.15 e,c,c,c,e 415A	D1B.15 e,c,c,c,f 415A	PipeII- 1V 8,9 176 2h	DOB.15 f,'c,c,c,f 415A	19
20	Syni F16 2c	Corrector WordInError F00 2c	Syn3 D_Dbufdly F00 2c	MemError ChkPh,etc. DMadr' 195	CD 0-5 176 2e	G 2,3,10,11 F16 2e	G 4,5,12,13 F16 2g	G 6,7,14,15 F16 2g	PipeII- 1V 4,5 176 2g	PipeII- 1V 6,7 176 2h	PipeII- 1V 10,11 176 2h	PipeII- 1V 12,13 176 2h	20
21	DblError 170	Error ChkErrEn' 109	Syn3 D_Dbufdly 231 2c	EcCheck stuff MU164	6-11 176 2e	FG 2,3 174	FG 4,5 174	FG 6,7 174	G 16,17 F16 2g	PipeII- 1V 14,15 176 2e	1-5 Midas 176	6-11 176	21
22	Flips16,17 ChkErrEn' 102	Flips0-7 162	Flips8-15 162	dCD 0-3 113	12-17 176 2f	G 0,1,8,9 F16 2f	preWrite 231 *	X_YS MU164	FG 8 174	PipeII- 1V 16,17 176 2e	MuxData 164	Midas 2 Bank0CE 103	22
23	4-7 F16 1c	dPipe4 8-11 F16 1c	12-15 F16 1c	4-7 113	8-11 113	FG 0,1 174	dMdM_D DntLoad1 dd_Dly 106	preWrite bTransport 102	DadH_ 231 0	Fout.0 DntLd1 DadH_ GenPh1	SinD.12-15 D_CDDlydly 176 2f	Sout drvvr 14-15 231 2f	23
24	Sout drvvr 6-7 231 2d	Sout drvvr 4-5 231 2d	SinD.4-7 EcInD.1 ChkPh5w.o. 176 2d	12-15 113	16,17 DMadr.05' 113	EcOut 1,3,5,7 D_dly' 176 2f	MakeX rcvvr 176 2d	bFastD.Dbff preWrite 1664	Fout drivers 11-15,17 176 2d	5-10 176 2e	0-4,16 176 2f	Sout drvvr 12-13 231 2f	24

Cxxx
D chip code: Dad.0-1,2-8,10-12,CE,Write
a 11 b 26 c 39 d 55 e 70 f 86 99 g 114 h 129 i 143 j 159 k 174 l D

PEROX	Project Dorado	Reference Memory data board Layout	File MemD23.sil	Designer D. Clark	Rev Be	Date 7/09/79	Page 23
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