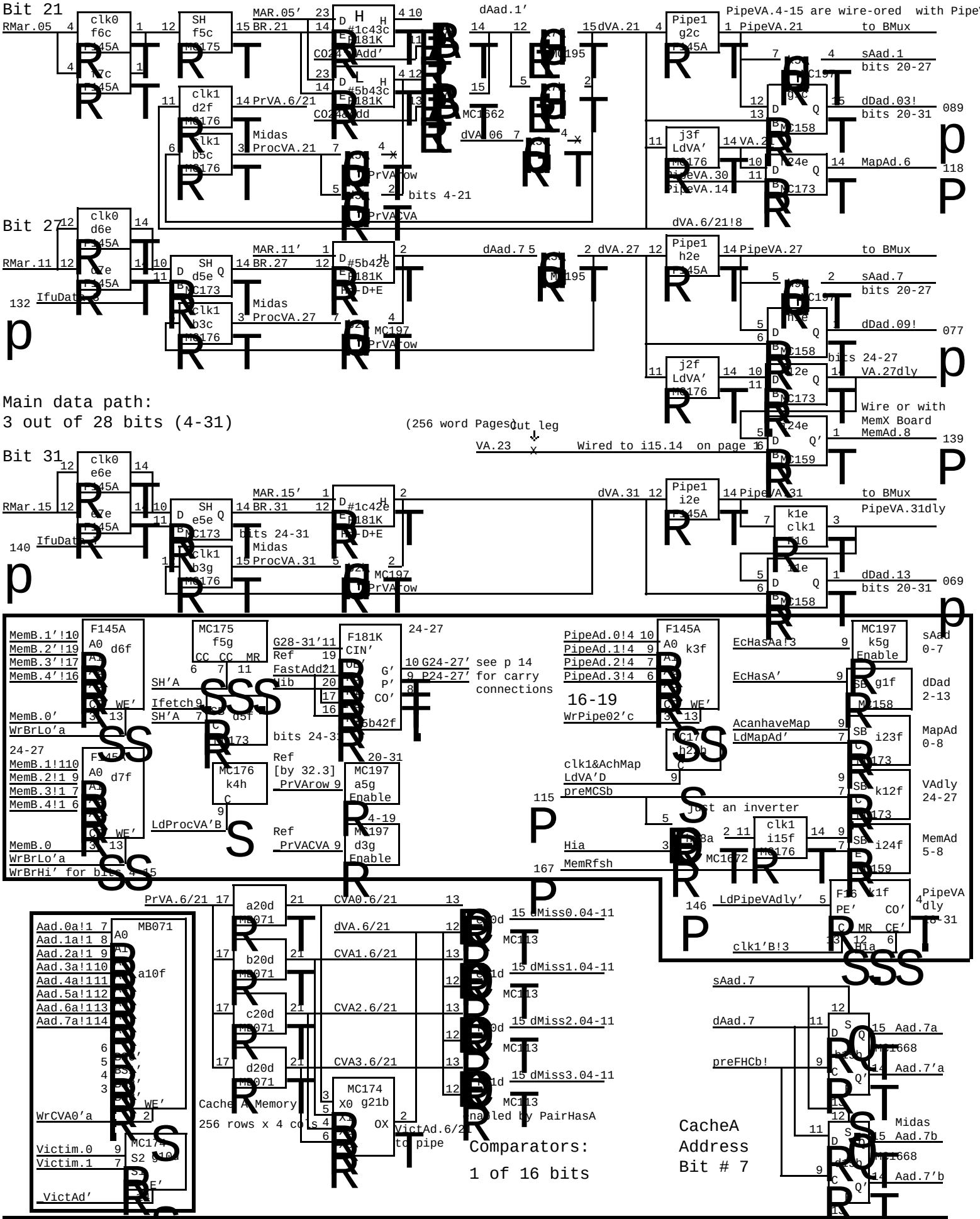
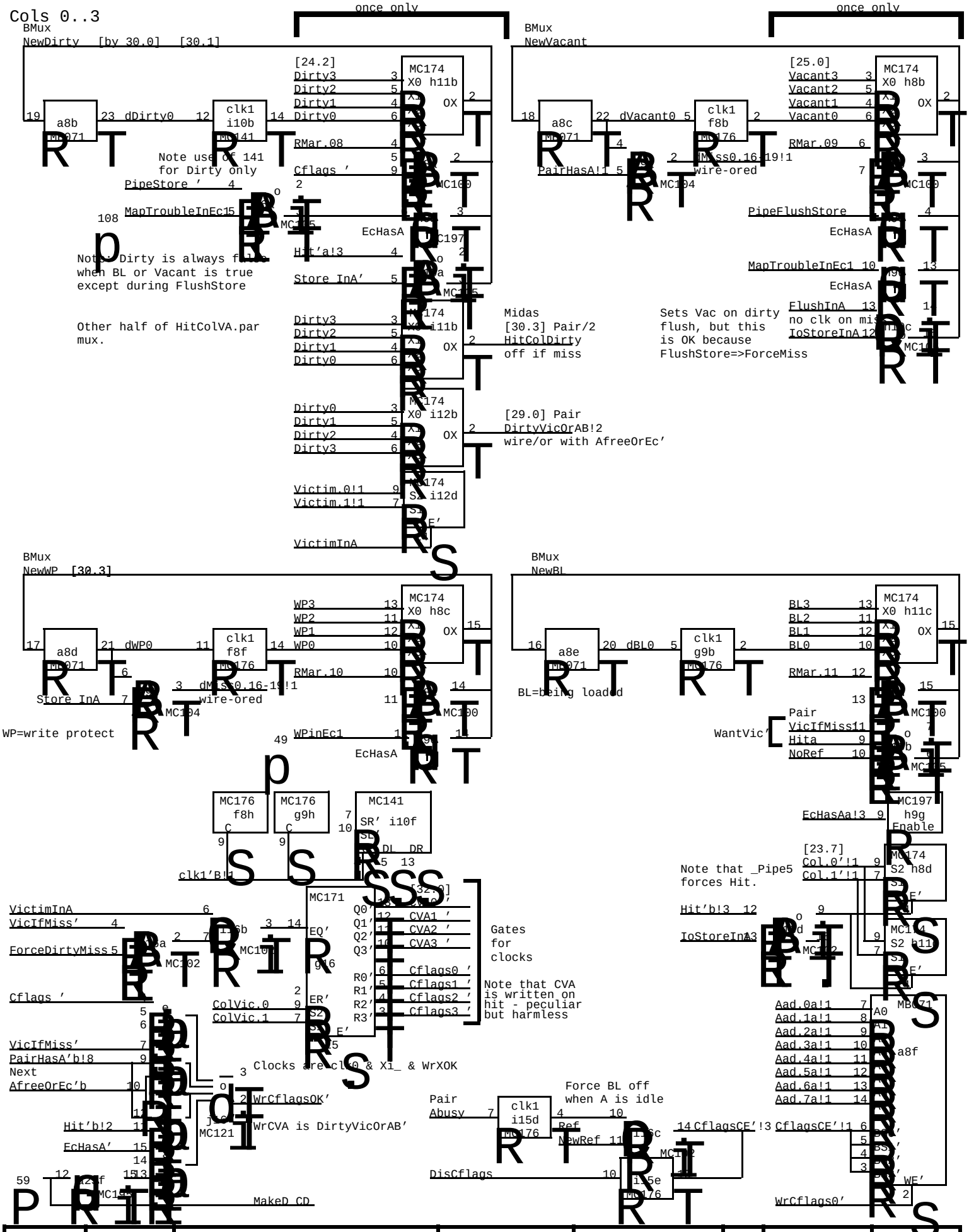
D O R A D O S C H E M A T I C S

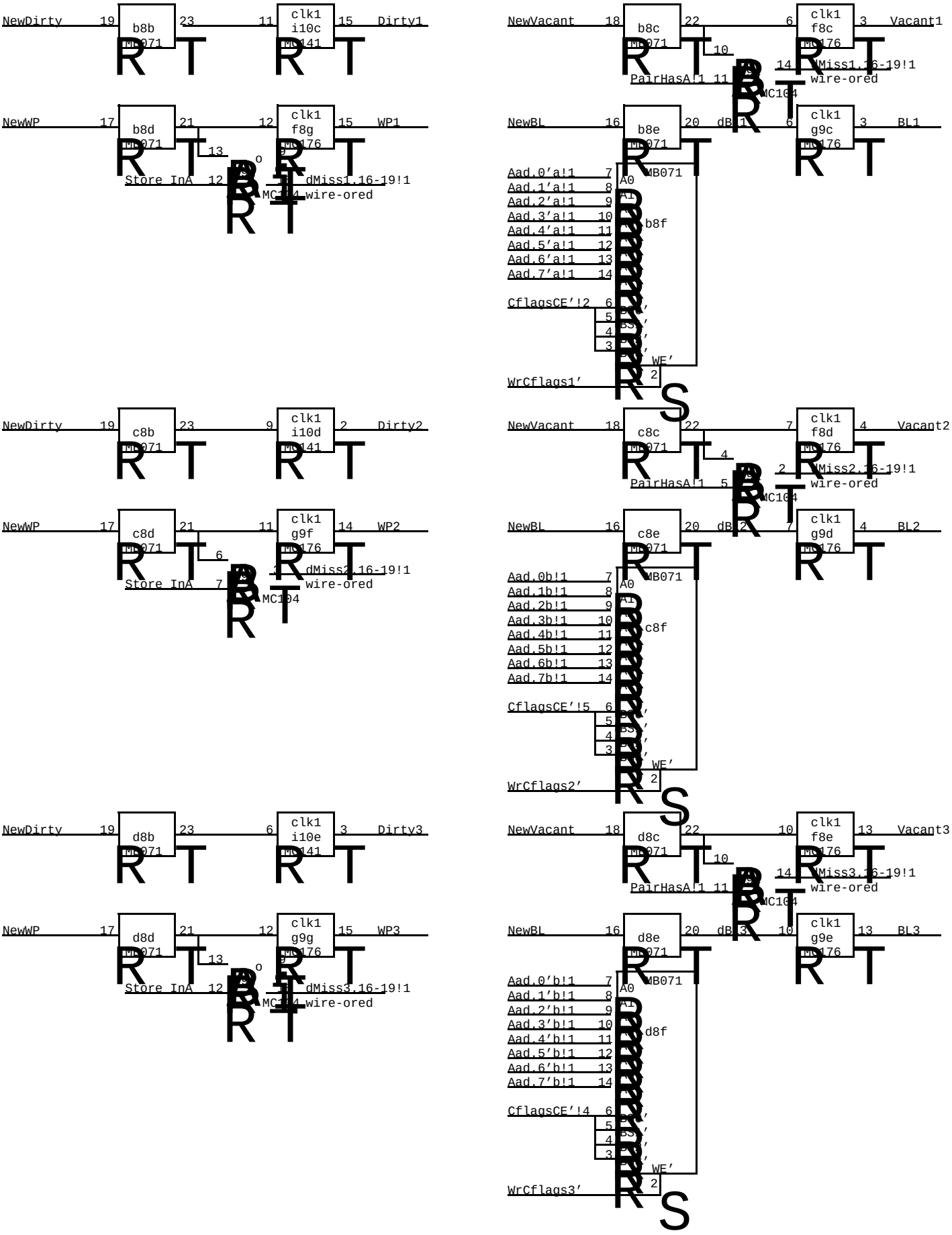
M e m o r y C o n t r o l

Table of contents

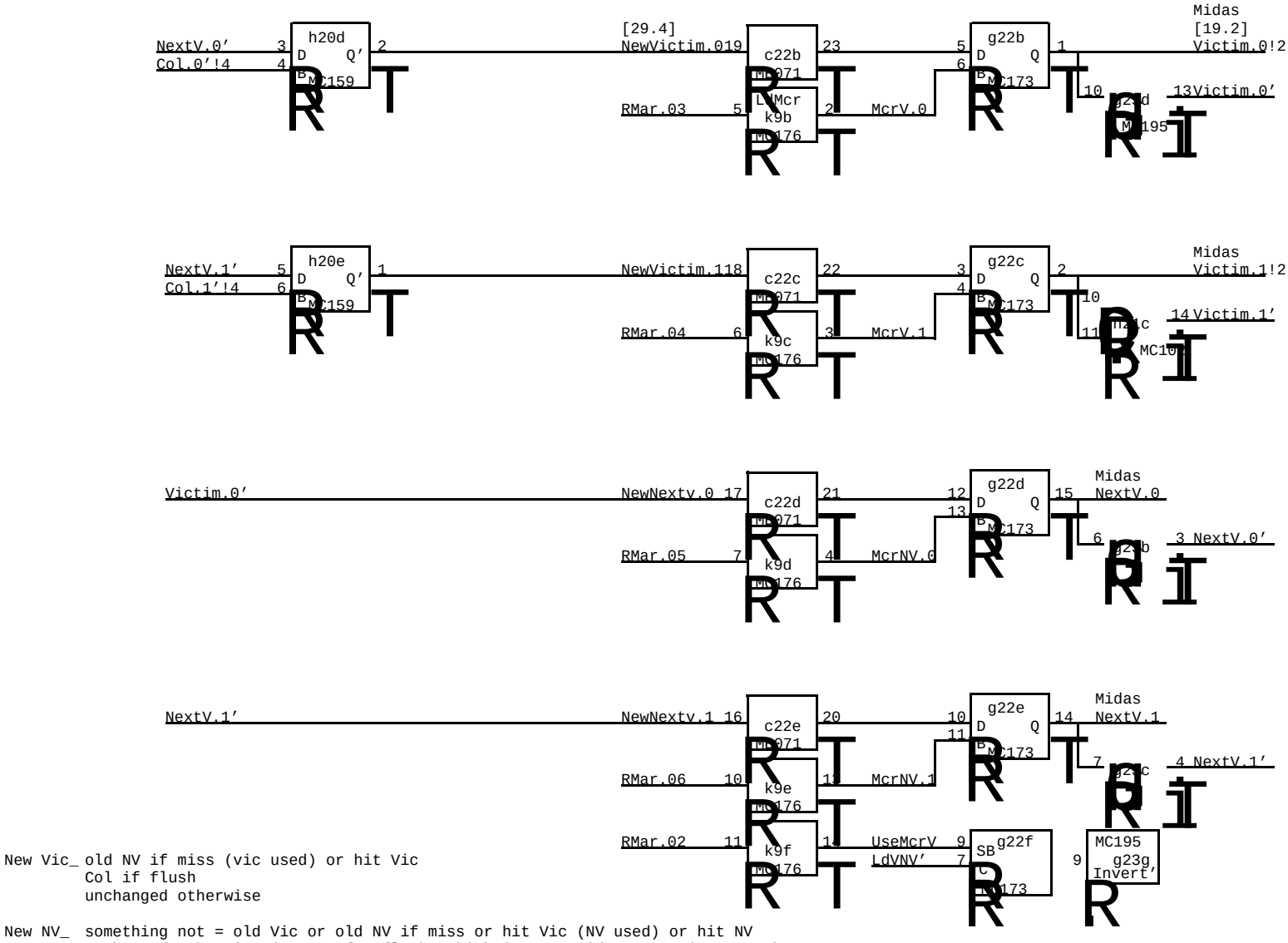

Bit 21
Bit 27
Bit 31
Main data path:
3 out of 28 bits (4-31)
(256 word Pages)
Out leg
Wired to i15.14 on page 16
PipeVA.4-15 are wire-ored with PipeV
to BMux
sAad.1
bits 20-27
dDad.03!
bits 20-31
MapAd.6
sAad.7
dDad.09!
VA.27dly
MemAd.8
PipeVA.31dly
dDad.13
Midas
ProcVA.21
ProcVA.27
ProcVA.31
PrVArow
PrVACVA
bits 4-21
dVA.6/21!8
Wire or with
MemX Board
Cache A Memory
256 rows x 4 cols
Comparators:
1 of 16 bits
CacheA
Address
Bit # 7
Enabled by PairHasA
to pipe
Just an inverter
see p 14
for carry
connections
16-19
24-27
Project
Dorado
Drawing
Main data paths
File
MemC01.sil
Designer
Lampson
Rev
Be
Date
7/30/85
Page
01
XEROX
PARC



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Cache flags	MemC02.sil	Lampson	Be	7/30/85	02

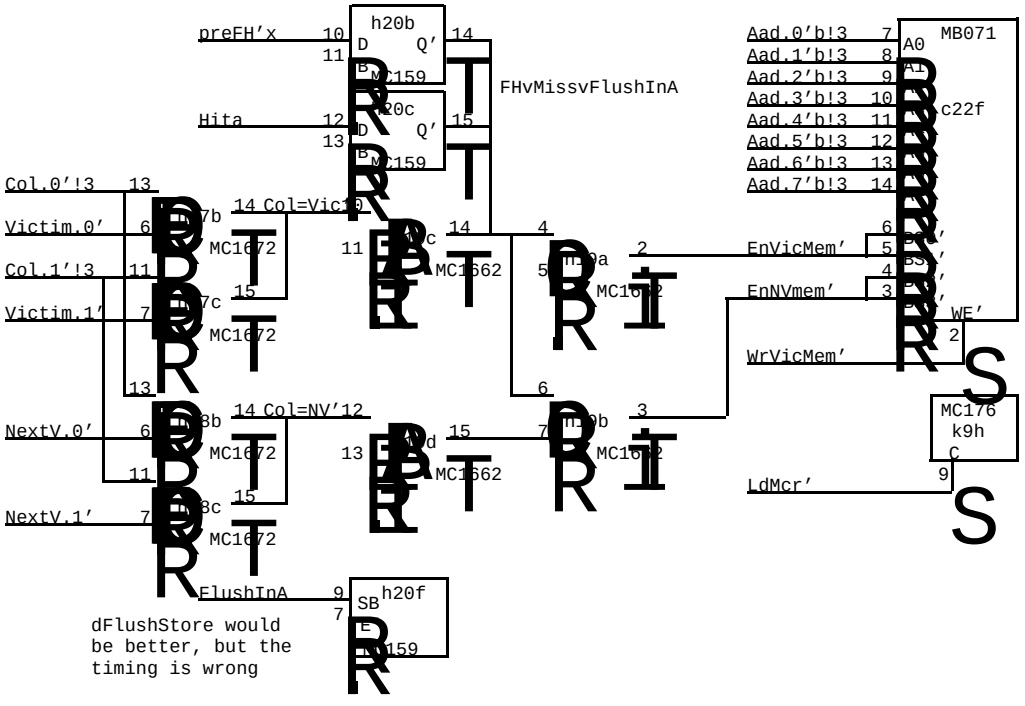


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Cache flags, cols1-3	MemC03.sil	Lampson	Be	7/01/79	03



New Vic_ old NV if miss (vic used) or hit Vic
Col if flush
unchanged otherwise

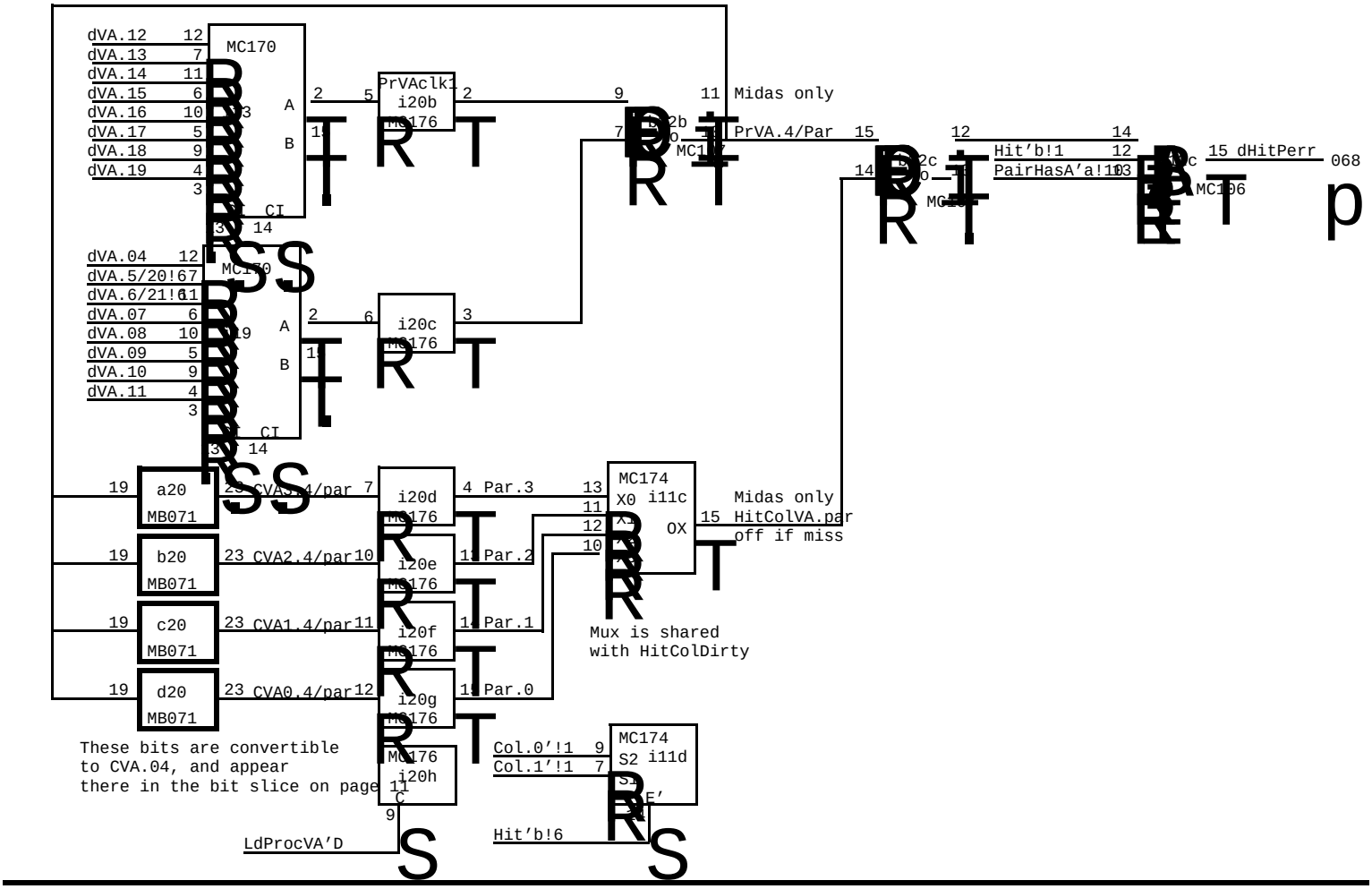
New NV_ something not = old Vic or old NV if miss or hit Vic (NV used) or hit NV
unchanged otherwise (except for flush, which is an accident, not important)

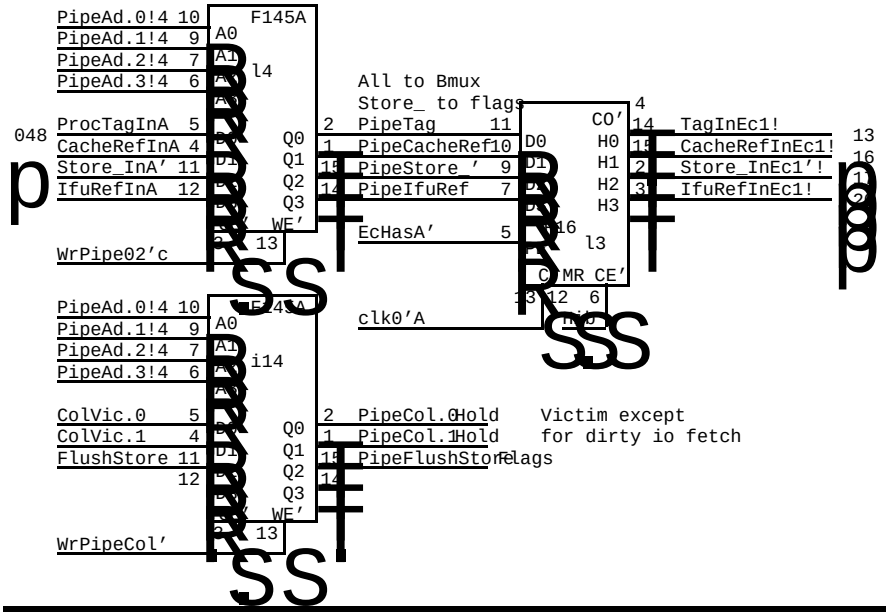


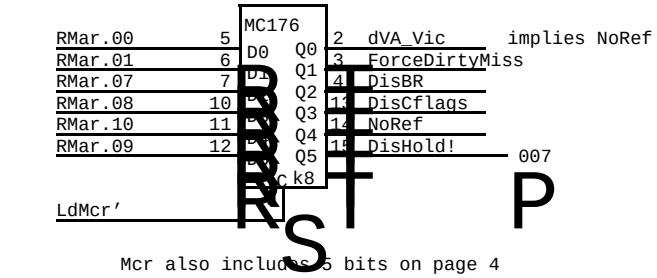
The Victim memory is written on a CacheRef, PreFetch or IfuRef that misses, and on any FlushStore or Flush_.

For a Flush_, Victim is first written with 0 on a miss or with the column of the hit. NextV is garbaged at the same time. On a dirty hit, a FlushStore follows, smashing Victim and NextV again.

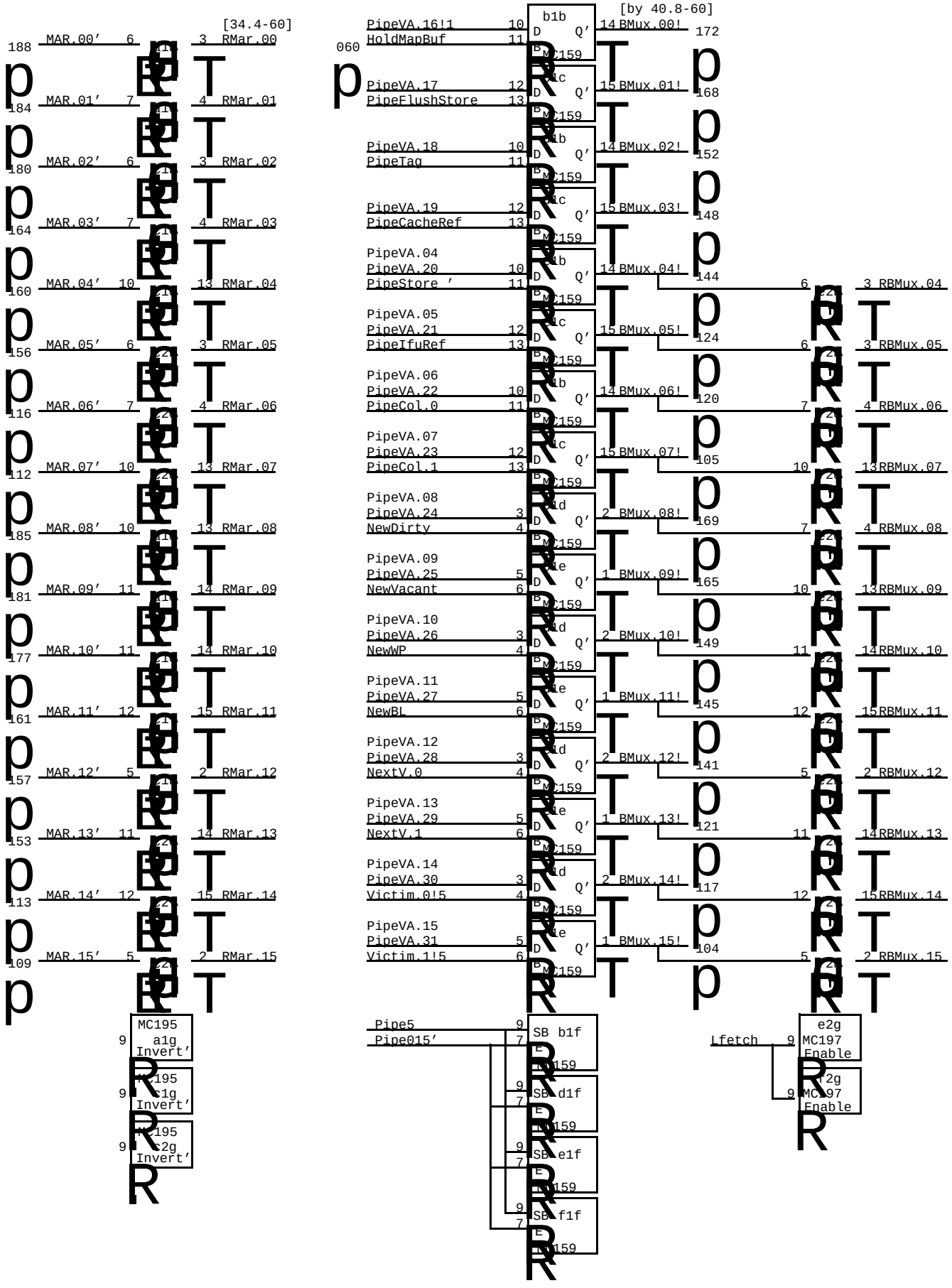
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Victim + NextVictim	MemC04.sil	Lampson	Be	7/01/79	04



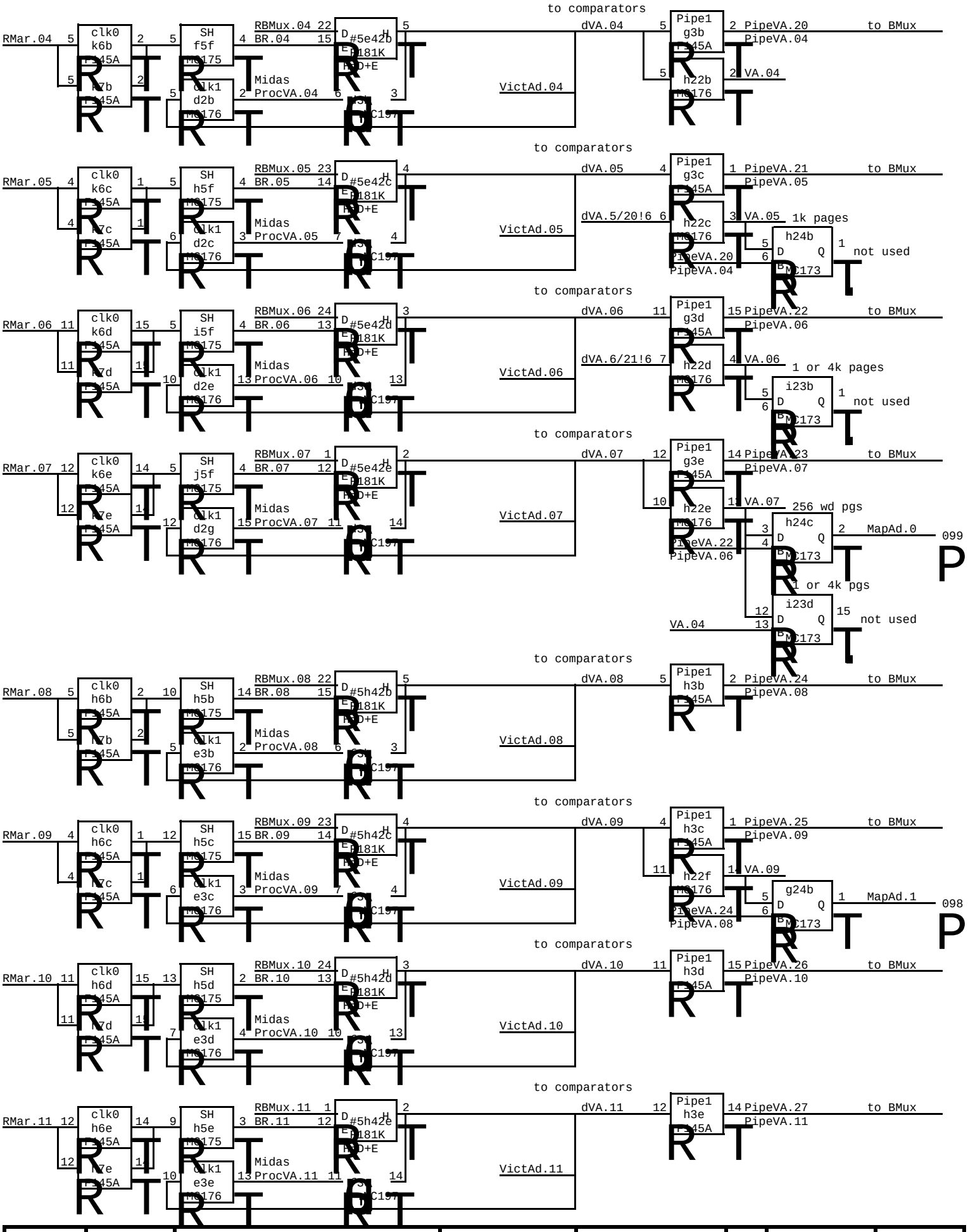




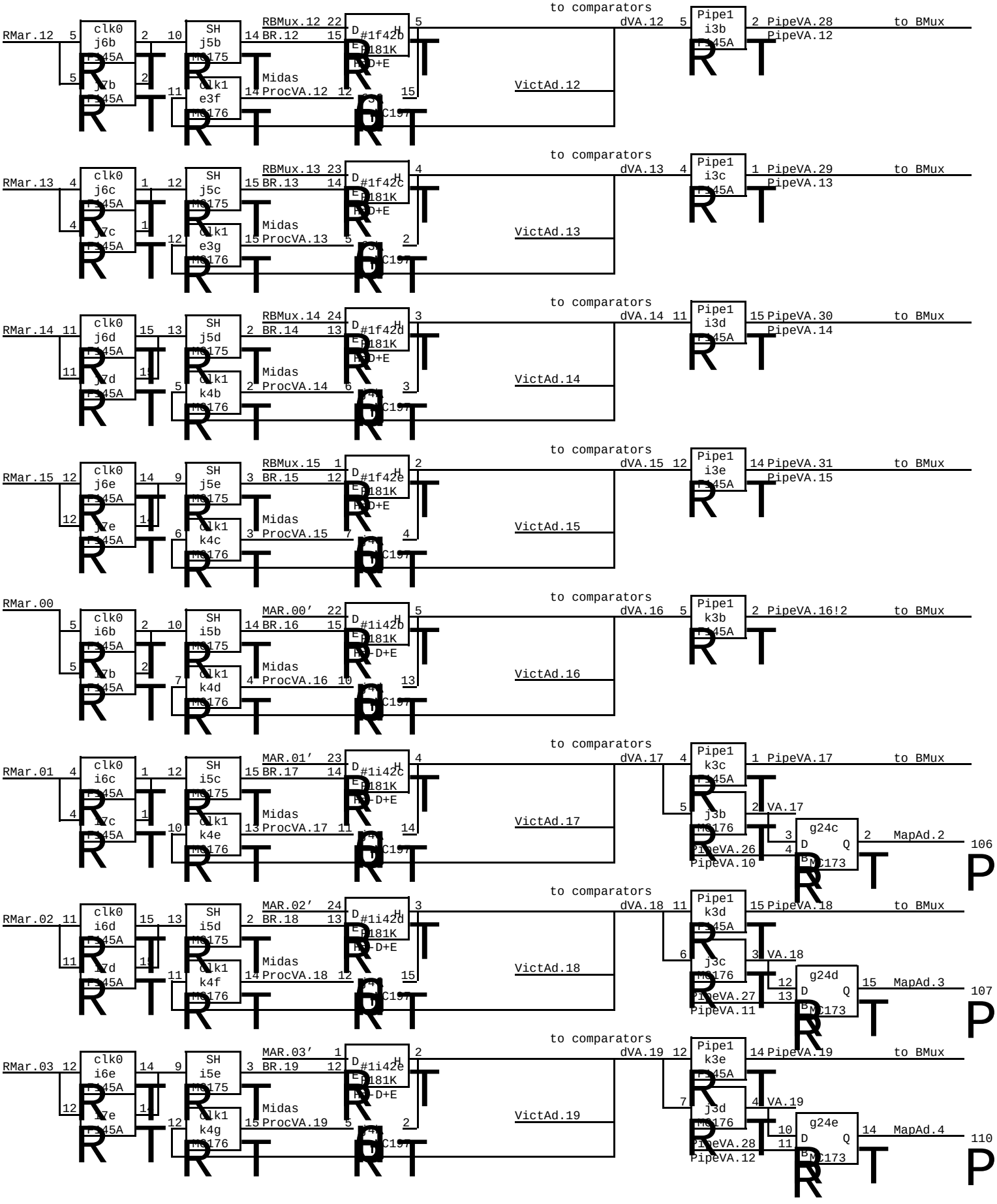
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Parity, pipe, Mcr	MemC05.sil	Lampson	Be	7/16/85	05



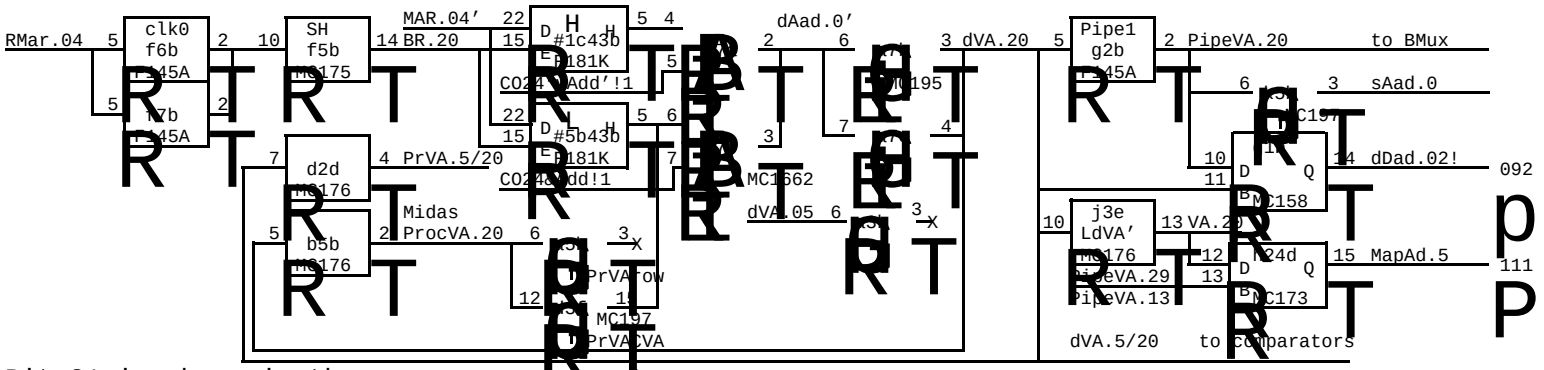
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Mar and BMux interface	MemC06.sil	Lampson	Be	7/30/85	06



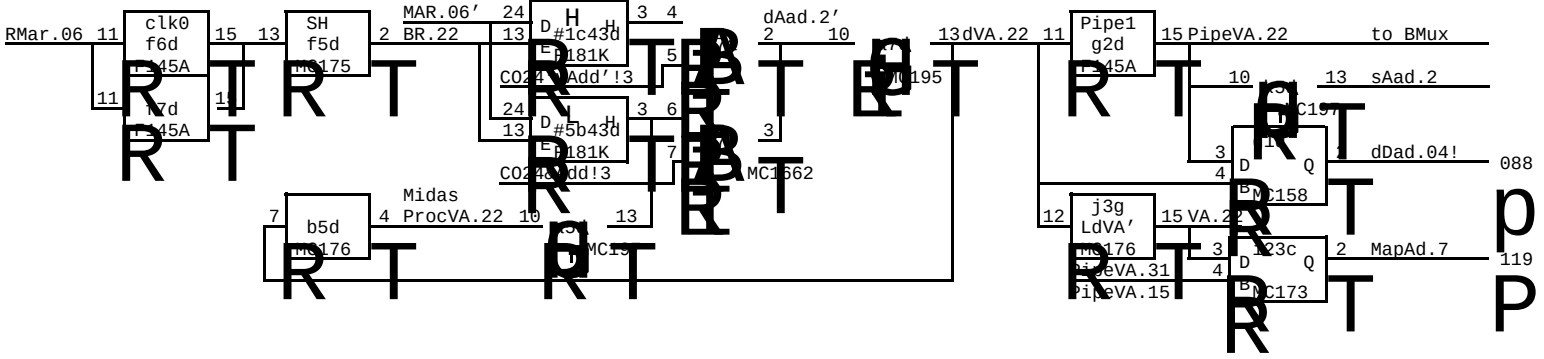
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Main data paths: 4-11	MemC07.sil	Lampson	Be	7/17/85	07

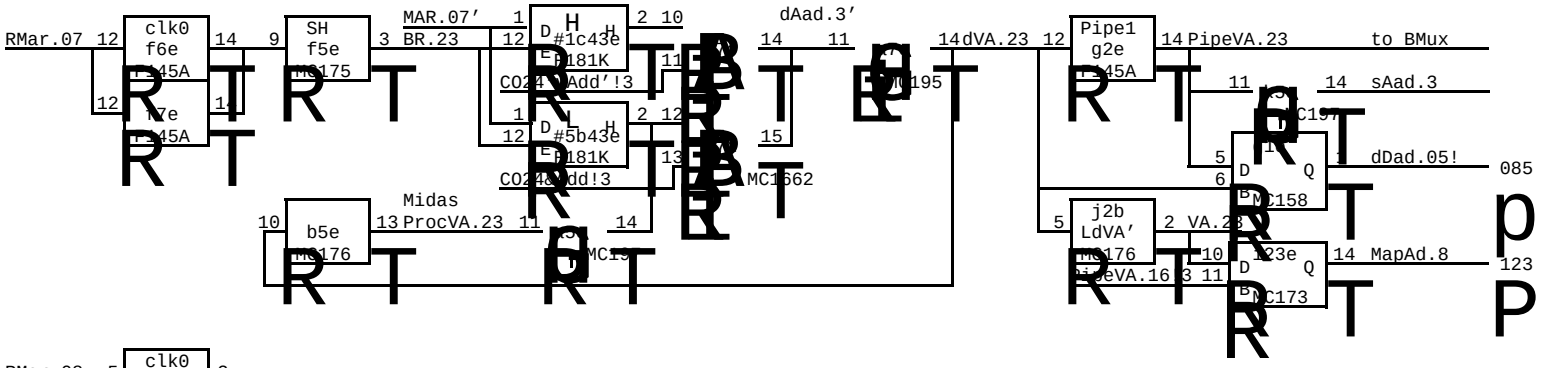


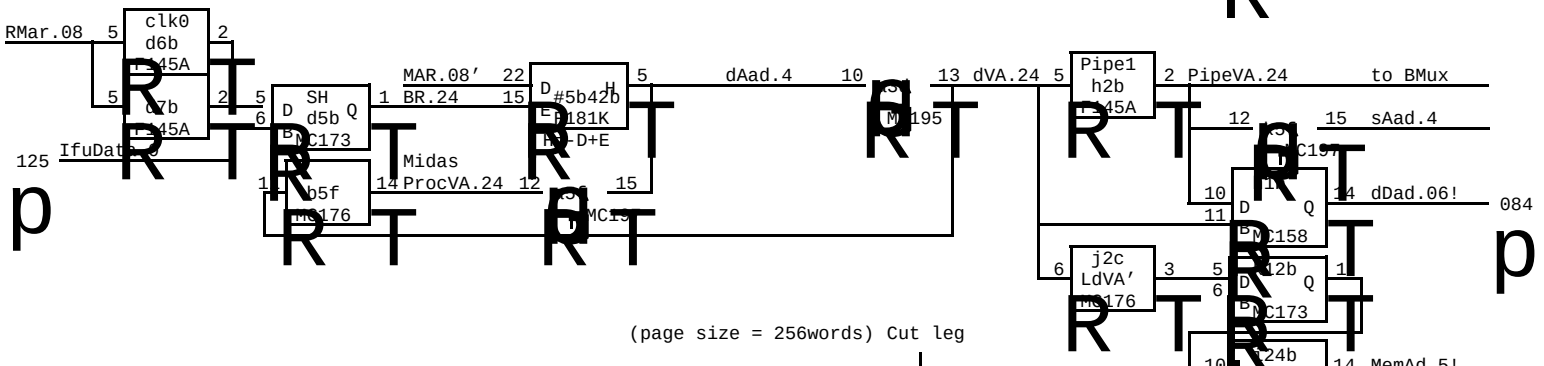
XEROX PARCb	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Main data paths: 12-19	MemC08.sil	Lampson	Be	7/17/85	08

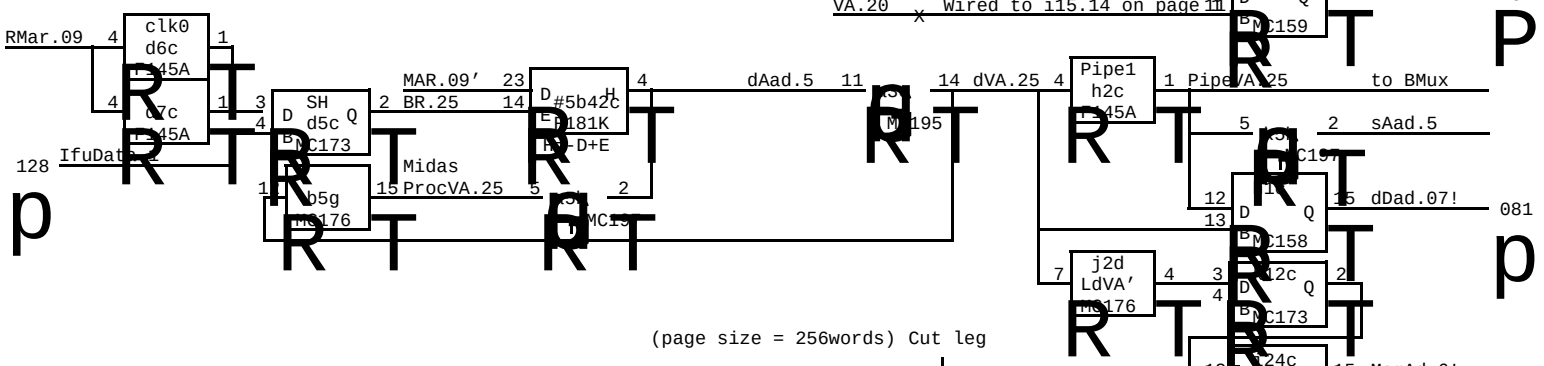


Bit 21 is shown in the summary on page 1

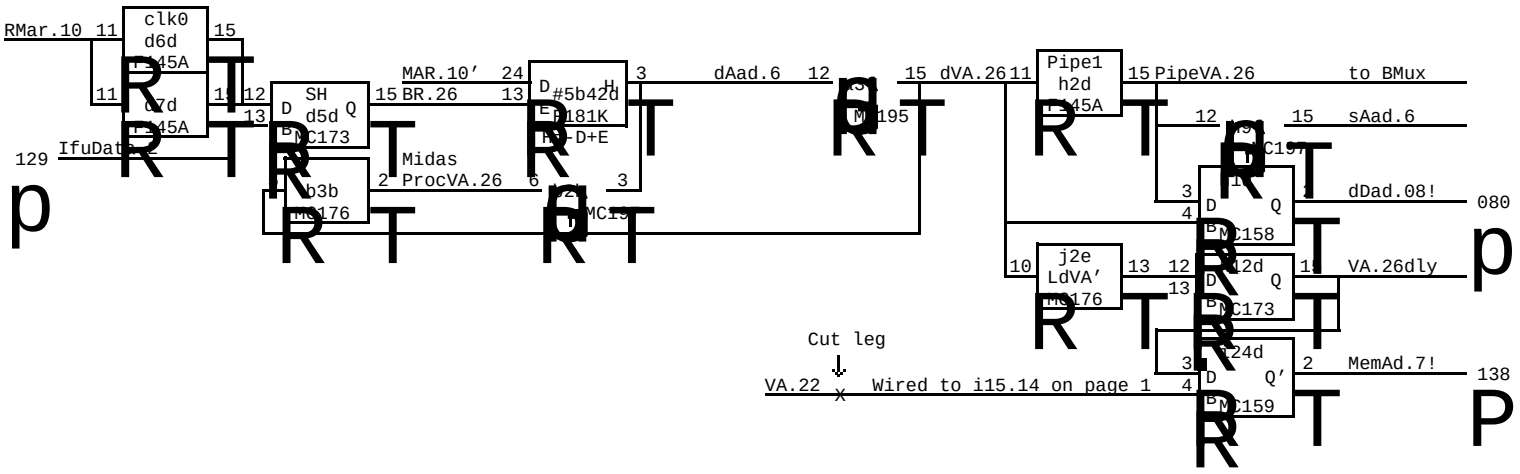




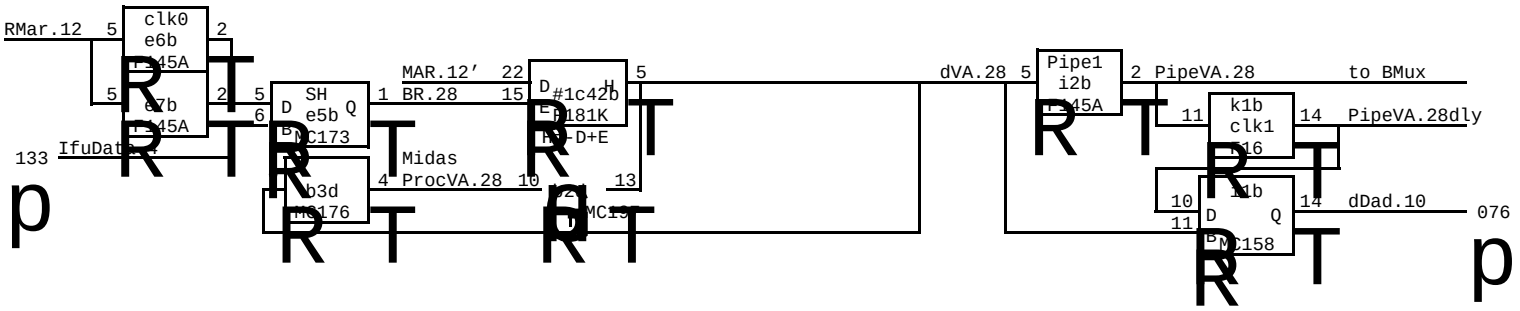


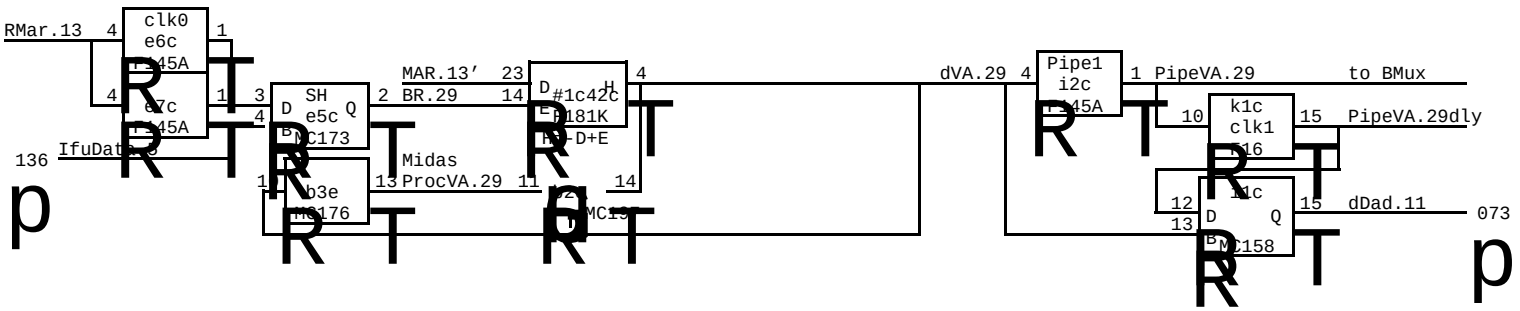


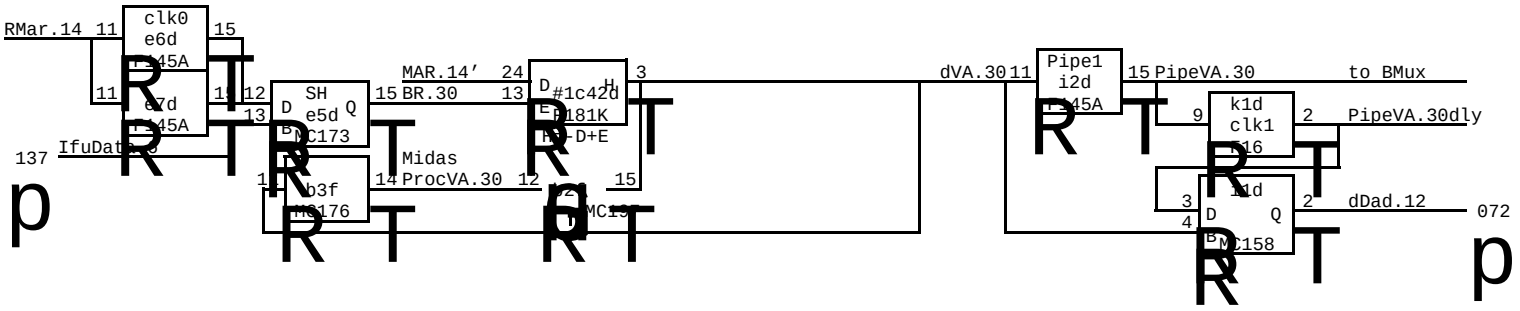
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Main data paths: 20-26	MemC09.sil	Lampson	Be	7/11/85	09



Bit 27 is shown in the summary on page 1

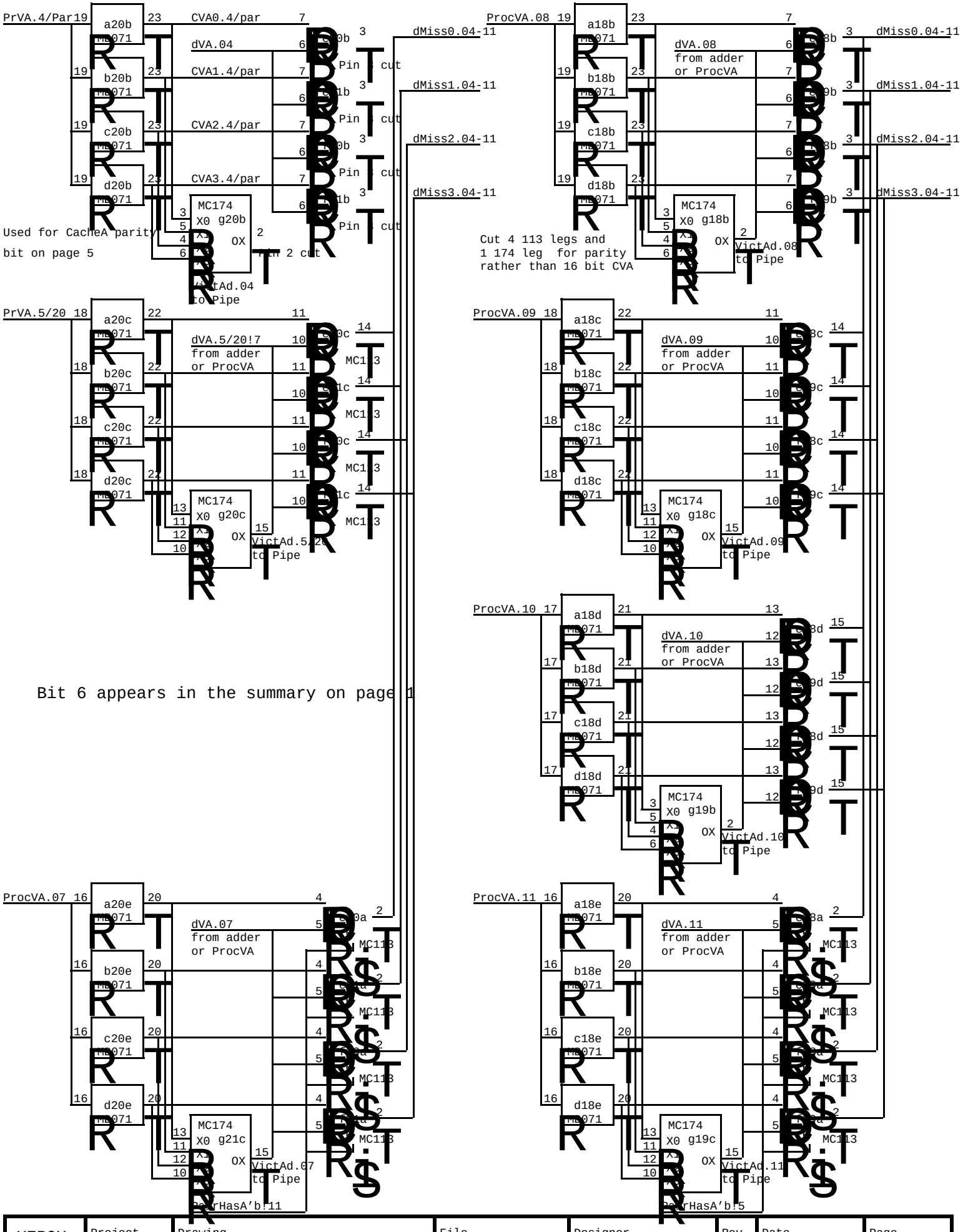




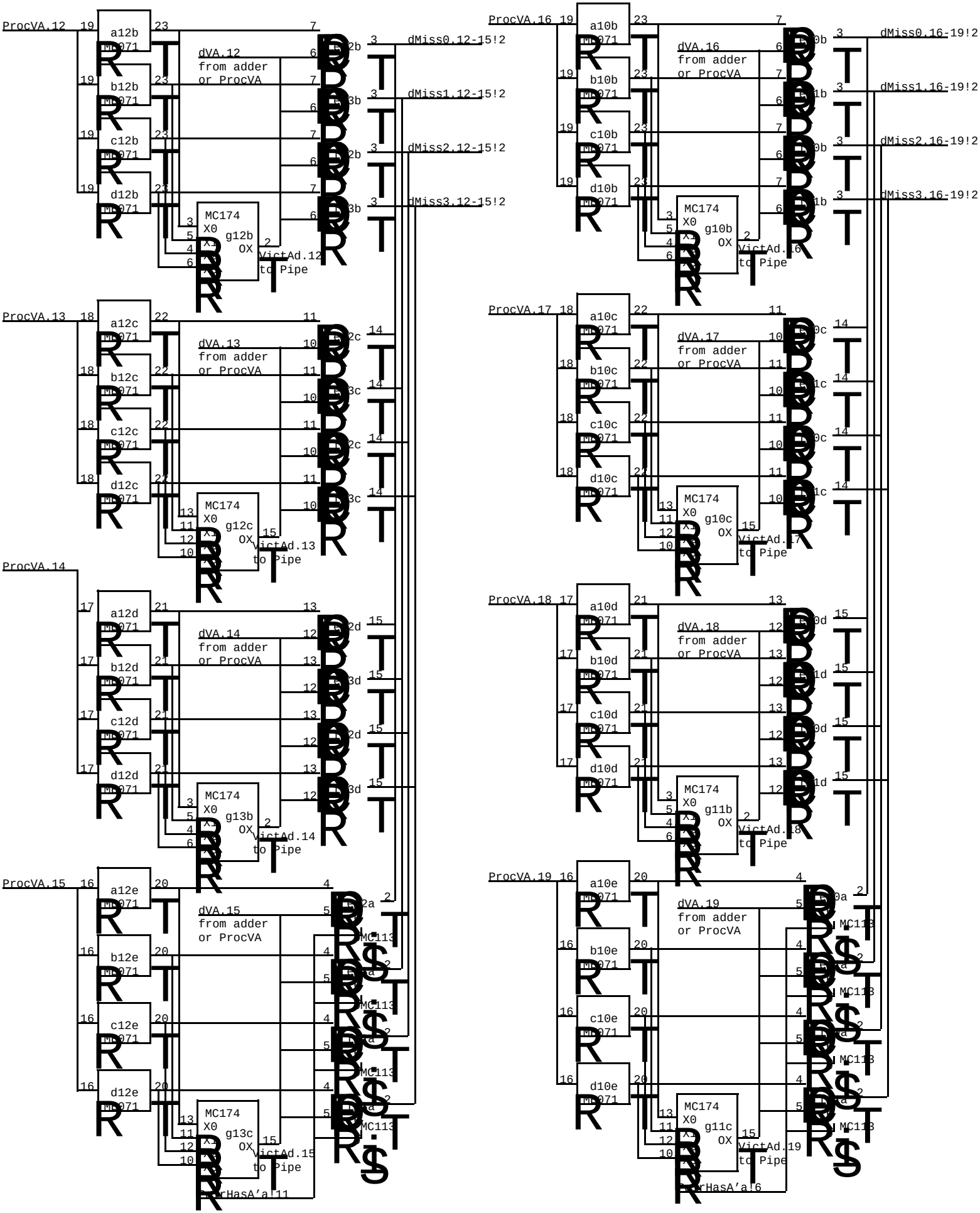


Bit 31 is shown in the summary on page 1

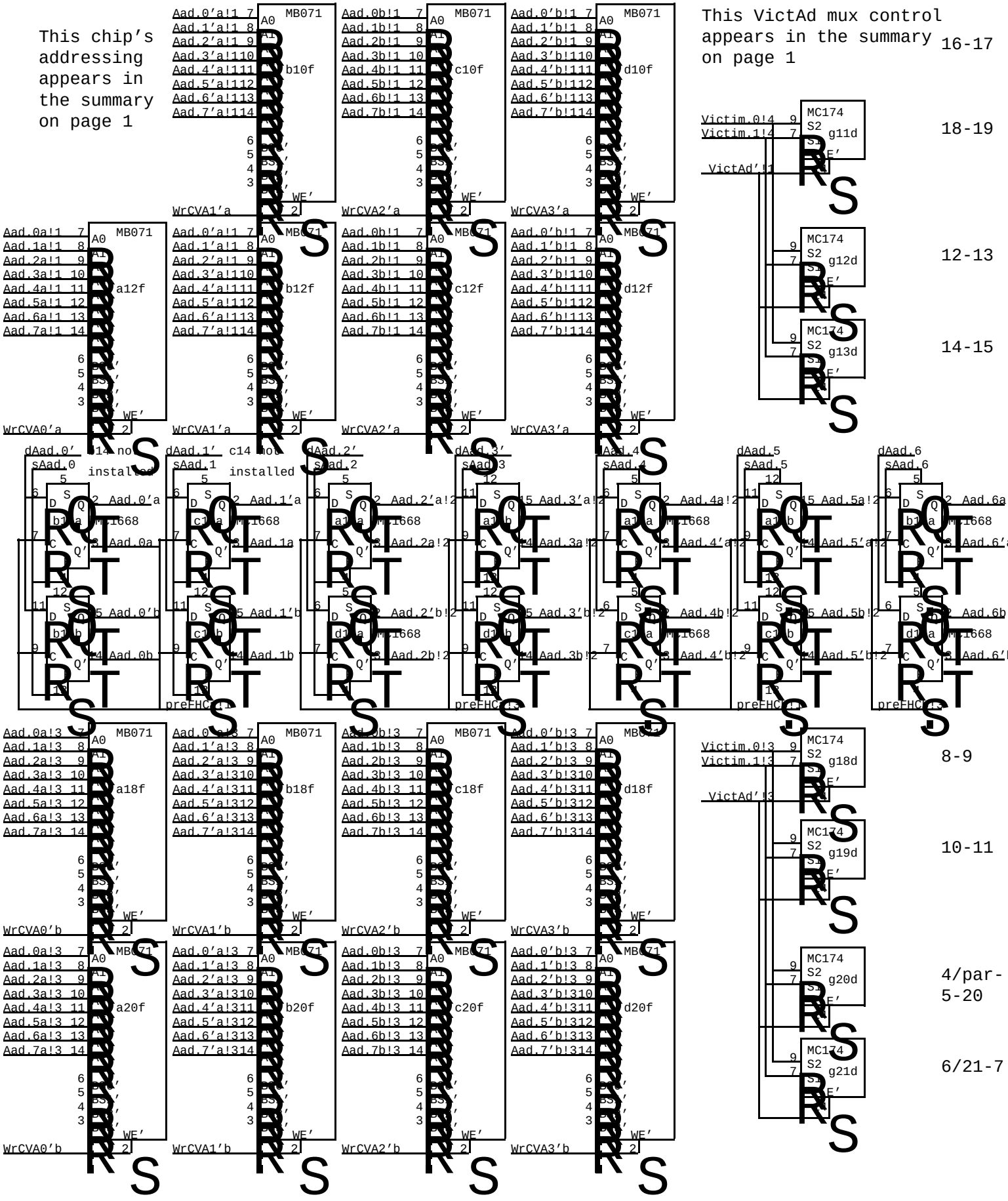
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Main data paths: 26-31	MemC10.sil	Lampson	Be	7/15/85	10



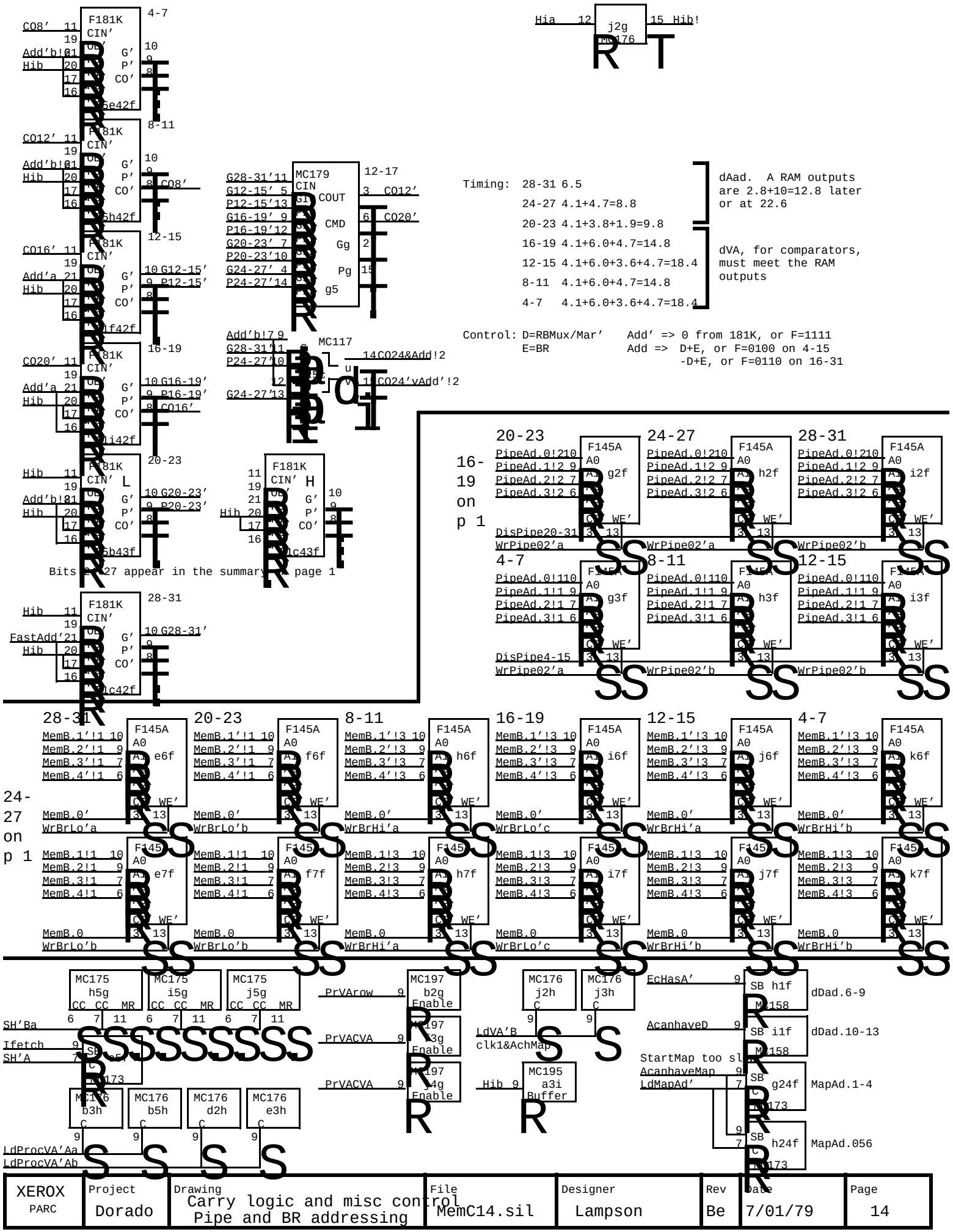
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CVA and comparators: 4-11	MemC11.sil	Lampson	Be	7/17/85	11



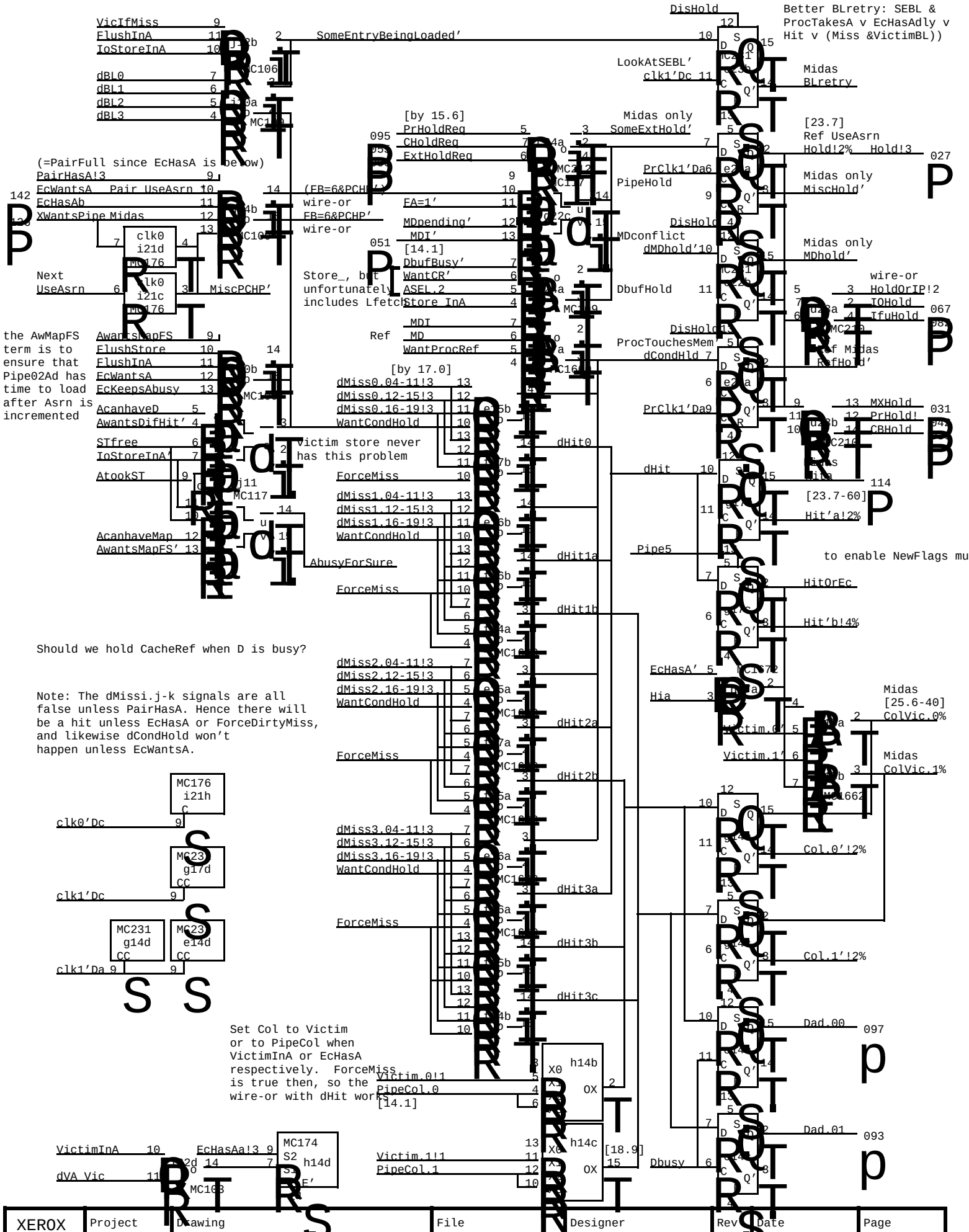
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CVA and comparators: 12-19	MemC12.sil	Lampson	Be	7/30/85	12

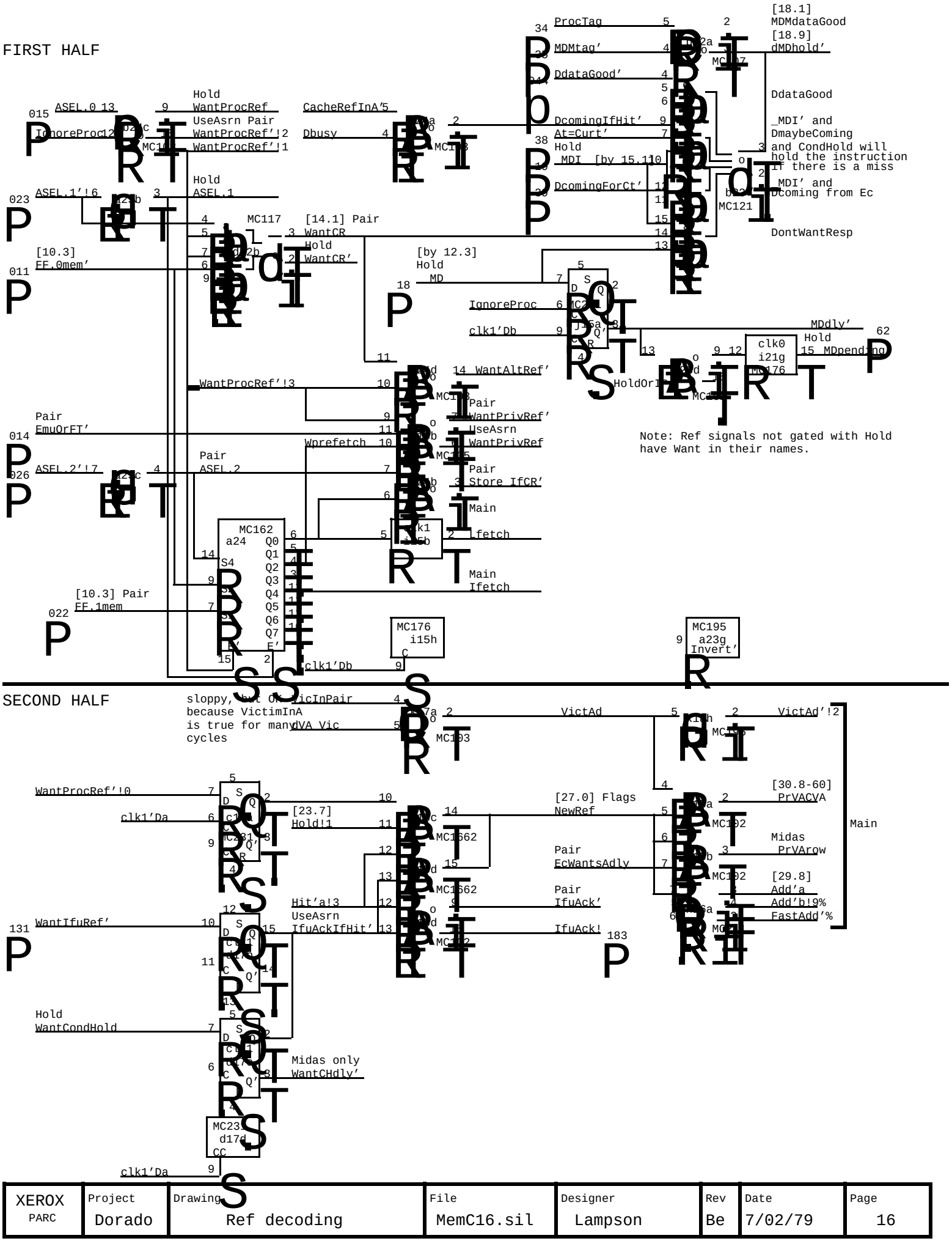


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	A memory addressing	MemC13.sil	Lampson	Be	7/17/85	13

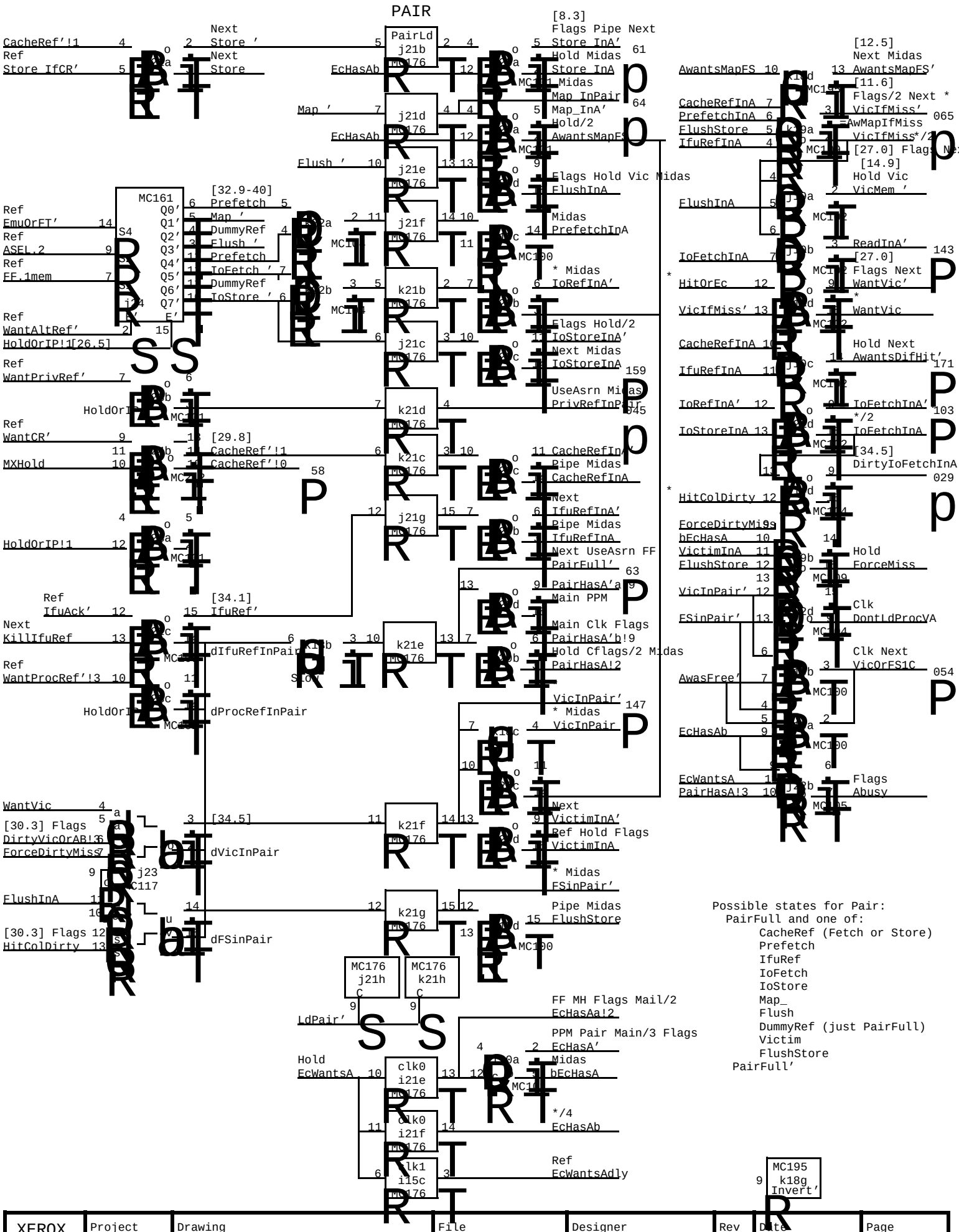


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Carry logic and misc control Pipe and BR addressing	MemC14.sil	Lampson	Be	7/01/79	14


VicIfMiss
FlushInA
IoStoreInA
dBL0
dBL1
dBL2
dBL3
SomeEntryBeingLoaded'
(=PairFull since EcHasA is below)
PairHasA!3
EcWantsA
EcHasAb
XWantsPipe
Pair
Midas
UseAsrn
Next
clk0 i21d MC176
clk0 i21c MC176
MiscPCHP'
(FB=6&PCHP)' wire-or
FB=6&PCHP' wire-or
[by 15.6]
PrHoldReq
CHoldReq
ExtHoldReq
FA=1'
MDpending'
MDI'
[14.1]
DbufBusy'
WantCR'
ASEL.2
Store_, but unfortunately includes Lfetch
Store InA
MDI
Ref
MD
WantProcRef
[by 17.0]
dMiss0.04-11!3
dMiss0.12-15!3
dMiss0.16-19!3
WantCondHold
dMiss1.04-11!3
dMiss1.12-15!3
dMiss1.16-19!3
dMiss2.04-11!3
dMiss2.12-15!3
dMiss2.16-19!3
dMiss3.04-11!3
dMiss3.12-15!3
dMiss3.16-19!3
ForceMiss
AwantsMapFS
FlushStore
FlushInA
EcWantsA
EcKeepsAbusy
AcanhaveD
AwantsDifHit'
STfree
IoStoreInA'
AtookST
AcanhaveMap
AwantsMapFS'
Victim store never has this problem
AbusyForSure
the AwMapFS term is to ensure that Pipe02Ad has time to load after Asrn is incremented
Should we hold CacheRef when D is busy?
Note: The dMissi.j-k signals are all false unless PairHasA. Hence there will be a hit unless EcHasA or ForceDirtyMiss, and likewise dCondHold won't happen unless EcWantsA.
MC176 i21h
clk0'Dc
MC231 g17d
clk1'Dc
MC231 g14d
MC231 e14d
clk1'Da
Set Col to Victim or to PipeCol when VictimInA or EcHasA respectively. ForceMiss is true then, so the wire-or with dHit works.
VictimInA
dVA.Vic
EcHasAa!3
MC174 S2 h14d
MC163
dHit0
dHit1a
dHit1b
dHit2a
dHit2b
dHit3a
dHit3b
dHit3c
h14b
h14c
Victim.0!1
PipeCol.0
[14.1]
Victim.1!1
PipeCol.1
[18.9]
DisHold
Better BLretry: SEBL & ProcTakesA v EcHasAdly v Hit v (Miss &VictimBL))
LookAtSEBL'
clk1'Dc
Midas BLretry
Midas only SomeExtHold'
[23.7] Ref UseAsrn Hold!2% Hold!3
PrClk1'Da6
PipeHold
Midas only MiscHold'
DisHold
MDconflict
dMDhold'10
Midas only MDhold'
DbufHold
DisHold
ProcTouchesMem
dCondHld
wire-or HoldOrIP!2
IOHold
IfuHold
Ref Midas RefHold'
PrClk1'Da9
MXHold
PrHold!
CBHold
dHit
[23.7-60]
Hit'a!2%
Pipe5
to enable NewFlags mu
HitOrEc
Hit'b!4%
EcHasA'
Hia
Midas [25.6-40] ColVic.0%
Victim.0'
Victim.1'
Midas ColVic.1%
Col.0'!2%
Col.1'!2%
Dad.00
Dad.01
Dbusy
XERO X PARC
Project Dorado
Drawing Miss, Hold
File MemC15.sil
Designer Lampson
Rev Be
Date 7/01/79
Page 15



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Ref decoding	MemC16.sil	Lampson	Be	7/02/79	16


PAIR
CacheRef'!1
Ref
Store IfCR'
Next
Store '
Next
Store
PairLd
j21b
EcHasAb
[8.3]
Flags Pipe Next
Store InA'
Hold Midas
Store InA
Midas
Map InPair
Map_InA'
Hold/2
AwantsMapFS
Flags Hold Vic Midas
FlushInA
Midas
PrefetchInA
* Midas
IoRefInA'
Flags Hold/2
IoStoreInA'
Next Midas
IoStoreInA
UseAsrn Midas
PrivRefInPair'
CacheRefInA'
Pipe Midas
CacheRefInA
Next
IfuRefInA'
Pipe Midas
IfuRefInA
Next UseAsrn FF
PairFull'
PairHasA'a!9
Main PPM
Main Clk Flags
PairHasA'b!9
Hold Cflags/2 Midas
PairHasA!2
VicInPair'
* Midas
VicInPair
Next
VictimInA'
Ref Hold Flags
VictimInA
* Midas
FSinPair'
Pipe Midas
FlushStore
Map '
Flush '
[32.9-40]
Prefetch
Map '
DummyRef
Flush '
IoFetch '
DummyRef
IoStore '
MC161
Ref
EmuOrFT'
Ref
ASEL.2
Ref
FF.1mem
Ref
WantAltRef'
HoldOrIP!1[26.5]
Ref
WantPrivRef'
Ref
WantCR'
MXHold
HoldOrIP!1
Ref
IfuAck'
Next
KillIfuRef
Ref
WantProcRef'!3
HoldOrIP!1
[29.8]
CacheRef'!1
CacheRef'!0
[34.1]
IfuRef'
dIfuRefInPair
dProcRefInPair
WantVic
[30.3] Flags
DirtyVicOrAB!3
ForceDirtyMiss
FlushInA
[30.3] Flags
HitColDirty
[34.5]
dVicInPair
dFSinPair
MC176
j21h
MC176
k21h
LdPair'
Hold
EcWantsA
FF MH Flags Mail/2
EcHasAa!2
PPM Pair Main/3 Flags
EcHasA'
Midas
bEcHasA
*/4
EcHasAb
Ref
EcWantsAdly
MC195
k18g
Invert'
[12.5]
Next Midas
AwantsMapFS'
[11.6]
Flags/2 Next *
VicIfMiss'
AwMapIfMiss
VicIfMiss*/2
[27.0] Flags Next
[14.9]
Hold Vic
VicMem '
ReadInA'
[27.0]
Flags Next
WantVic'
*
WantVic
Hold Next
AwantsDifHit'
IoFetchInA'
*/2
IoFetchInA
[34.5]
DirtyIoFetchInA'
Hold
ForceMiss
Clk
DontLdProcVA
Clk Next
VicOrFS1C
Flags
Abusy
AwantsMapFS
CacheRefInA
PrefetchInA
FlushStore
IfuRefInA
FlushInA
IoFetchInA
HitOrEc
VicIfMiss'
CacheRefInA
IfuRefInA
IoRefInA'
IoStoreInA
HitColDirty
ForceDirtyMiss
bEcHasA
VictimInA
FlushStore
VicInPair'
FSinPair'
AwasFree'
EcHasAb
EcWantsA
PairHasA!3
Possible states for Pair:
PairFull and one of:
CacheRef (Fetch or Store)
Prefetch
IfuRef
IoFetch
IoStore
Map_
Flush
DummyRef (just PairFull)
Victim
FlushStore
PairFull'
XEROX
PARC
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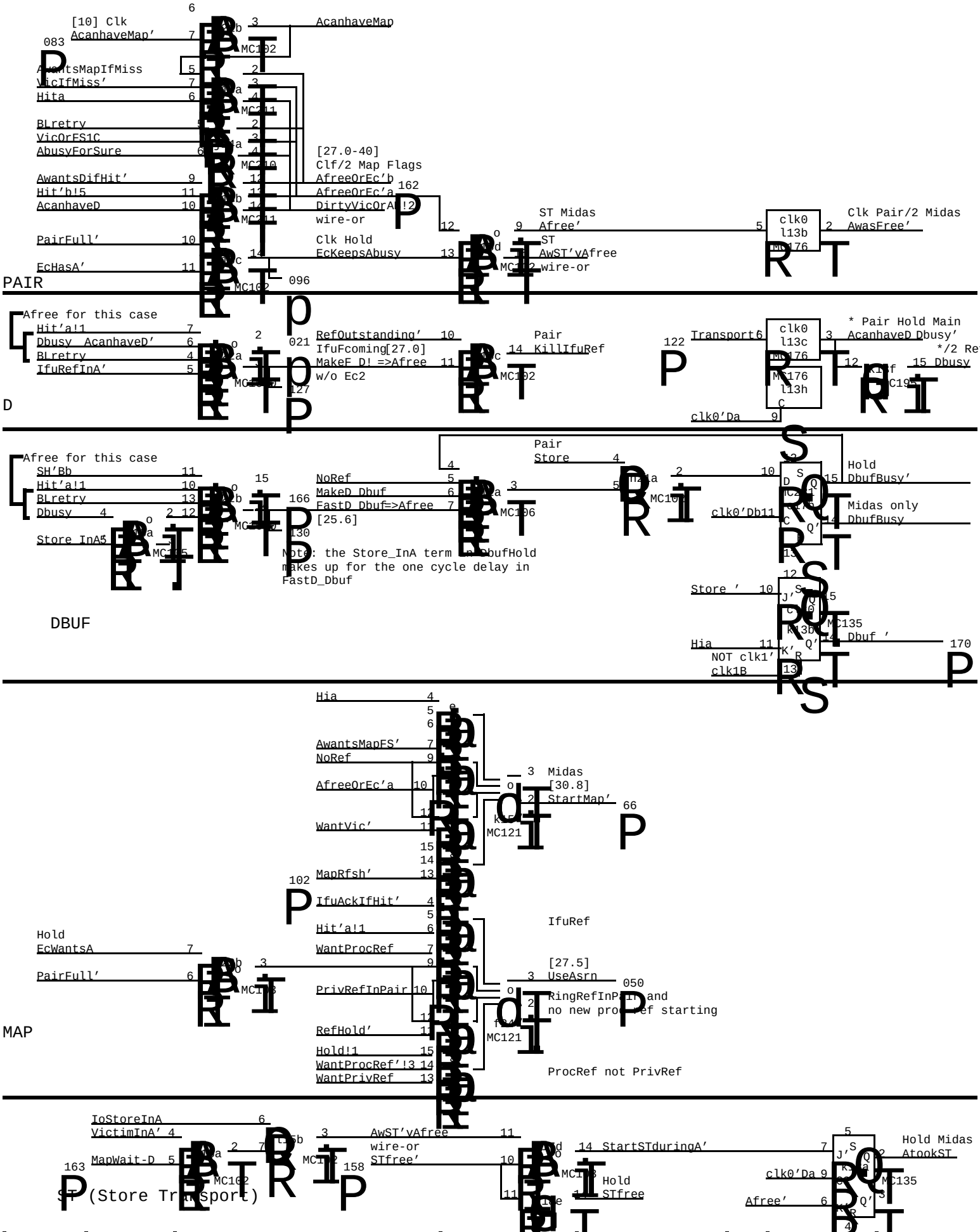
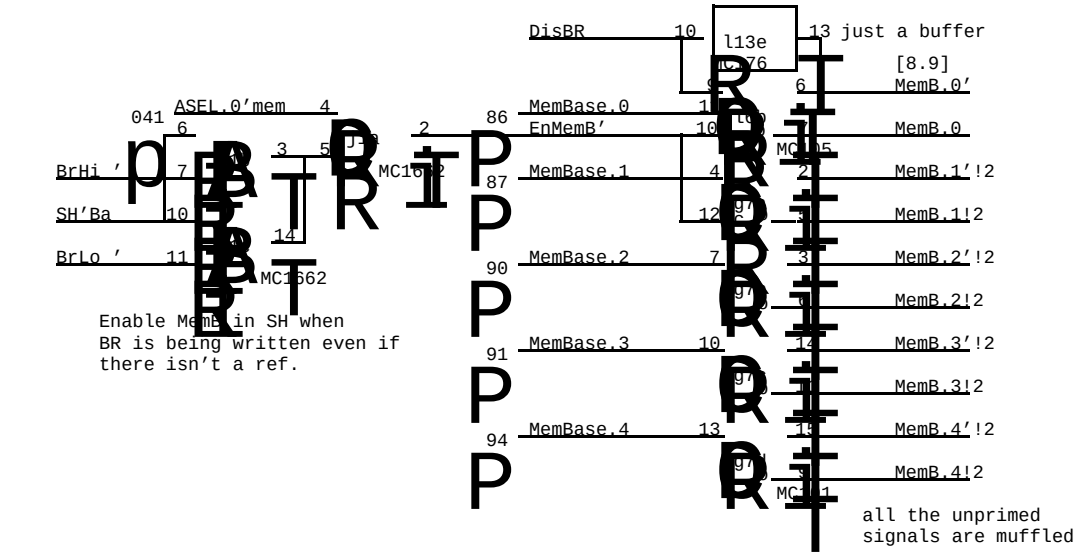
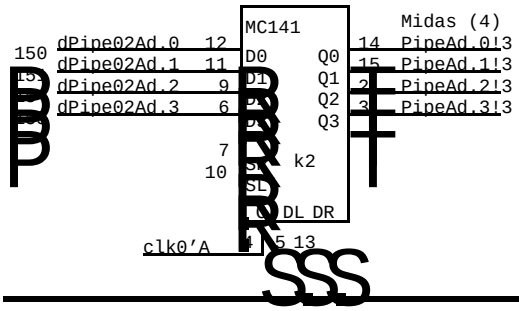
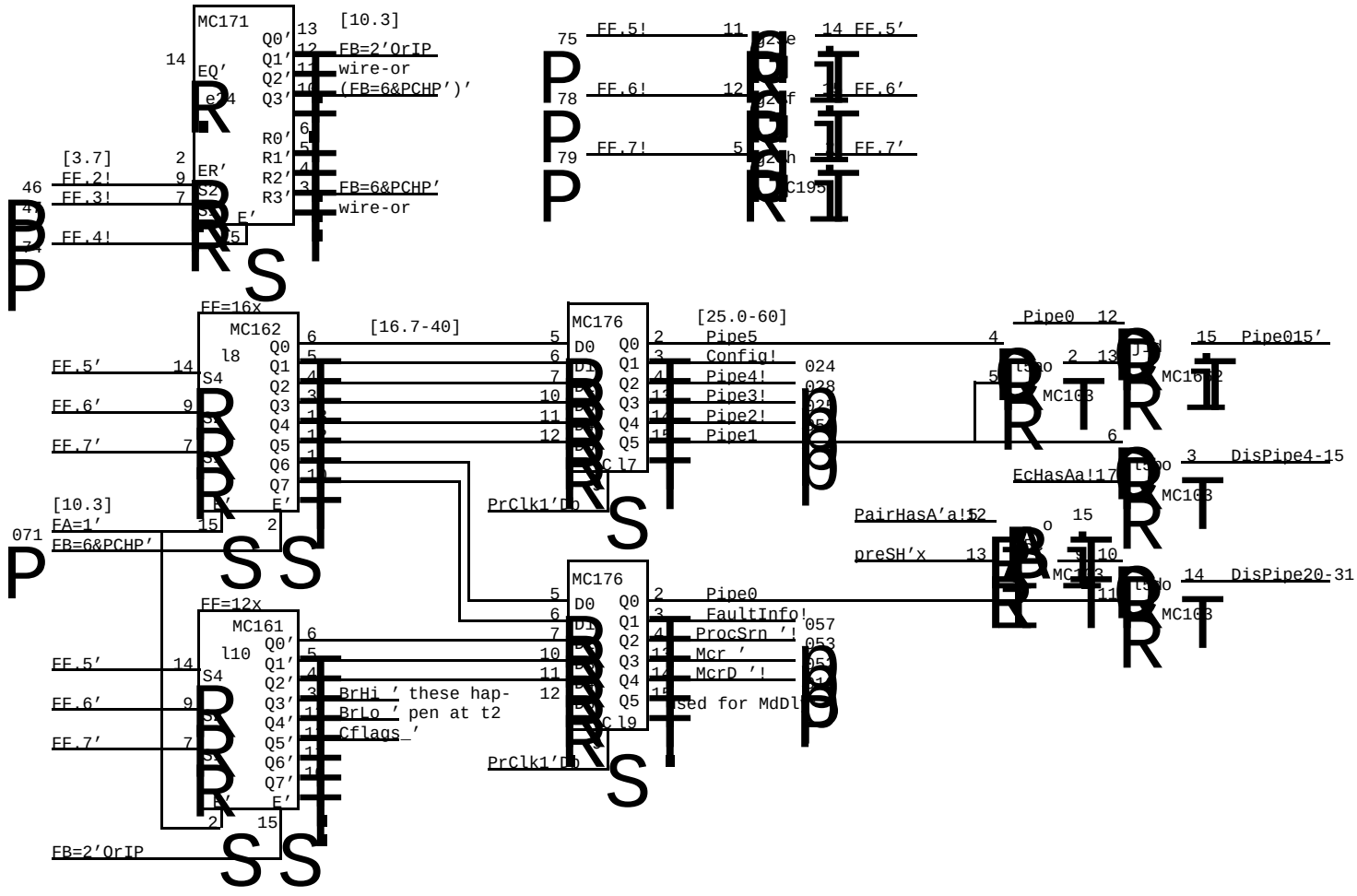


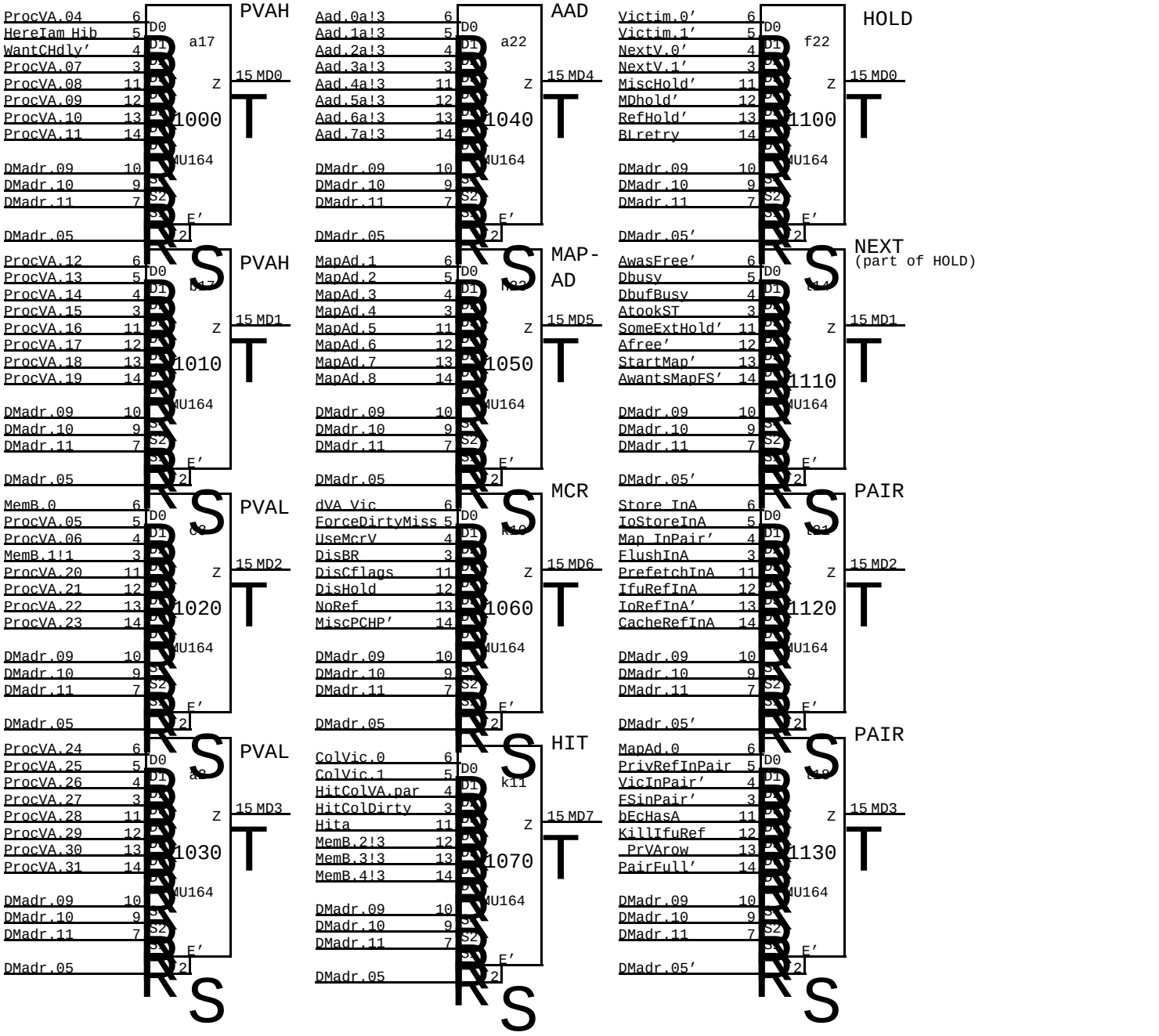
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Next	MemC18.sil	Lampson	Be	7/17/85	18

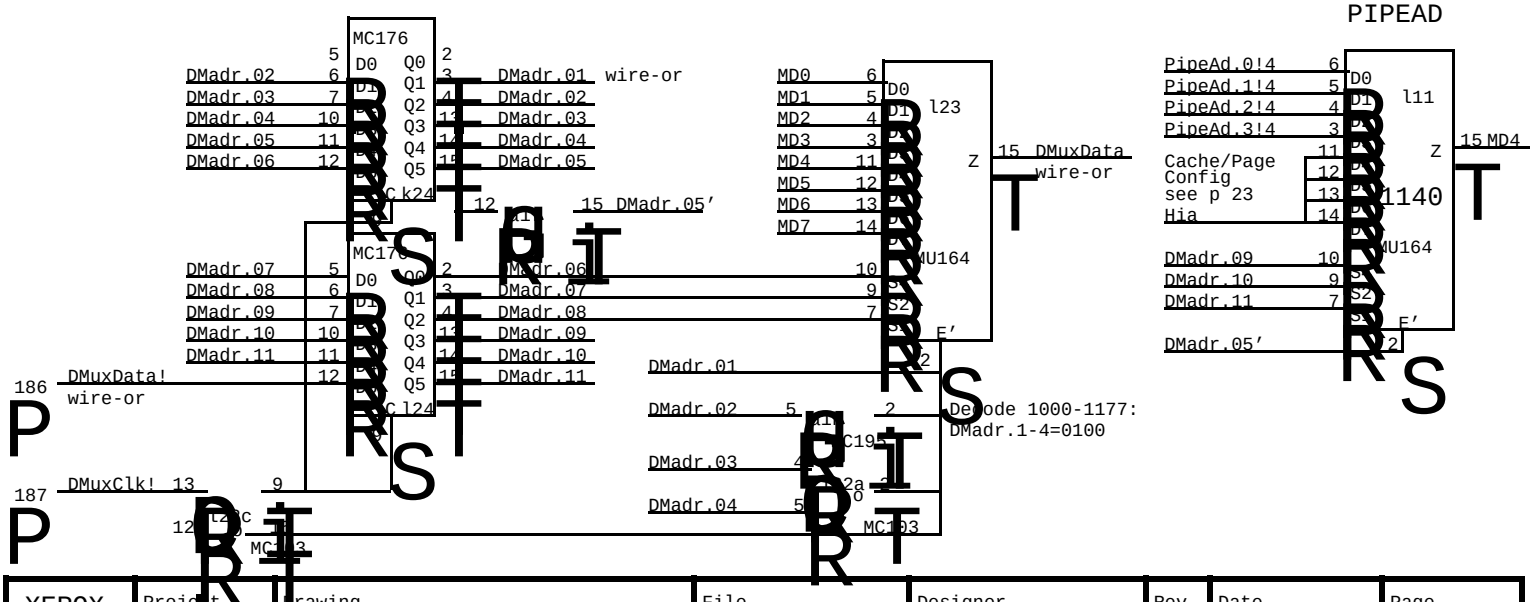




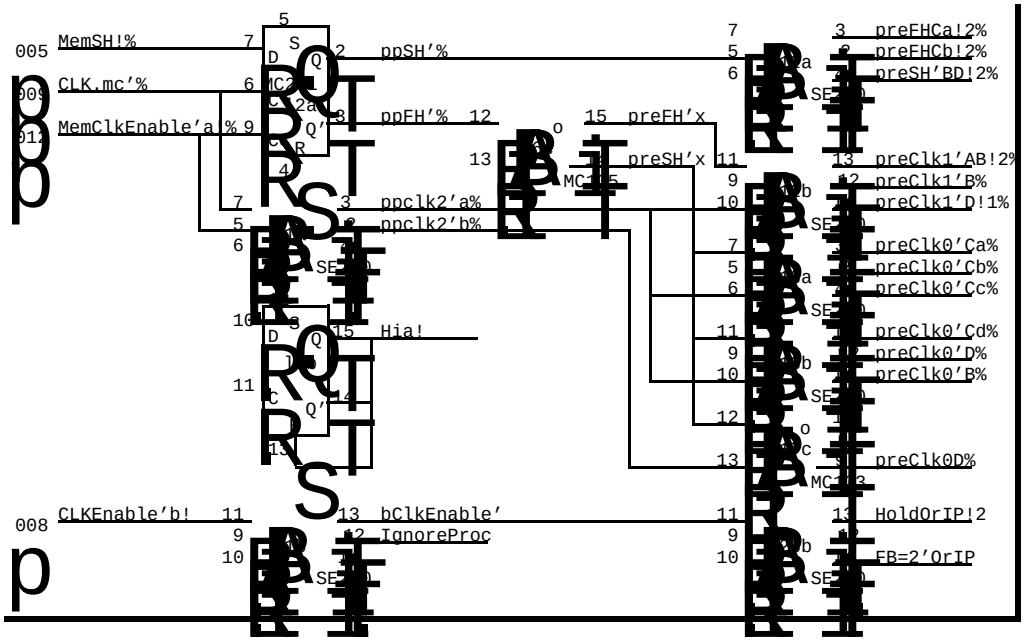


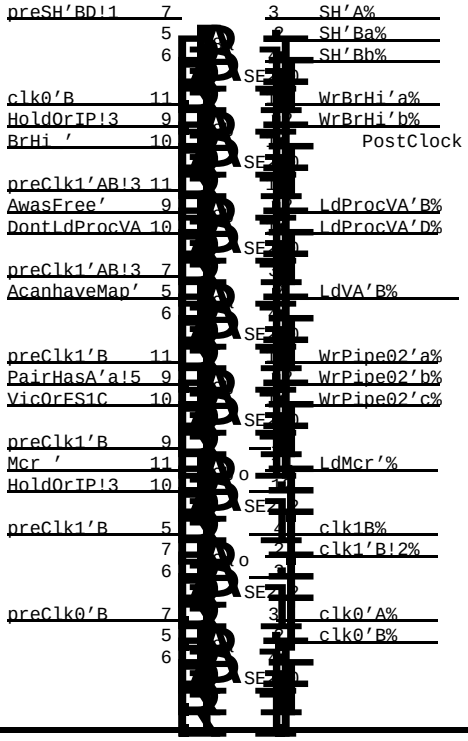
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	FF decoding, PipeAd, Mem	MemC19.sil	Lampson	Be	7/17/85	19

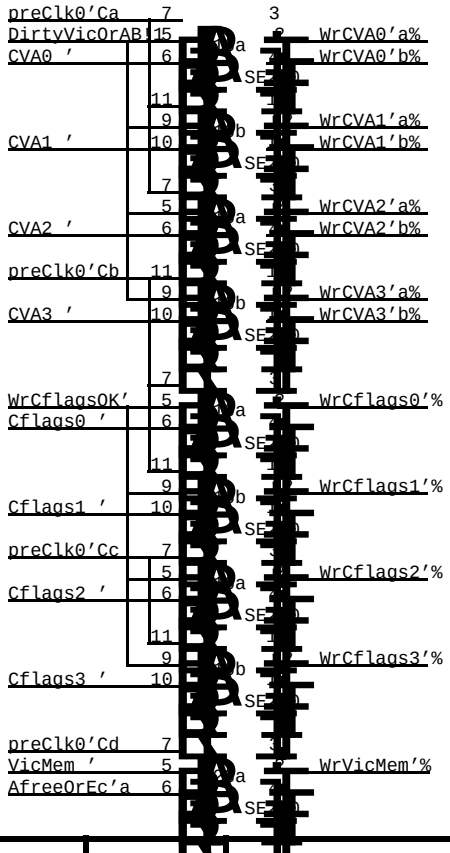




XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Midas control and mufflers	MemC20.sil	Lampson	Be	7/17/85	20





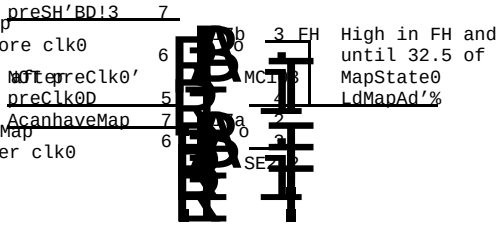


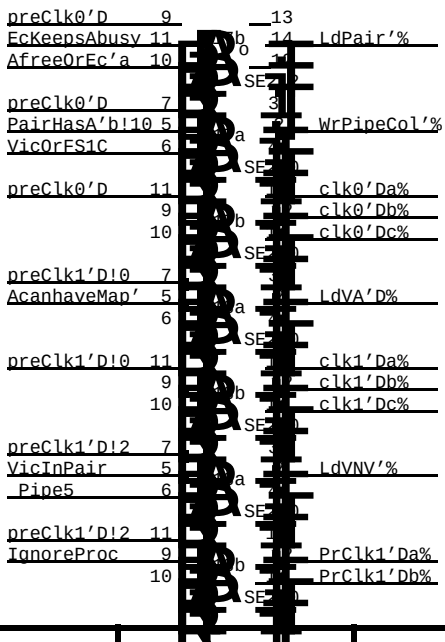
MapAd must be

low by 12.8 before clk0 of StartMap
to:let row MapAd through by 6 before clk0

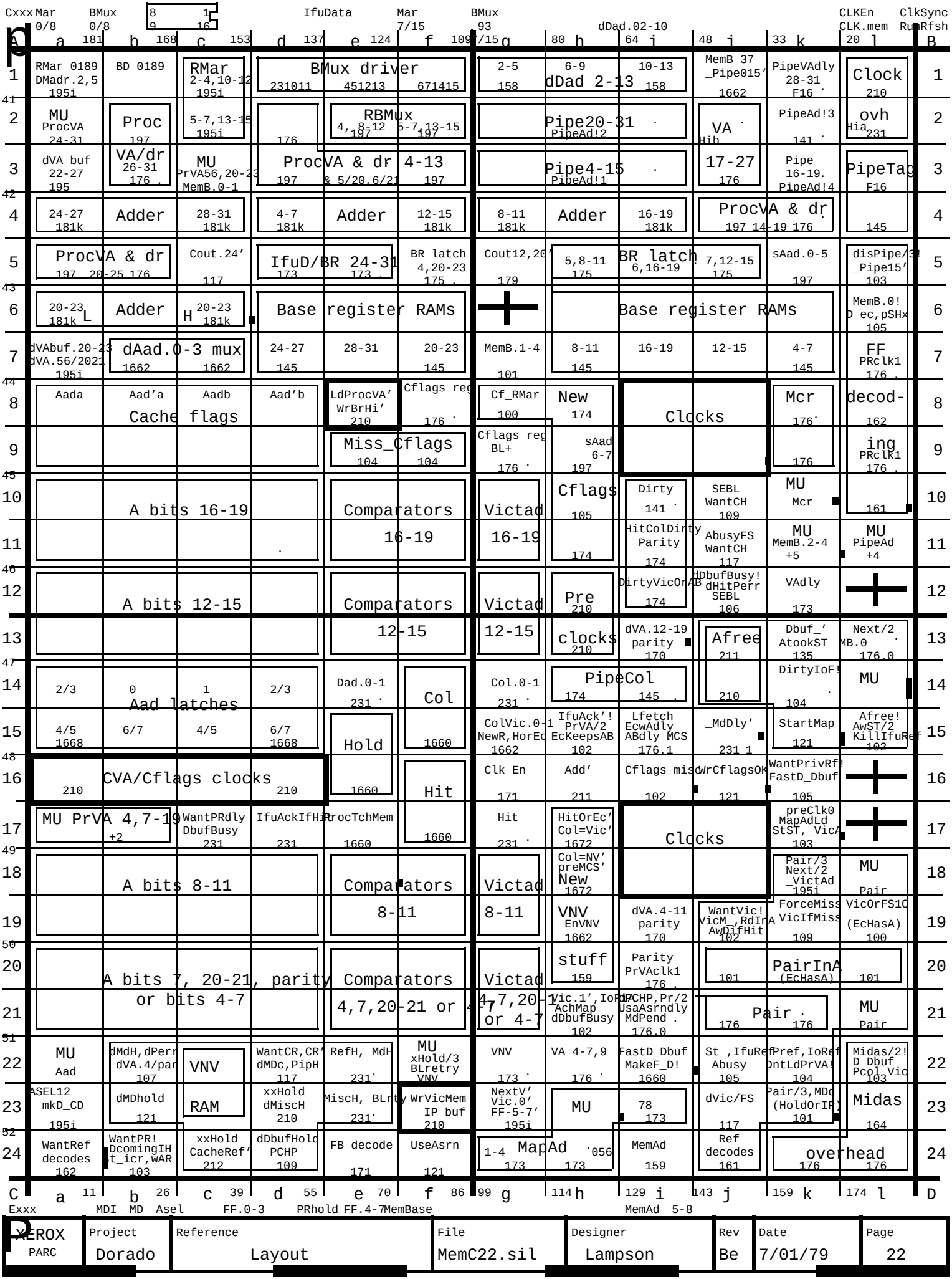
high from clk0 or StartMap to 27.5 after clk0
to:hold row MapAd

low by 2.8 before clk0 after StartMap
to:let col MapAd through by 4 after clk0





XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clock distribution	MemC21.sil	Lampson	Be	7/01/79	21


Cxxx Mar 0/8 BMux 0/8 8 9 1 16 IfuData Mar 7/15 BMux 93 7/15 dDad.02-10 CLKEn CLK.mem ClkSync Run Rfsh
A a 181 b 168 c 153 d 137 e 124 f 109 g 80 h 64 i 48 j 33 k 20 l B
RMar 0189 DMadr.2,5 195i
BD 0189
RMar 2-4,10-12 195i
5-7,13-15 195i
BMux driver 231011 451213 671415
2-5 158
6-9 dDad 2-13 158
10-13
MemB_37 _Pipe015' 1662
PipeVAdly 28-31 F16
Clock 210
MU ProcVA 24-31
Proc 197
RBMux 4, 8-12 197 5-7, 13-15 197
Pipe20-31 PipeAd!2
VA Hib
PipeAd!3 141
ovh Hia 231
dVA buf 22-27 195
VA/dr 26-31 176
MU PrVA56,20-23 MemB.0-1
ProcVA & dr 4-13 197 & 5/20.6/21 197
Pipe4-15 PipeAd!1
17-27 176
Pipe 16-19. PipeAd!4
PipeTag F16
24-27 181k
Adder
28-31 181k
4-7 181k
Adder
12-15 181k
8-11 181k
Adder
16-19 181k
ProcVA & dr 197 14-19 176
145
ProcVA & dr 197 20-25 176
Cout.24' 117
IfuD/BR 24-31 173 173
BR latch 4,20-23 175
Cout12,20' 179
5,8-11 175
BR latch 6,16-19
7,12-15 175
sAad.0-5 197
disPipe/3! _Pipe15' 103
20-23 181k L
Adder
H 20-23 181k
Base register RAMs
Base register RAMs
MemB.0! D_ec,pSHx 105
dVAbuf.20-23 dVA.56/2021 195i
dAad.0-3 mux 1662 1662
24-27 145
28-31 145
20-23 145
MemB.1-4 101
8-11 145
16-19 145
12-15 145
4-7 145
FF PRclk1 176
Aada
Aad'a
Aadb
Aad'b
Cache flags
LdProcVA' WrBrHi' 210
Cflags reg 176
Cf_RMar 100
New 174
Clocks
Mcr 176
decod- 162
Miss_Cflags 104 104
Cflags reg BL+ 176
sAad 6-7 197
ing PRclk1 176
A bits 16-19
Comparators 16-19
Victad 16-19
Cflags 105
Dirty 141
SEBL WantCH 109
MU Mcr 161
HitColDirty Parity 174
AbusyFS WantCH 117
MU MemB.2-4 +5
MU PipeAd +4
A bits 12-15
Comparators 12-15
Victad 12-15
Pre 210
DirtyVicOrAB 174
dDbufBusy! dHitPerr SEBL 106
VAdly 173
clocks 210
dVA.12-19 parity 170
Afree 211
Dbuf_' AtookST 135
Next/2 MB.0 176.0
Aad latches
2/3
0
1
2/3
Dad.0-1 231
Col 1660
Col.0-1 231
PipeCol 174 145
210
DirtyIoF! 104
MU
4/5 1668
6/7
4/5
6/7 1668
Hold 1660
ColVic.0-1 NewR,HorEc 1662
IfuAck'! _PrVA/2 EcKeepsAB 102
Lfetch EcwAdly ABdly MCS 176.1
_MdDly' 231 1
StartMap 121
Afree! AwST/2 KillIfuRe 102
CVA/Cflags clocks 210 210
Hit 1660
Clk En 171
Add' 211
Cflags miss 102
WrCflagsOK 121
WantPrivRf! FastD_Dbuf 105
MU PrVA 4,7-19 +2
WantPRdly DbufBusy 231
IfuAckIfHit 231
ProcTchMem 1660
Hit 231
HitOrEc' Col=Vic' 1672
Clocks
_preClk0 MapAdLd StST,_VicA 103
A bits 8-11
Comparators 8-11
Victad 8-11
Col=NV' preMCS' New 1672
Pair/3 Next/2 _VictAd 195i
MU Pair
VNV EnVNV 1662
dVA.4-11 parity 170
WantVic! VicM_,RdInA AwDirHit 102
ForceMiss VicIfMiss 109
VicOrFS1C (EcHasA) 100
A bits 7, 20-21, parity or bits 4-7
Comparators 4,7,20-21 or 4-7
Victad 4,7,20-21 or 4-7
stuff 159
Parity PrVAclk1 176
101
PairInA (EcHasA) 101
Vic.1', IoRdA AchMap dDbufBusy 102
dPCHP,Pr/2 UsaAsrndly MdPend 176.0
Pair 176 176
MU Pair
MU Aad
dMdH,dPerr dVA.4/par 107
VNV
RAM
WantCR,CR' dMDc,PipH 117
RefH, MdH 231
MU xHold/3 BLretry VNV
VNV 173
VA 4-7,9 176
FastD_Dbuf MakeF_D! 1660
St_,IfuRef Abusy 105
Pref,IoRef DntLdPrVA! 104
Midas/2! D_Dbuf Pcol_Vic 103
ASEL12 mkD_CD 195i
dMDhold 121
xxHold dMiscH 210
MiscH, BLrty 231
WrVicMem IP buf 210
NextV' Vic.0' FF-5-7' 195i
MU
78 173
dVic/FS 117
Pair/3,MDC (HoldOrIP) 101
Midas 164
WantRef decodes 162
WantPR! DcomingIH t_icr,wAR 103
xxHold CacheRef' 212
dDbufHold PCHP 109
FB decode 171
UseAsrn 121
1-4 MapAd 173 173 056
MemAd 159
Ref decodes 161
overhead 176 176
C a 11 b 26 c 39 d 55 e 70 f 86 g 99 h 114 i 129 j 143 k 159 l 174 D
Exxx _MDI _MD Asel FF.0-3 PRhold FF.4-7 MemBase MemAd 5-8
XEROX PARC
Project Dorado
Reference Layout
File MemC22.sil
Designer Lampson
Rev Be
Date 7/01/79
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CACHE CONFIGURATIONS

4k CacheConfig=3			16k Not used CacheConfig=2			16k without parity Not used CacheConfig=1		
Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)
a03	195	3x 4x cut 5-6 from 5/20-6/21	a03	195	3-6 4-7 connect 5-6 to 5/20-6/21	a03	195	3-6 4-7 connect 5-6 to 5/20-6/21
a07	195	2-15 3-4 connect 20-21 to 5/20-6/21	a07	195	2x 4x cut 20-21 from 5/20-6/21	a07	195	2x 4x cut 20-21 from 5/20-6/21
a05	197	3x 4x read ProcVA.20-21 for CVA	d03	197	2x 15x read ProcVA.20-21 for row	d03	197	2x 15x read ProcVA.20-21 for row
b14	1668	remove disconnect Aad.0						
c14	1668	remove disconnect Aad.1						
e20	113	3x	e20	113	3x	b22	107	7x 9x 14x 15x 6-10 connect 4 to 4/par disconnect Perr reporting
e21	113	3x	e21	113	3x			
f20	113	3x	f20	113	3x			
f21	113	3x keep parity from comparators	f21	113	3x			
g20	174	2x keep parity from CVA	g20	174	2x			
			l11	164	12x make CacheConfig=2	l11	164	11x make CacheConfig=1

PAGE SIZE CONFIGURATIONS

256 words PageConfig=3			1k words Not used PageConfig=2			4k words Not used PageConfig=1		
Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)
i24	159	4x 6x 11x 13x 4-6-11-13-9 MemRA_0 0 0 0	i24	159	11x 13x 11-13-9 MemRA_0 0 22 23			MemRA_20 21 22 23
			h24	173	3x 4x 1-2 MapAd.0_4-5 for 6-7	h24	173	10x 12x 10-3 12-5 MapAd.5,6_5,7 for 20,21
			i23	173	3x 10x 3-5 10-12 MapAd.7,8_6,7 for 22,23	i23	173	3x 10x 3-5 10-13 MapAd.7,8_6,4 for 22,23
			l11	164	14x make PageConfig=2	l11	164	13x make PageConfig=1

C U R R E N T L Y N O N E