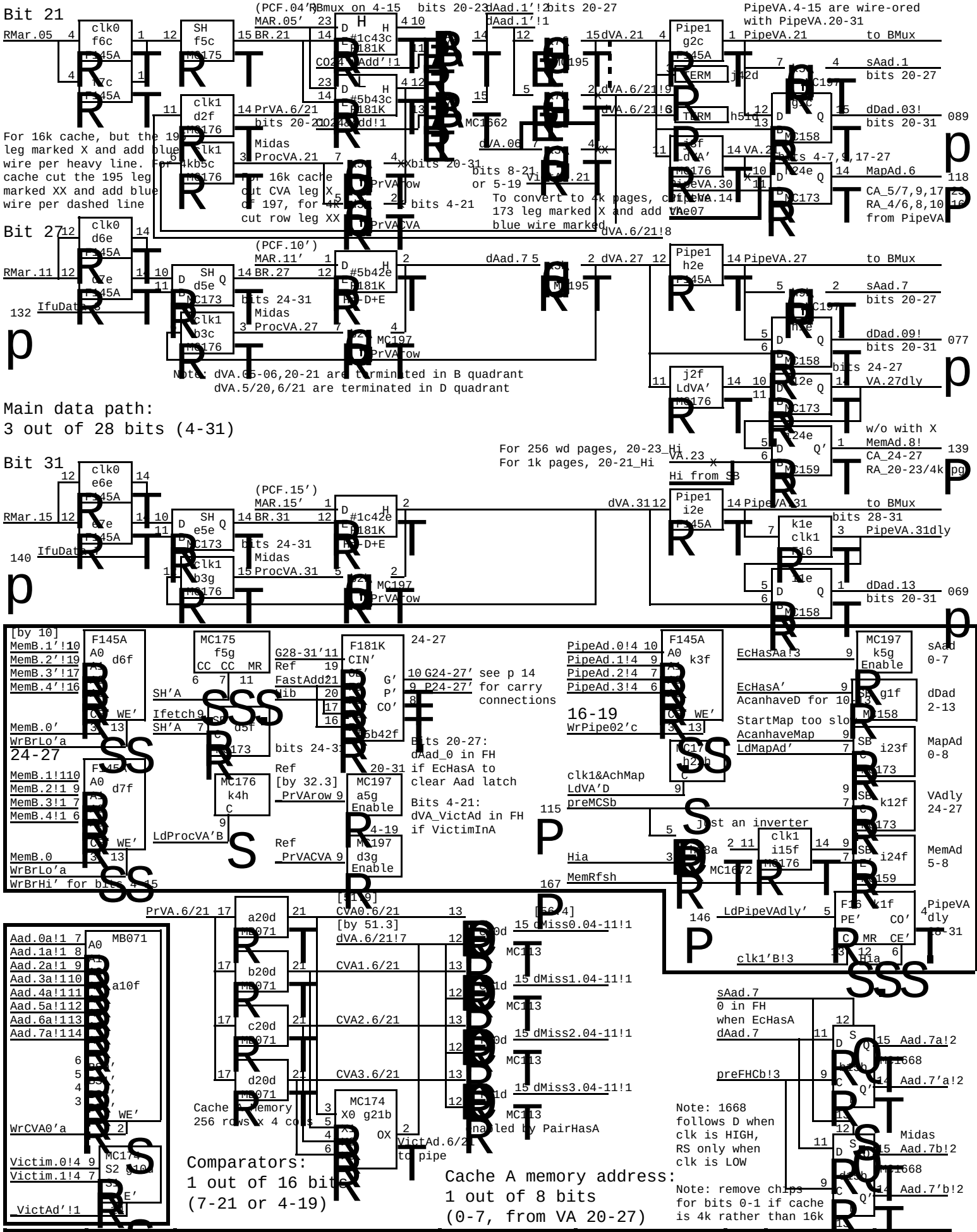
D O R A D O S C H E M A T I C S

M e m o r y C o n t r o l

Table of contents


Bit 21
Bit 27
Bit 31
Main data path:
3 out of 28 bits (4-31)
For 16k cache, but the 19 leg marked X and add blue wire per heavy line. For 4kb5c cache cut the 195 leg marked XX and add blue wire per dashed line
For 16k cache cut CVA leg X of 197, for 4k cut row leg XX
To convert to 4k pages, cut 173 leg marked X and add blue wire marked
Note: dVA.05-06,20-21 are terminated in B quadrant
dVA.5/20,6/21 are terminated in D quadrant
For 256 wd pages, 20-23_Hi
For 1k pages, 20-21_Hi
PipeVA.4-15 are wire-ored with PipeVA.20-31
Comparators:
1 out of 16 bits
(7-21 or 4-19)
Cache A memory address:
1 out of 8 bits
(0-7, from VA 20-27)
Note: 1668 follows D when clk is HIGH, RS only when clk is LOW
Note: remove chips for bits 0-1 if cache is 4k rather than 16k
Cache A memory
256 rows x 4 cols
enabled by PairHasA
XEROX
PARC
Project
Dorado
Drawing
Main data paths
File
MemC01.sil
Designer
Lampson
Rev
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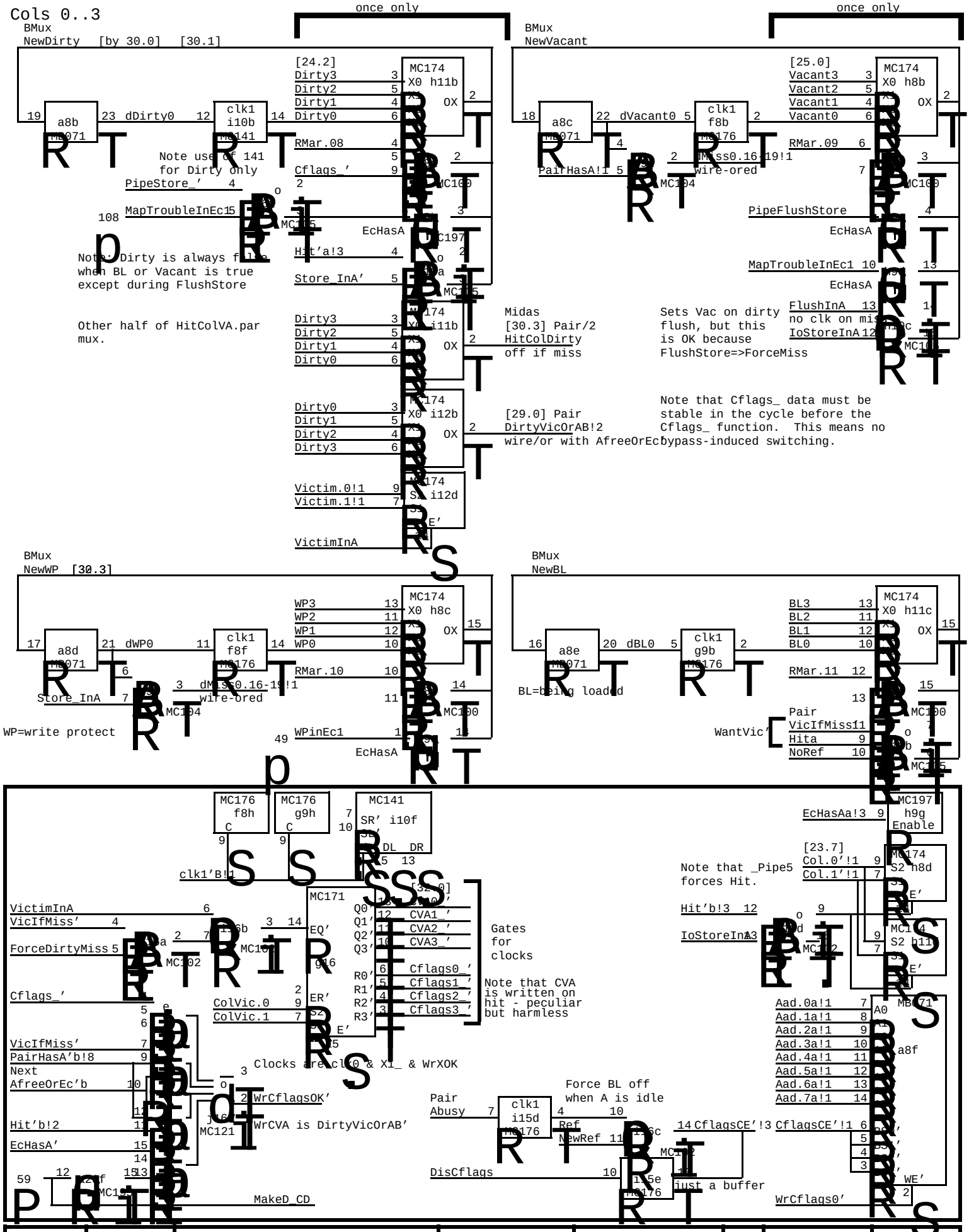
Cols 0..3
BMux
NewDirty [by 30.0] [30.1]
once only
a8b
MB071
clk1
i10b
MC141
dDirty0
Note use of 141
for Dirty only
PipeStore_'
MapTroubleInEc1
[24.2]
Dirty3
Dirty2
Dirty1
Dirty0
RMar.08
Cflags_'
MC174
X0 h11b
OX
MC100
MC105
EcHasA
MC197
Hit'a!3
Store_InA'
Note: Dirty is always false
when BL or Vacant is true
except during FlushStore
Other half of HitColVA.par
mux.
Midas
[30.3] Pair/2
HitColDirty
off if miss
[29.0] Pair
DirtyVicOrAB!2
wire/or with AfreeOrEc
BMux
NewVacant
once only
a8c
MB071
clk1
f8b
MC176
dVacant0
[25.0]
Vacant3
Vacant2
Vacant1
Vacant0
RMar.09
PairHasA!1
dMiss0.16-19!1
wire-ored
MC104
PipeFlushStore
EcHasA
MapTroubleInEc1
FlushInA
no clk on mis
IoStoreInA
Sets Vac on dirty
flush, but this
is OK because
FlushStore=>ForceMiss
Note that Cflags_ data must be
stable in the cycle before the
Cflags_ function. This means no
bypass-induced switching.
BMux
NewWP [30.3]
a8d
MB071
clk1
f8f
MC176
dWP0
WP3
WP2
WP1
WP0
RMar.10
dMiss0.16-19!1
wire-ored
MC104
Store_InA
WP=write protect
WPinEc1
EcHasA
BMux
NewBL
a8e
MB071
clk1
g9b
MC176
dBL0
BL3
BL2
BL1
BL0
RMar.11
BL=being loaded
Pair
VicIfMiss
Hita
NoRef
WantVic'
MC141
SR' i10f
DL DR
clk1'B!1
MC171
Q0'
Q1'
Q2'
Q3'
CVA1_'
CVA2_'
CVA3_'
Gates
for
clocks
Note that CVA
is written on
hit - peculiar
but harmless
VictimInA
VicIfMiss'
ForceDirtyMiss
Cflags_'
ColVic.0
ColVic.1
EQ'
ER'
S2
VicIfMiss'
PairHasA'b!8
Next
AfreeOrEc'b
Hit'b!2
EcHasA'
Clocks are clk0 & X1_ & WrXOK
WrCflagsOK'
WrCVA is DirtyVicOrAB'
MakeD_CD
Pair
Abusy
clk1
i15d
MC176
Ref
NewRef
Force BL off
when A is idle
DisCflags
just a buffer
CflagsCE'!3
MC197
h9g
Enable
EcHasAa!3
[23.7]
Col.0'!1
Col.1'!1
Note that _Pipe5
forces Hit.
Hit'b!3
IoStoreInA3
Aad.0a!1
Aad.1a!1
Aad.2a!1
Aad.3a!1
Aad.4a!1
Aad.5a!1
Aad.6a!1
Aad.7a!1
a8f
CflagsCE'!1
WE'
WrCflags0'
XEROX
PARC
Project
Dorado
Drawing
Cache flags
File
MemC02.sil
Designer
Lampson
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7/01/79
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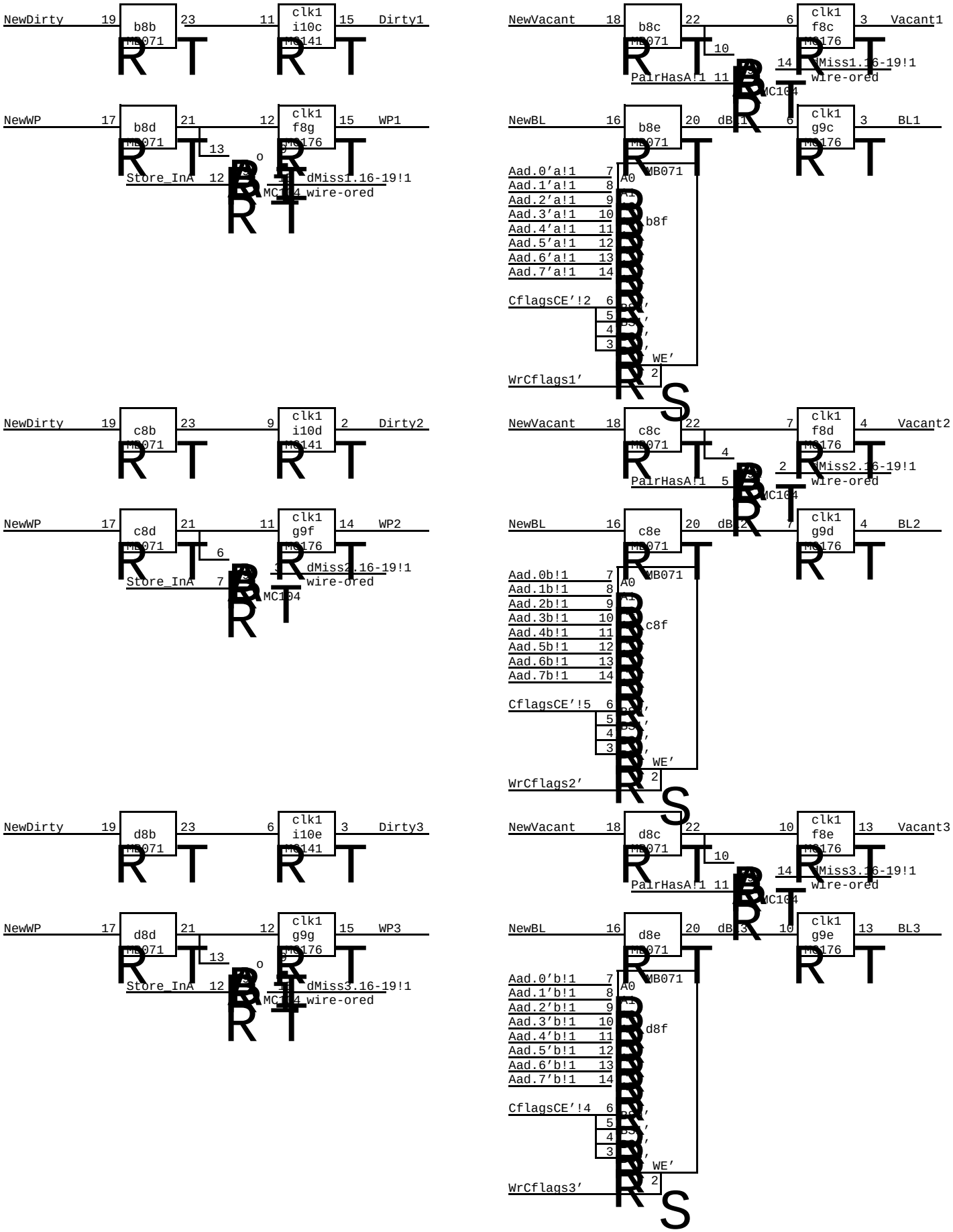
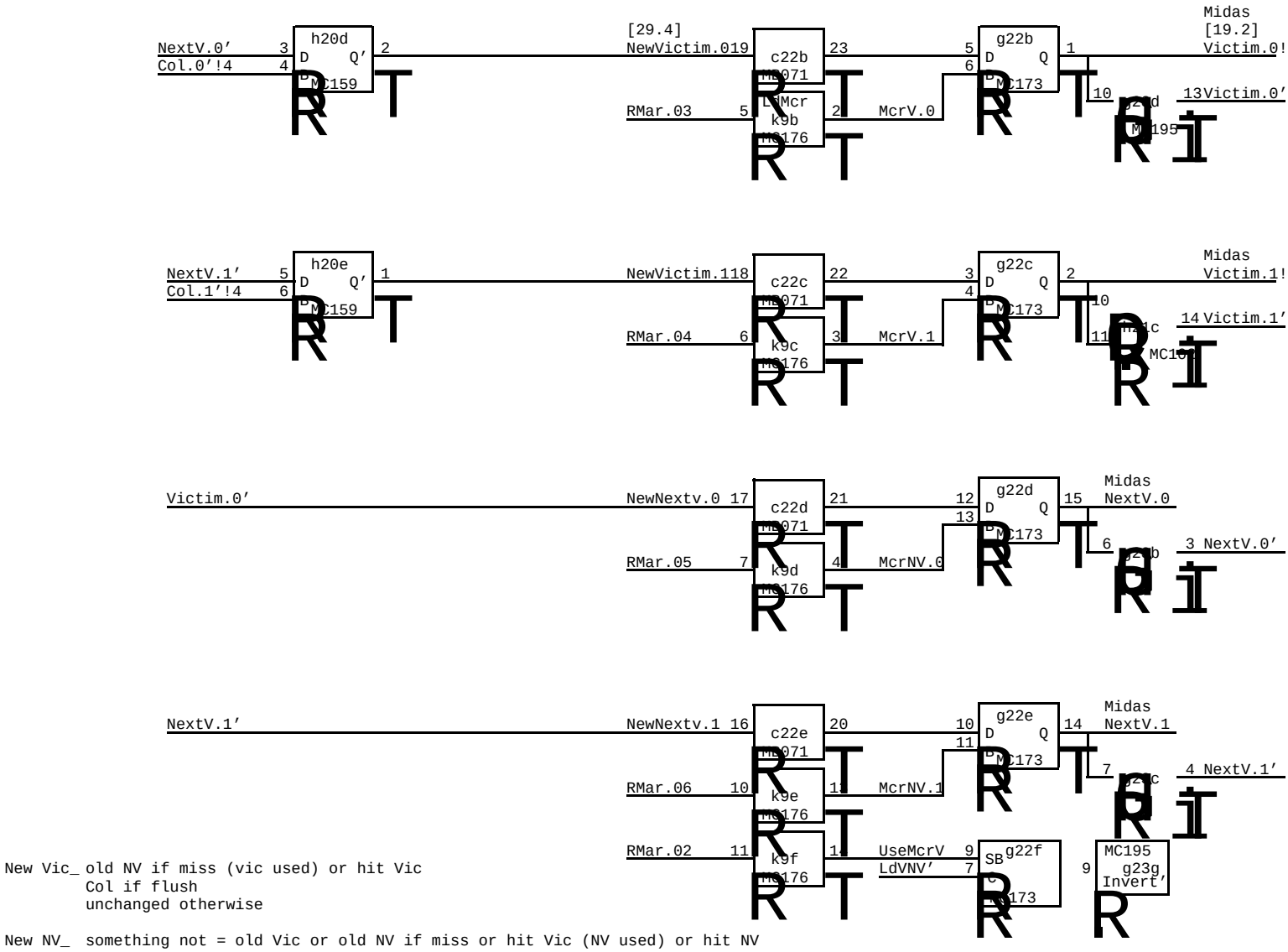
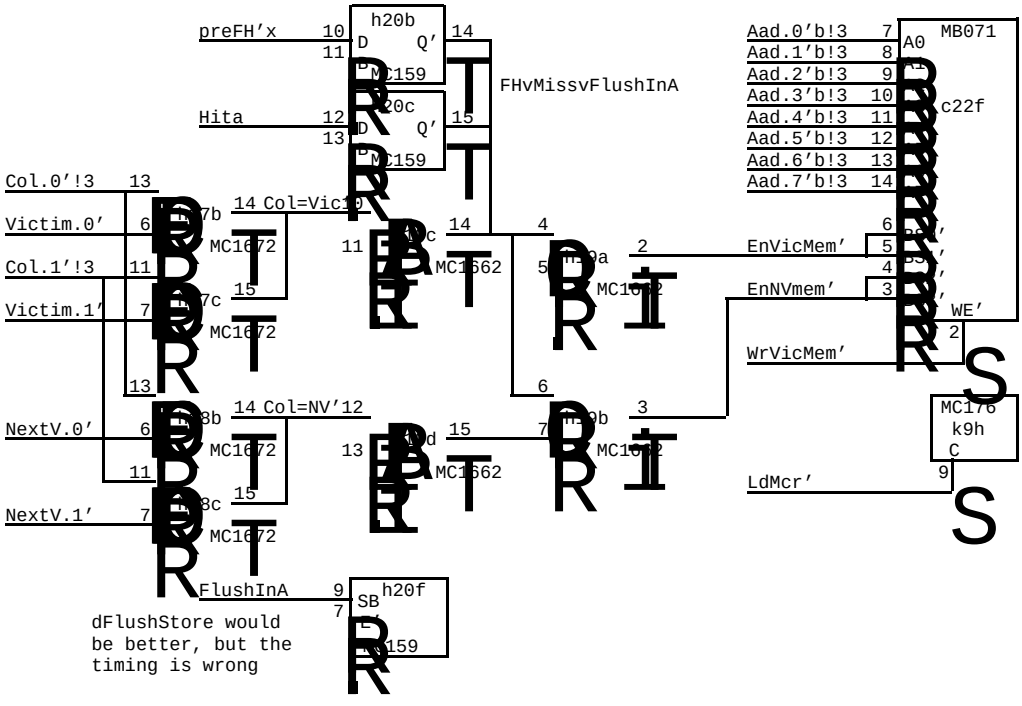


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Cache flags, cols1-3	MemC03.sil	Lampson	Be	7/01/79	03



New Vic_ old NV if miss (vic used) or hit Vic
Col if flush
unchanged otherwise

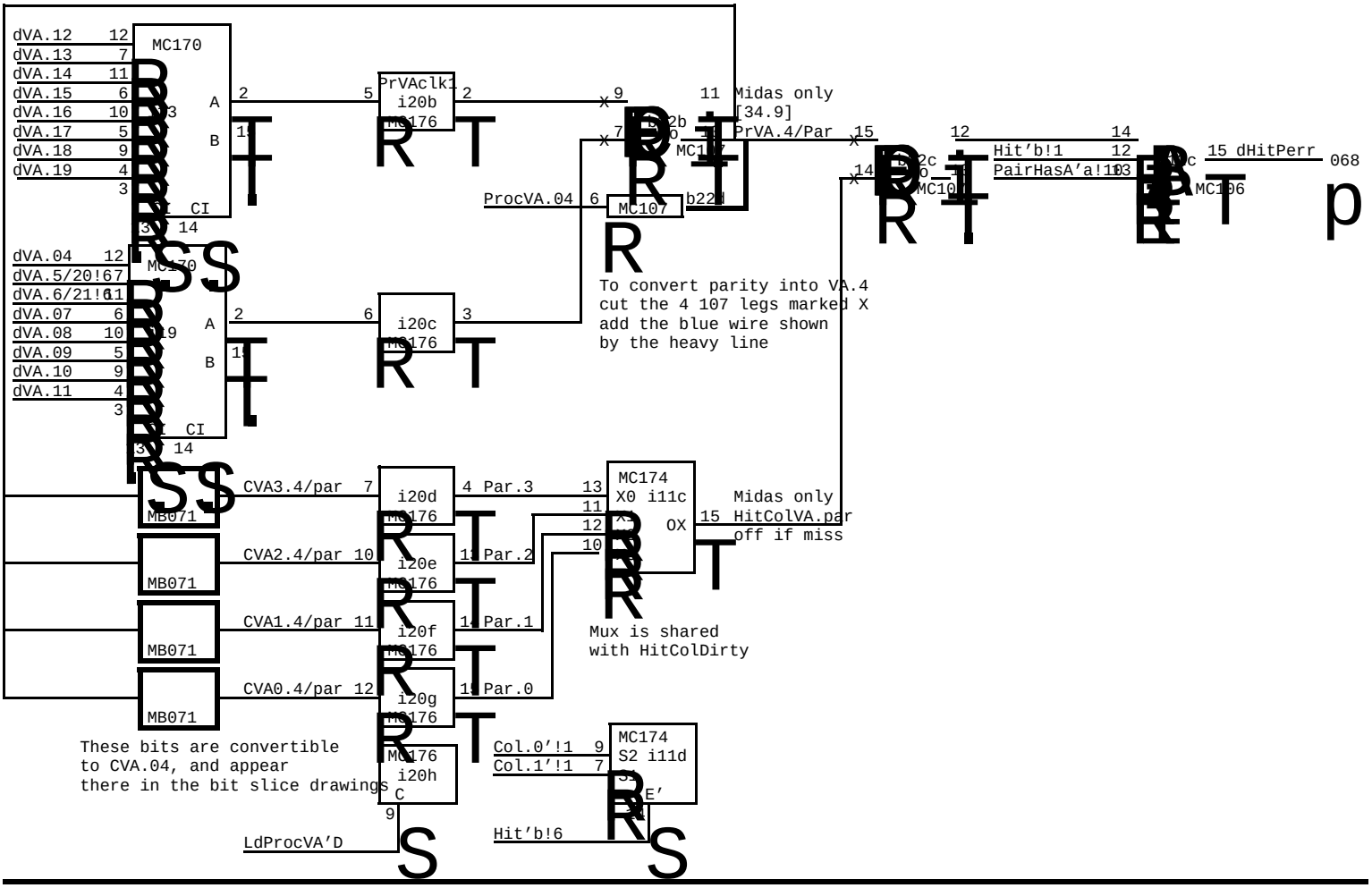
New NV_ something not = old Vic or old NV if miss or hit Vic (NV used) or hit NV
unchanged otherwise (except for flush, which is an accident, not important)

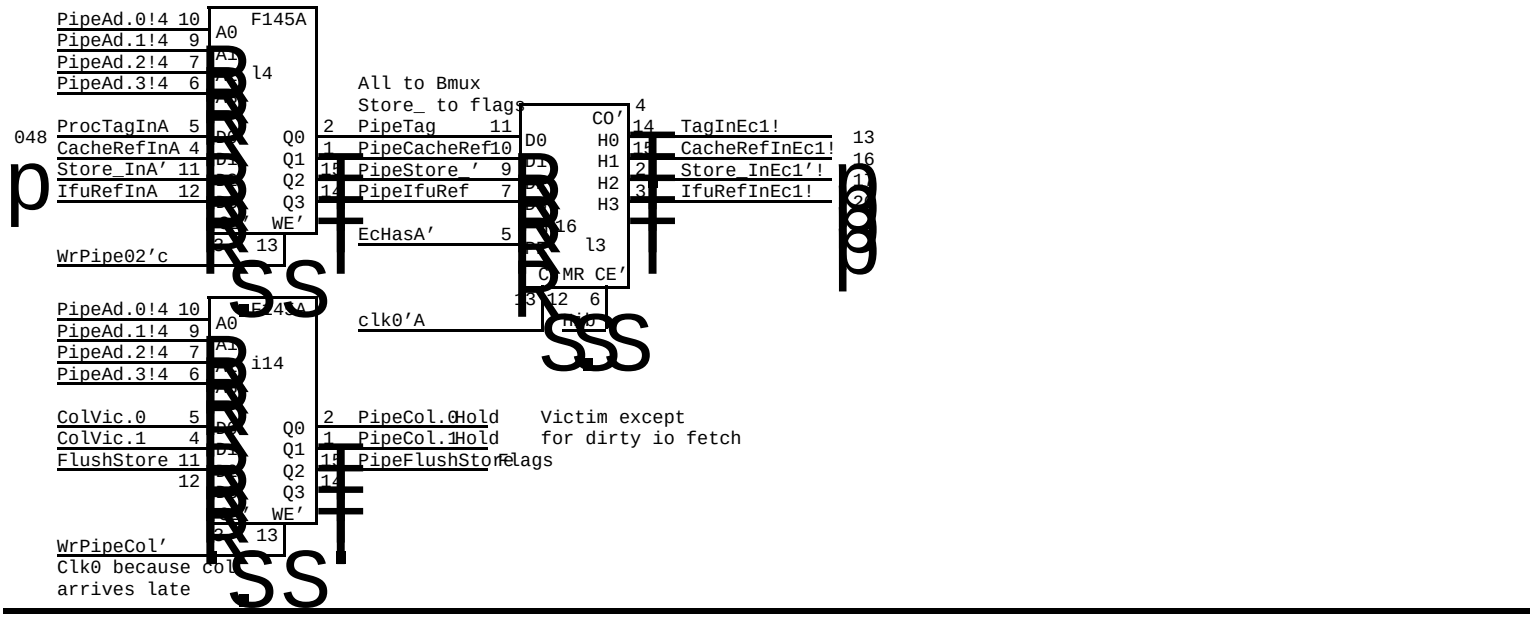


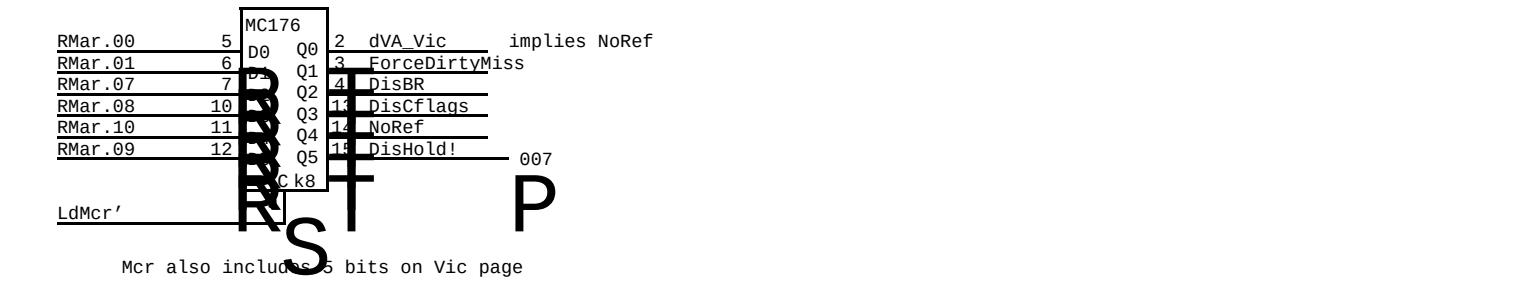
The Victim memory is written on a CacheRef, PreFetch or IfuRef that misses, and on any FlushStore or Flush_.

For a Flush_, Victim is first written with 0 on a miss or with the column of the hit. NextV is garbaged at the same time. On a dirty hit, a FlushStore follows, smashing Victim and NextV again.

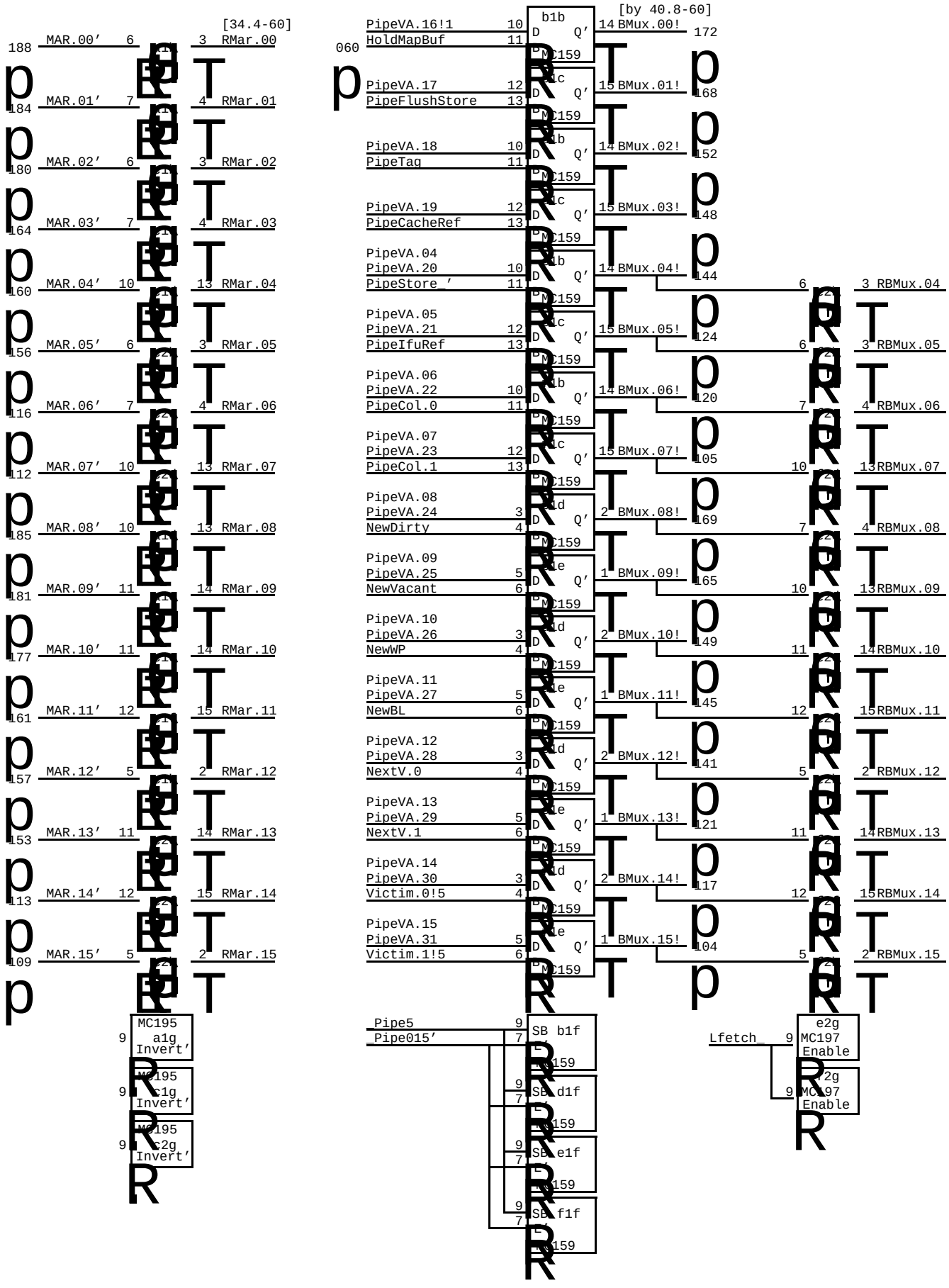
XEROX PARC	Project Dorado	Drawing Victim + NextVictim	File MemC04.sil	Designer Lampson	Rev Be	Date 7/01/79	Page 04



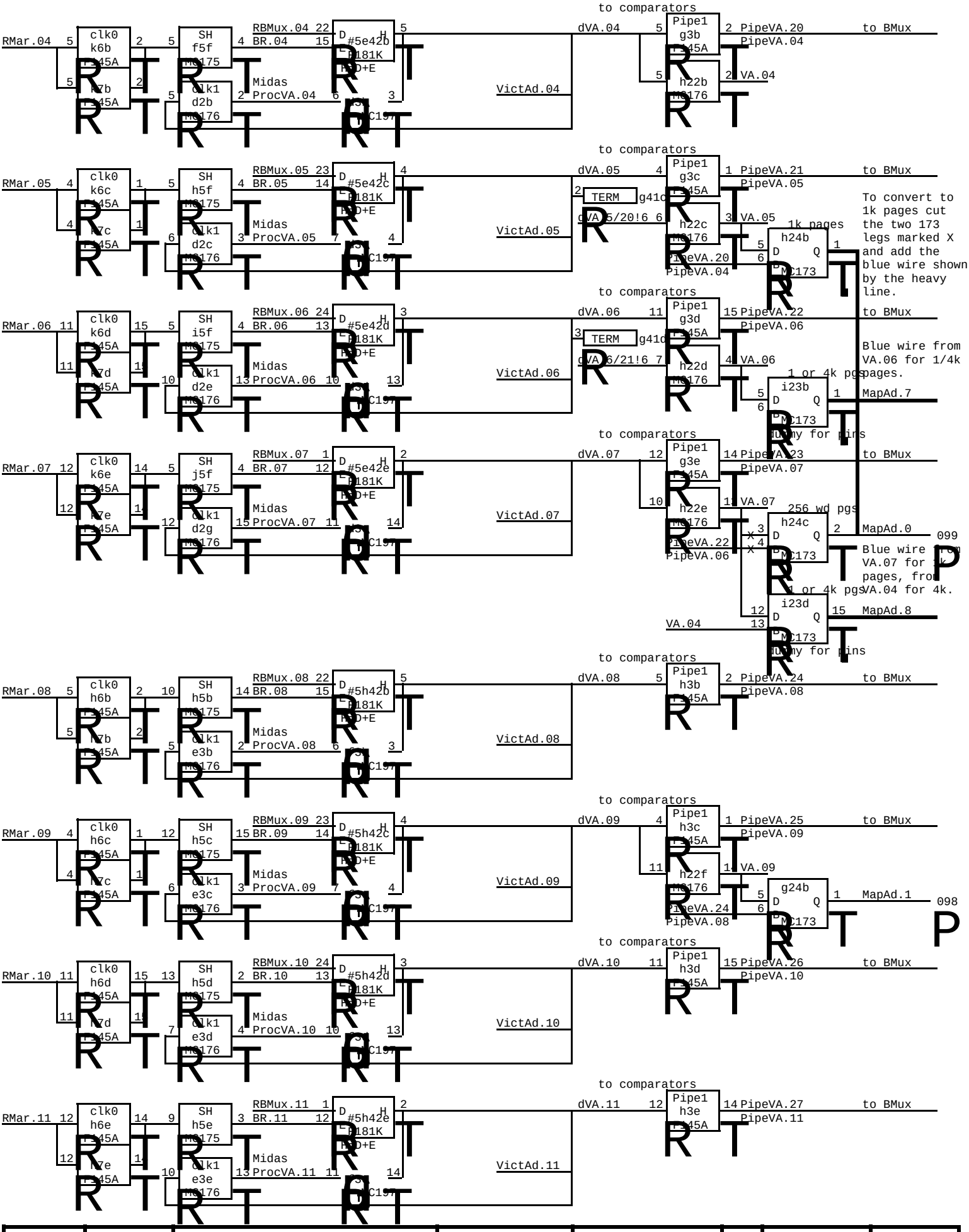




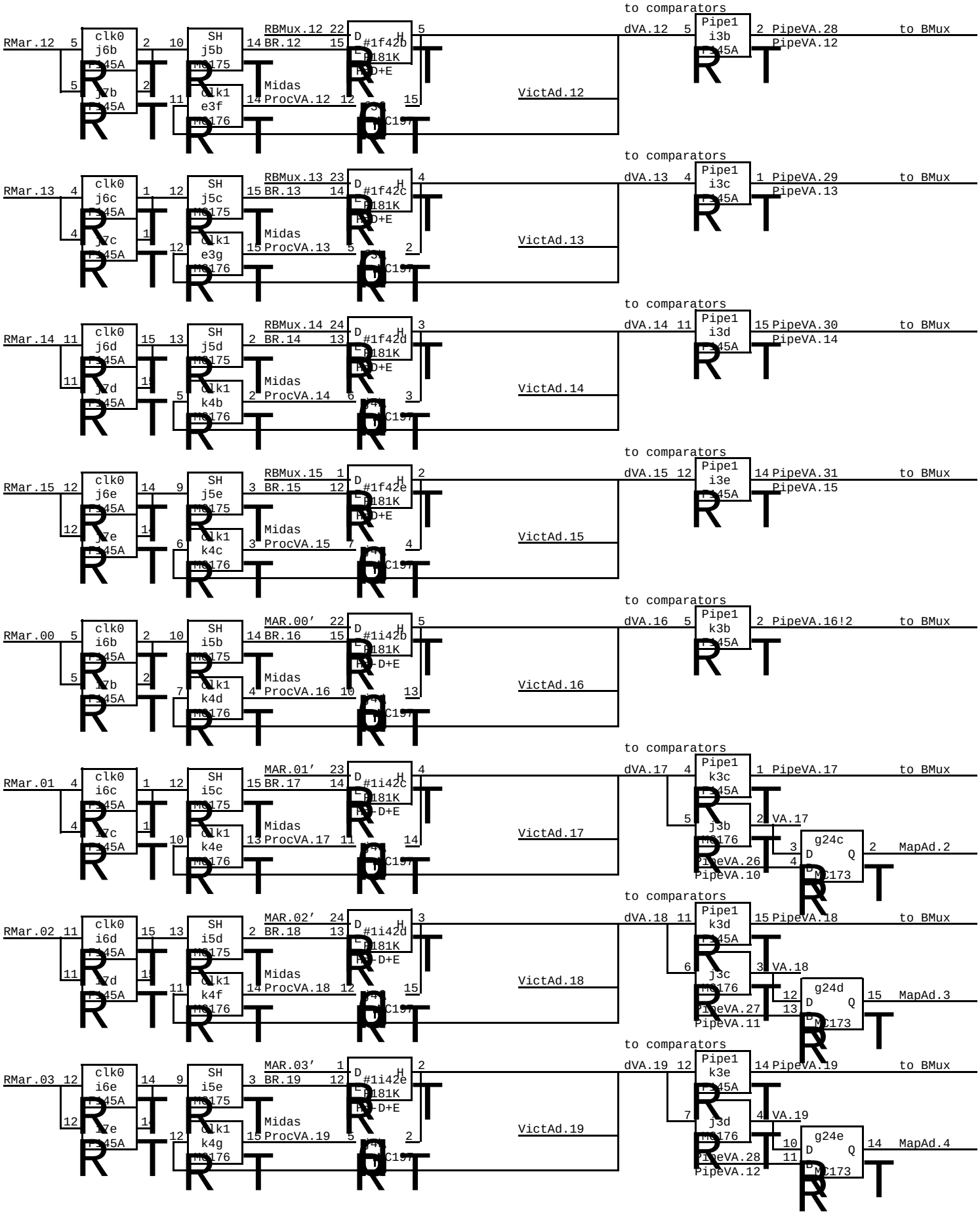
XEROX PARC	Project Dorado	Drawing Parity, pipe, Mcr	File MemC05.sil	Designer Lampson	Rev Be	Date 7/01/79	Page 05



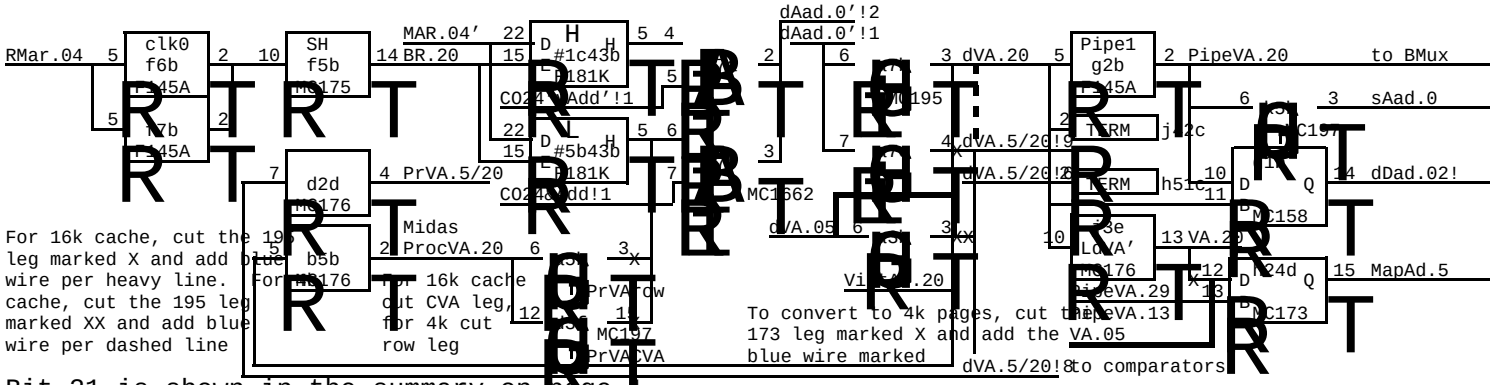
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Mar and BMux interface	MemC06.sil	Lampson	Be	7/01/79	06



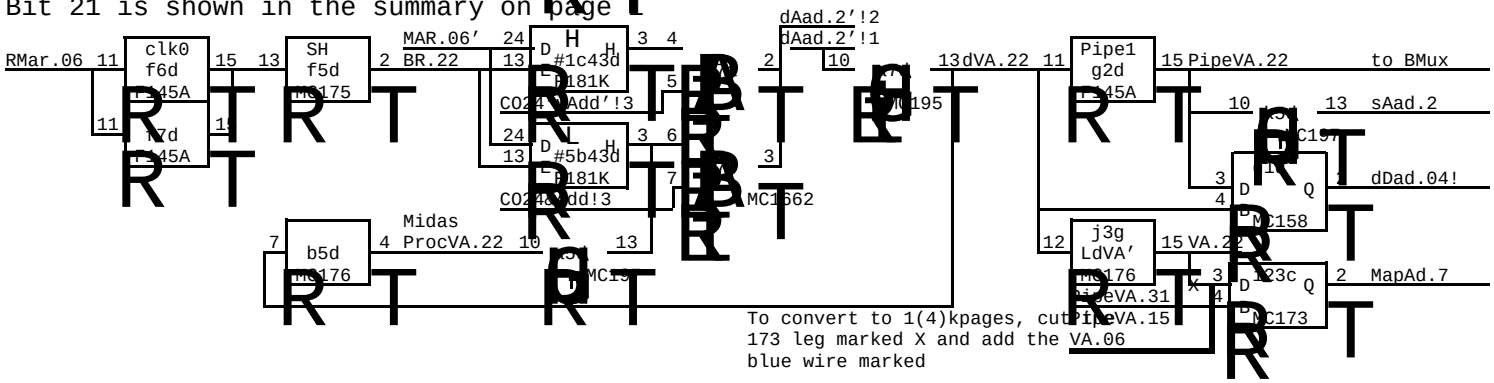
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Main data paths: 4-11	MemC07.sil	Lampson	Be	7/01/79	07

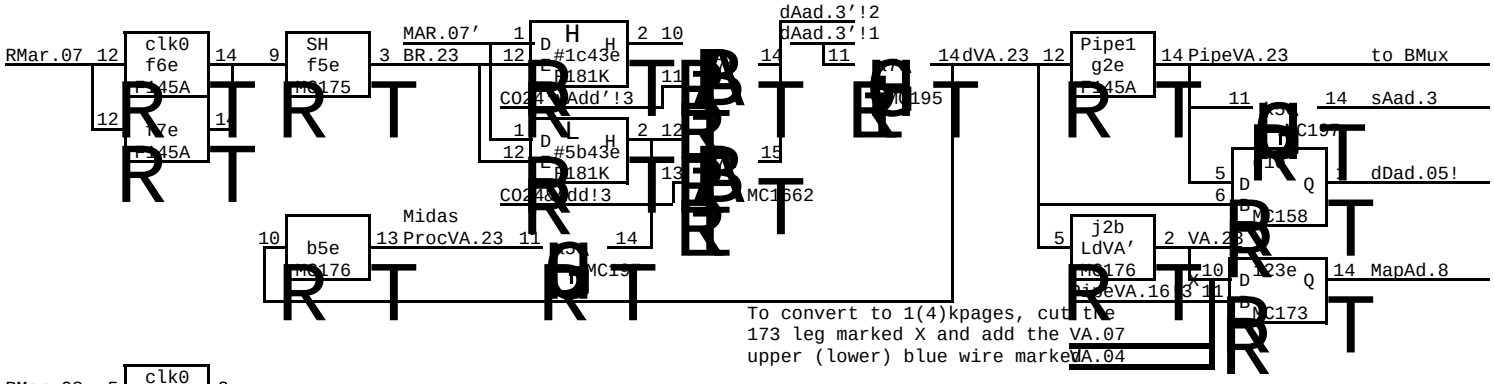


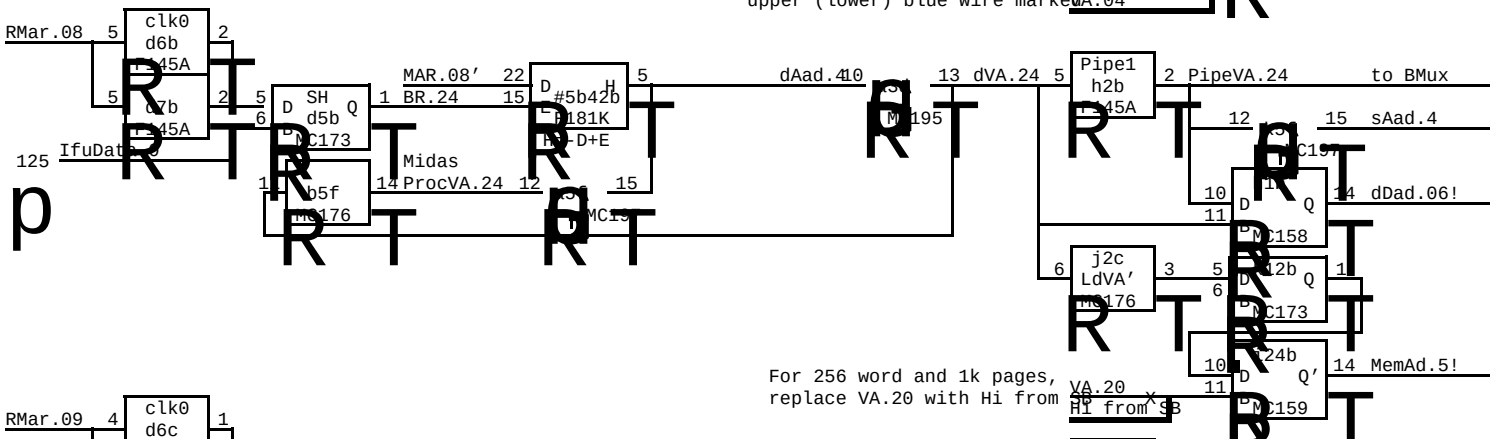
XEROX PARCb	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Main data paths: 12-19	MemC08.sil	Lampson	Be	7/01/79	08

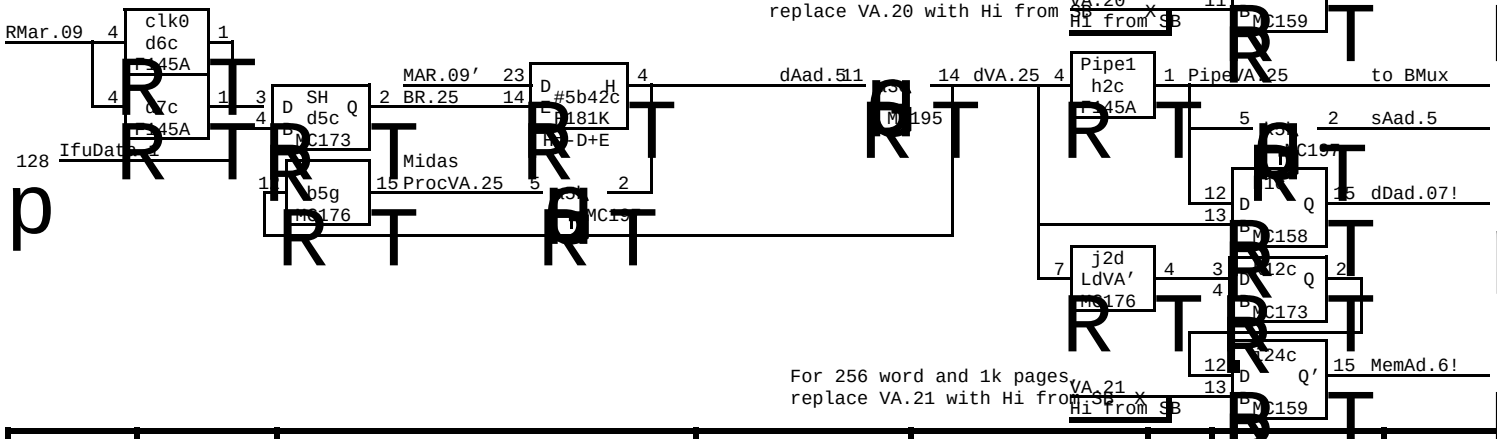


Bit 21 is shown in the summary on page 1

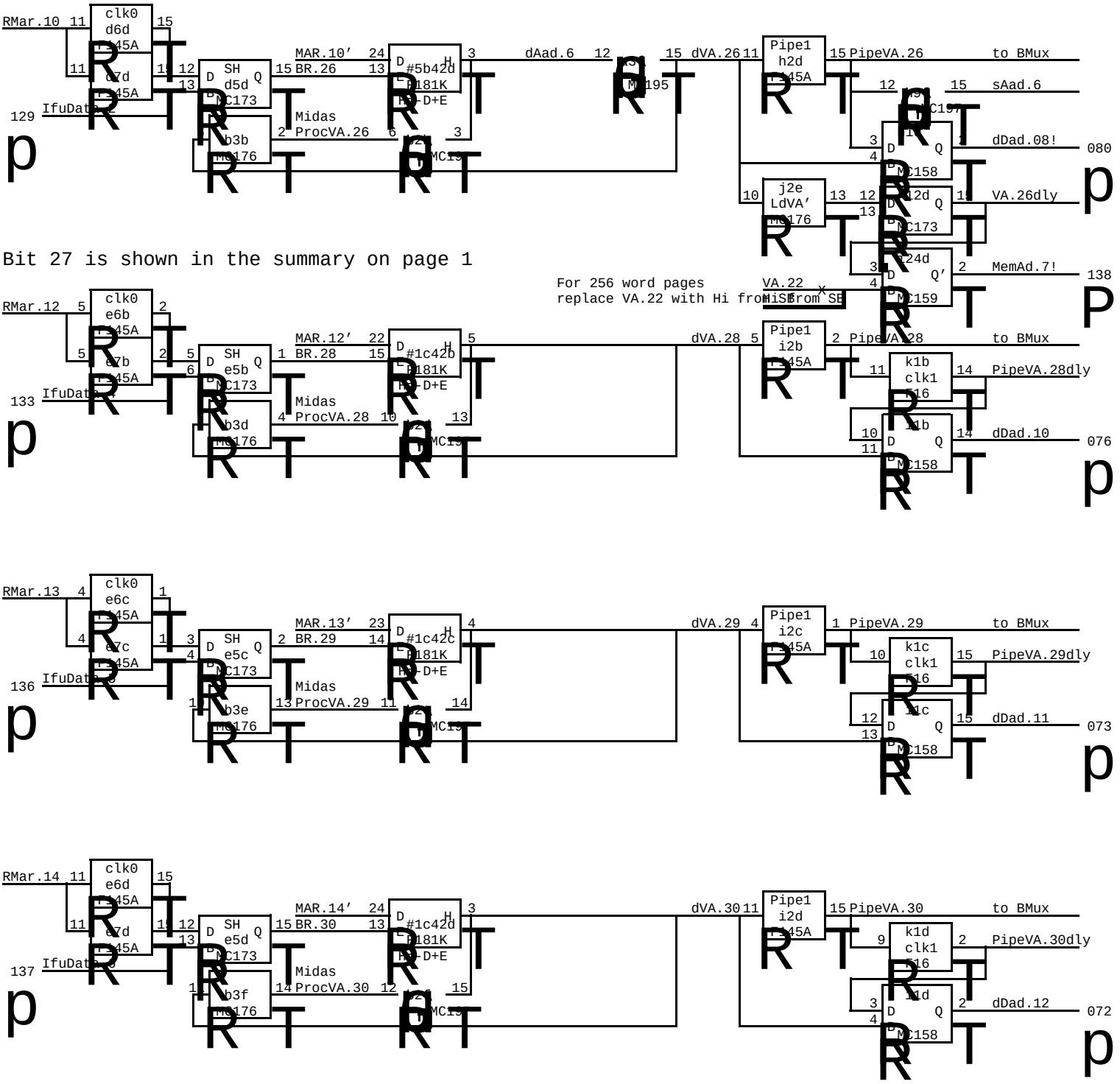






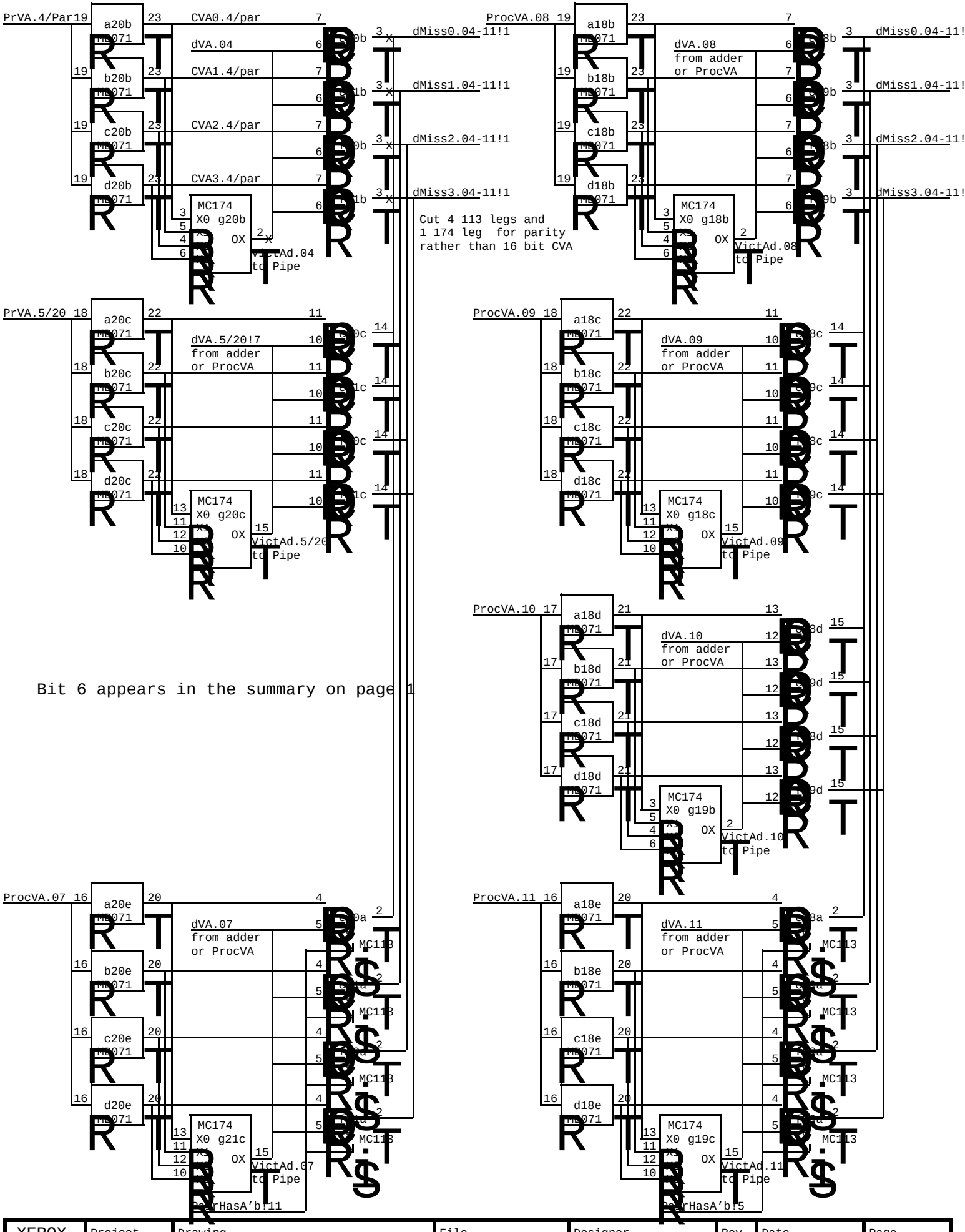


XEROX PARC	Project	Drawing	File	Desiogner	Rev	Date	Page
	Dorado	Main data paths: 20-26	MemC09.sil	Lampson	Be	7/01/79	09

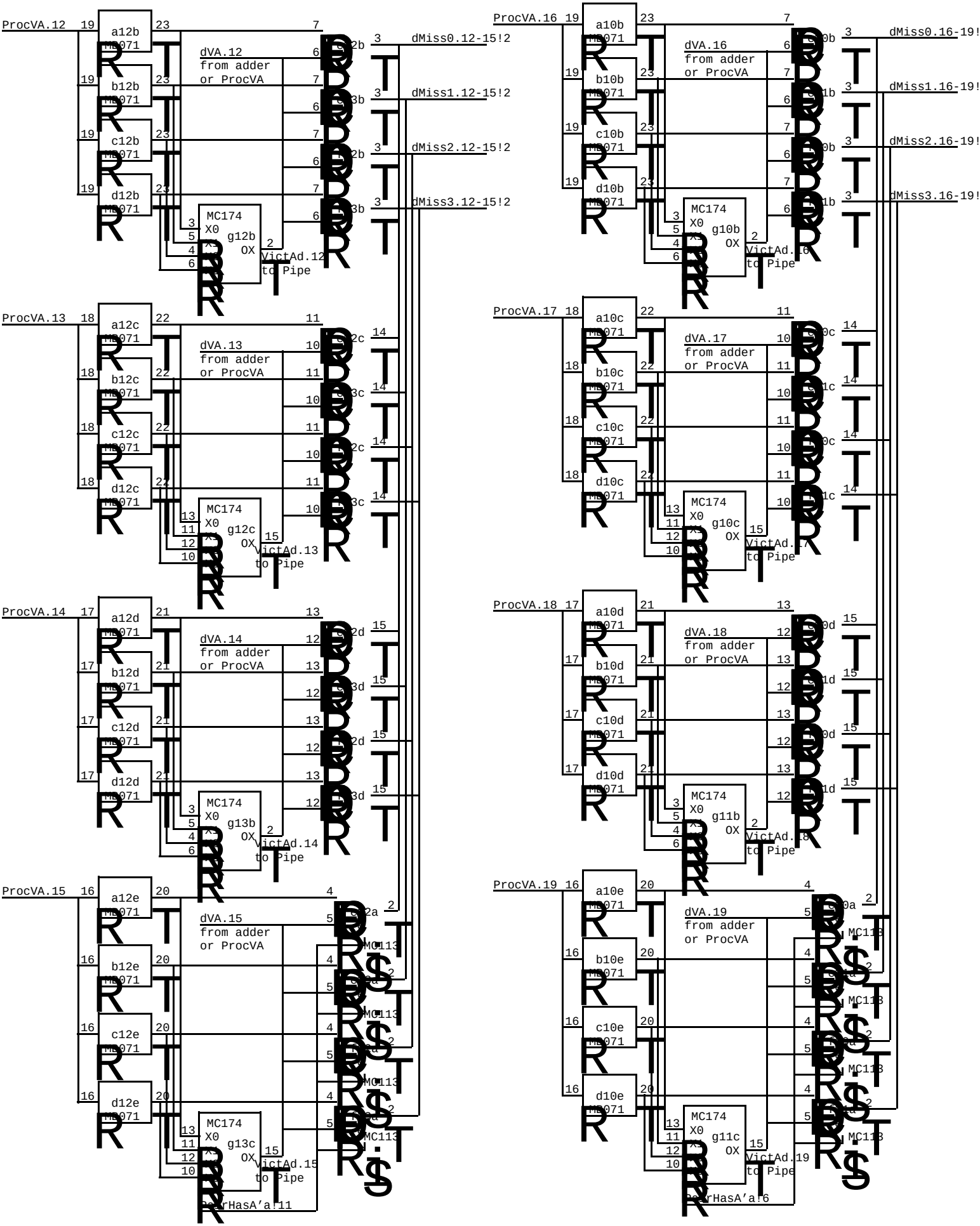


Bit 27 is shown in the summary on page 1

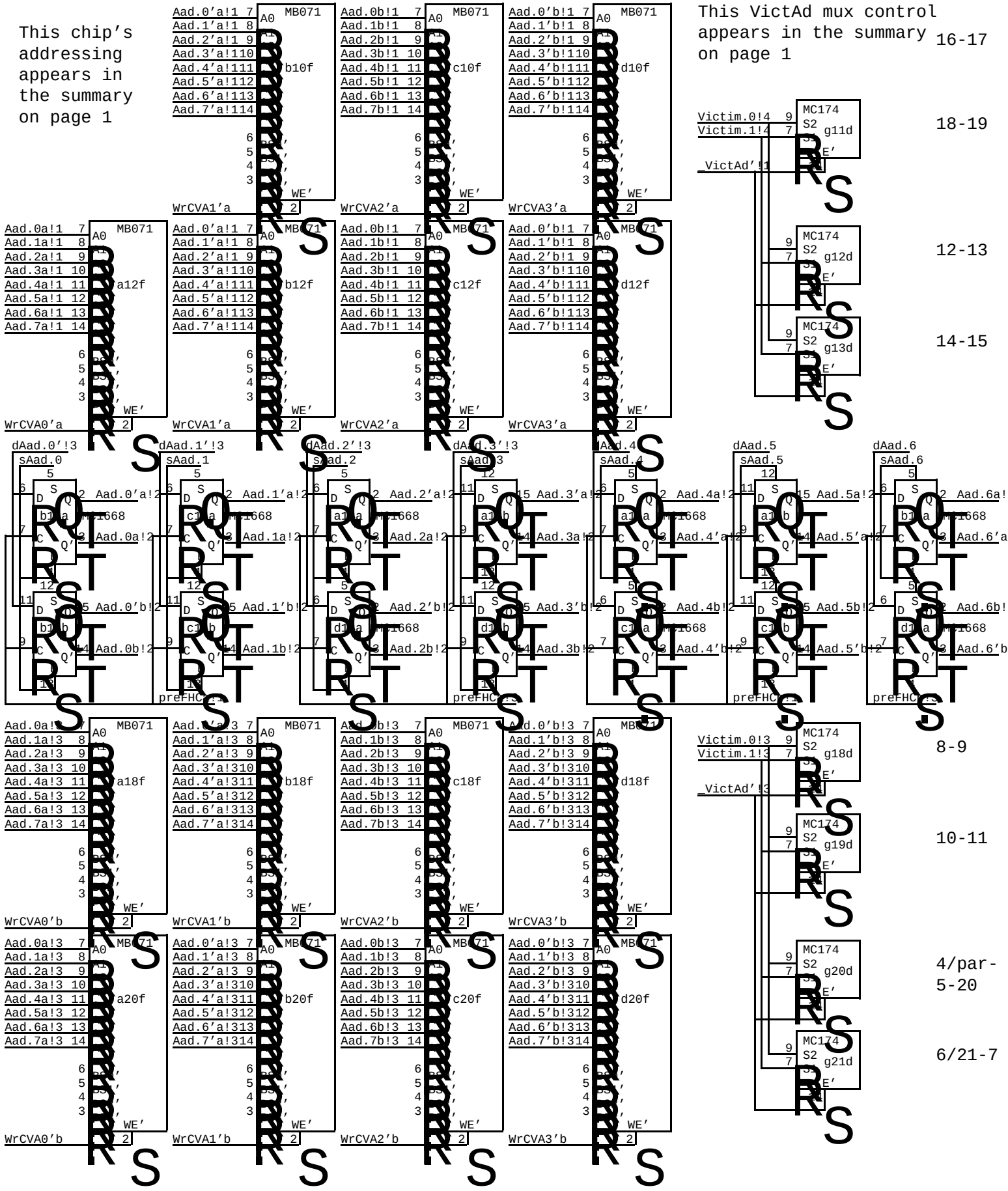
Bit 31 is shown in the summary on page 1



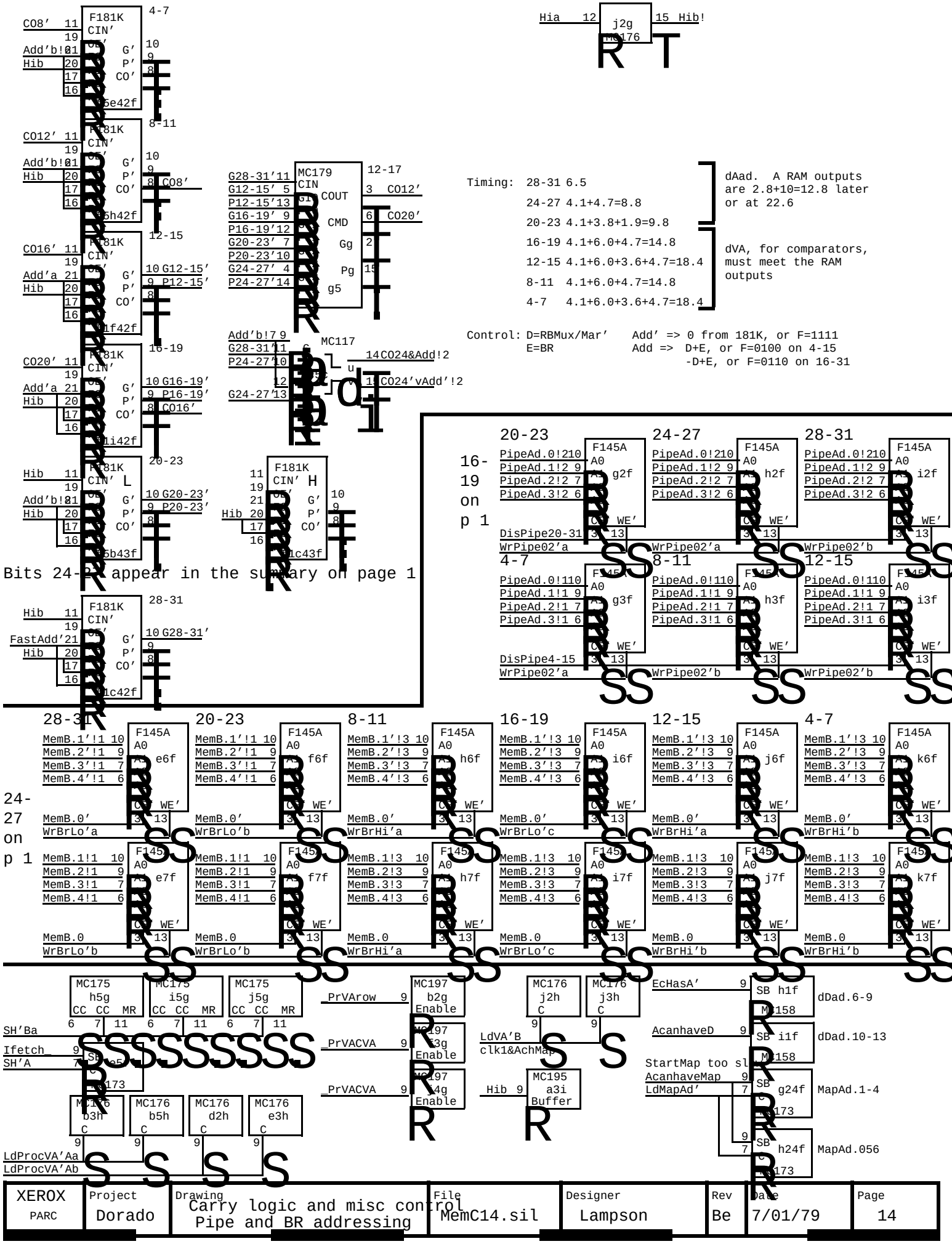
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CVA and comparators: 4-11	MemC11.sil	Lampson	Be	7/01/79	11



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CVA and comparators: 12-19	MemC12.sil	Lampson	Be	7/01/79	12



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	A memory addressing	MemC13.sil	Lampson	Be	7/01/79	13


F181K CIN' 4-7
F181K CIN' 8-11
F181K CIN' 12-15
F181K CIN' 16-19
F181K CIN' L 20-23
F181K CIN' H
F181K CIN' 28-31
MC179 CIN COUT CMD Gg Pg g5 12-17
MC117
j2g MC176
Timing: 28-31 6.5
24-27 4.1+4.7=8.8
20-23 4.1+3.8+1.9=9.8
16-19 4.1+6.0+4.7=14.8
12-15 4.1+6.0+3.6+4.7=18.4
8-11 4.1+6.0+4.7=14.8
4-7 4.1+6.0+3.6+4.7=18.4
dAad. A RAM outputs are 2.8+10=12.8 later or at 22.6
dVA, for comparators, must meet the RAM outputs
Control: D=RBMux/Mar' E=BR
Add' => 0 from 181K, or F=1111
Add => D+E, or F=0100 on 4-15
-D+E, or F=0110 on 16-31
Bits 24-27 appear in the summary on page 1
16-19 on p 1
24-27 on p 1
20-23
24-27
28-31
4-7
8-11
12-15
16-19
F145A
MC175 h5g
MC175 i5g
MC175 j5g
MC197 b2g Enable
MC197 j3g Enable
MC197 j4g Enable
MC176 j2h C
MC176 j3h C
MC195 a3i Buffer
MC176 b3h C
MC176 b5h C
MC176 d2h C
MC176 e3h C
SB h1f MC158
SB i1f MC158
SB g24f MC173
SB h24f MC173
dDad.6-9
dDad.10-13
MapAd.1-4
MapAd.056
XEROX PARC
Project Dorado
Drawing Carry logic and misc control Pipe and BR addressing
File MemC14.sil
Designer Lampson
Rev Be
Date 7/01/79
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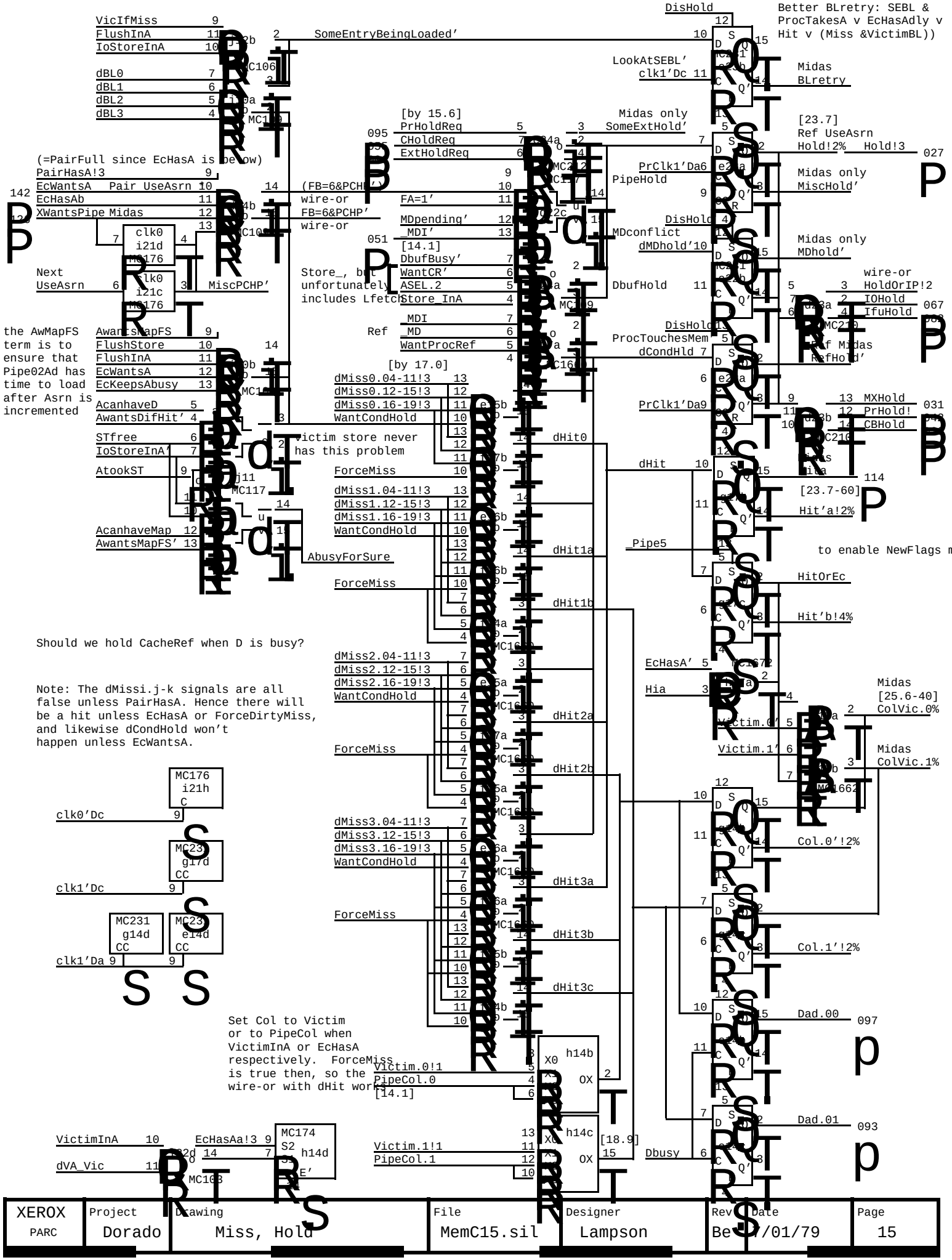
VicIfMiss 9
FlushInA 11
IoStoreInA 10
dBL0 7
dBL1 6
dBL2 5
dBL3 4
SomeEntryBeingLoaded'
(=PairFull since EcHasA is below)
PairHasA!3 9
EcWantsA Pair UseAsrn 10
EcHasAb 11
XWantsPipe Midas 12
13
clk0 i21d MC176
clk0 i21c MC176
Next UseAsrn 6
MiscPCHP'
(FB=6&PCHP wire-or
FB=6&PCHP' wire-or
[by 15.6]
PrHoldReq 5
CHoldReq 7
ExtHoldReq 6
FA=1' 11
MDpending' 12
_MDI' 13
[14.1]
DbufBusy' 7
WantCR' 6
ASEL.2 5
Store_InA 4
_MDI 7
Ref _MD 6
WantProcRef 5
Store_, but unfortunately includes Lfetch
AwantsMapFS 9
FlushStore 10
FlushInA 11
EcWantsA 12
EcKeepsAbusy 13
the AwMapFS term is to ensure that Pipe02Ad has time to load after Asrn is incremented
AcanhaveD 5
AwantsDifHit' 4
STfree 6
IoStoreInA' 7
AtookST 9
AcanhaveMap 12
AwantsMapFS' 13
victim store never has this problem
AbusyForSure
[by 17.0]
dMiss0.04-11!3 13
dMiss0.12-15!3 12
dMiss0.16-19!3 11
WantCondHold 10
ForceMiss 10
dMiss1.04-11!3 13
dMiss1.12-15!3 12
dMiss1.16-19!3 11
WantCondHold 10
ForceMiss
dMiss2.04-11!3 7
dMiss2.12-15!3 6
dMiss2.16-19!3 5
WantCondHold 4
ForceMiss
dMiss3.04-11!3 7
dMiss3.12-15!3 6
dMiss3.16-19!3 5
WantCondHold 4
ForceMiss
dHit0
dHit1a
dHit1b
dHit2a
dHit2b
dHit3a
dHit3b
dHit3c
Should we hold CacheRef when D is busy?
Note: The dMissi.j-k signals are all false unless PairHasA. Hence there will be a hit unless EcHasA or ForceDirtyMiss, and likewise dCondHold won't happen unless EcWantsA.
MC176 i21h C
clk0'Dc 9
MC231 g17d CC
clk1'Dc 9
MC231 g14d CC
MC231 e14d CC
clk1'Da 9 9
Set Col to Victim or to PipeCol when VictimInA or EcHasA respectively. ForceMiss is true then, so the wire-or with dHit works
Victim.0!1 5
PipeCol.0 4
[14.1] 6
h14b X0 OX
Victim.1!1 11
PipeCol.1 12
10
h14c X0 OX
[18.9] 15
VictimInA 10
dVA_Vic 11
EcHasAa!3 9
14 7
MC174 S2 h14d
MC168
DisHold 12
LookAtSEBL'
clk1'Dc 11
Midas BLretry
Better BLretry: SEBL & ProcTakesA v EcHasAdly v Hit v (Miss &VictimBL))
Midas only SomeExtHold'
PrClk1'Da6
PipeHold
DisHold
MDconflict
dMDhold'10
Midas only MDhold'
DbufHold 11
DisHold
ProcTouchesMem
dCondHld 7
PrClk1'Da9
[23.7] Ref UseAsrn Hold!2% Hold!3 027
Midas only MiscHold'
wire-or HoldOrIP!2
IOHold 067
IfuHold
Ref Midas RefHold'
MXHold 031
PrHold!
CBHold
[23.7-60] 114
Hit'a!2%
dHit 10
_Pipe5
to enable NewFlags m
HitOrEc
Hit'b!4%
EcHasA' 5
Hia 3
Midas [25.6-40] ColVic.0%
Victim.0' 5
Victim.1' 6
Midas ColVic.1%
Col.0'!2%
Col.1'!2%
Dad.00 097
Dad.01 093
Dbusy 6
XEROX PARC
Project Dorado
Drawing Miss, Hold
File MemC15.sil
Designer Lampson
Rev Date Be 7/01/79
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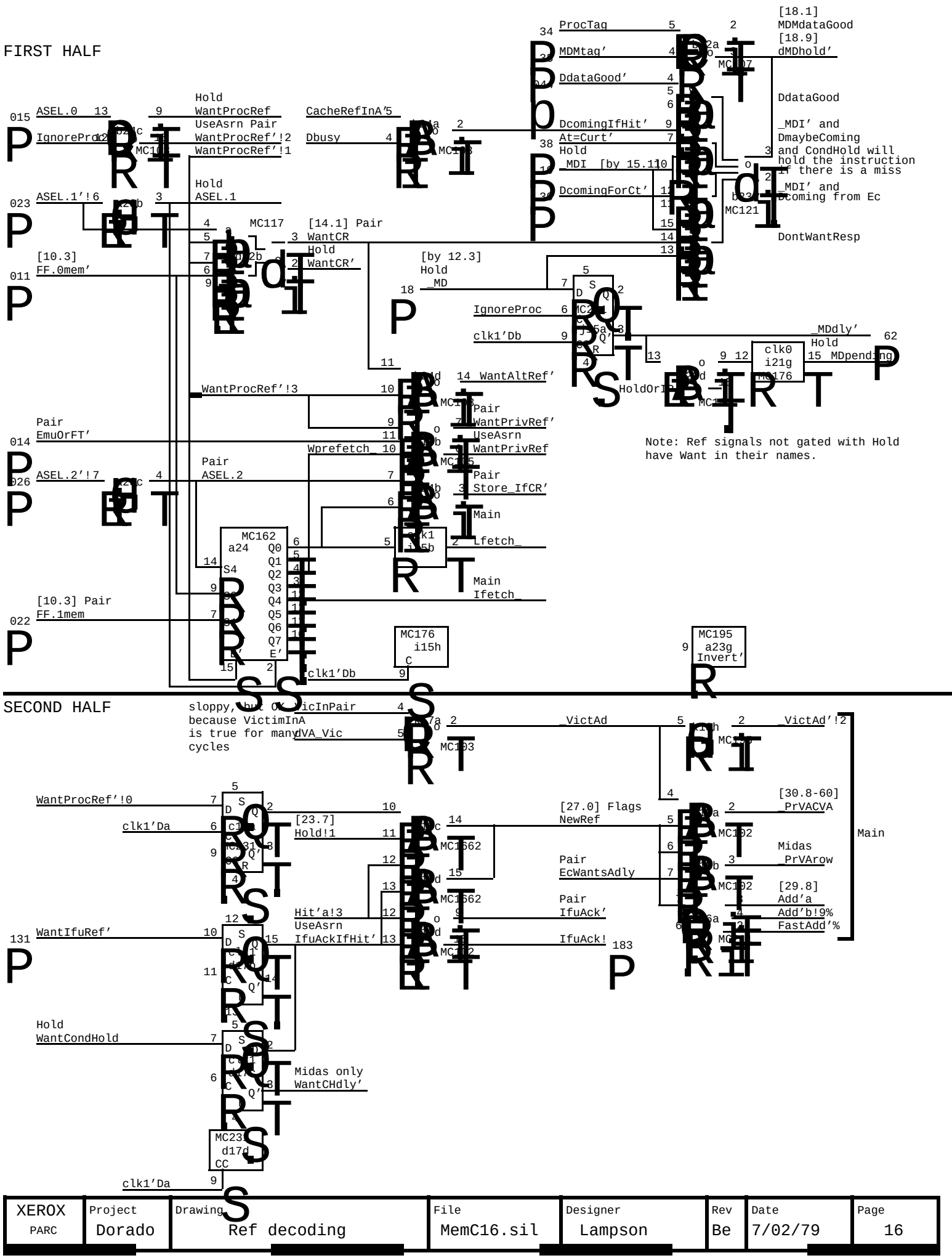
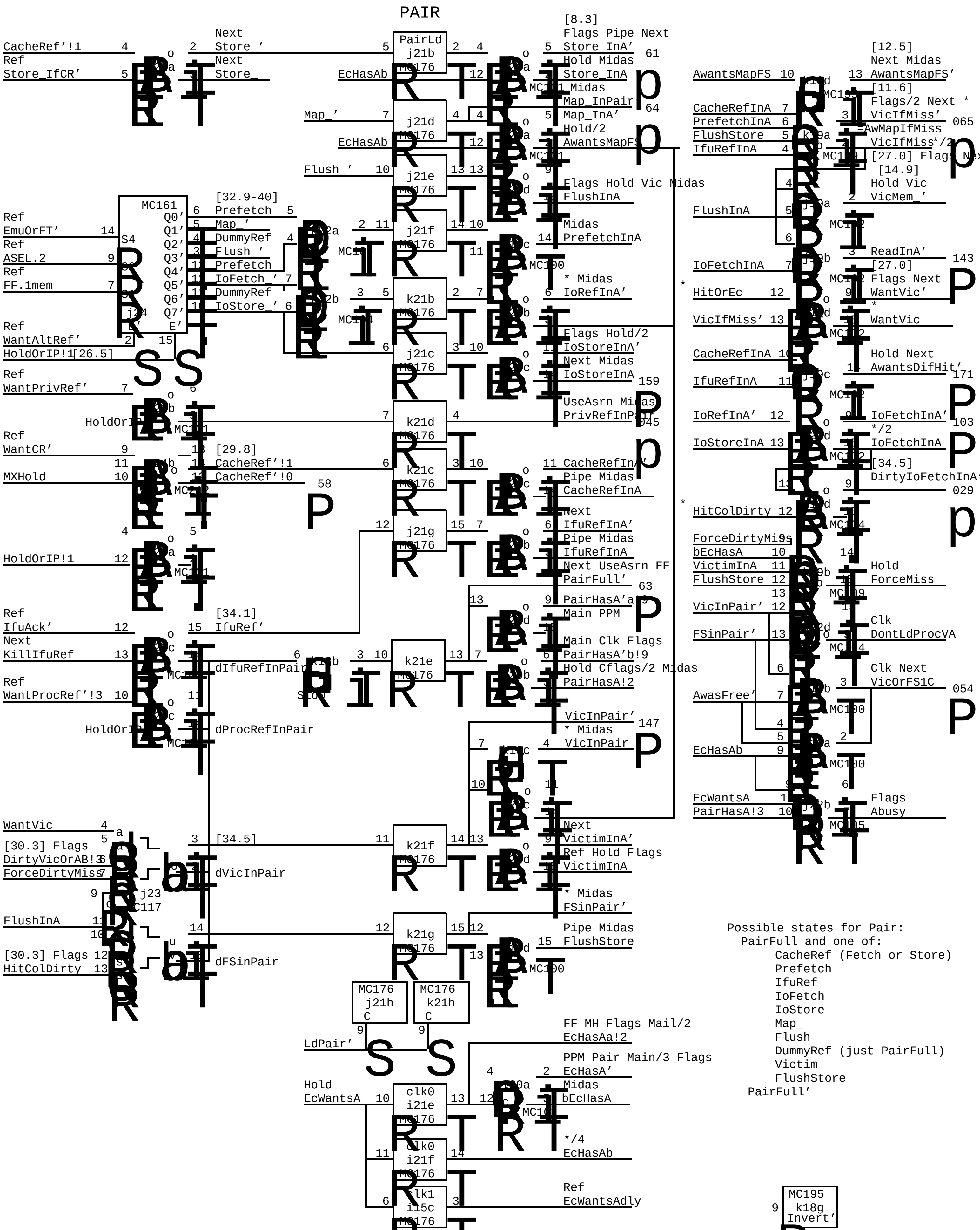


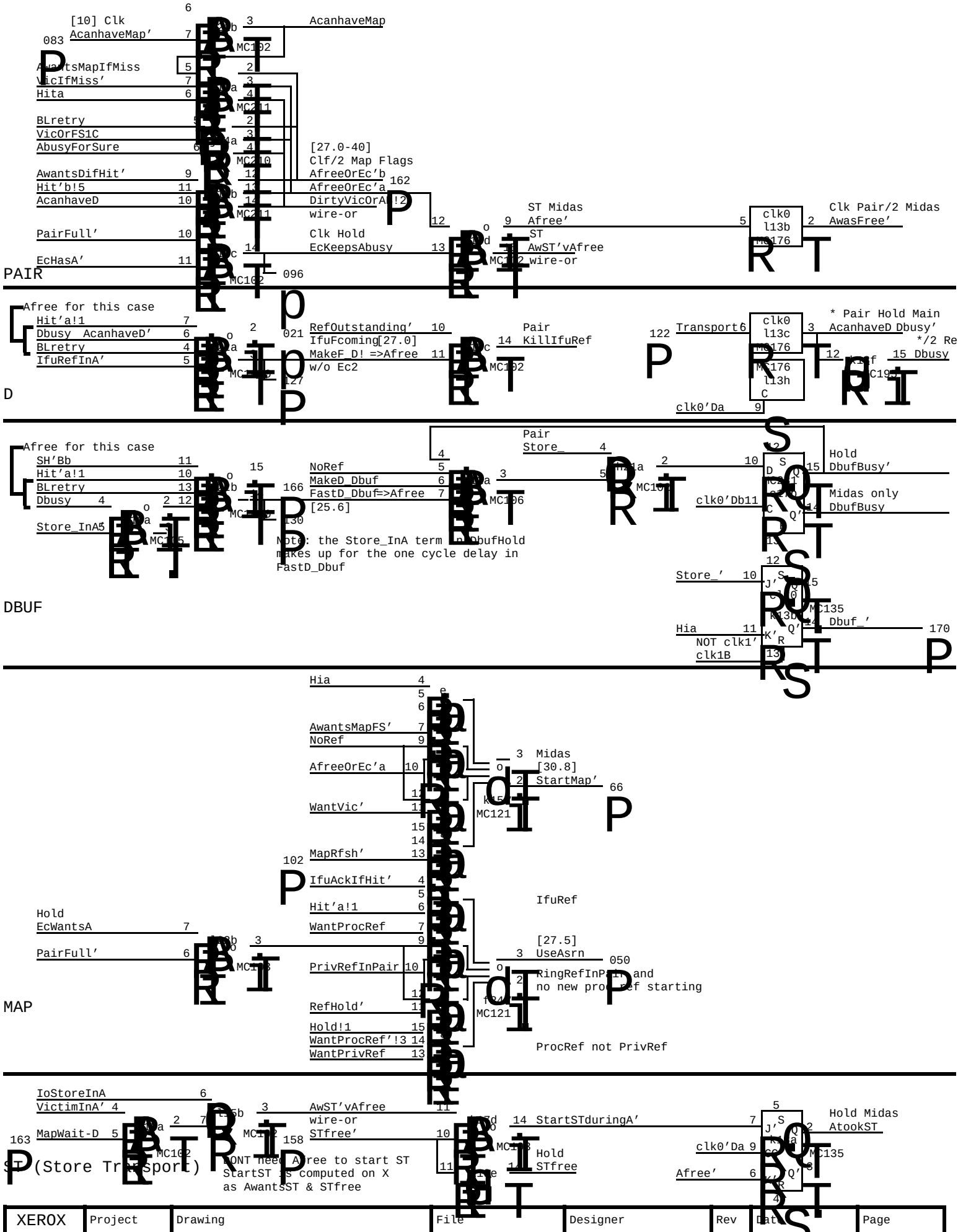
XEROX PARC	Project Dorado	Drawing Ref decoding	File MemC16.sil	Designer Lampson	Rev Be	Date 7/02/79	Page 16

PAIR

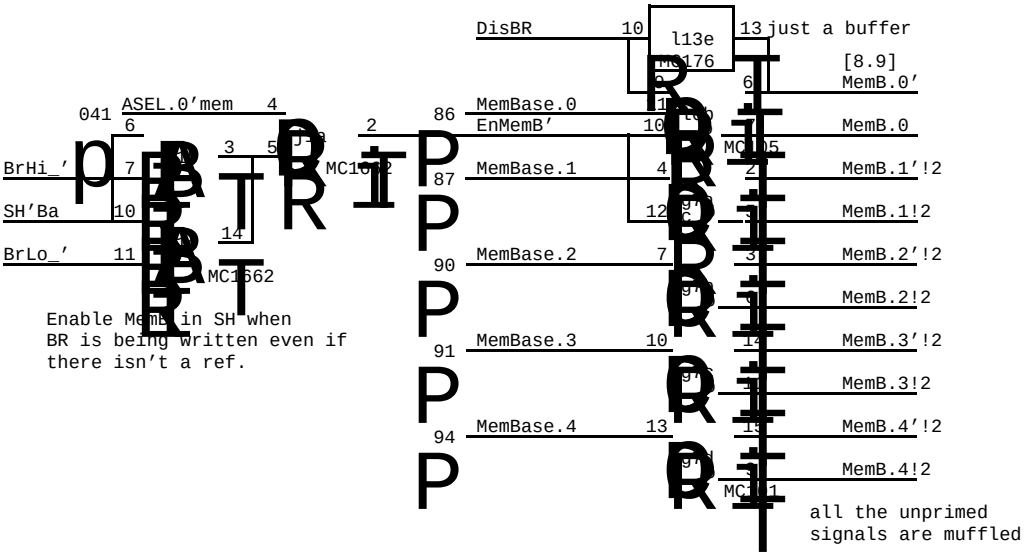

[8.3]
Flags Pipe Next
CacheRef'!1
Ref Store_IfCR'
Next Store_'
Next Store_
PairLd j21b MC176
EcHasAb
Store_InA'
Hold Midas Store_InA
Midas Map_InPair
Map_InA'
Hold/2 AwantsMapFS
Map_'
j21d MC176
Flush_'
j21e MC176
Flags Hold Vic Midas FlushInA
Midas PrefetchInA
MC161
Ref EmuOrFT'
Ref ASEL.2
Ref FF.1mem
[32.9-40]
Prefetch
Map_'
DummyRef
Flush_'
Prefetch
IoFetch_'
DummyRef
IoStore_'
j21f MC176
k21b MC176
* Midas IoRefInA'
Ref WantAltRef'
HoldOrIP!1[26.5]
j21c MC176
Flags Hold/2 IoStoreInA'
Next Midas IoStoreInA
Ref WantPrivRef'
k21d MC176
UseAsrn Midas PrivRefInPair
Ref WantCR'
MXHold
[29.8] CacheRef'!1
CacheRef'!0
k21c MC176
CacheRefInA'
Pipe Midas CacheRefInA
j21g MC176
Next IfuRefInA'
Pipe Midas IfuRefInA
HoldOrIP!1
Next UseAsrn FF PairFull'
PairHasA'a!9
Main PPM
Ref IfuAck'
Next KillIfuRef
[34.1] IfuRef'
dIfuRefInPair
k21e MC176
Main Clk Flags PairHasA'b!9
Hold Cflags/2 Midas PairHasA!2
Ref WantProcRef'!3
dProcRefInPair
VicInPair'
* Midas VicInPair
WantVic
[30.3] Flags DirtyVicOrAB!3
ForceDirtyMiss
j23 MC117
FlushInA
[34.5]
dVicInPair
k21f MC176
Next VictimInA'
Ref Hold Flags VictimInA
* Midas FSinPair'
[30.3] Flags HitColDirty
dFSinPair
k21g MC176
Pipe Midas FlushStore
MC176 j21h
MC176 k21h
LdPair'
FF MH Flags Mail/2 EcHasAa!2
PPM Pair Main/3 Flags EcHasA'
Midas bEcHasA
Hold EcWantsA
clk0 i21e MC176
clk0 i21f MC176
clk1 i15c MC176
*/4 EcHasAb
Ref EcWantsAdly
[12.5]
Next Midas AwantsMapFS'
AwantsMapFS
[11.6] Flags/2 Next * VicIfMiss'
CacheRefInA
PrefetchInA
FlushStore
IfuRefInA
=AwMapIfMiss VicIfMiss*/2
[27.0] Flags Next
[14.9] Hold Vic VicMem_'
FlushInA
ReadInA'
IoFetchInA
[27.0] Flags Next WantVic'
HitOrEc
* WantVic
VicIfMiss'
CacheRefInA
Hold Next AwantsDifHit'
IfuRefInA
IoRefInA'
IoFetchInA'
IoStoreInA
*/2 IoFetchInA
[34.5] DirtyIoFetchInA'
HitColDirty
ForceDirtyMiss
bEcHasA
VictimInA
FlushStore
Hold ForceMiss
VicInPair'
FSinPair'
Clk DontLdProcVA
Clk Next VicOrFS1C
AwasFree'
EcHasAb
EcWantsA
PairHasA!3
Flags Abusy
MC195 k18g Invert'

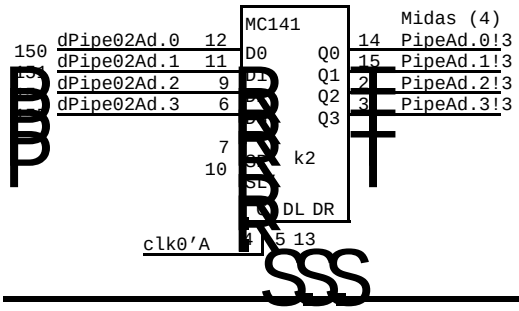
Possible states for Pair:
- PairFull and one of:
  - CacheRef (Fetch or Store)
  - Prefetch
  - IfuRef
  - IoFetch
  - IoStore
  - Map_
  - Flush
  - DummyRef (just PairFull)
  - Victim
  - FlushStore
- PairFull'

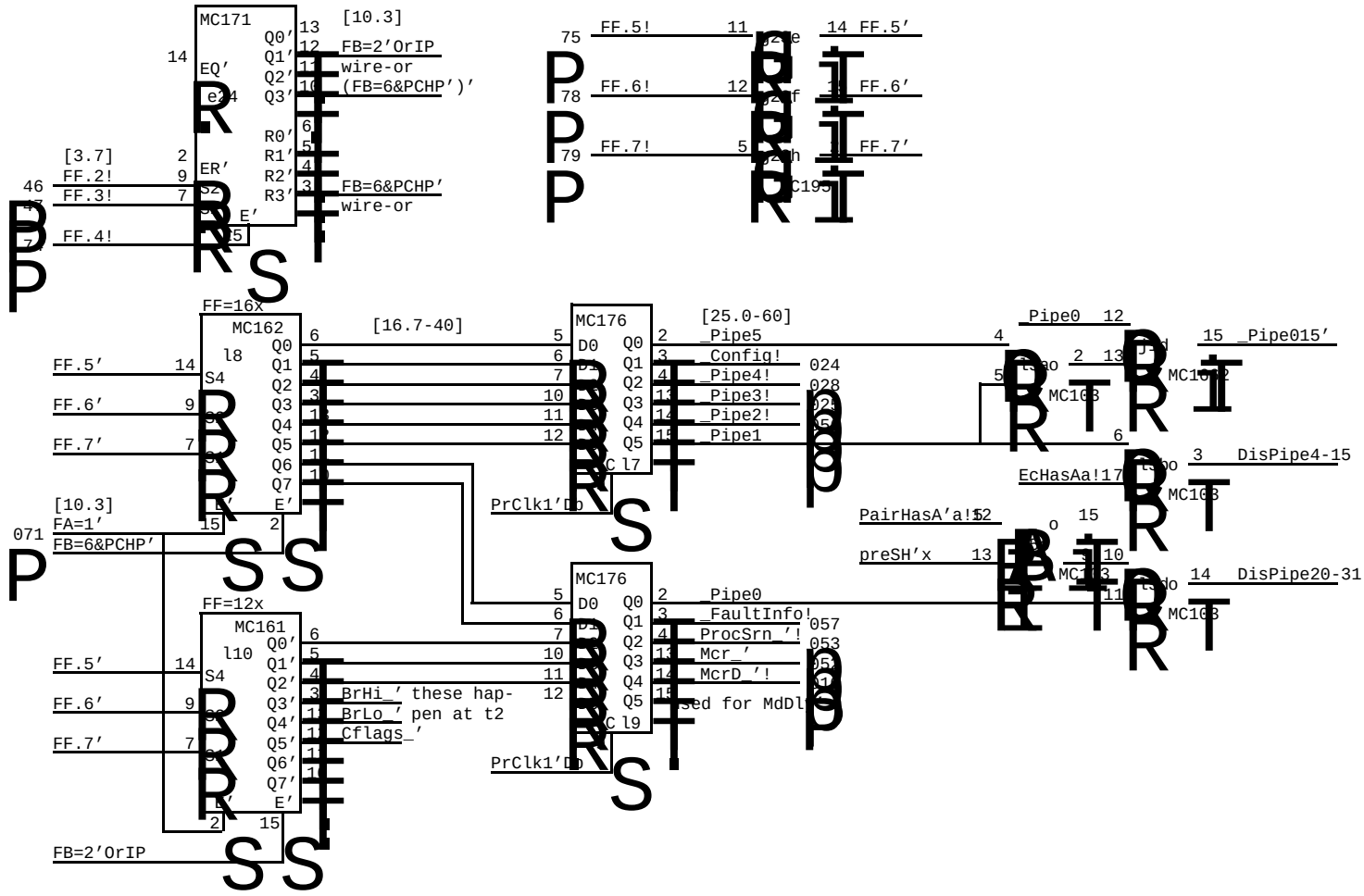
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Pair	MemC17.sil	Lampson	Be	7/02/79	17



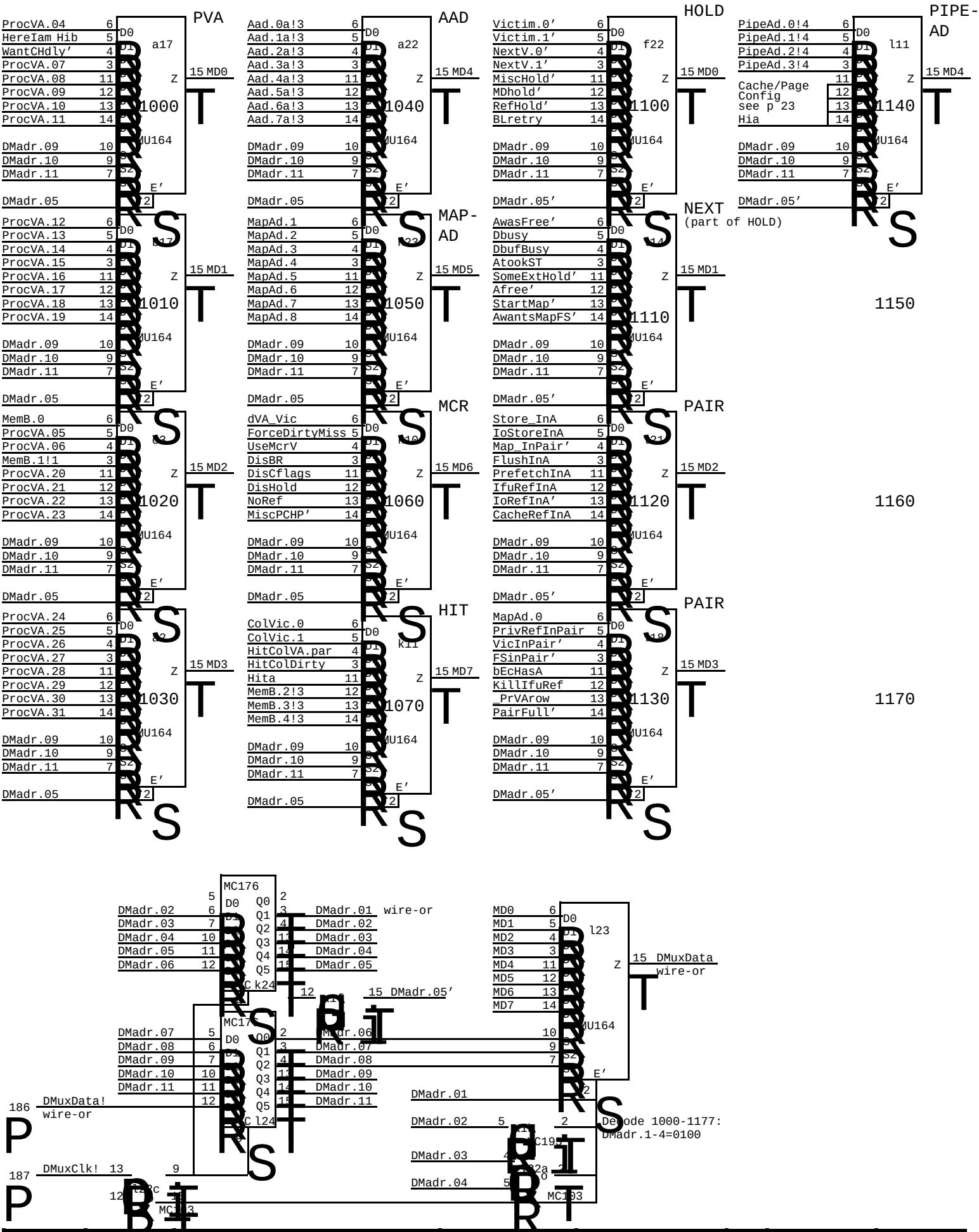
XEROX PARC	Project Dorado	Drawing Next	File MemC18.sil	Designer Lampson	Rev Be	Date 7/03/79	Page 18



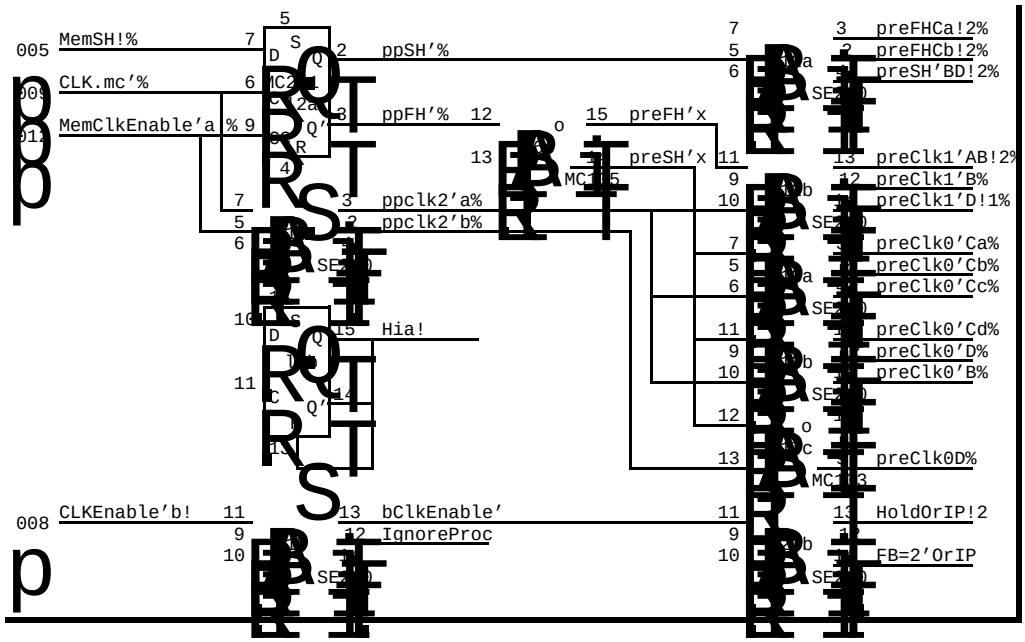


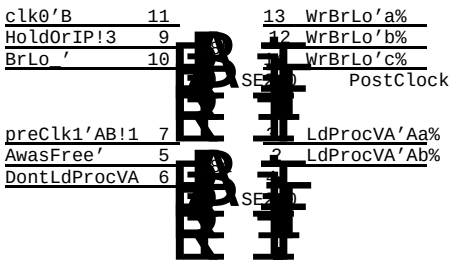


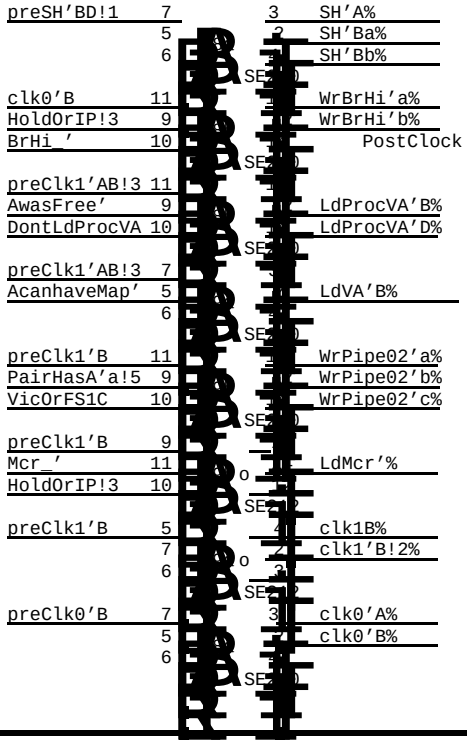
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	FF decoding, PipeAd, MemB	MemC19.sil	Lampson	Be	7/01/79	19



XEROX PARC	Project: Dorado	Drawing: Midas control and mufflers	File: MemC20.sil	Designer: Lampson	Rev: Be	Date: 7/01/79	Page: 20





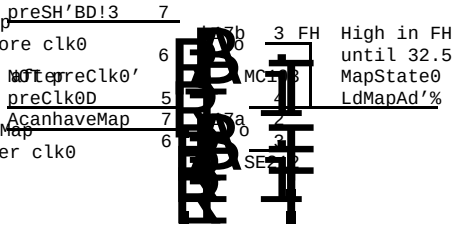


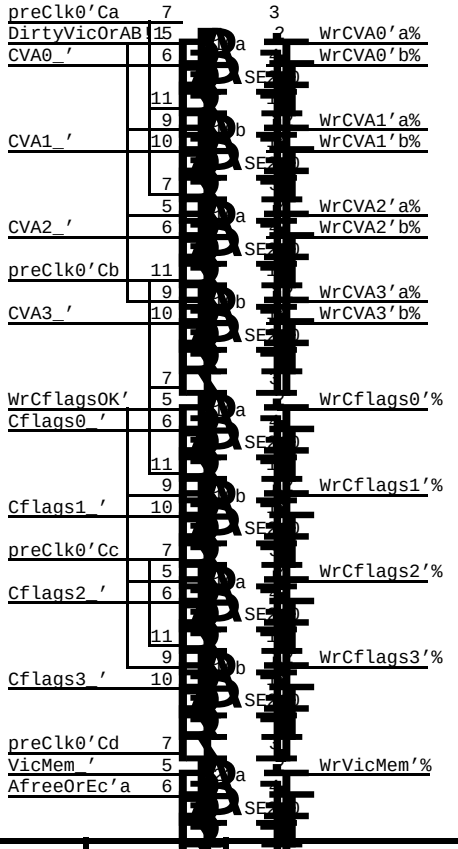
MapAd must be

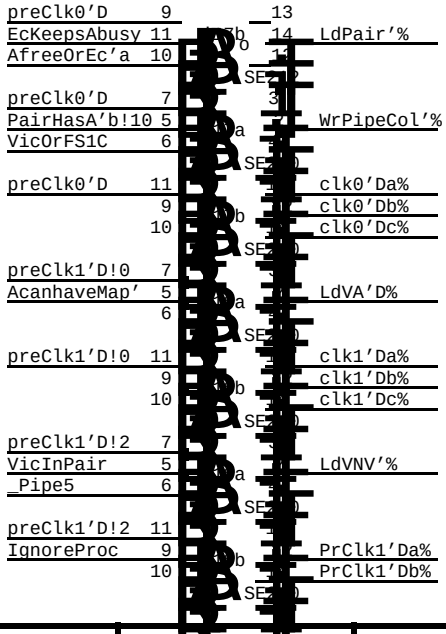
low by 12.8 before clk0 of StartMap
to:let row MapAd through by 6 before clk0

high from clk0 or StartMap to 27.5 after clk0
to:hold row MapAd

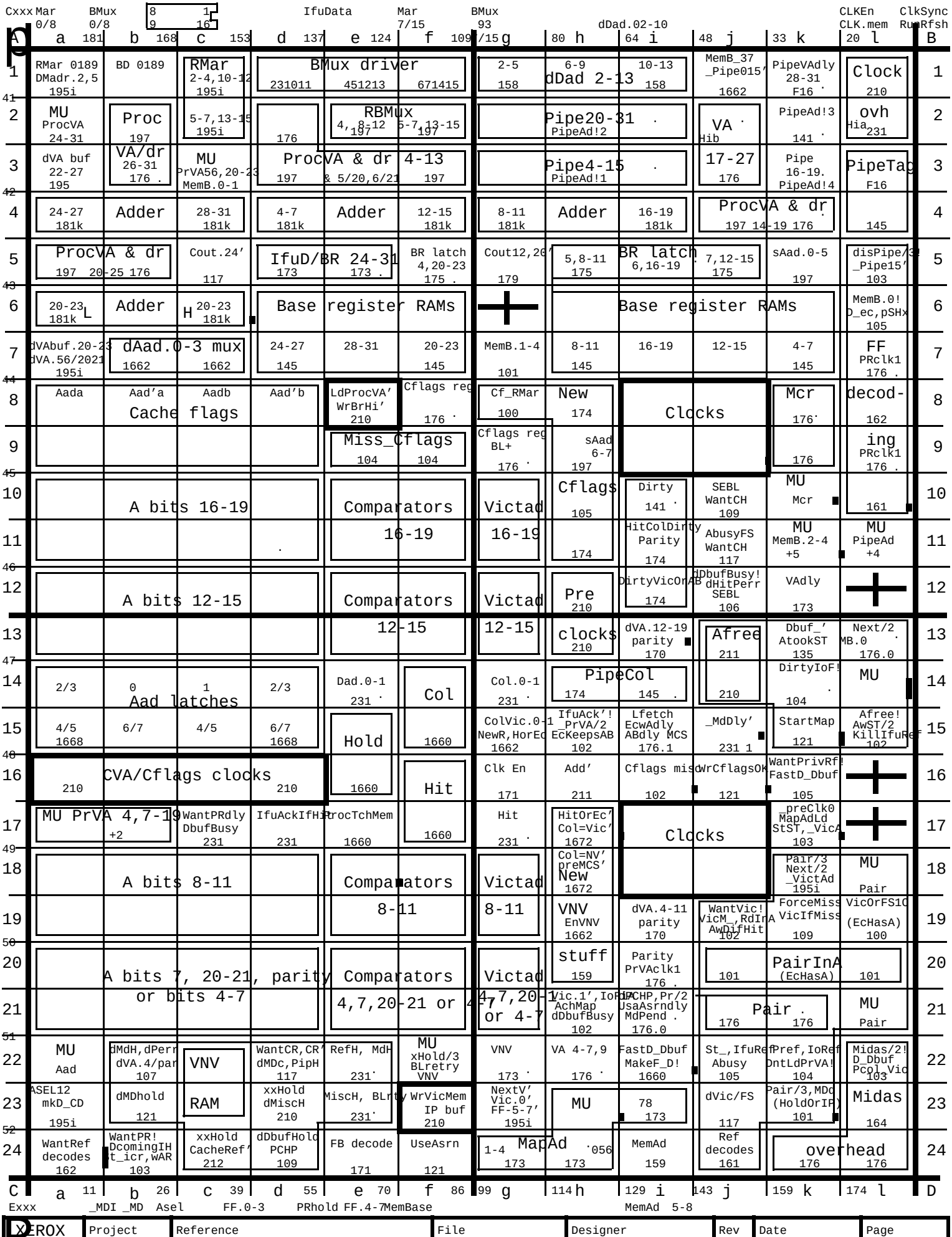
low by 2.8 before clk0 after StartMap
to:let col MapAd through by 4 after clk0







XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clock distribution	MemC21.sil	Lampson	Be	7/01/79	21


Cxxx Mar 0/8 BMux 0/8 8 9 1 16 IfuData Mar 7/15 BMux 93 dDad.02-10 CLKEn CLK.mem ClkSync RunRfsh
A a 181 b 168 c 153 d 137 e 124 f 109 /15 g 80 h 64 i 48 j 33 k 20 l B
RMar 0189 DMadr.2,5 195i
BD 0189
RMar 2-4,10-12 195i
BMux driver
231011 451213 671415
2-5 158
6-9 dDad 2-13 10-13 158
MemB_37 _Pipe015' 1662
PipeVAdly 28-31 F16
Clock 210
MU ProcVA 24-31
Proc 197
5-7,13-15 195i
RBMux 4,8-12 197 5-7,13-15 197
176
Pipe20-31 PipeAd!2
VA Hib
PipeAd!3 141
ovh Hia 231
dVA buf 22-27 195
VA/dr 26-31 176
MU PrVA56,20-23 MemB.0-1
ProcVA & dr 4-13 197 & 5/20,6/21 197
Pipe4-15 PipeAd!1
17-27 176
Pipe 16-19. PipeAd!4
PipeTag F16
24-27 181k
Adder
28-31 181k
4-7 181k
Adder
12-15 181k
8-11 181k
Adder
16-19 181k
ProcVA & dr 197 14-19 176
145
ProcVA & dr 197 20-25 176
Cout.24' 117
IfuD/BR 24-31 173 173
BR latch 4,20-23 175
Cout12,20' 179
5,8-11 175
BR latch 6,16-19 7,12-15 175
sAad.0-5 197
disPipe/3! _Pipe15' 103
20-23 181k L
Adder
H 20-23 181k
Base register RAMs
Base register RAMs
MemB.0! D_ec,pSHx 105
dVAbuf.20-23 dVA.56/2021 195i
dAad.0-3 mux 1662 1662
24-27 145
28-31 145
20-23 145
MemB.1-4 101
8-11 145
16-19 145
12-15 145
4-7 145
FF PRclk1 176
Aada
Aad'a
Aadb
Aad'b
LdProcVA' WrBrHi' 210
Cflags reg 176
Cf_RMar 100
New 174
Clocks
Mcr 176
decod- 162
Cache flags
Miss_Cflags 104 104
Cflags reg BL+ 176
sAad 6-7 197
176
ing PRclk1 176
A bits 16-19
Comparators 16-19
Victad 16-19
Cflags 105
Dirty 141
SEBL WantCH 109
MU Mcr
161
HitColDirty Parity 174
AbusyFS WantCH 117
MU MemB.2-4 +5
MU PipeAd +4
174
A bits 12-15
Comparators 12-15
Victad 12-15
Pre 210
DirtyVicOrAB 174
dDbufBusy! dHitPerr SEBL 106
VAdly 173
clocks 210
dVA.12-19 parity 170
Afree 211
Dbuf_' AtookST 135
Next/2 MB.0 176.0
Aad latches
2/3
0
1
2/3
Dad.0-1 231
Col
Col.0-1 231
PipeCol 174 145
210
DirtyIoF! 104
MU
4/5 1668
6/7
4/5
6/7 1668
Hold 1660
ColVic.0-1 NewR,HorEc 1662
IfuAck'! _PrVA/2 EcKeepsAB 102
Lfetch EcwAdly ABdly MCS 176.1
_MdDly' 231 1
StartMap 121
Afree! AwST/2 KillIfuRef 102
CVA/Cflags clocks
210
210
1660
Hit 1660
Clk En 171
Add' 211
Cflags misc 102
WrCflagsOK 121
WantPrivRf! FastD_Dbuf 105
MU PrVA 4,7-19 +2
WantPRdly DbufBusy 231
IfuAckIfHit 231
ProcTchMem 1660
Hit 231
HitOrEc' Col=Vic' 1672
Clocks
_preClk0 MapAdLd StST,_VicA 103
Col=NV' preMCS' New 1672
Pair/3 Next/2 _VictAd 195i
MU Pair
A bits 8-11
Comparators 8-11
Victad 8-11
VNV EnVNV 1662
dVA.4-11 parity 170
WantVic! VicM_,RdInA AwDifHit 102
ForceMiss VicIfMiss 109
VicOrFS1C (EcHasA) 100
stuff 159
Parity PrVAclk1 176
101
PairInA (EcHasA) 101
A bits 7, 20-21, parity or bits 4-7
Comparators 4,7,20-21 or 4-7
Victad 4,7,20-21 or 4-7
Vic.1',IoRdA AchMap dDbufBusy 102
PCHP,Pr/2 UsaAsrndly MdPend 176.0
Pair 176
176
MU Pair
MU Aad
dMdH,dPerr dVA.4/par 107
VNV
RAM
WantCR,CR' dMDc,PipH 117
RefH, MdH 231
MU xHold/3 BLretry VNV
VNV 173
VA 4-7,9 176
FastD_Dbuf MakeF_D! 1660
St_,IfuRef Abusy 105
Pref,IoRef OntLdPrVA! 104
Midas/2! D_Dbuf Pcol_Vic 103
ASEL12 mkD_CD 195i
dMDhold 121
xxHold dMiscH 210
MiscH, BLrty 231
WrVicMem IP buf 210
NextV' Vic.0' FF-5-7' 195i
MU
78 173
dVic/FS 117
Pair/3,MDc (HoldOrIP) 101
Midas 164
WantRef decodes 162
WantPR! DcomingIH t_icr,wAR 103
xxHold CacheRef' 212
dDbufHold PCHP 109
FB decode 171
UseAsrn 121
1-4 MapAd 173 173
.056
MemAd 159
Ref decodes 161
overhead 176 176
C a 11 b 26 c 39 d 55 e 70 f 86 99 g 114 h 129 i 143 j 159 k 174 l D
Exxx _MDI _MD Asel FF.0-3 PRhold FF.4-7 MemBase MemAd 5-8
XEROX PARC
Project Dorado
Reference Layout
File MemC22.sil
Designer Lampson
Rev Be
Date 7/01/79
Page 22

CACHE CONFIGURATIONS

4k CacheConfig=3			16k CacheConfig=2			16k without parity CacheConfig=1		
Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)
a03	195	3x 4x cut 5-6 from 5/20-6/21	a03	195	3-6 4-7 connect 5-6 to 5/20-6/21	a03	195	3-6 4-7 connect 5-6 to 5/20-6/21
a07	195	2-15 3-4 connect 20-21 to 5/20-6/21	a07	195	2x 4x cut 20-21 from 5/20-6/21	a07	195	2x 4x cut 20-21 from 5/20-6/21
a05	197	3x 4x read ProcVA.20-21 for CVA	d03	197	2x 15x read ProcVA.20-21 for row	d03	197	2x 15x read ProcVA.20-21 for row
b14	1668	remove disconnect Aad.0						
c14	1668	remove disconnect Aad.1						
e20	113	3x	e20	113	3x	b22	107	7x 9x 14x 15x 6-10 connect 4 to 4/par disconnect Perr reporting
e21	113	3x	e21	113	3x			
f20	113	3x	f20	113	3x			
f21	113	3x keep parity from comparators	f21	113	3x			
g20	174	2x keep parity from CVA	g20	174	2x			
			l11	164	12x make CacheConfig=2	l11	164	11x make CacheConfig=1

PAGE SIZE CONFIGURATIONS

256 words PageConfig=3			1k words PageConfig=2			4k words PageConfig=1		
Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)	Position	Chip	Cut (X) or wire (pin-pin)
i24	159	4x 6x 11x 13x 4-6-11-13-9 MemRA_0 0 0 0	i24	159	11x 13x 11-13-9 MemRA_0 0 22 23			MemRA_20 21 22 23
			h24	173	3x 4x 1-2 MapAd.0_4-5 for 6-7	h24	173	10x 12x 10-3 12-5 MapAd.5,6_5,7 for 20,21
			i23	173	3x 10x 3-5 10-12 MapAd.7,8_6,7 for 22,23	i23	173	3x 10x 3-5 10-13 MapAd.7,8_6,4 for 22,23
			l11	164	14x make PageConfig=2	l11	164	13x make PageConfig=1

Note: Muffler signals 1144-1147 specify the configuration as follows:
1144-1145 are CacheConfig
1146-1147 are PageConfig
and the meaning of their values is as listed in the tables above

Need information here about the two missing holes

C U R R E N T L Y N O N E