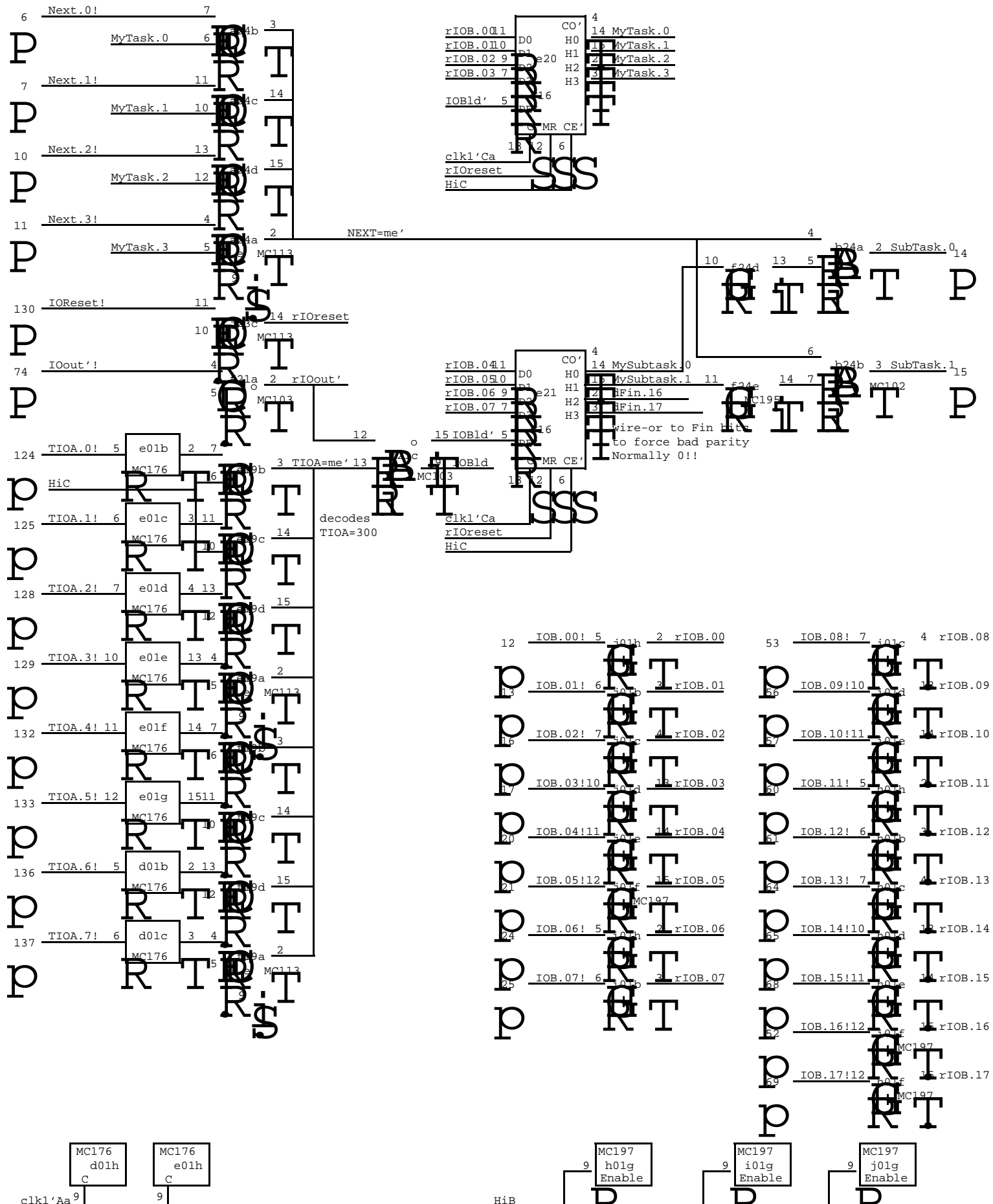


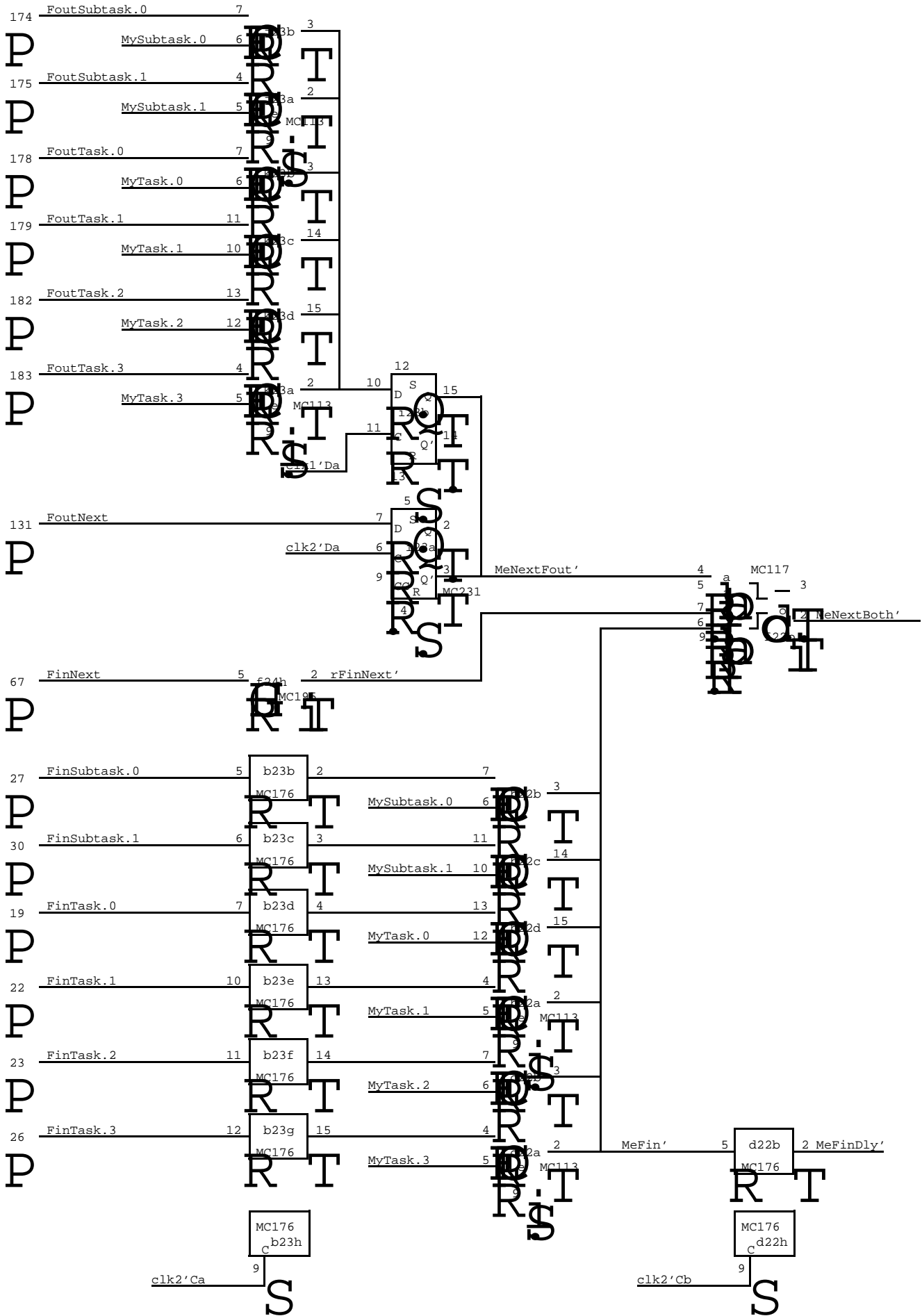
D O R A D O D R A W I N G S

Fast I/O test board

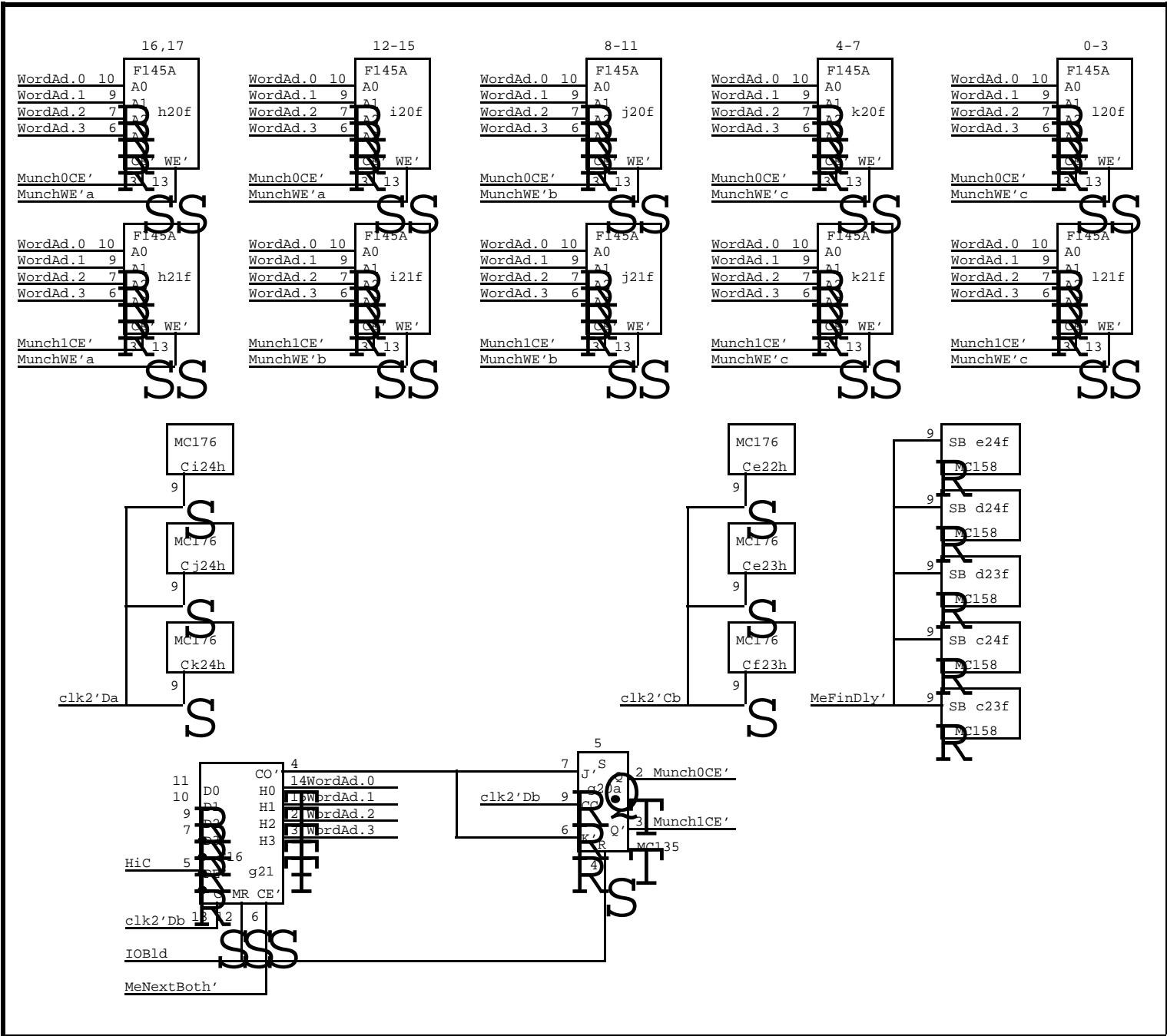
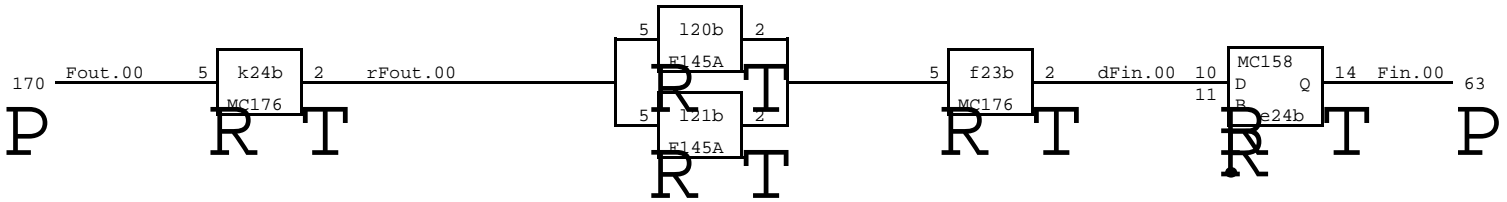
Table of contents

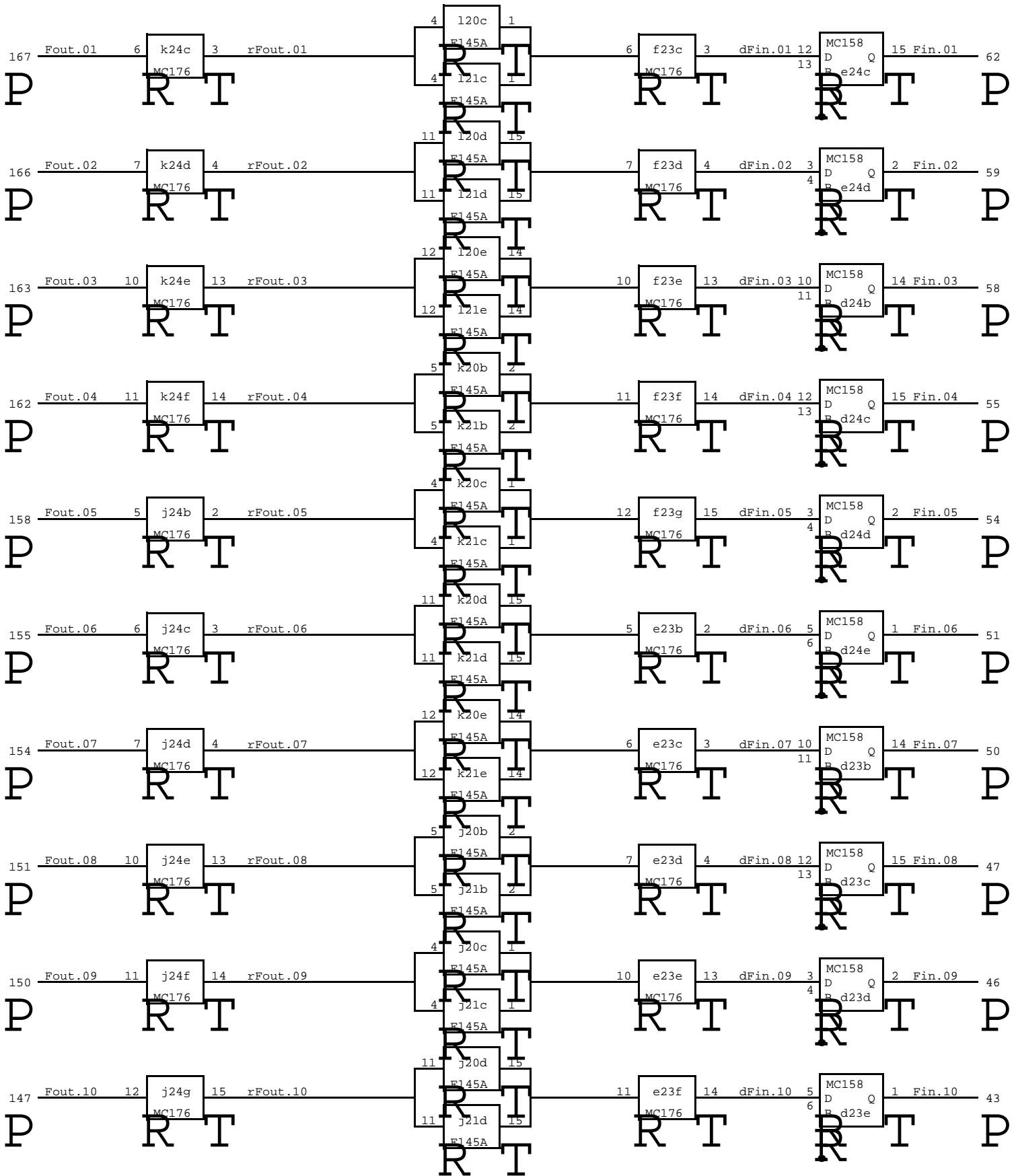
<u>TITLE</u>	<u>PAGE</u>
Slow IO Interface	01
Fast IO Control	02
Sample Bit Slice 00	03
Bits 01 - 10	04
Bits 11 - 17	05
Selected Ecl Chip Qualifier	06
Clock Distribution	07
Layout	08

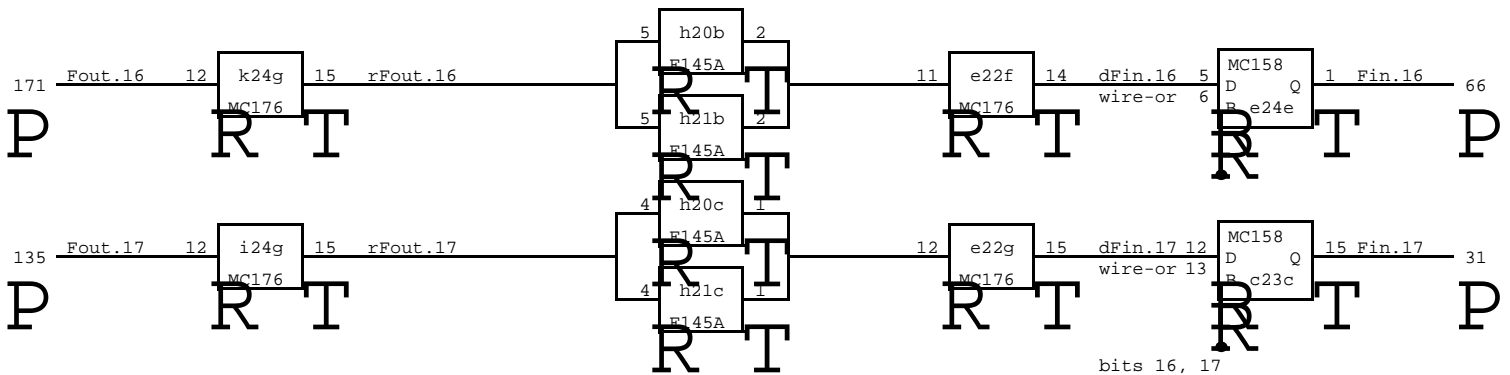
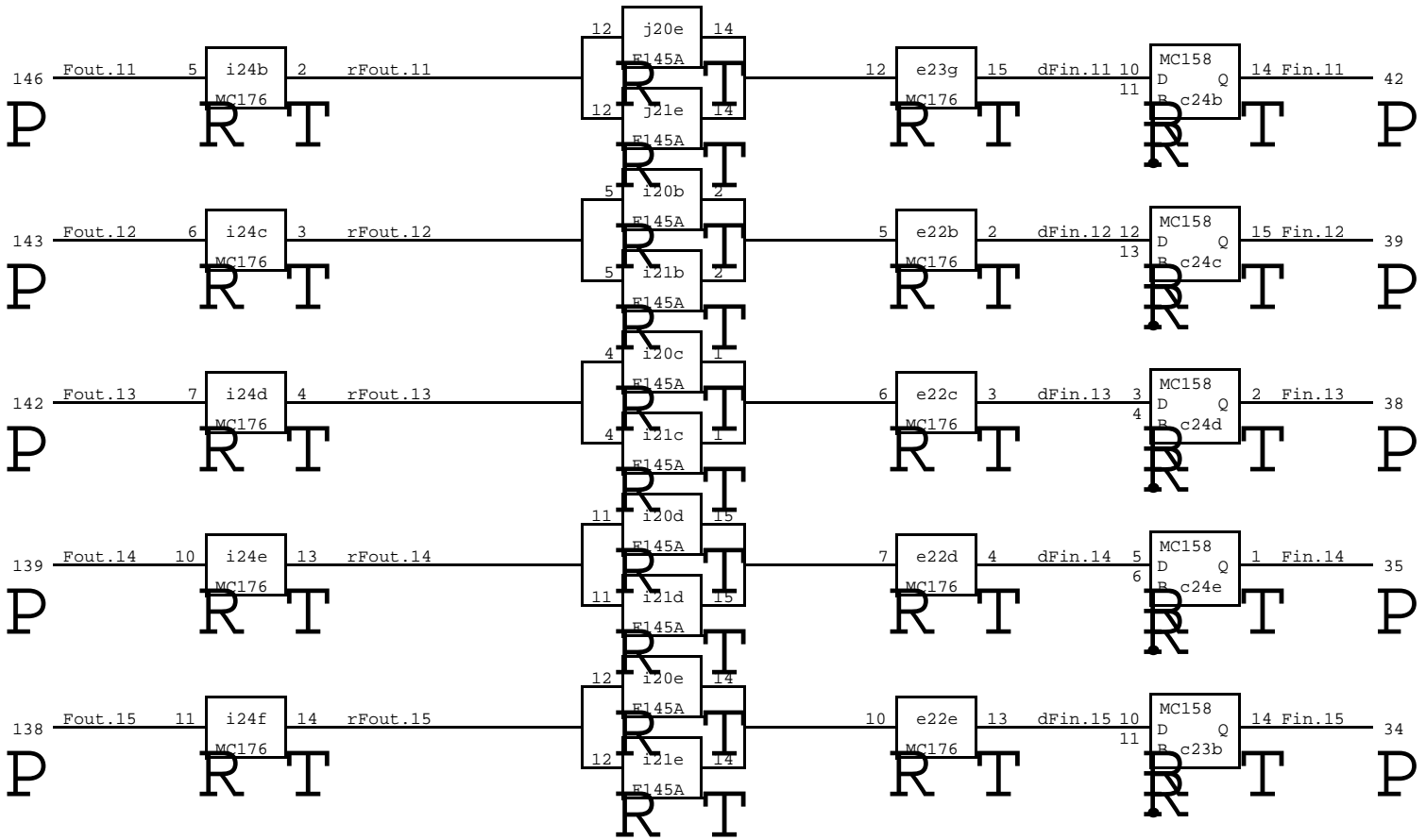




BITS 0-17

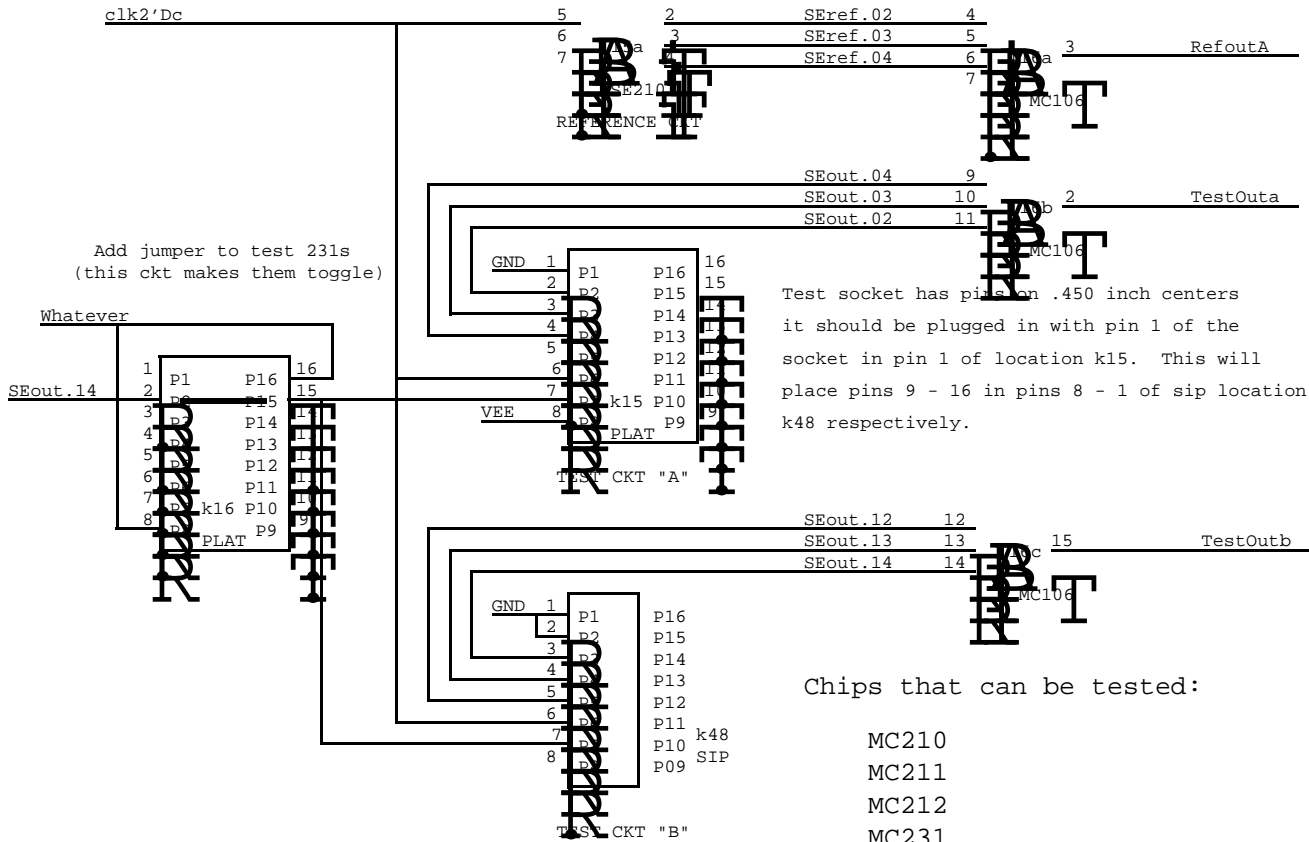






bits 16, 17
 wire-ored with
 bits in control
 register so parity can
 be played with

Place 1 unit load on all test outputs



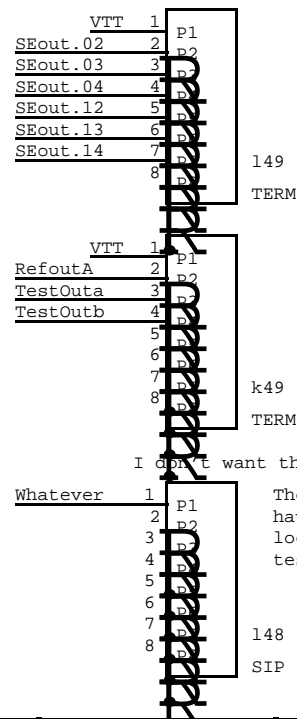
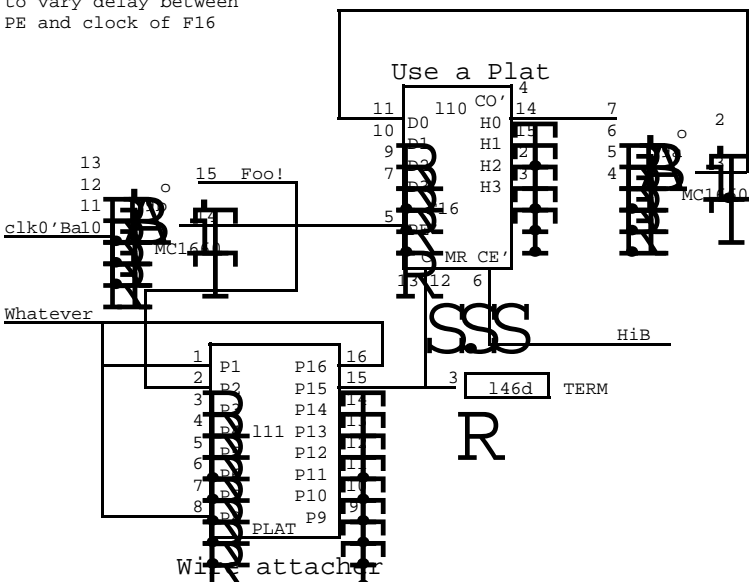
Chips that can be tested:

- MC210
- MC211
- MC212
- MC231

Check outputs on pins 2 & 3 and pin 14 -- pin 15 can't be tested
Jumper in k16 pin 2-15 must be added

Severo's F16 Tester

Hook variable length wire between Plat P1 and P16 to vary delay between PE and clock of F16

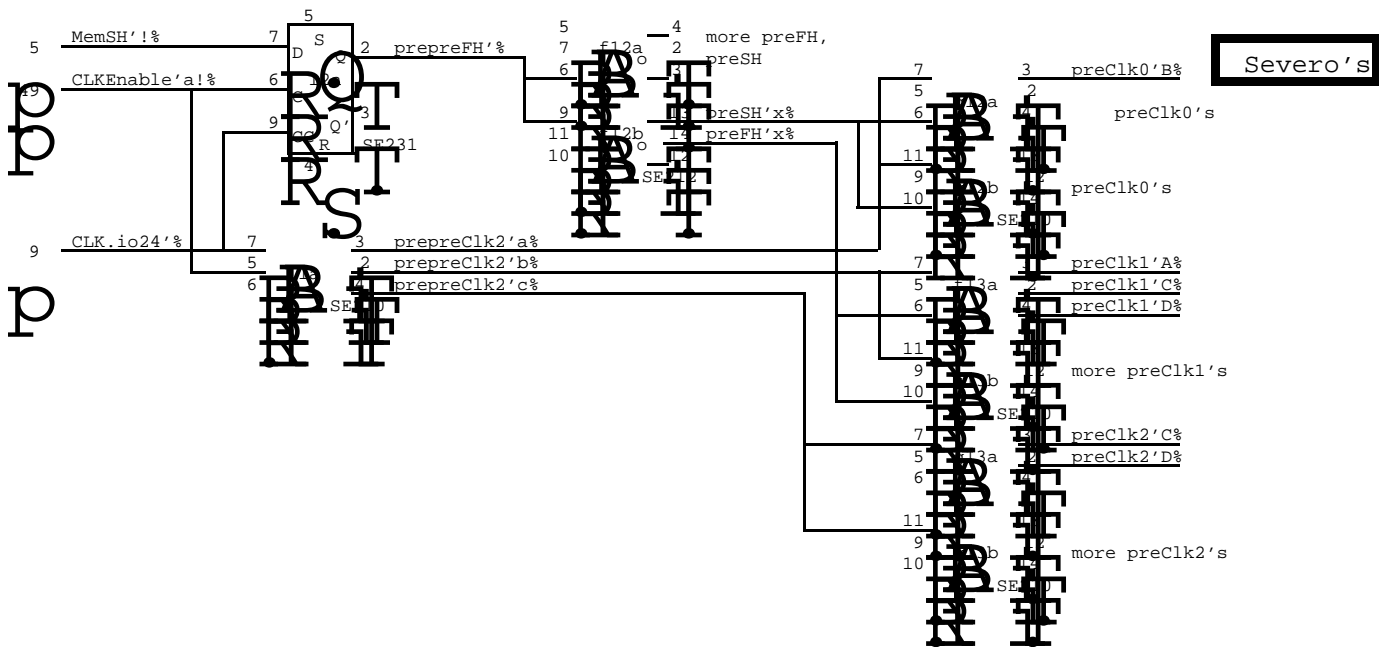


These signals are not recognised by Route as ECL outputs, so I have to explicitly terminate them.

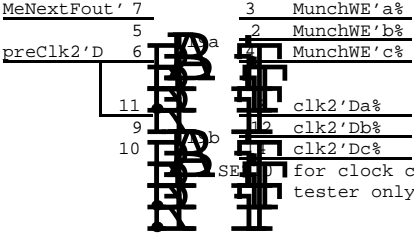
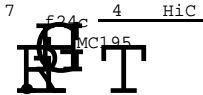
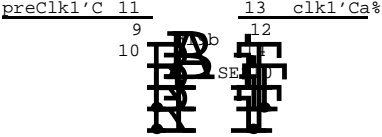
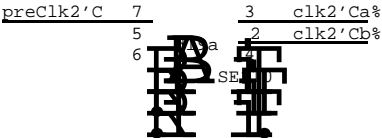
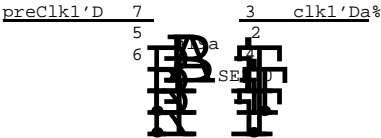
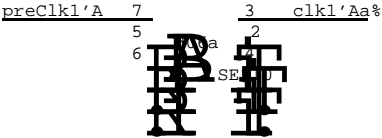
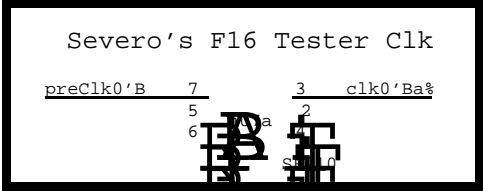
These signals don't go any where, so I have to explicitly terminate them.

I don't want this location used for termination.

The decoupling capacitors have been removed for this location to accomodate the test socket.



Severo's



for clock chip tester only

Cxx

	a 181	b 168	c 153	d 137	e 124	f 109	g 93	h 80	i 64	j 48	k 33	l 20	B
1				TIOA rcvr 176 1a 176 1a				IOB receiver 11-15,17 197	6-10,16 197	0-5 197		clock stuff 210	1
2												231	2
3													3
4													4
5													5
6				clk1'Aa 210									6
7										clk0'Ba SMO 210			7
8													8
9												SE 1660	9
10												VE F16	10
11												RO' wire Plat	11
12						clock stuff 212							12
13							210	210					13
14													14
15											TEST SOCKET	SE tester 210	15
16											SE tester Jumper	SE tester 106	16
17													17
18													18
19				clk2'Ca,b clk1'Ca 210	TIOA Comp 113 113				MunchWE' clk2'Da,b 210	clk1'Da 210			19
20					MyTask F16 1a		MunchCE' 135 2b	16,17 145 WEa	12-15 145 WEa	8-11 145 WEB	4-7 145 WEC	0-3 145 WEC	20
21					MySubTsk dFin.16,17 F16 1a	IOBld' rIOout 103	WordAd F16 2b		Two-Munch Memory 145 WEa 145 WEB 145 WEB 145 WEC 145 WEC				21
22		FinTask Comp 113	MeFinDly' 113	dFin 12-17 176 2b	MeNextBth 117								22
23		FinTask rcvr 176 2a	Fin drivers 15,17 158	7-10 158	6-11 176 2b	0-5 176 2b			MeNextFout 1a 231	FoutTask Comp rIOreset 113			23
24	NEXT rcvr 113	SubTask drivers 102	11-14 158	3-6 158	0-2,16 158	rFinNext 195			Fout receiver 11-15,17 176 2a 5-10 176 2a 0-4,16 176 2a				24

C a 11 b 26 c 39 d 55 e 70 f 86 g 99 h 114 i 129 j 143 k 159 l 174 D

PEROX PARC/CSL	Project Dorado	Reference Layout	File IOtest08.sil	Directory <Clark>/SMO	Rev Ad	Date 3/02/84	Page 08
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