D O R A D O D R A W I N G S

Fast I/O test board

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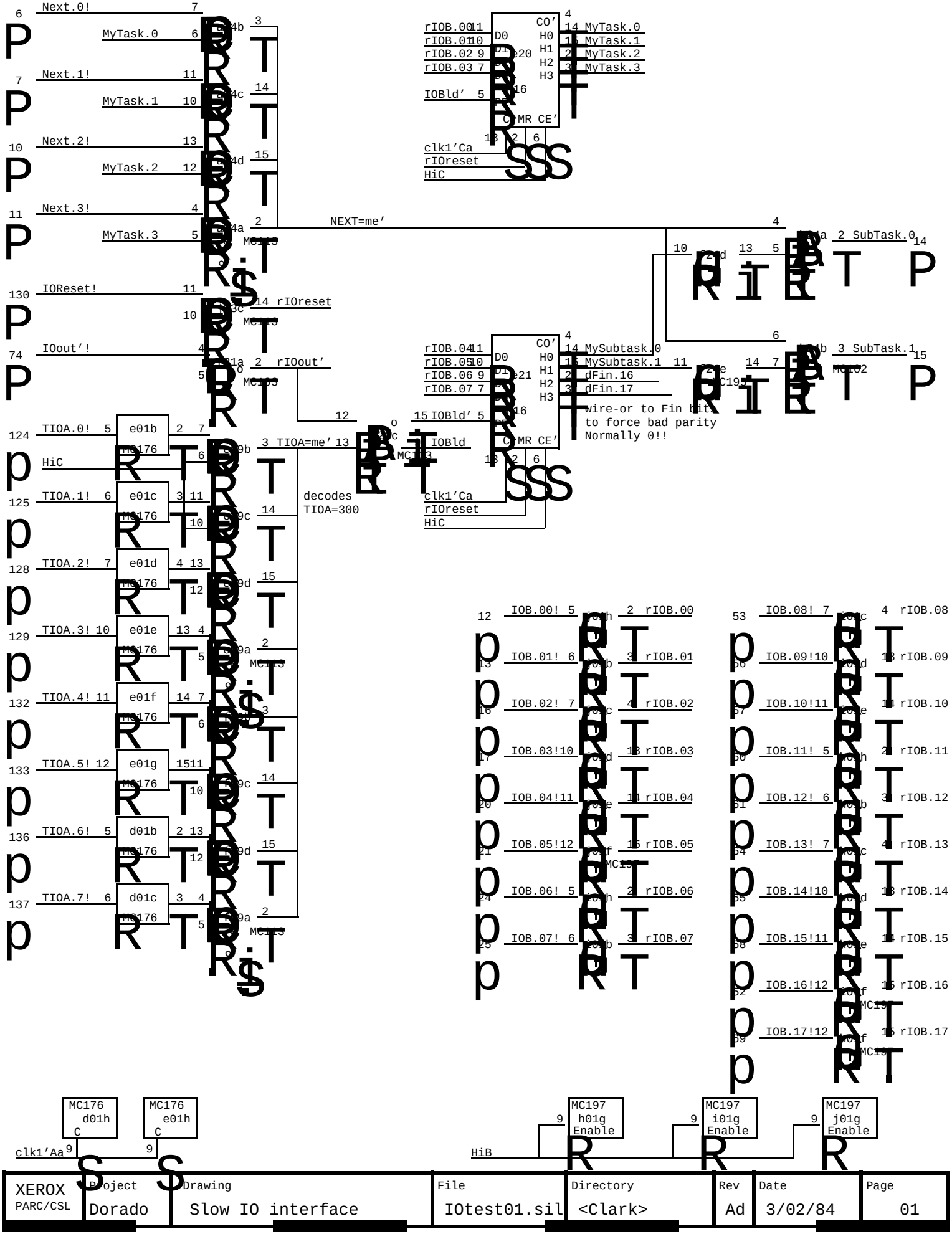
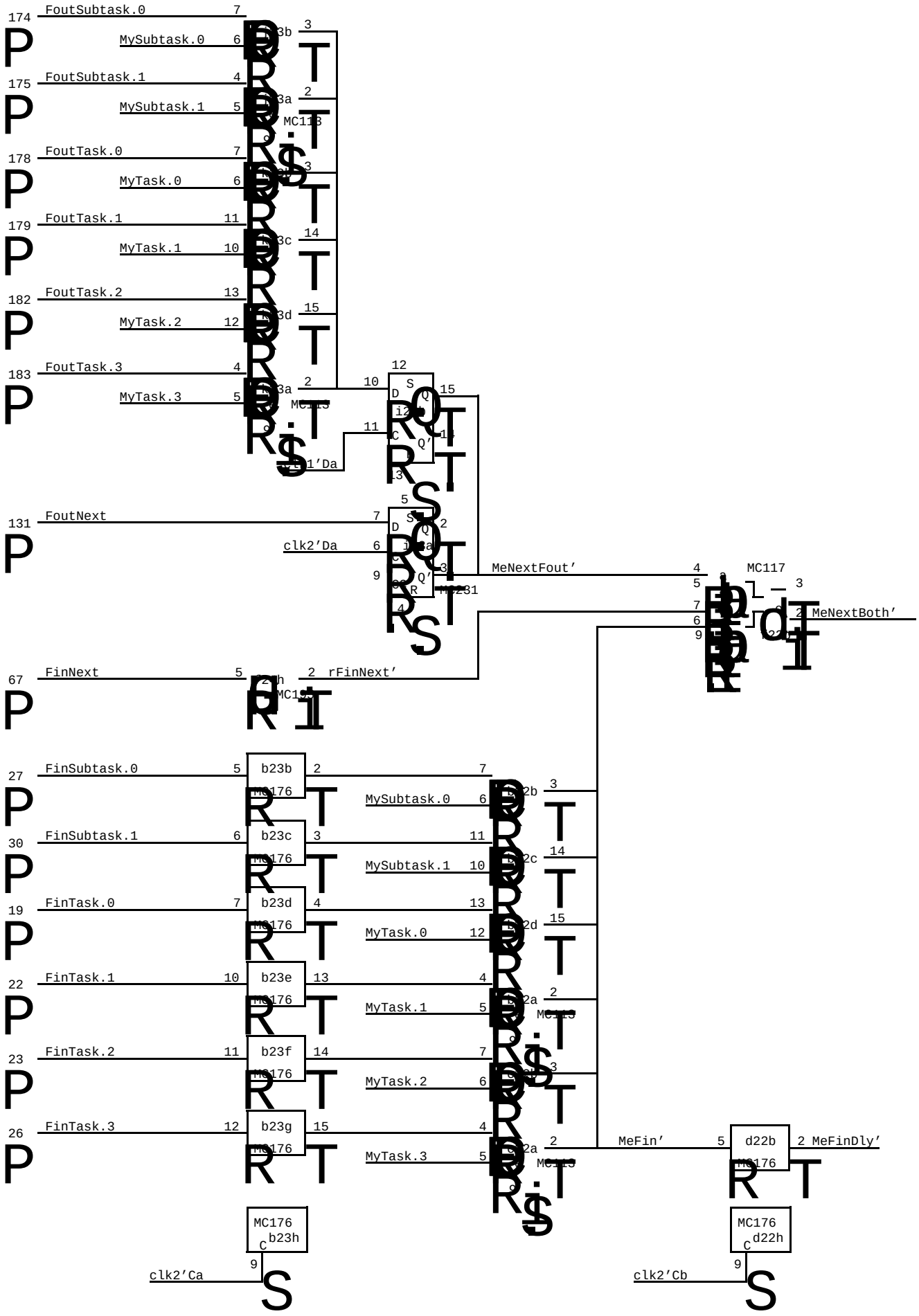
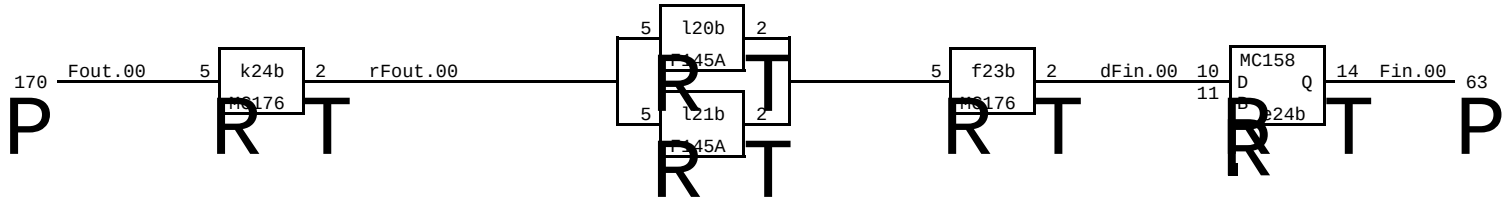


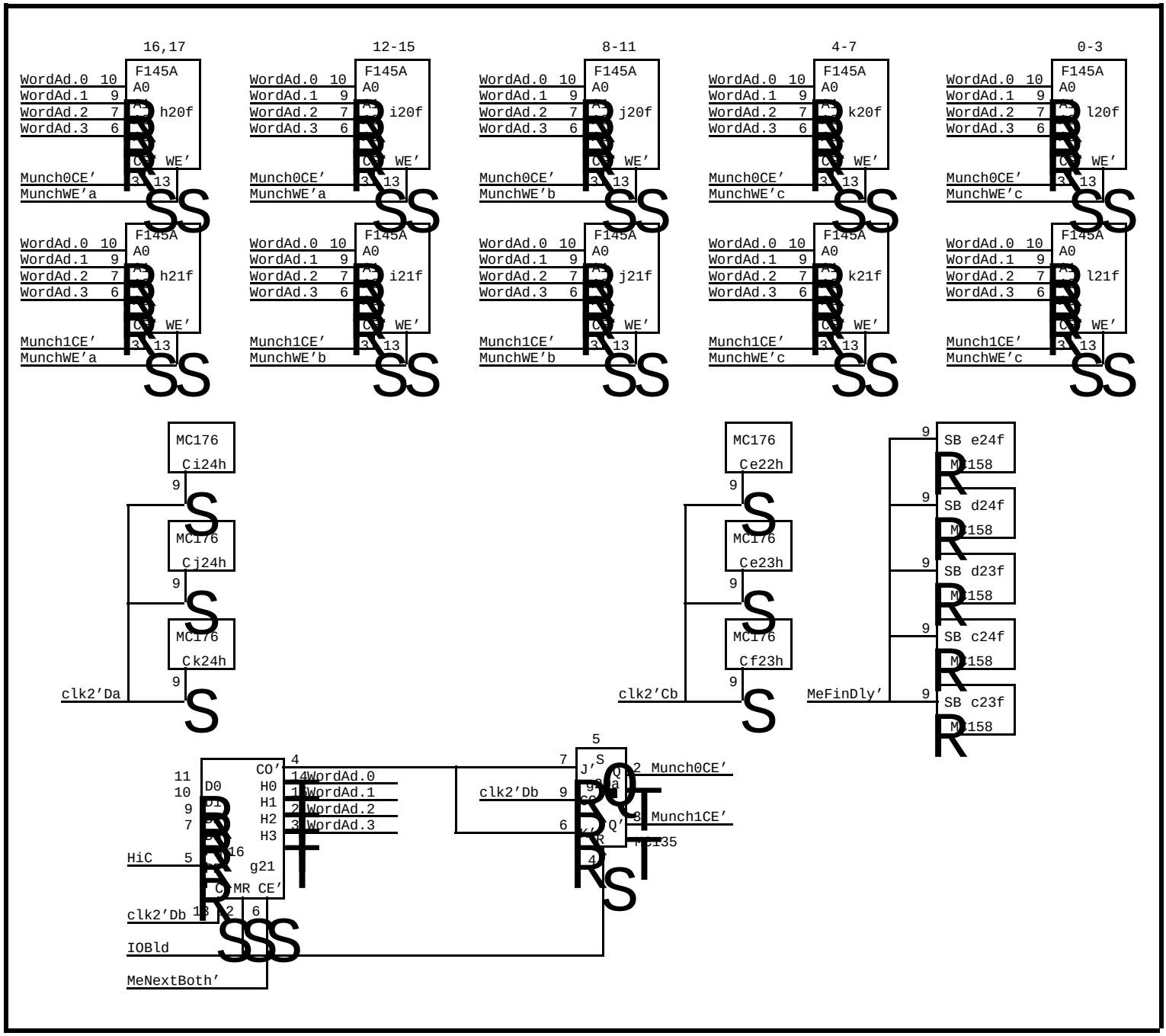
XEROX PARC/CSL	Project	Drawing	File	Directory	Rev	Date	Page
	Dorado	Slow IO interface	IOtest01.sil	<Clark>	Ad	3/02/84	01



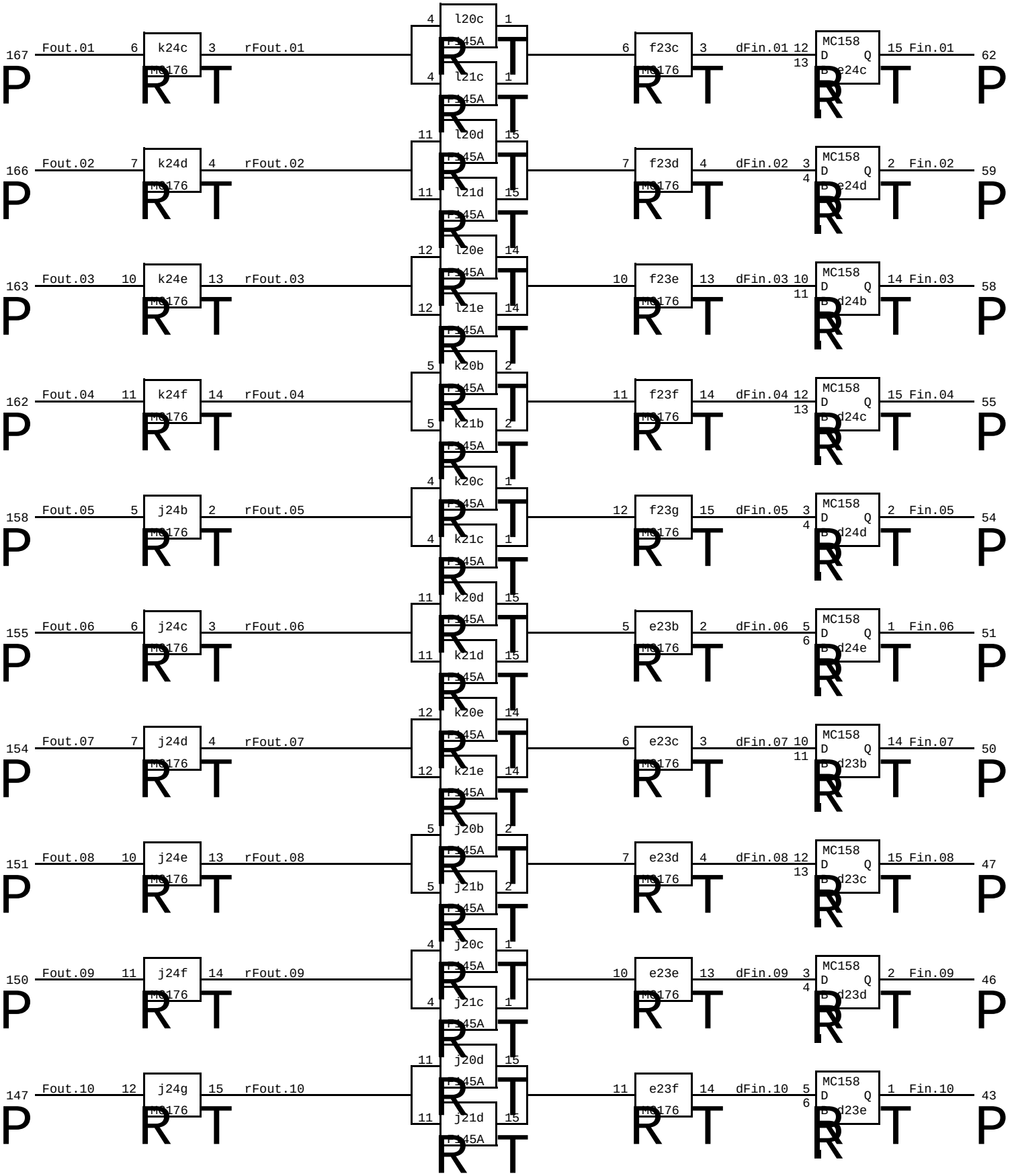
XEROX PARC/CSL	Project	Drawing	File	Directory	Rev	Date	Page
	Dorado	Control	IOtest02.sil	<Clark>	Ad	3/02/84	02

BITS 0-17

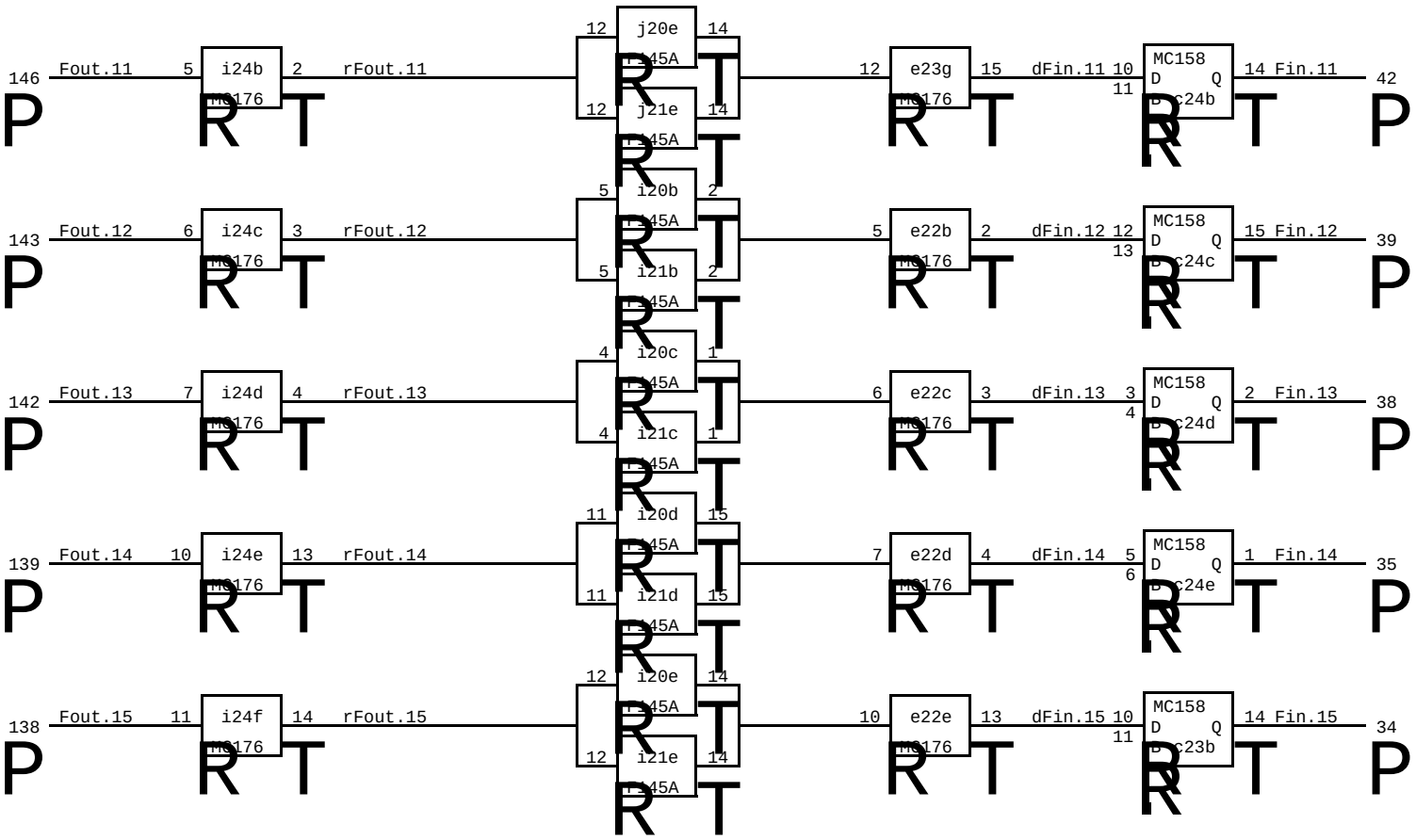


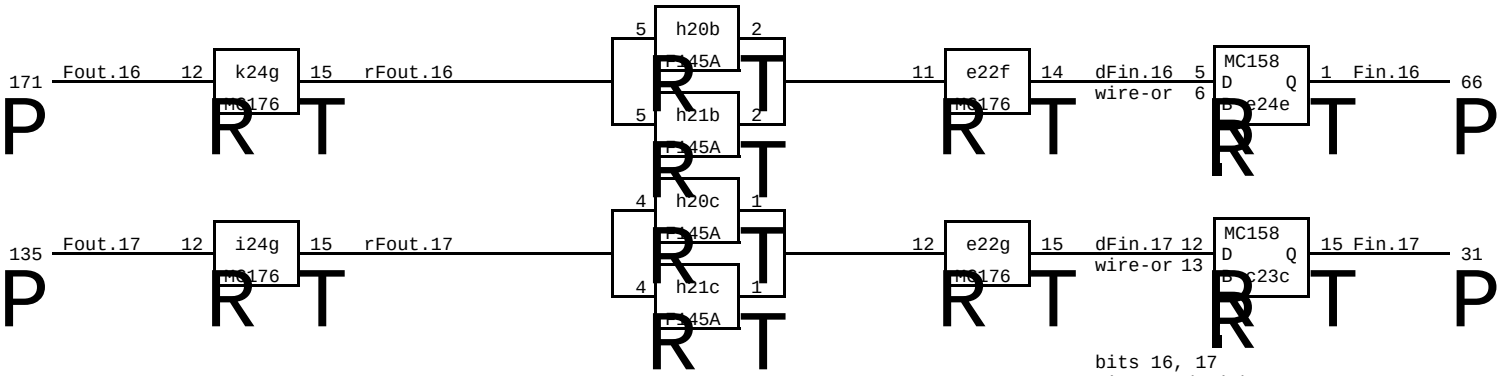


XEROX PARC/CSL	Project	Drawing	File	Directory	Rev	Date	Page
	Dorado	Sample bit-slice	IOtest03.sil	<Clark>	Ad	3/02/84	03



XEROX PARC/CSL	Project	Drawing	File	Directory	Rev	Date	Page
	Dorado	Bits 1-10	IOtest04.sil	<Clark>	Ad	3/02/84	04

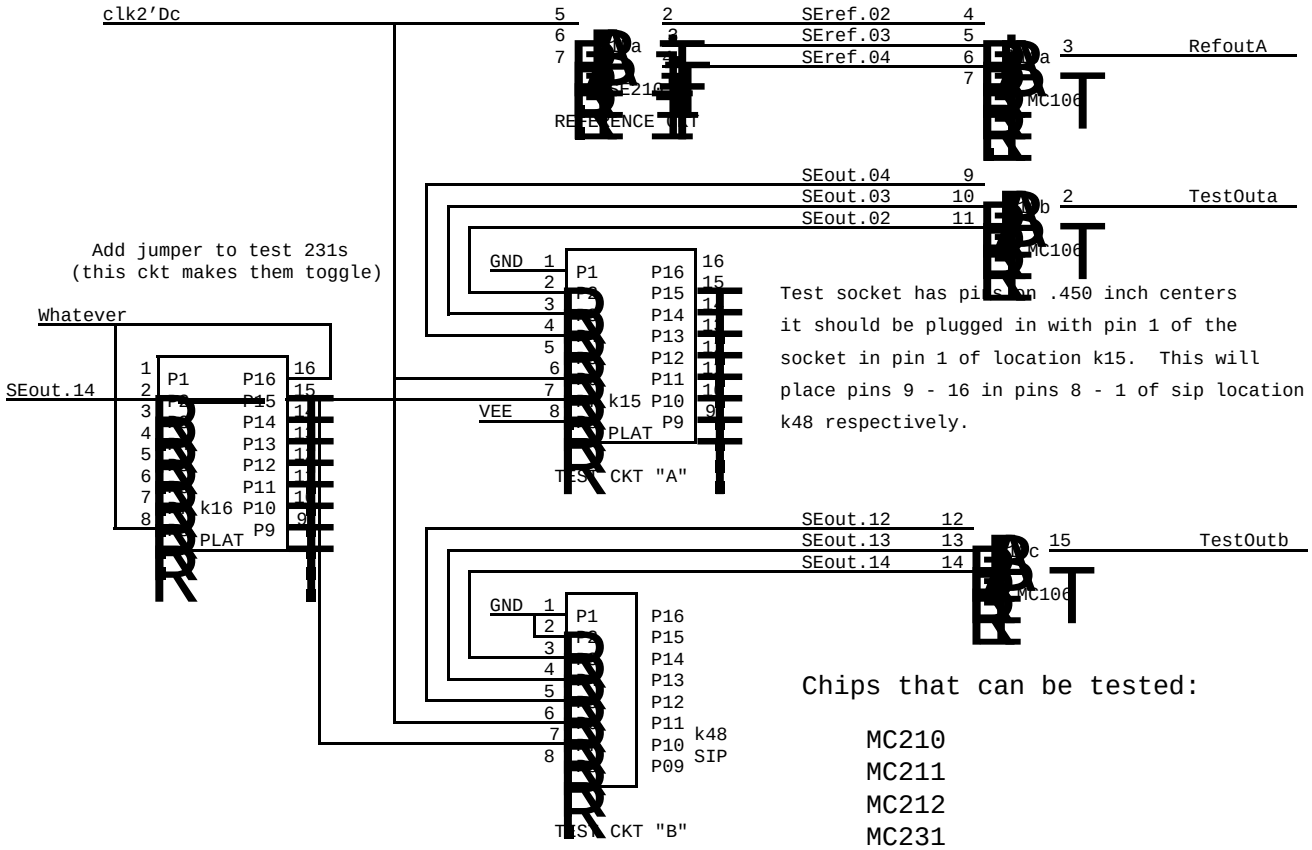




bits 16, 17
wire-ored with
bits in control
register so parity can
be played with

XEROX PARC/CSL	Project	Drawing	File	Directory	Rev	Date	Page
	Dorado	Bits 11-17	IOtest05.sil	<Clark>	Ad	3/02/84	05

Place 1 unit load on all test outputs



Test socket has pins on .450 inch centers it should be plugged in with pin 1 of the socket in pin 1 of location k15. This will place pins 9 - 16 in pins 8 - 1 of sip location k48 respectively.

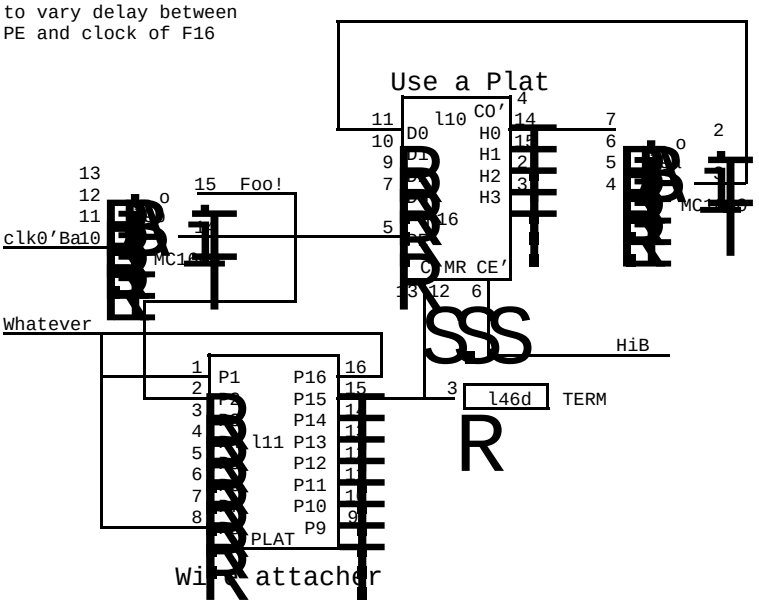
Chips that can be tested:

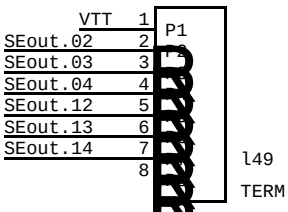
MC210
MC211
MC212
MC231

Check outputs on pins 2 & 3
and pin 14 -- pin 15 can't be tested
Jumper in k16 pin 2-15 must be added

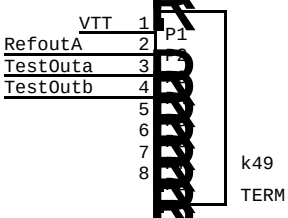
Severo's F16 Tester

Hook variable length wire
between Plat P1 and P16
to vary delay between
PE and clock of F16



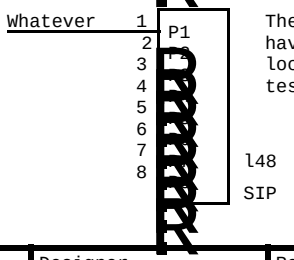


These signals are not recognised by Route as ECL outputs, so I have to explicidly terminate them.



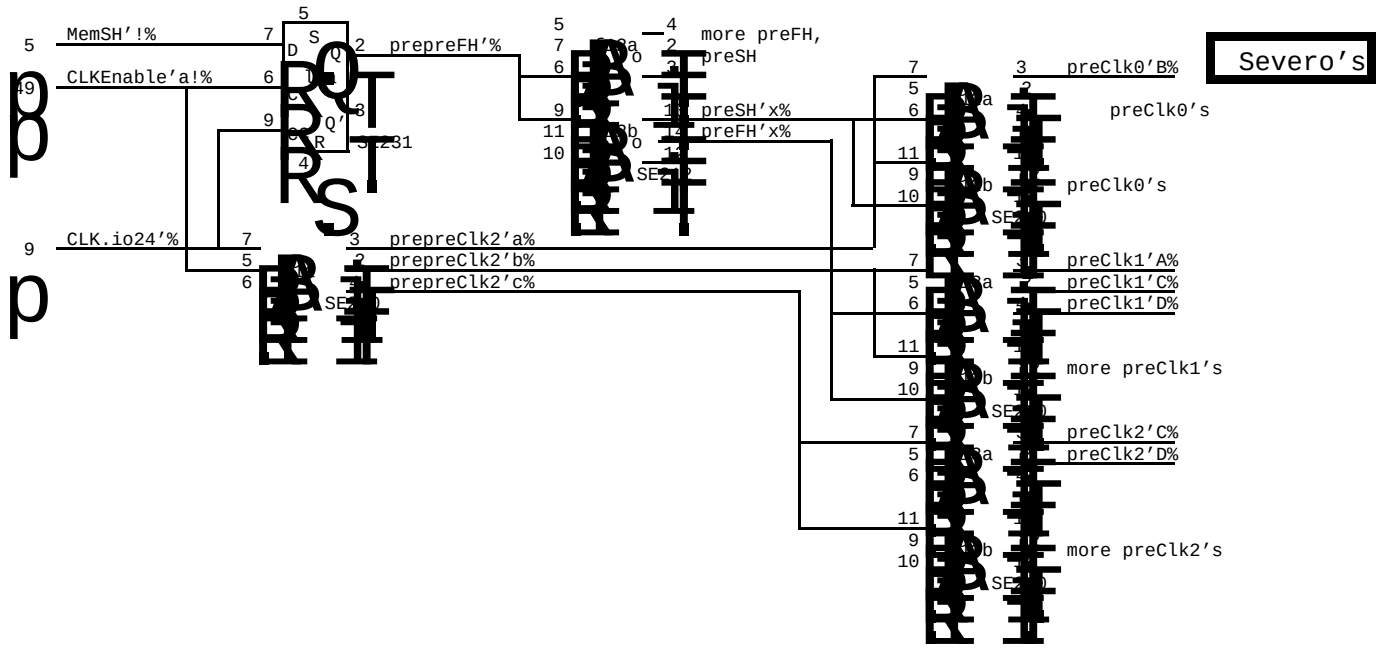
These signals don't go any where, so I have to explicidly terminate them.

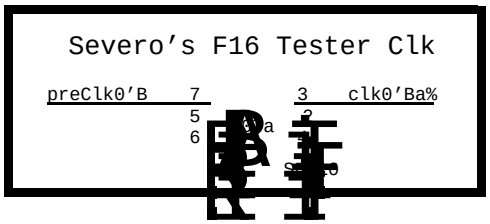
I don't want this location used for termination.

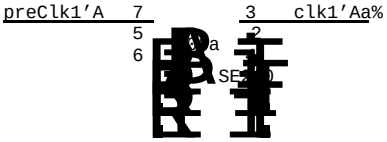


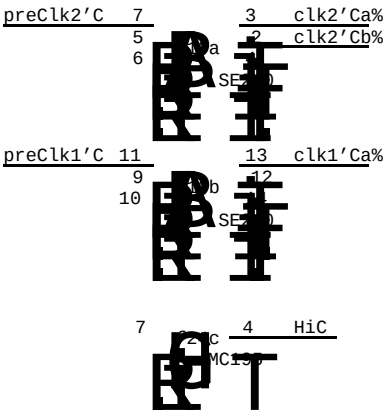
The decoupling capacitors have been removed for this location to accomodate the test socket.

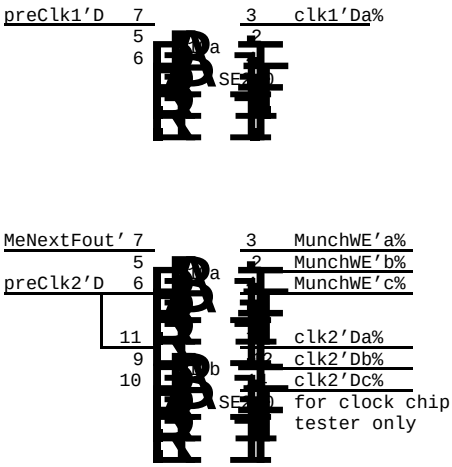
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Selected Ecl chip Qualifier	IOtest06.sil	R Bates/SMO	Ad	3/02/84	06



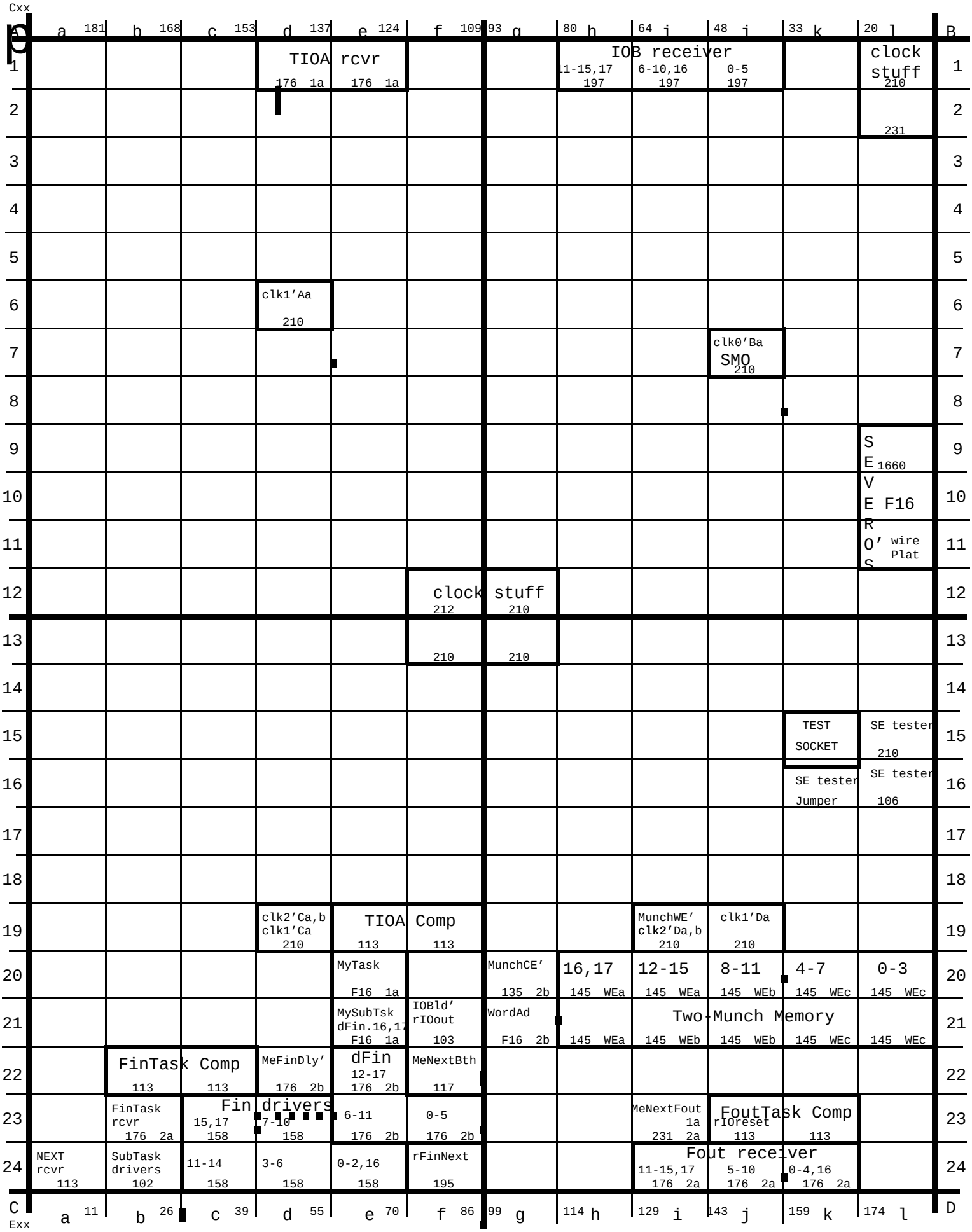








XEROX PARC/CSL	Project	Drawing	File	Directory	Rev	Date	Page
	Dorado	Clock Logic	IOtest07.sil	<Clark>/SMO	Ad	3/02/84	07



XEROX PARC/CSL	Project	Reference	File	Directory	Rev	Date	Page
	Dorado	Layout	IOtest08.sil	<Clark>/SMO	Ad	3/02/84	08