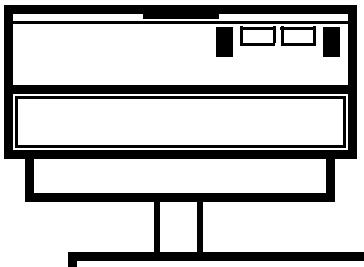
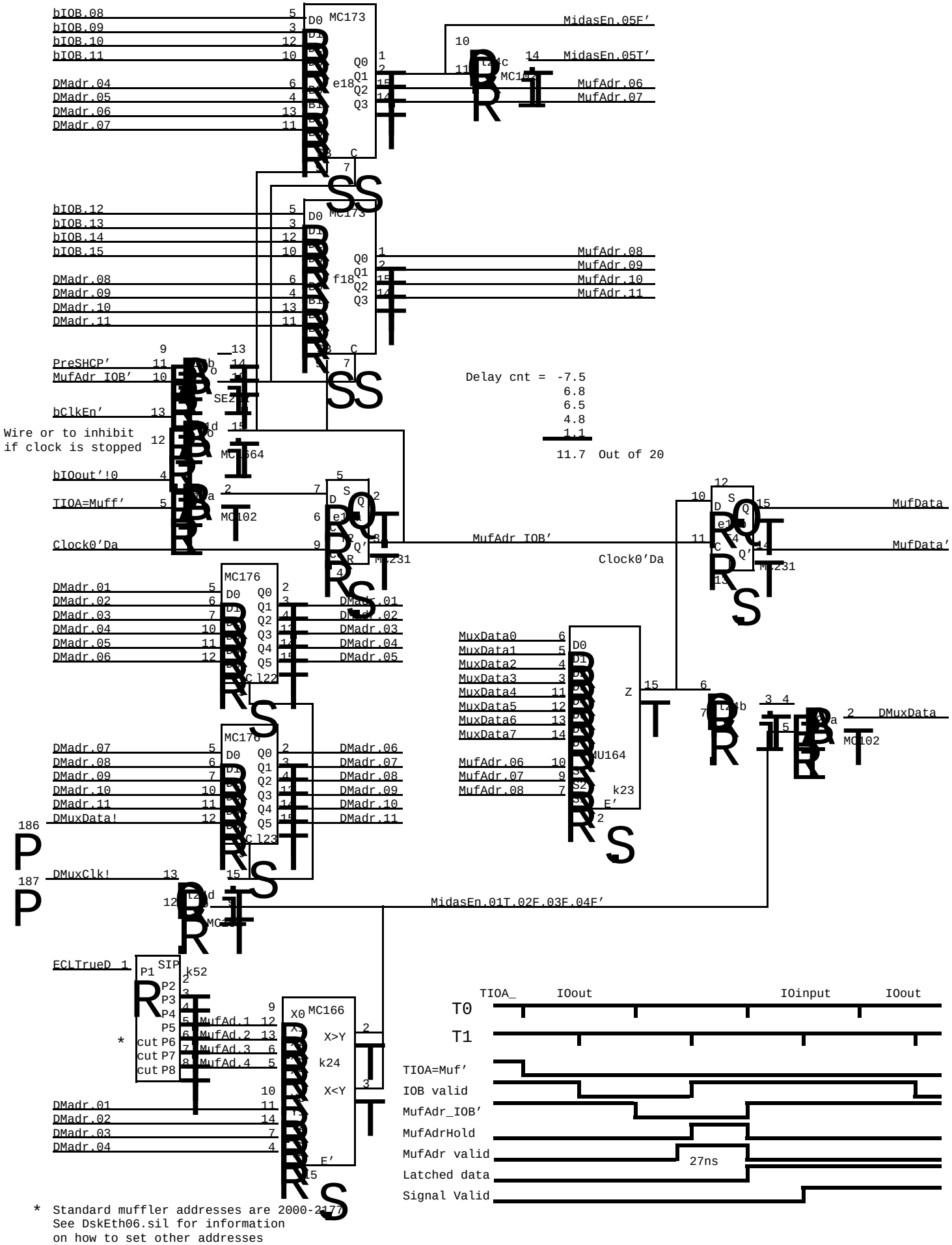


D O R A D O S C H E M A T I C S

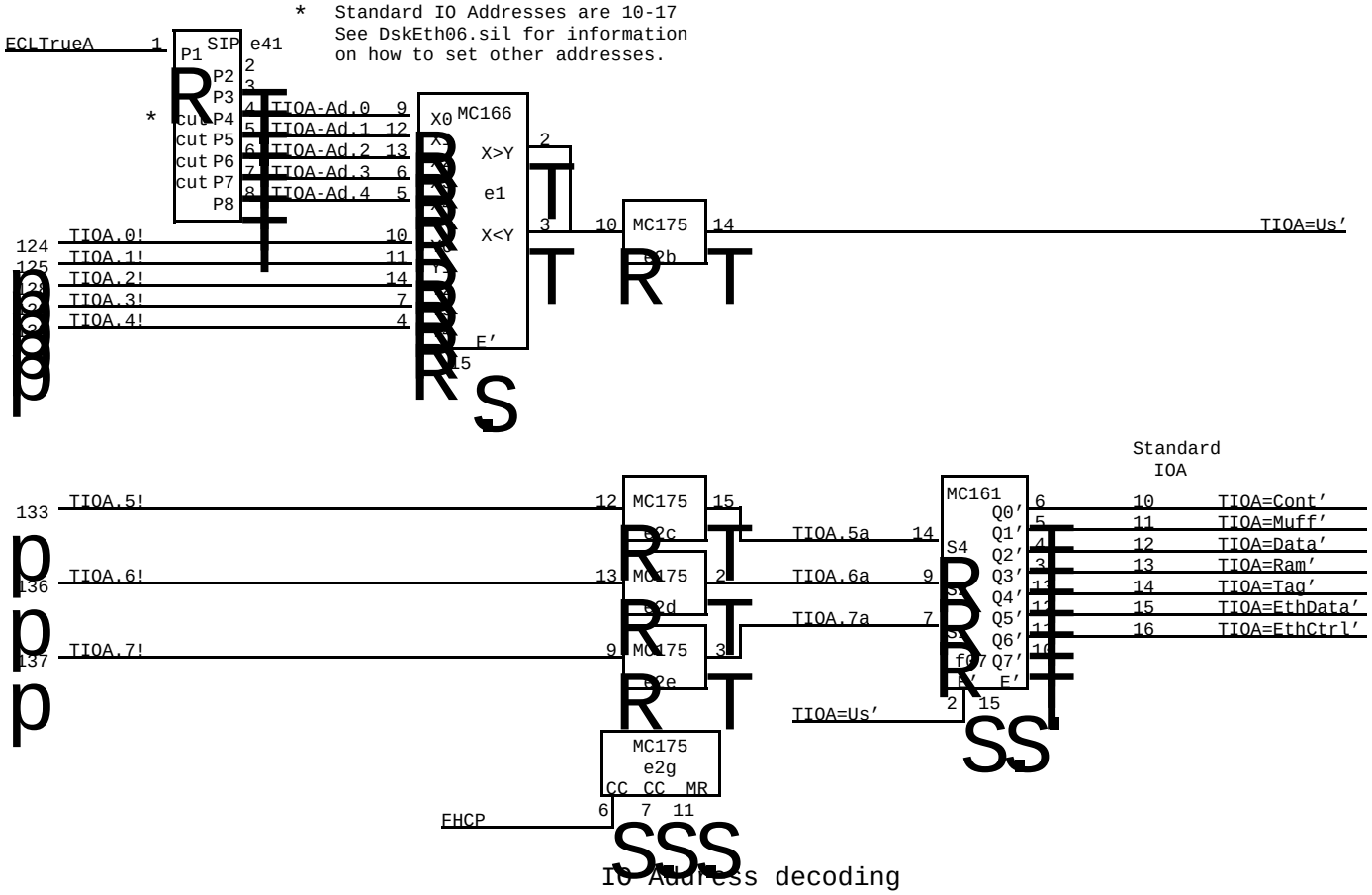
I / O H A R D W A R E

D I S K a n d E T H E R N E T



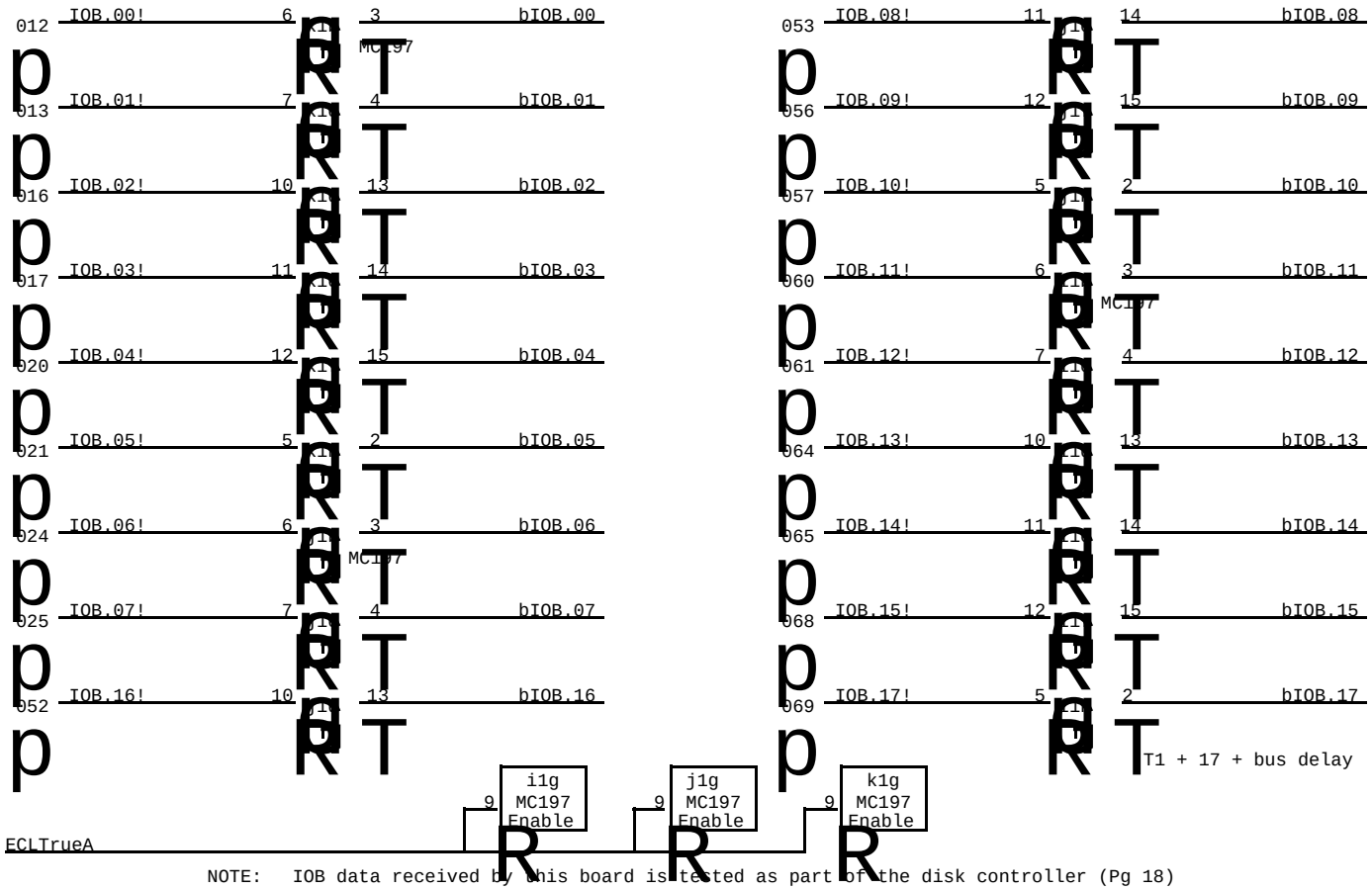
* Standard muffler addresses are 2000-2177
See DskEth06.sil for information
on how to set other addresses

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	DMux Control	DskEth01.sil	Roger Bates	Cf	7/19/79	01



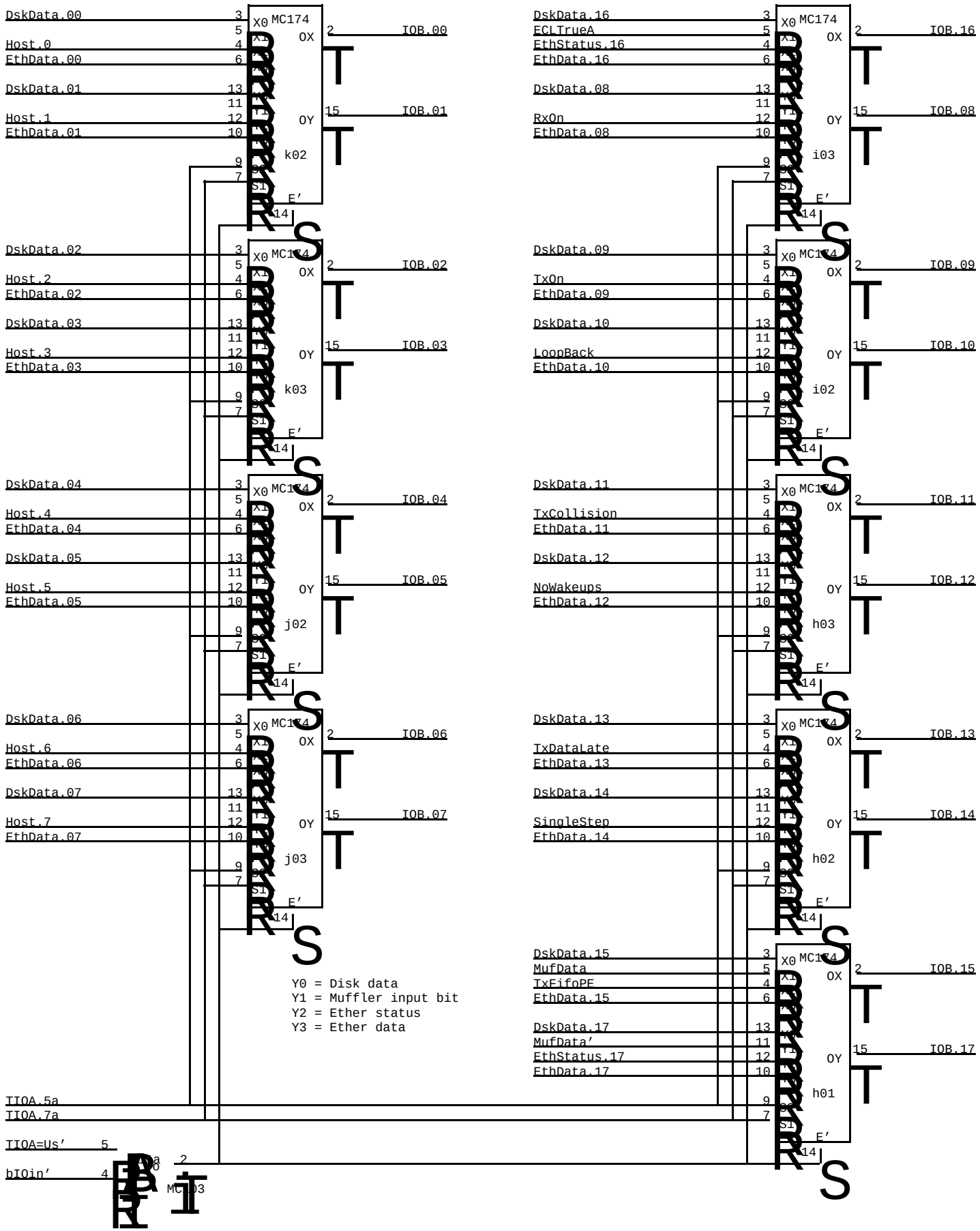
IO Address decoding

IOB receivers

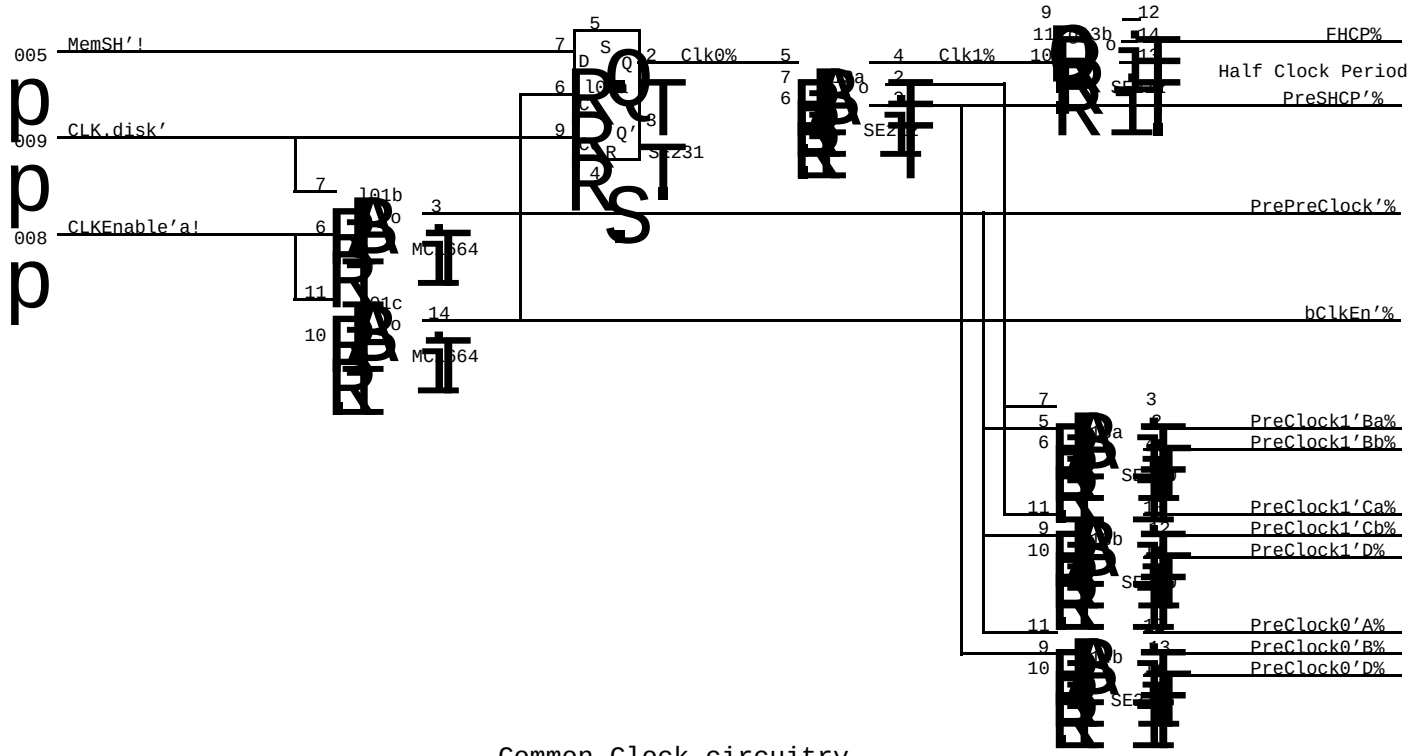


NOTE: IOB data received by this board is tested as part of the disk controller (Pg 18)
Both the disk and the Ethernet check the data parity after it has gone
through the respective FIFO's.

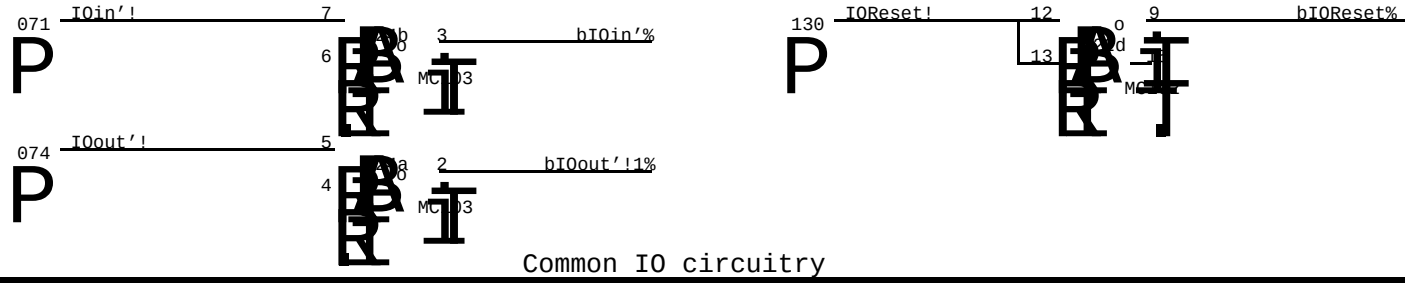
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	IOA & IOB	DskEth02.sil	Bates/Boggs	Cf	7/19/79	02



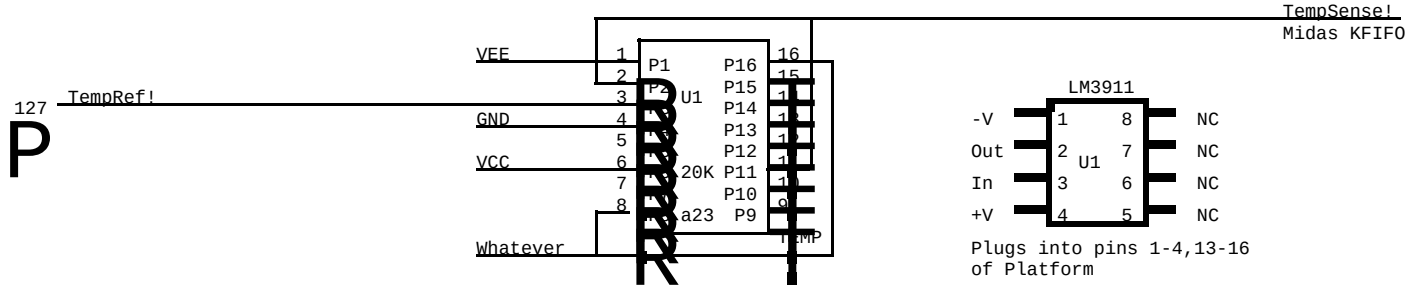
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	IOB data Select/Drivers	DskEth03.sil	Bates/Boggs	Cf	9/24/79	03



Common Clock circuitry



Common IO circuitry



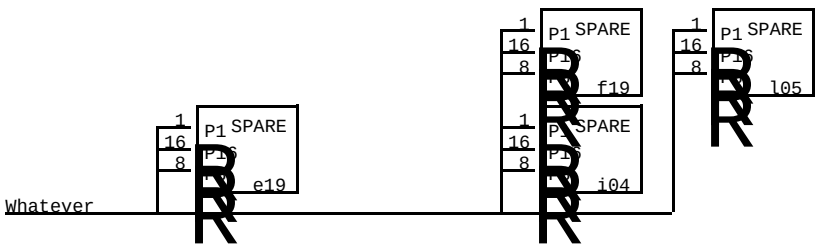
Temperature Sensor

Power connections are as follows:

Stitch-Weld: 1 & 16 are GND
8 is -5

Multiwire: 16 is GND
8 is -5

except in locations
a18, g03, and g16
which are uncommitted



Spare Socket locations for Multiwire

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clocks & IO Signals	DskEth04.sil	Bates/Boggs	Cf	2/09/82	04

31	chips common to Disk & Ether	
137	chips specific to Disk	
111	chips specific to Ether	
9	spare chip positions	
288	total chip positions	

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Stitch-Weld board Layout	DskEth05.sil	Bates/Boggs	Cf	2/09/82	05

Cut SIP legs at k52 to set the
Muffler addresses for the board.
* Standard addresses are 2000-2177.

	Muff Addr	P5	P6	P7	P8
	0000-0177	cut	cut	cut	cut
	0200-0377	cut	cut	cut	
	0400-0577	cut	cut		cut
	0600-0777	cut	cut		
	1000-1177	cut		cut	cut
	1200-1377	cut		cut	
	1400-1577	cut			cut
	1600-1777	cut			
*	2000-2177		cut	cut	cut
	2200-2377		cut	cut	
	2400-2577		cut		cut
	2600-2777		cut		
	3000-3177			cut	cut
	3200-3377			cut	
	3400-3577				cut
	3600-3777				

Cut SIP legs at e41 to set the
IOA bus addresses for the board.
* Standard addresses are 10-17.

	IOA	P4	P5	P6	P7	P8
	000-007	cut	cut	cut	cut	cut
*	010-017	cut	cut	cut	cut	
	020-027	cut	cut	cut		cut
	030-037	cut	cut	cut		
	040-047	cut	cut		cut	cut
	050-057	cut	cut		cut	
	060-067	cut	cut			cut
	070-077	cut	cut			
	100-107	cut		cut	cut	cut
	110-117	cut		cut	cut	
	120-127	cut		cut		cut
	130-137	cut		cut		
	140-147	cut			cut	cut
	150-157	cut			cut	
	160-167	cut				cut
	170-177	cut				
	200-207		cut	cut	cut	cut
	210-217		cut	cut	cut	
	220-227		cut	cut		cut
	230-237		cut	cut	cut	
	240-247		cut		cut	cut
	250-257		cut			
	260-267		cut			cut
	270-277		cut			
	300-307			cut	cut	cut
	310-317			cut	cut	
	320-327			cut		cut
	330-337			cut		
	340-347				cut	cut
	350-357				cut	
	360-367					cut
	370-377					

Cut SIP legs at j52 to set the
Task numbers for the Ethernet.
* Standard tasks are 6 & 7.

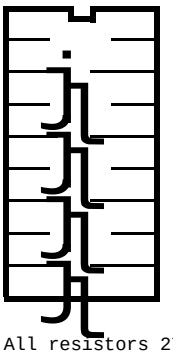
	Tasks	P6	P7	P8
	2 & 3			cut
	4 & 5		cut	
*	6 & 7		cut	cut
	8 & 9	cut		
	10 & 11	cut		cut
	12 & 13	cut	cut	
	14 & 15	cut	cut	cut

The EtherFifo ROMs are identical and interchangeable.
The DiskRead, EtherRcvr and EtherXmtr ROMs are not.

Name	Type	#	Location		
DskEth					
Disk					
DiskRead	SG139	2	a20	a21	
DiskTag	MC149	1	d21		
DiskUnits	S288	1	d05		
DiskFifo	MC149	1	b14		
Ether					
EtherPD	MC149	1	h22		
EtherRcvr	MC149	3	h09	h10	h11
EtherFifo	MC149	2	l10	l15	
EtherXmtr	MC149	3	h14	h15	h16

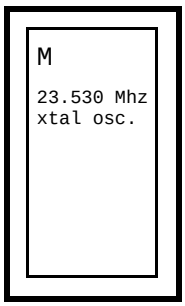
"DoradoProms DskEth" gets all proms for the DskEth board.
"DoradoProms Disk" gets all proms for the Trident half of the board.
"DoradoProms Ether" gets all proms for the Ethernet half of the board.

PLAT at a04

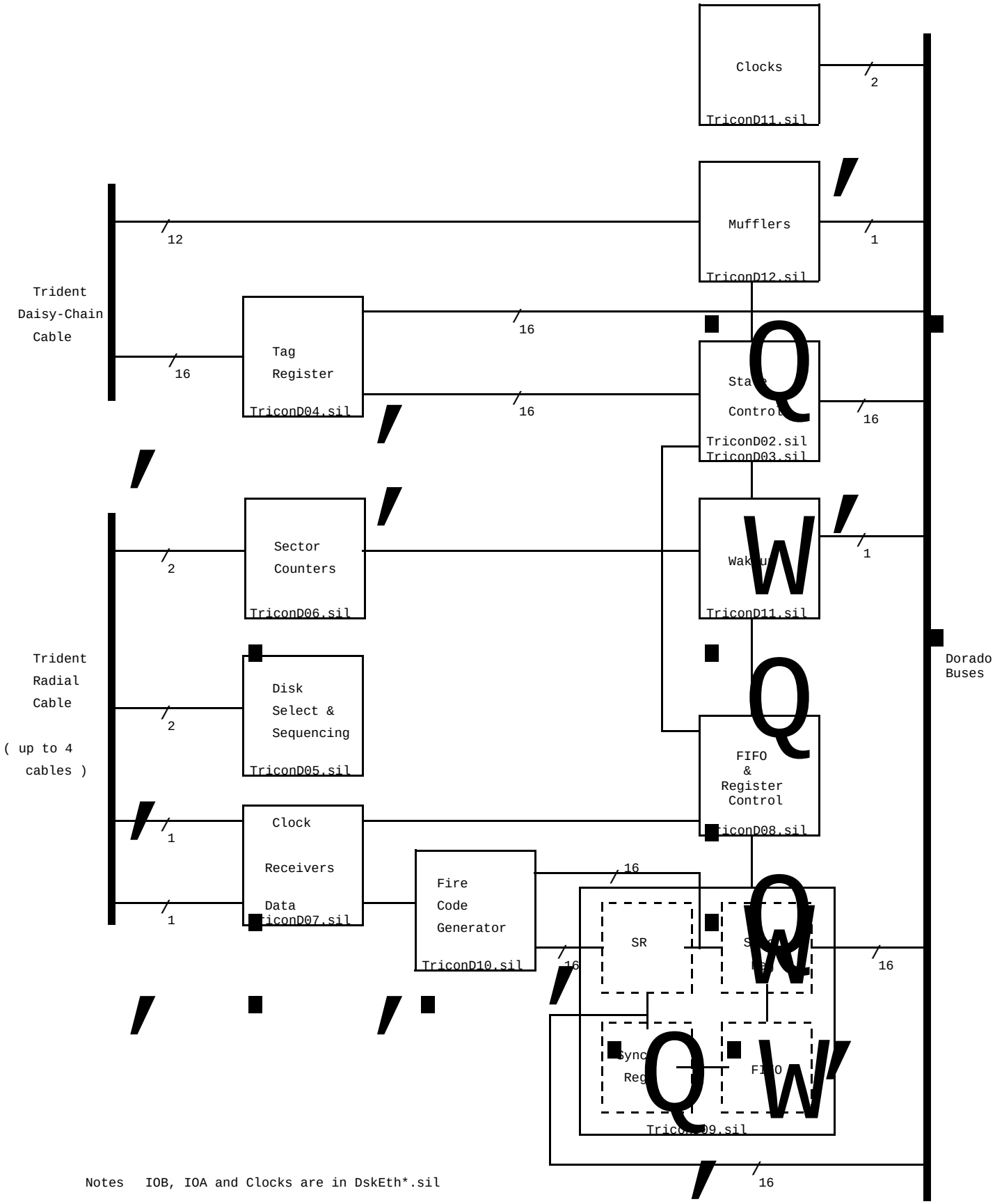


All resistors 27K
All capacitors 330pf

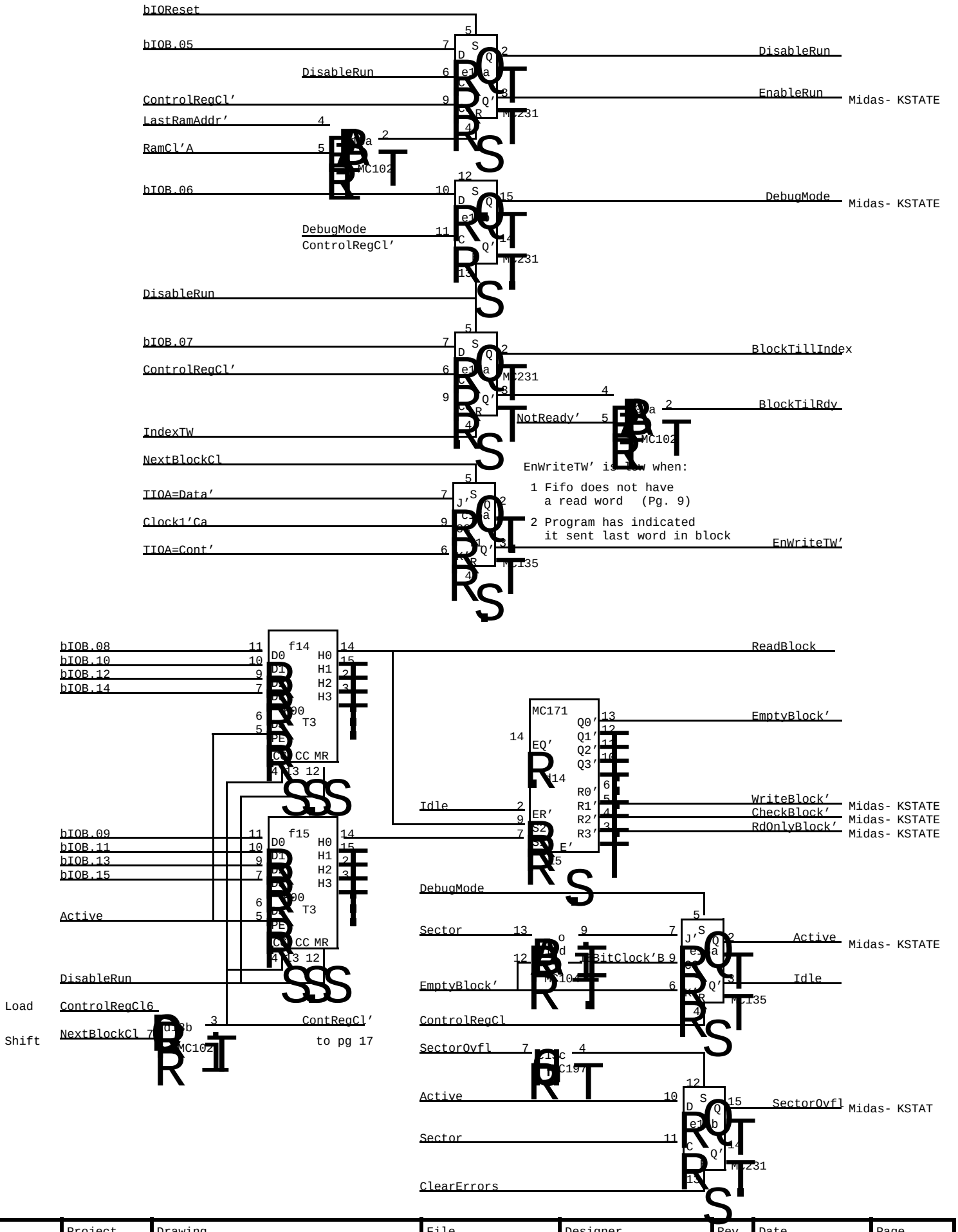
K1115A at j20



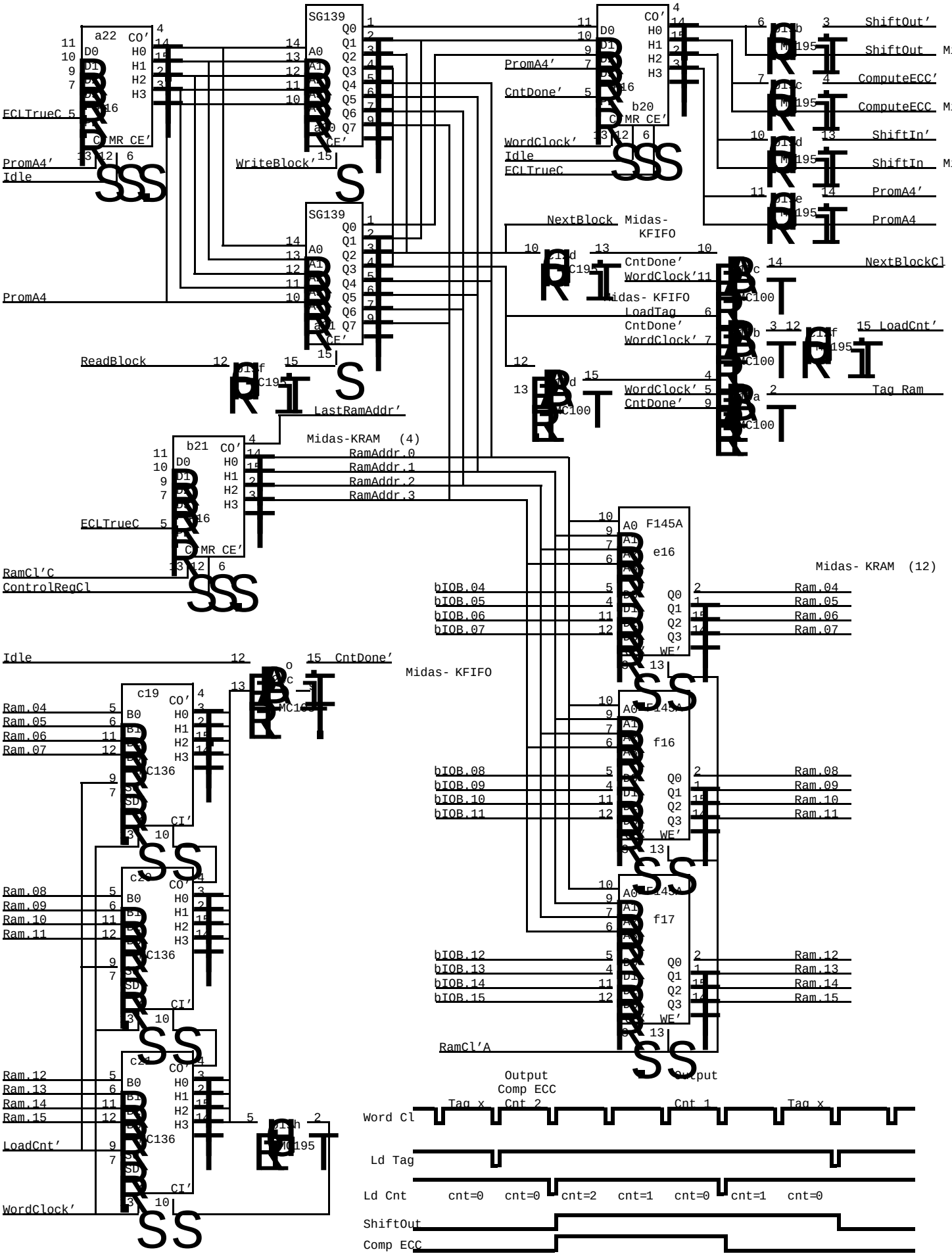
Logo is near pin 1.
This is a 14 pin pkg.
Board pins 8 & 9 aren't used.
Remove bypass cap above pin 1



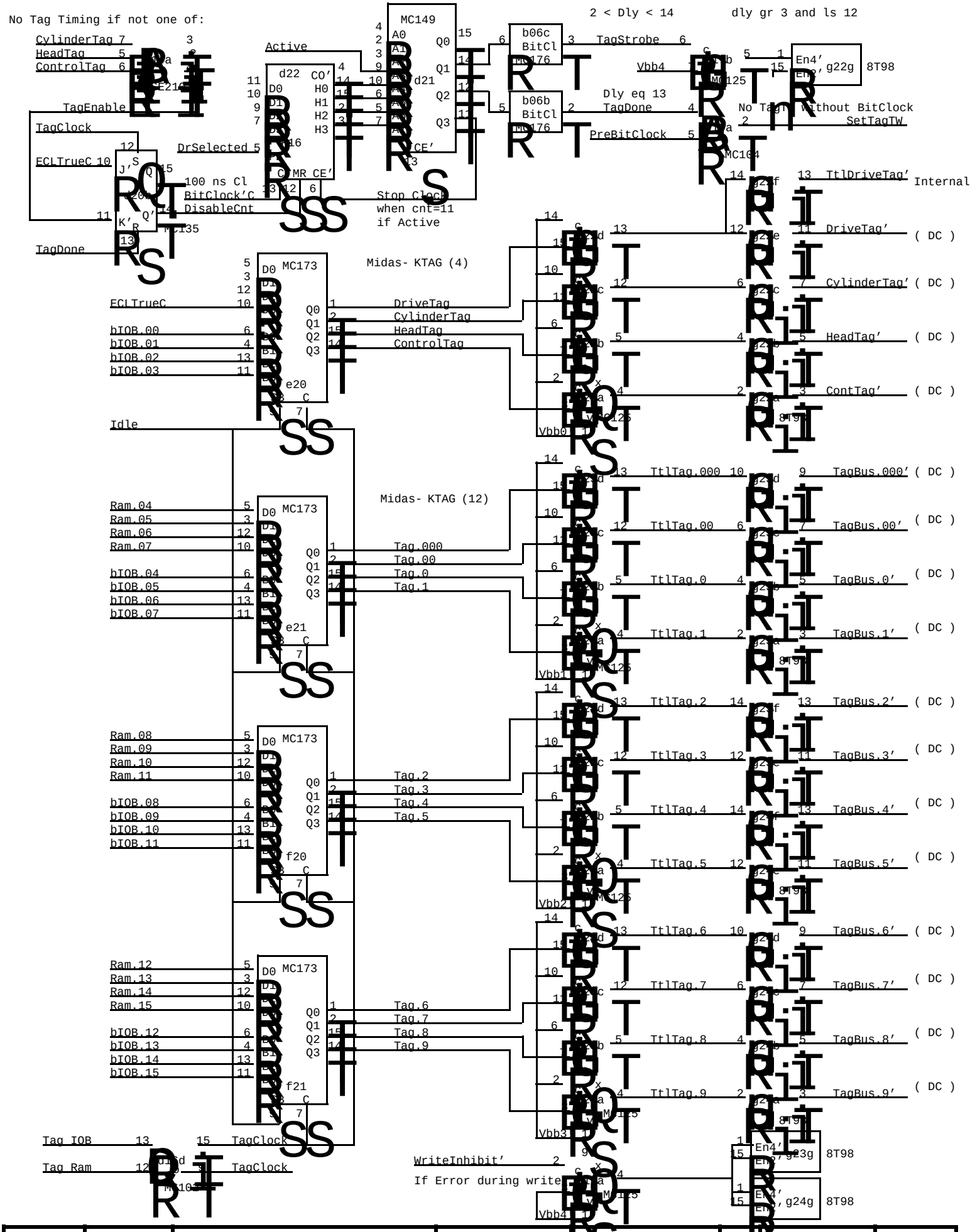
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Dorado Disc Controller	TriconD01.sil	Roger Bates	Cf	7/19/79	07



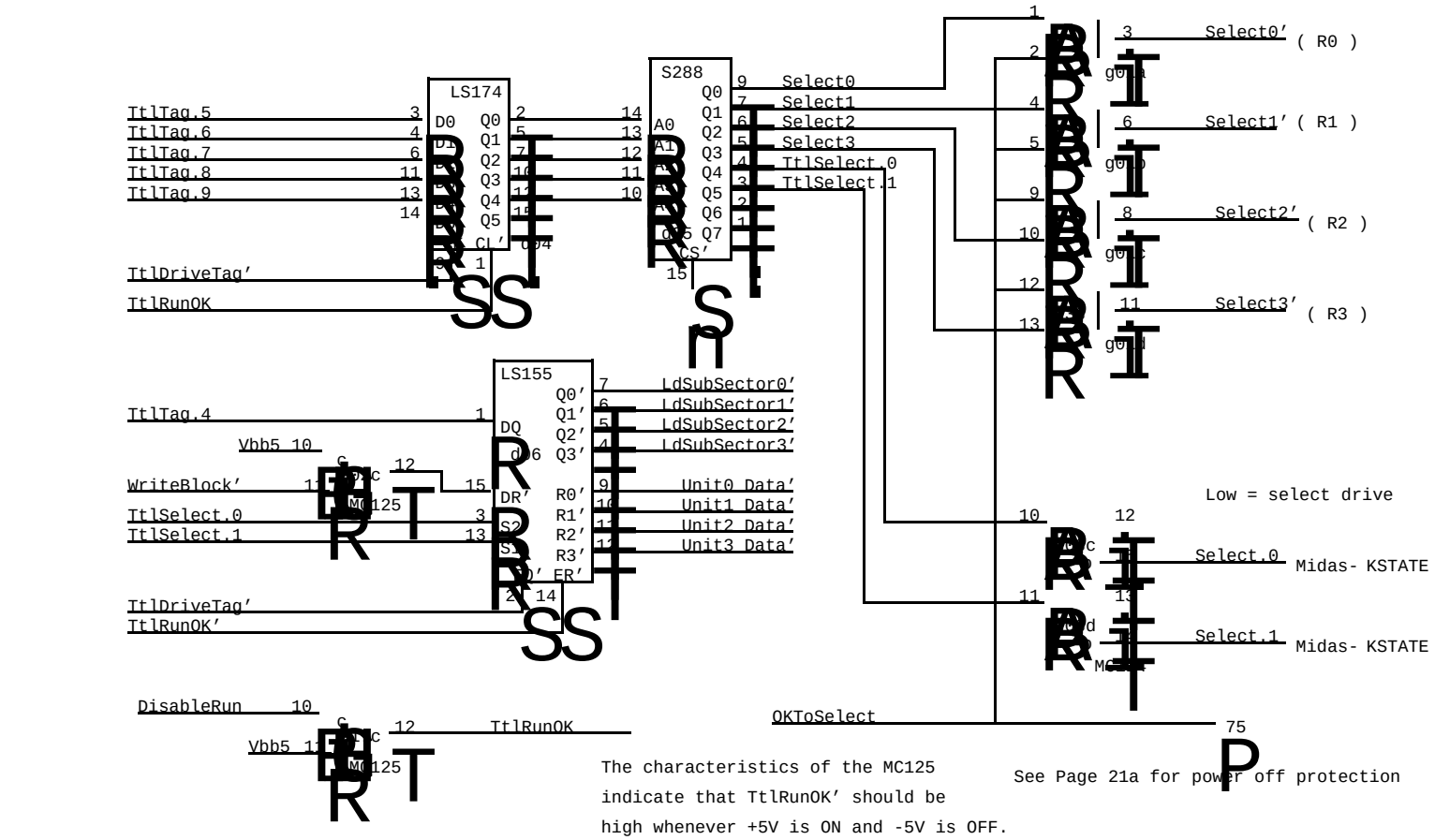
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	State Control Register	TriconD02.sil	Roger Bates	Cf	9/24/79	08

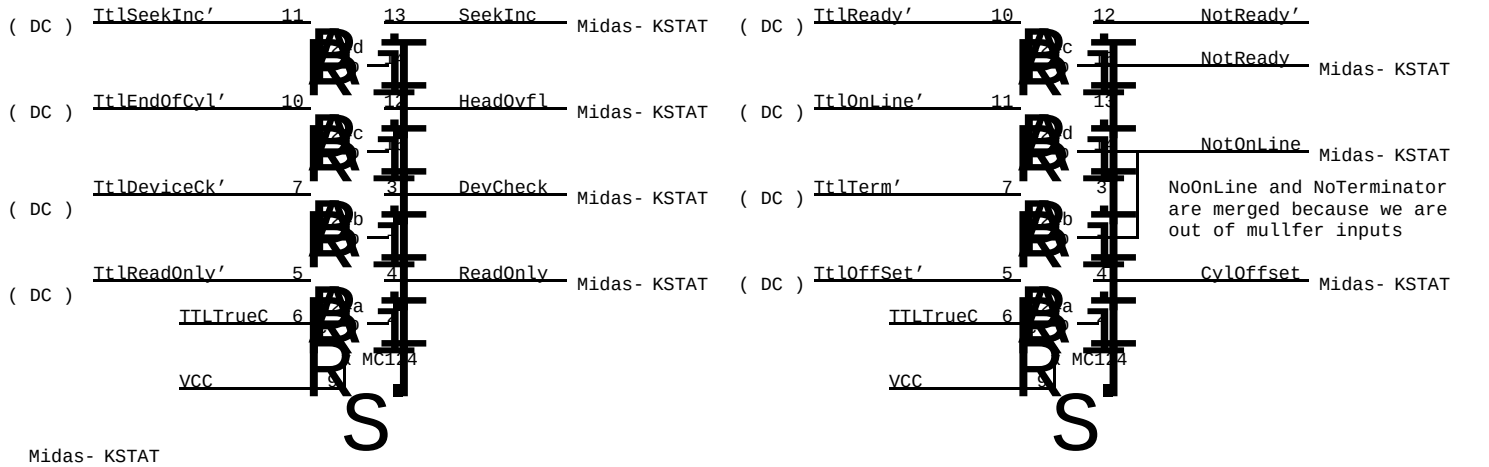


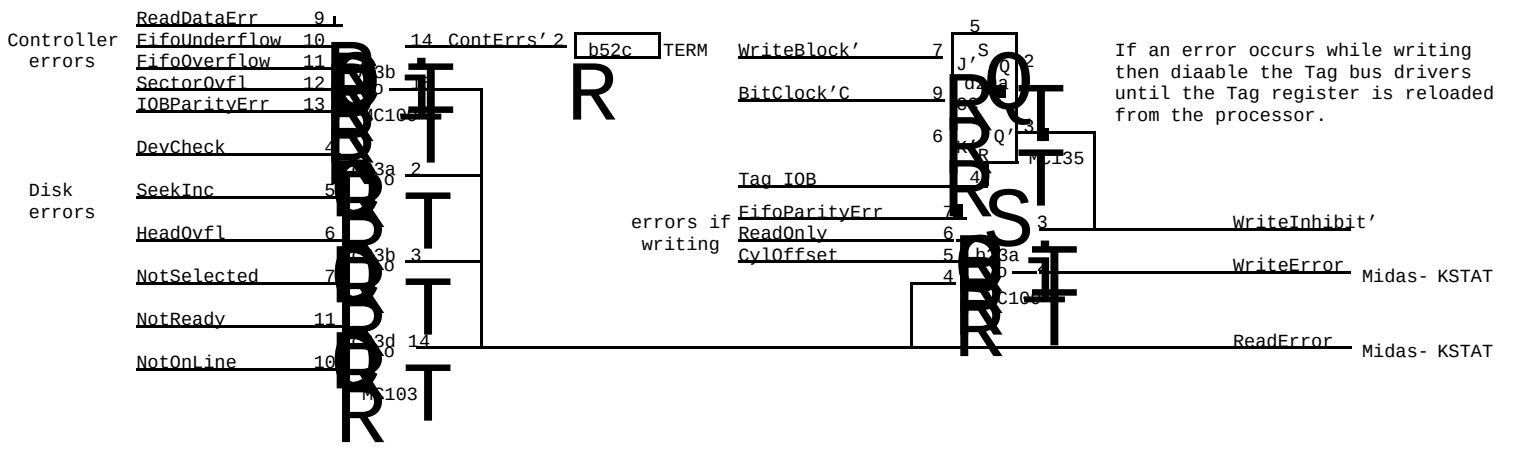
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Control RAM and Format Counter	TriconD03.sil	Roger Bates	Cf	9/24/79	09



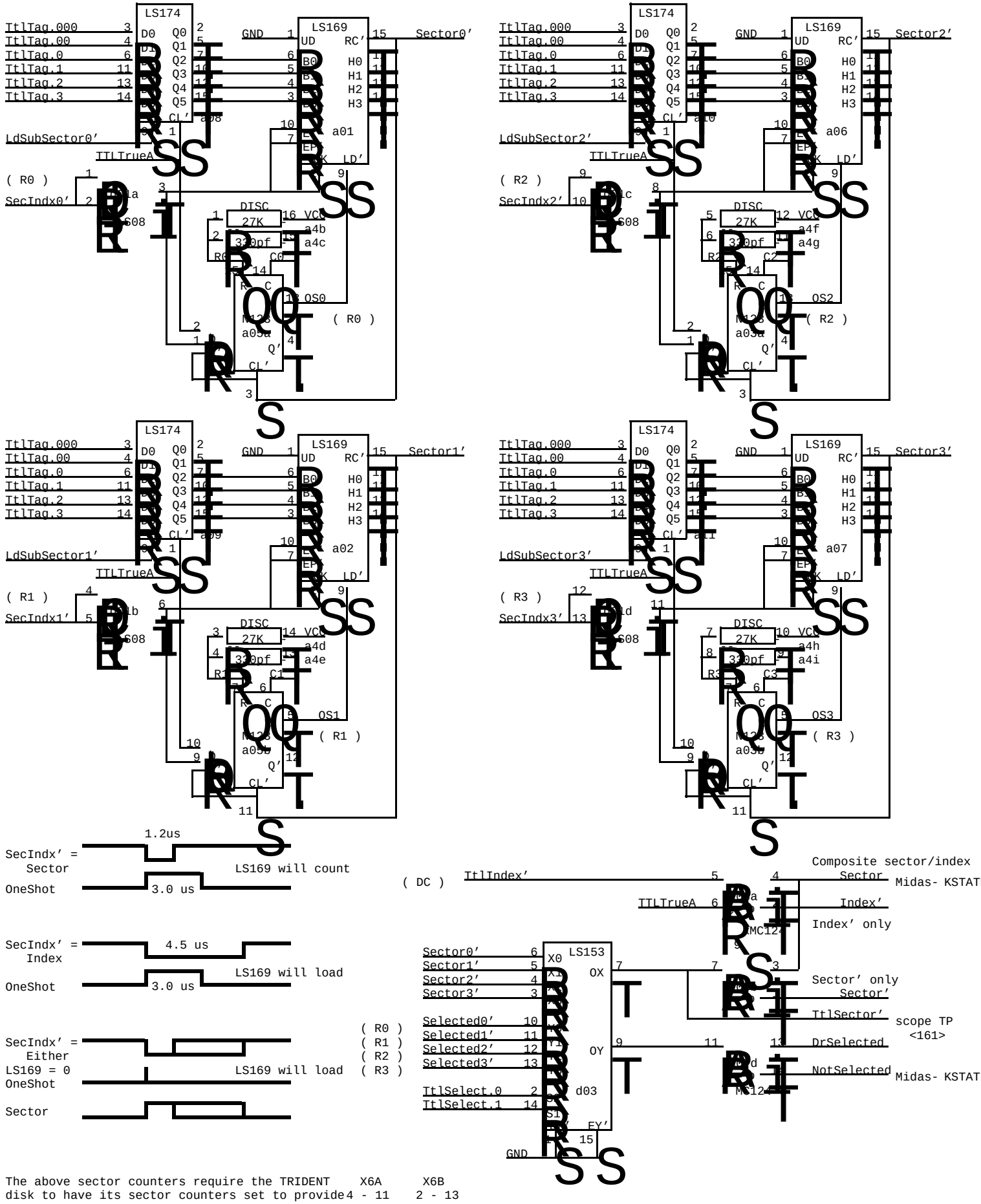
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	TAG register & Bus Drivers	TriconD04.sil	Roger Bates	Cf	7/23/79	10







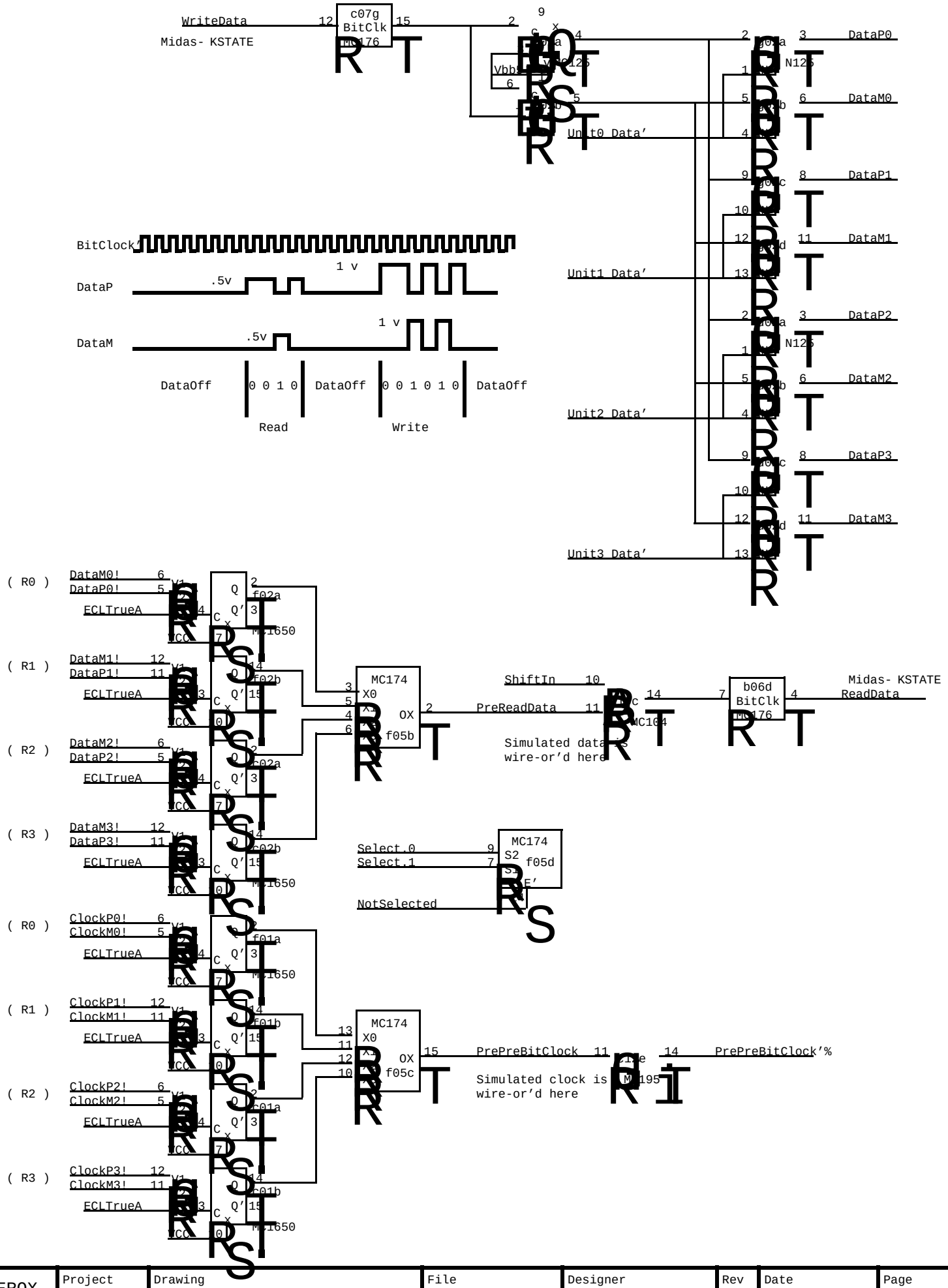
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Disk Drive Control	TriconD05.sil	Roger Bates	Cf	2/09/82	11



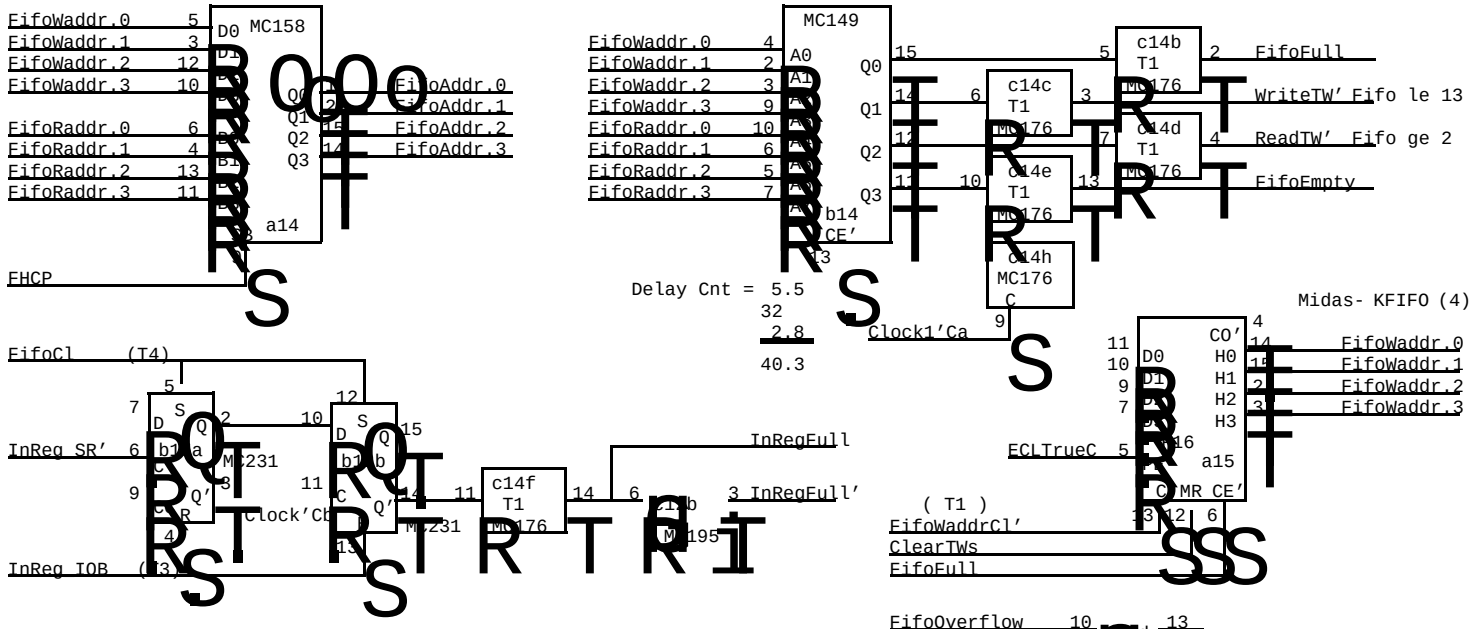
The above sector counters require the TRIDENT disk to have its sector counters set to provide 117 "sub-sector" pulses per revolution. This is done by setting the disk jumpers as follows:

X6A	X6B
4 - 11	2 - 13
5 - 10	3 - 12
	4 - 11
	5 - 10
	6 - 09

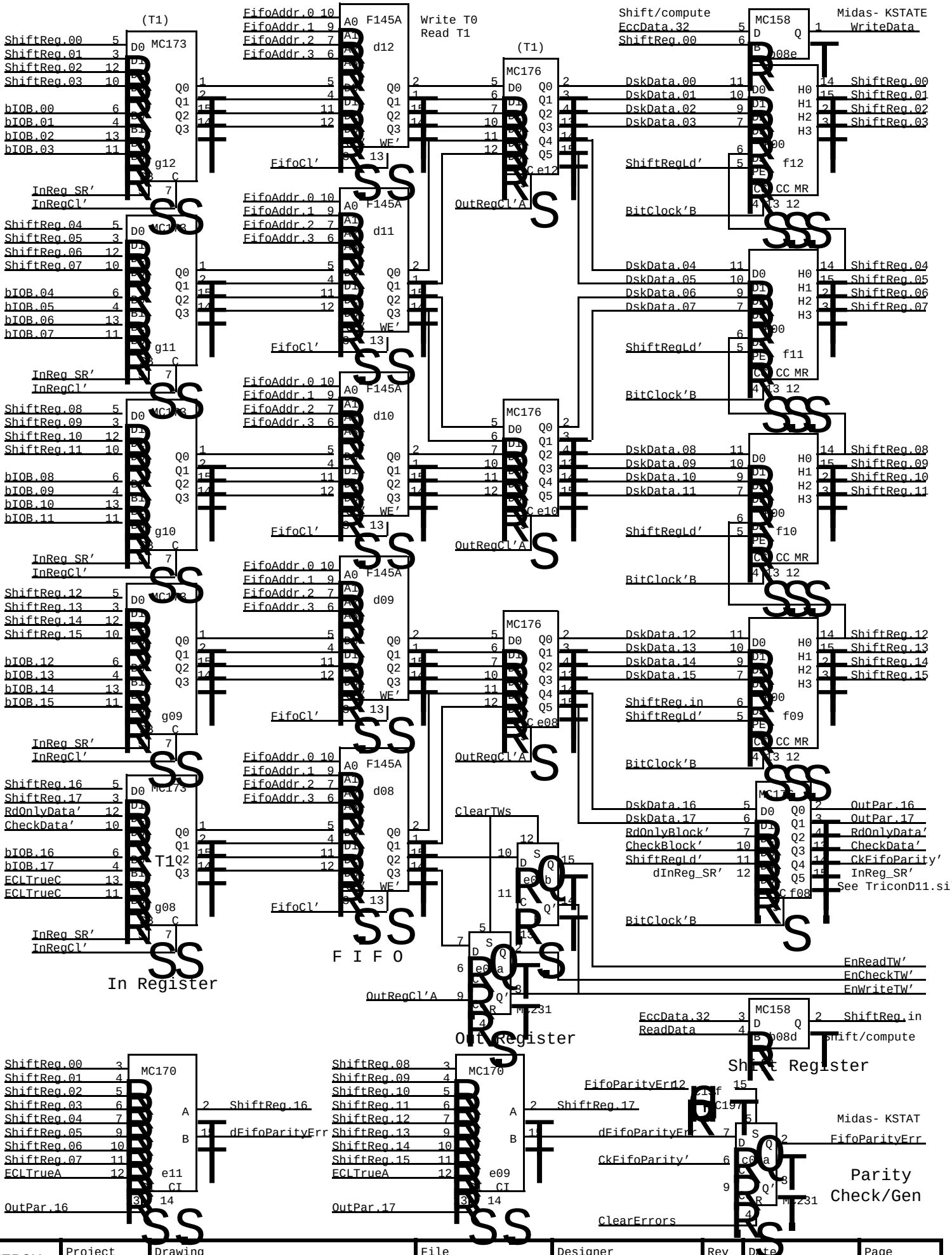
XEROX PARC	Project: Dorado	Drawing: Sector Length Counters	File: TriconD06.sil	Designer: Roger Bates	Rev: Cf	Date: 7/24/79	Page: 12



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clock and Data Input	TriconD07.sil	Roger Bates	Cf	7/23/79	13

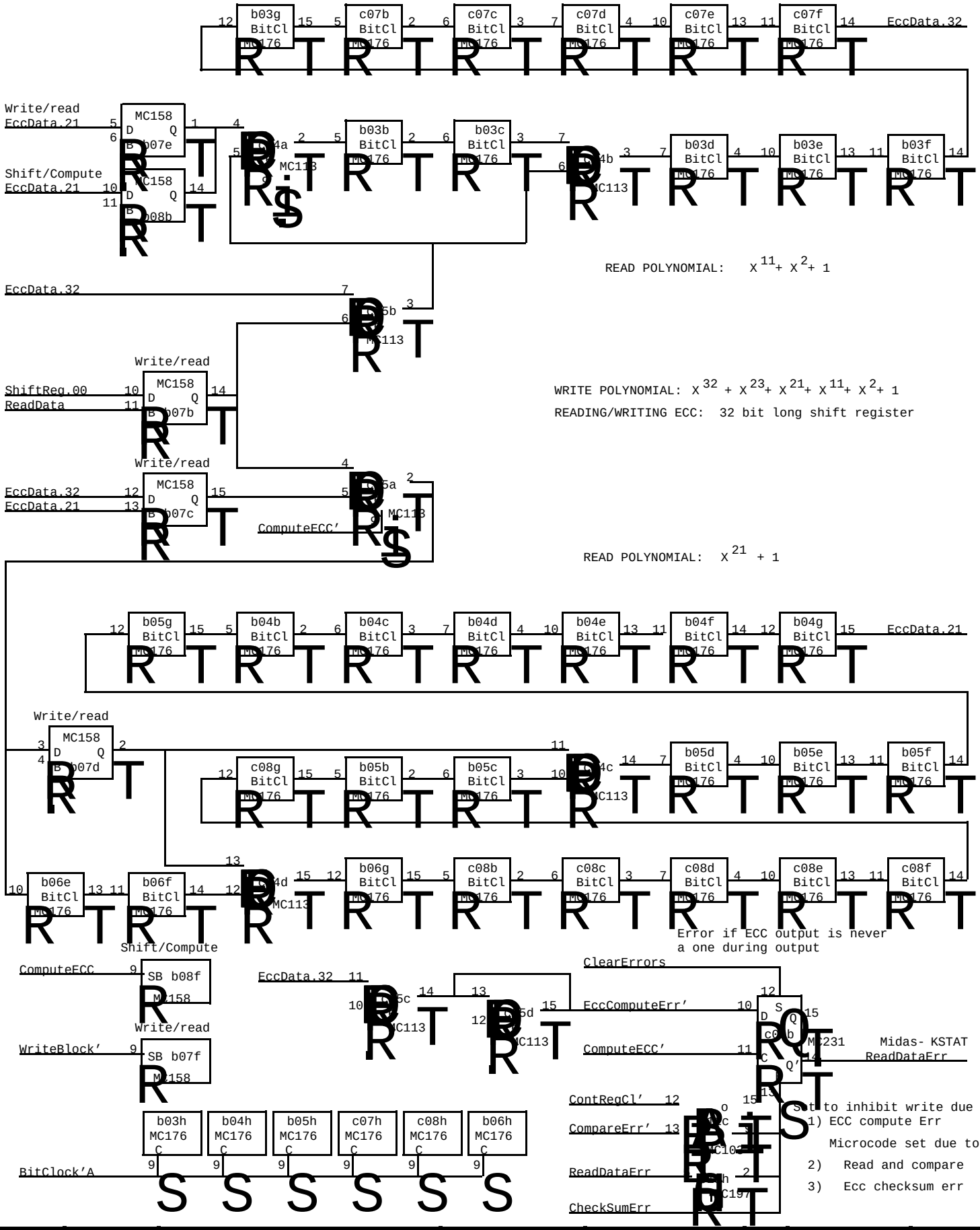


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	F I F O Control	TriconD08.sil	Roger Bates	Cf	9/24/79	14

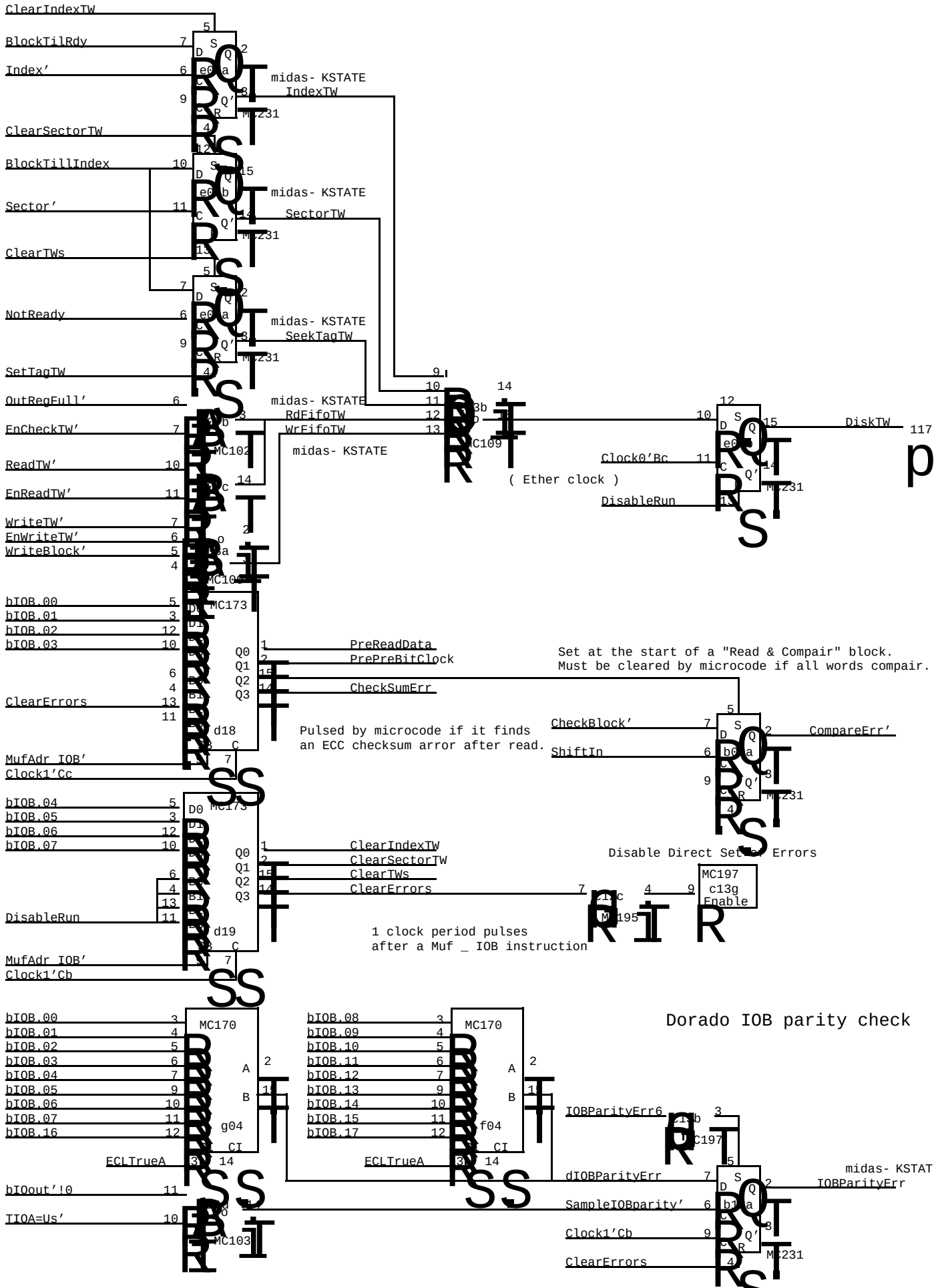


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	F I F O and Shift Register	TriconD09.sil	Roger Bates	Cf	7/08/79	15

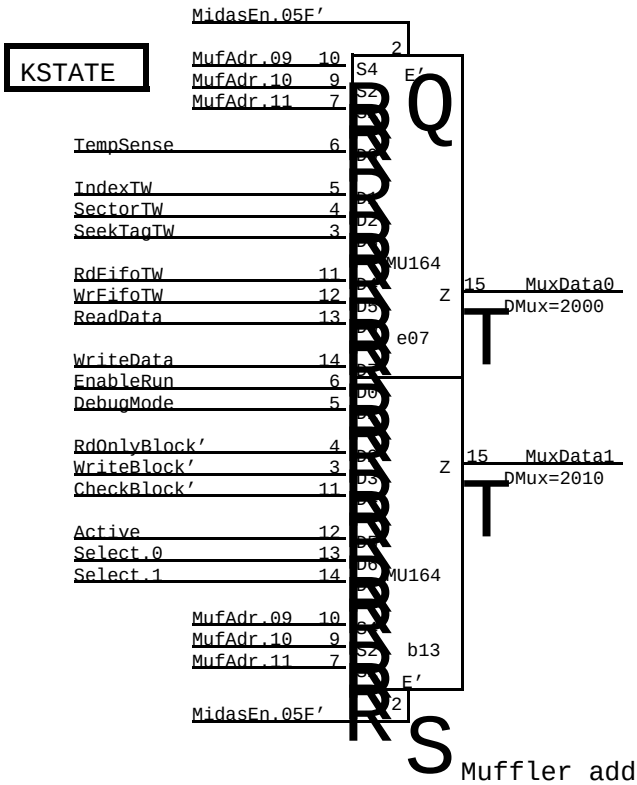
POLYNOMIAL DIVIDER FOR FIRE CODE GENERATION

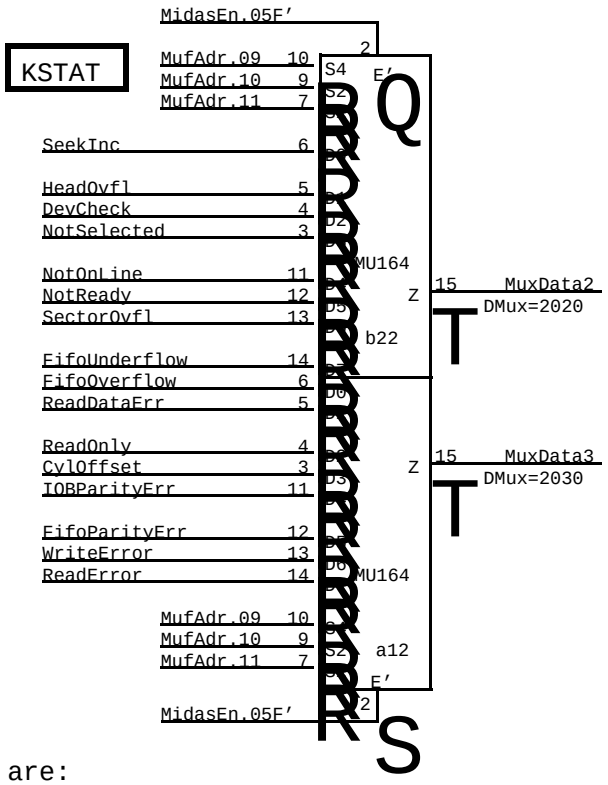


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Fire Code Generator	TriconD10.sil	Roger Bates	Cf	7/08/79	16



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Buss Parity Task Wake-Up	TriconD11.sil	Roger Bates	Cf	7/08/79	17

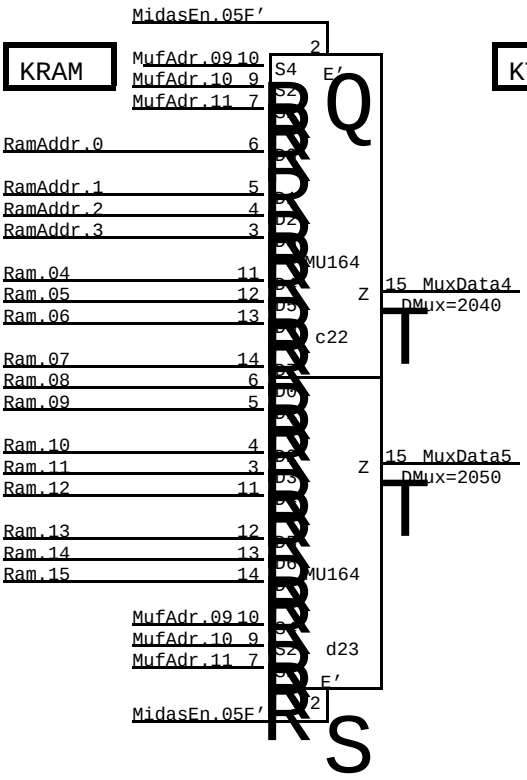


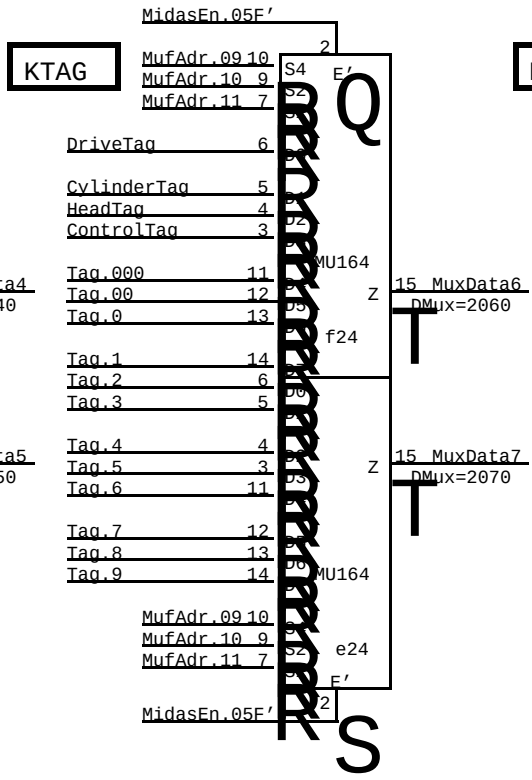


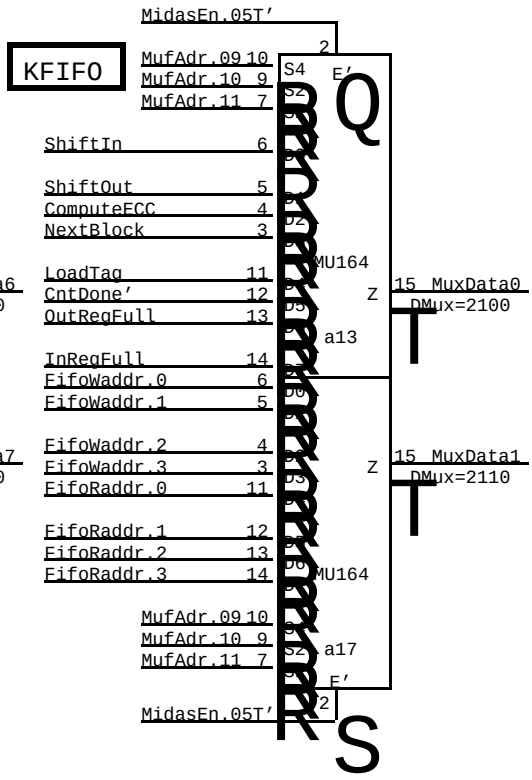
Muffler addresses are:

Value listed for Program input
Value plus 2000 for Midas input

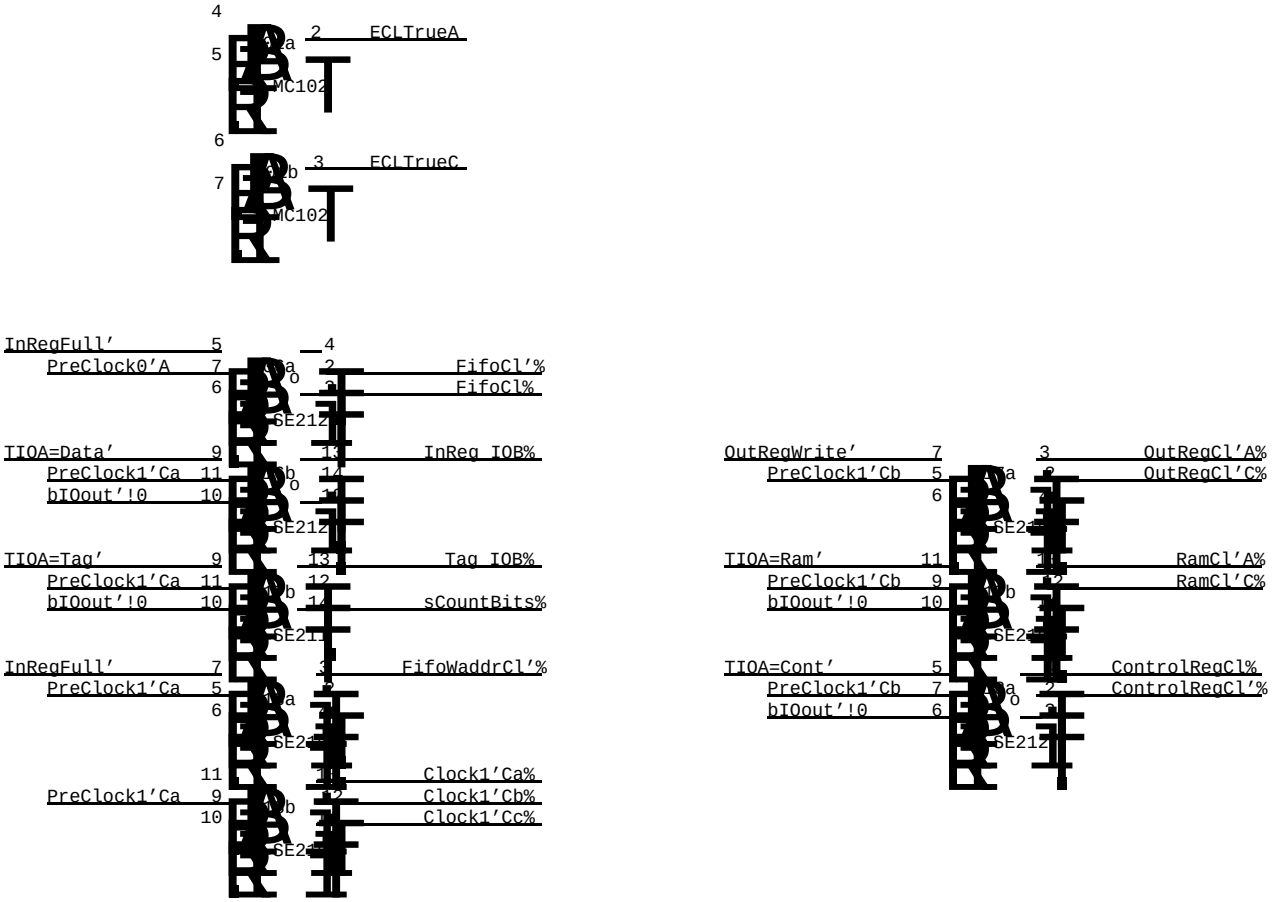
Values from 120 to 177 are
used by the Ethernet





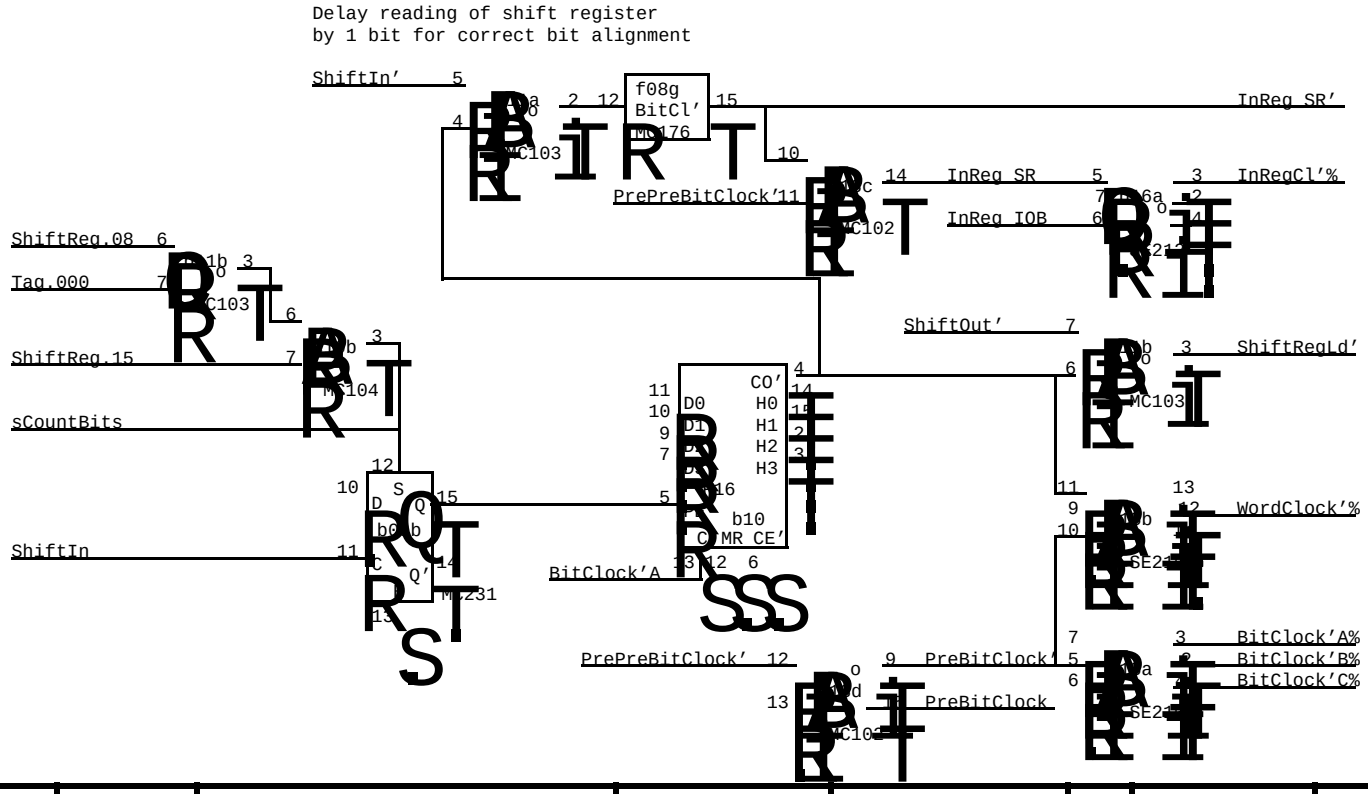


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	DMUX CONTROL	TriconD12.sil	Roger Bates	Cf	7/08/79	18

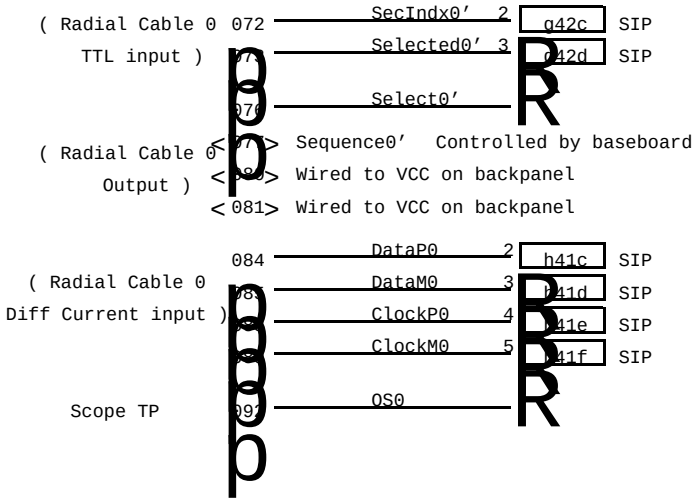


System Clocks

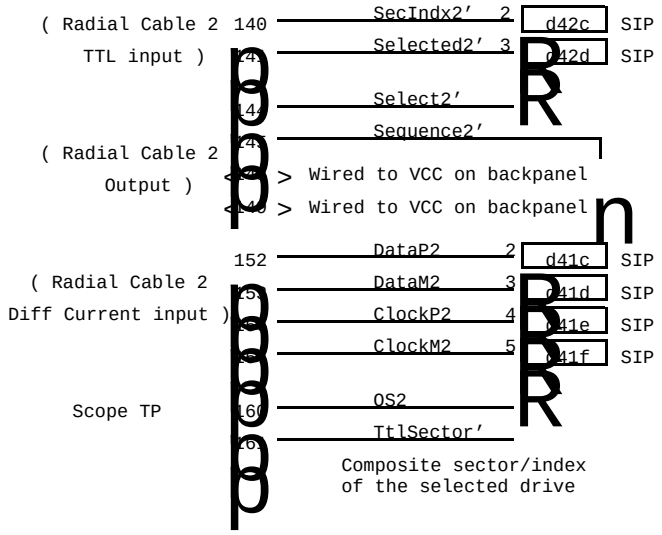
Disk Clocks



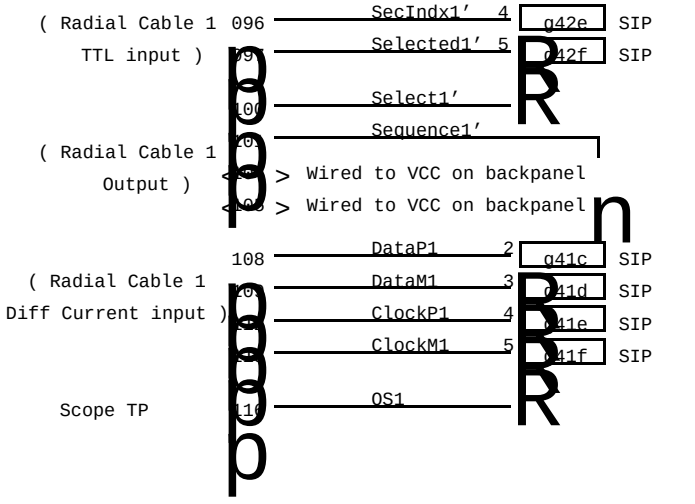
Radial Cable for Drive 0



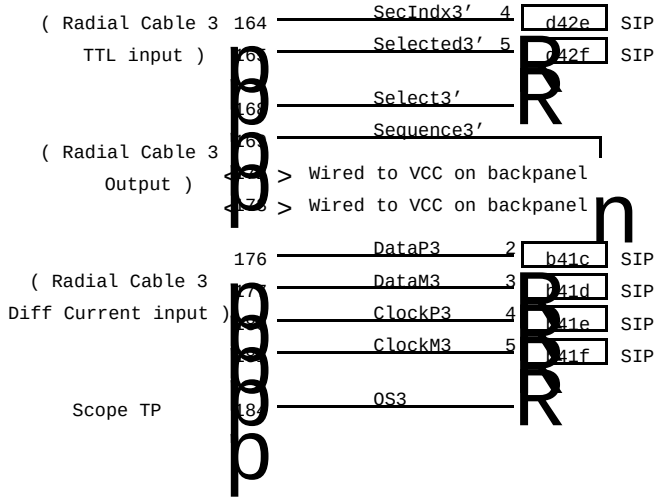
Radial Cable for Drive 2



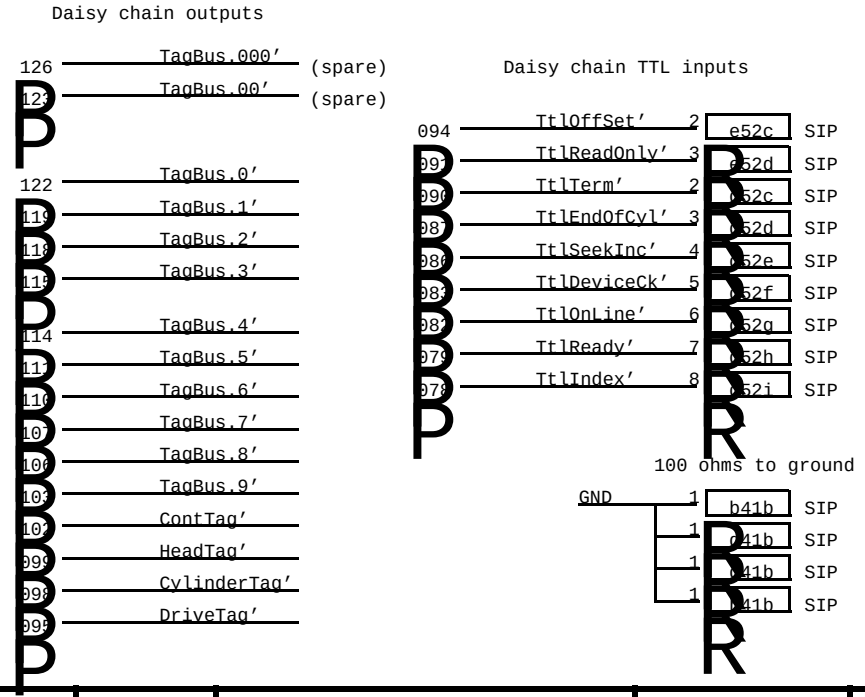
Radial Cable for Drive 1



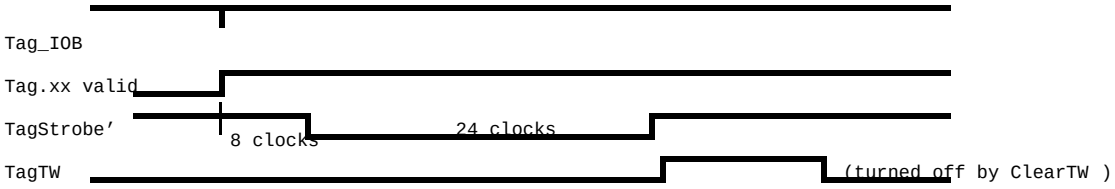
Radial Cable for Drive 3



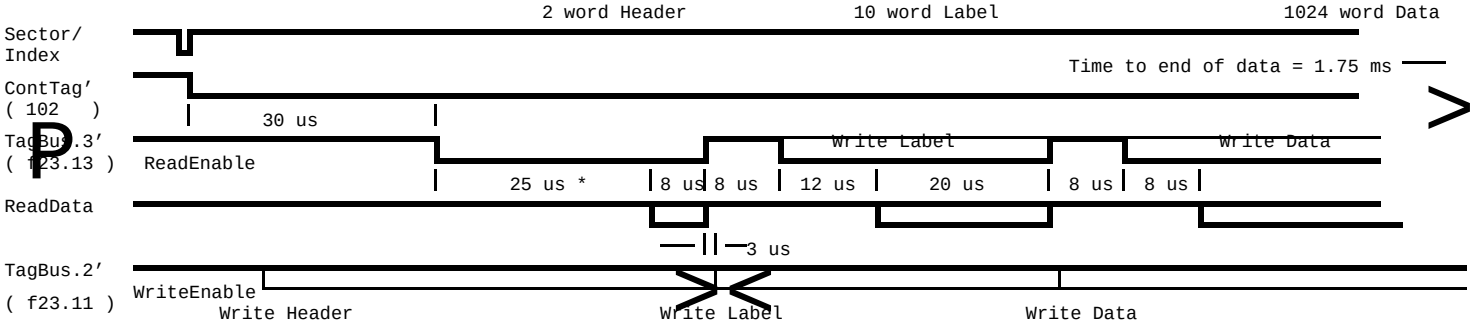
Daisy Chain Cable



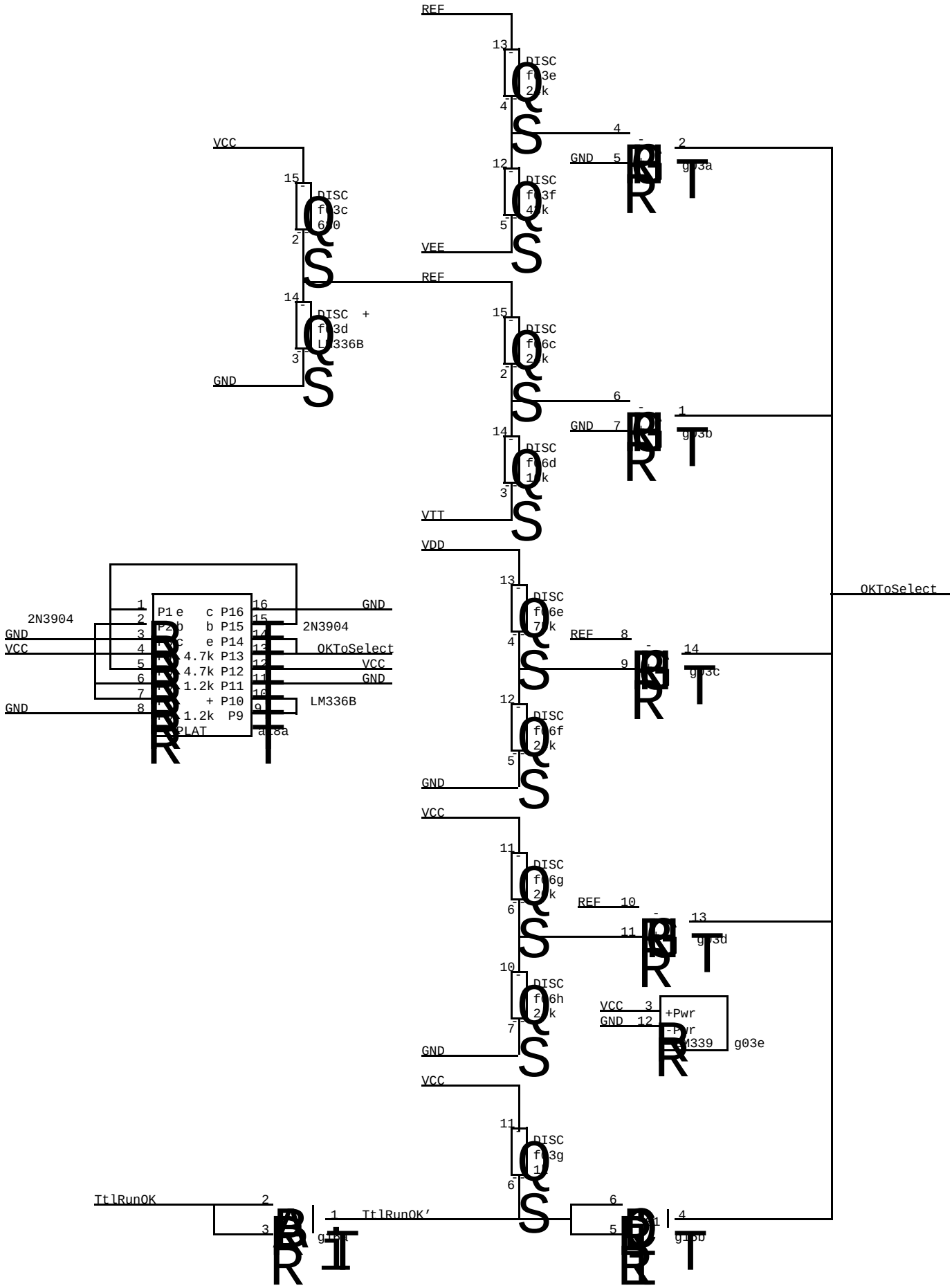
Head or Cylinder Tag Instruction



Read or Write Instruction



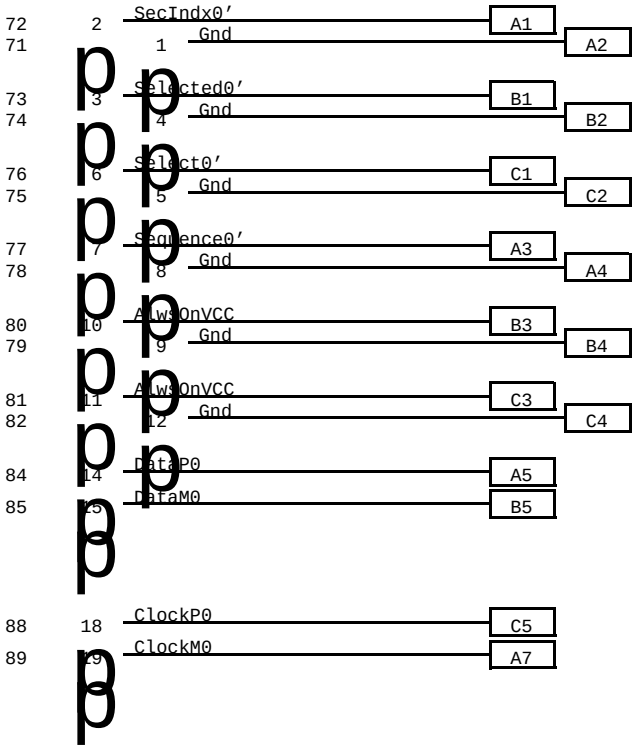
* This value if for reading a pack on the same drive that Headers were written
It may vary by +/- 15 us on other drives



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Disk Power Loss Portect	TriconD15a.sil	Tim Diebert	Cf	2/09/82	22a

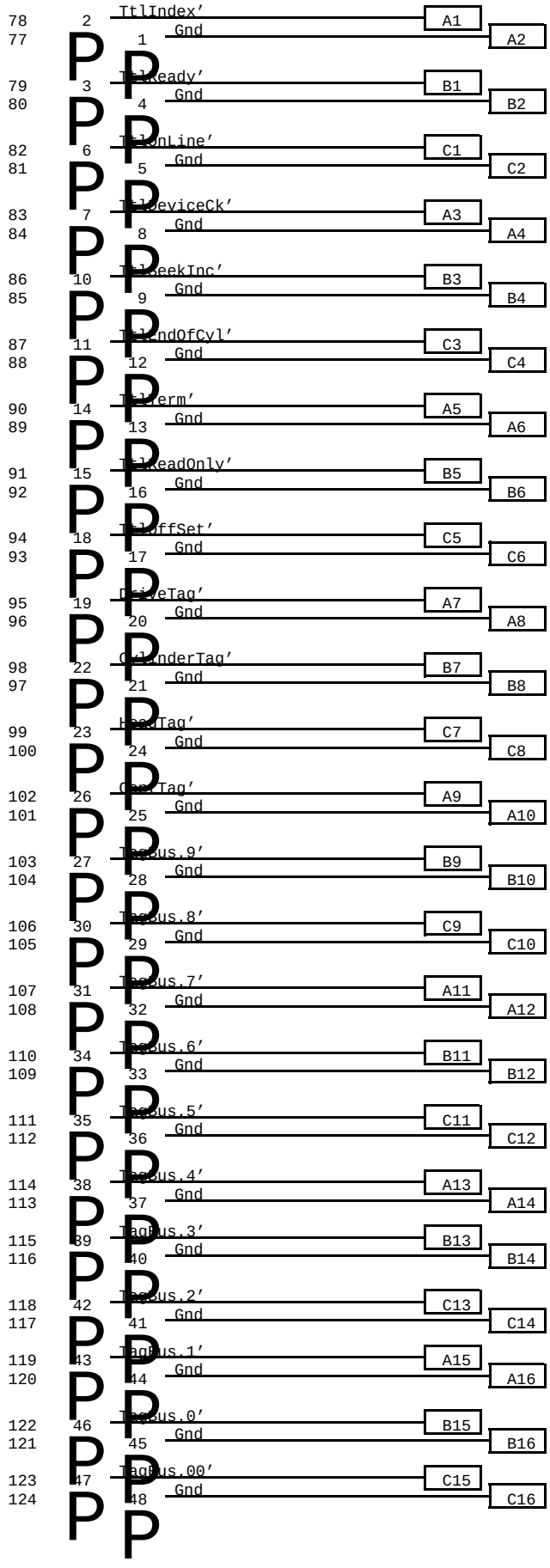
Radial Cable for Drive 0

AMP 204729-1



DAISEY CHAIN CABLE

AMP 204733-1

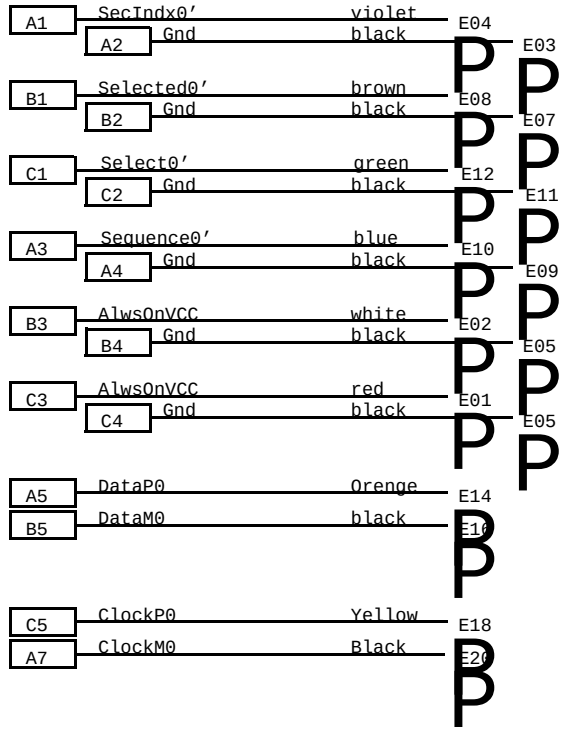


XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Internal Cables	TriconD16.sil	Roger Bates	Cf	7/08/79	23a

Radial Cable for Drive 0

Cal-Comp

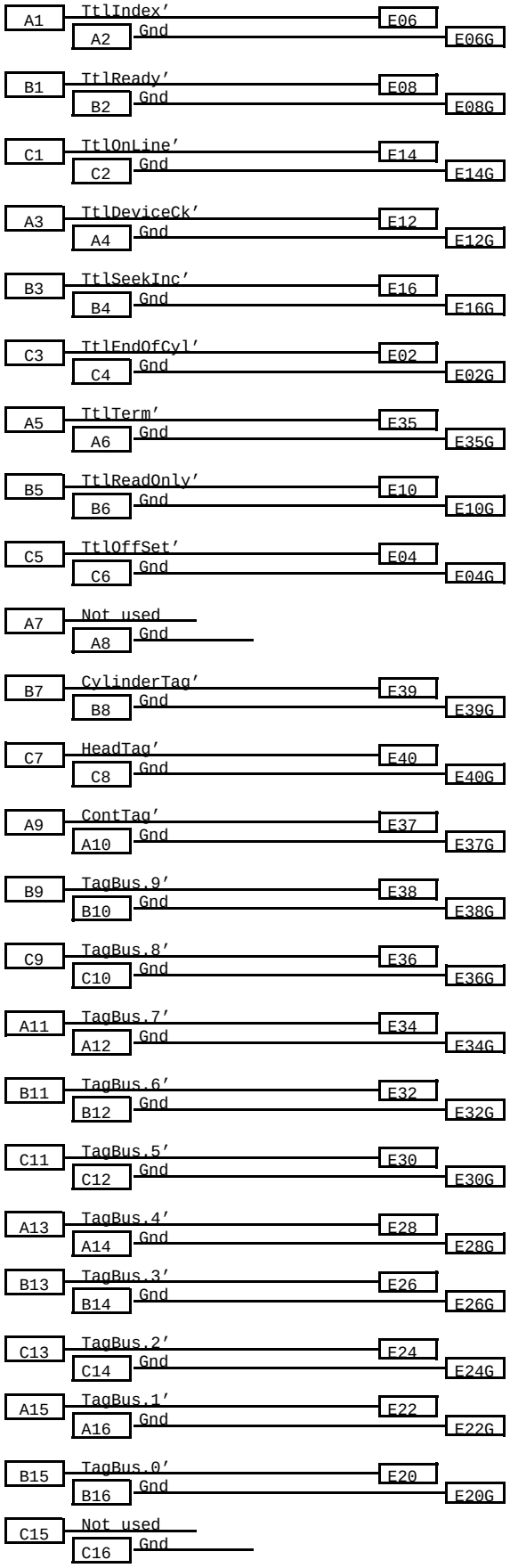
AMP 204742-1 Assembly 12433



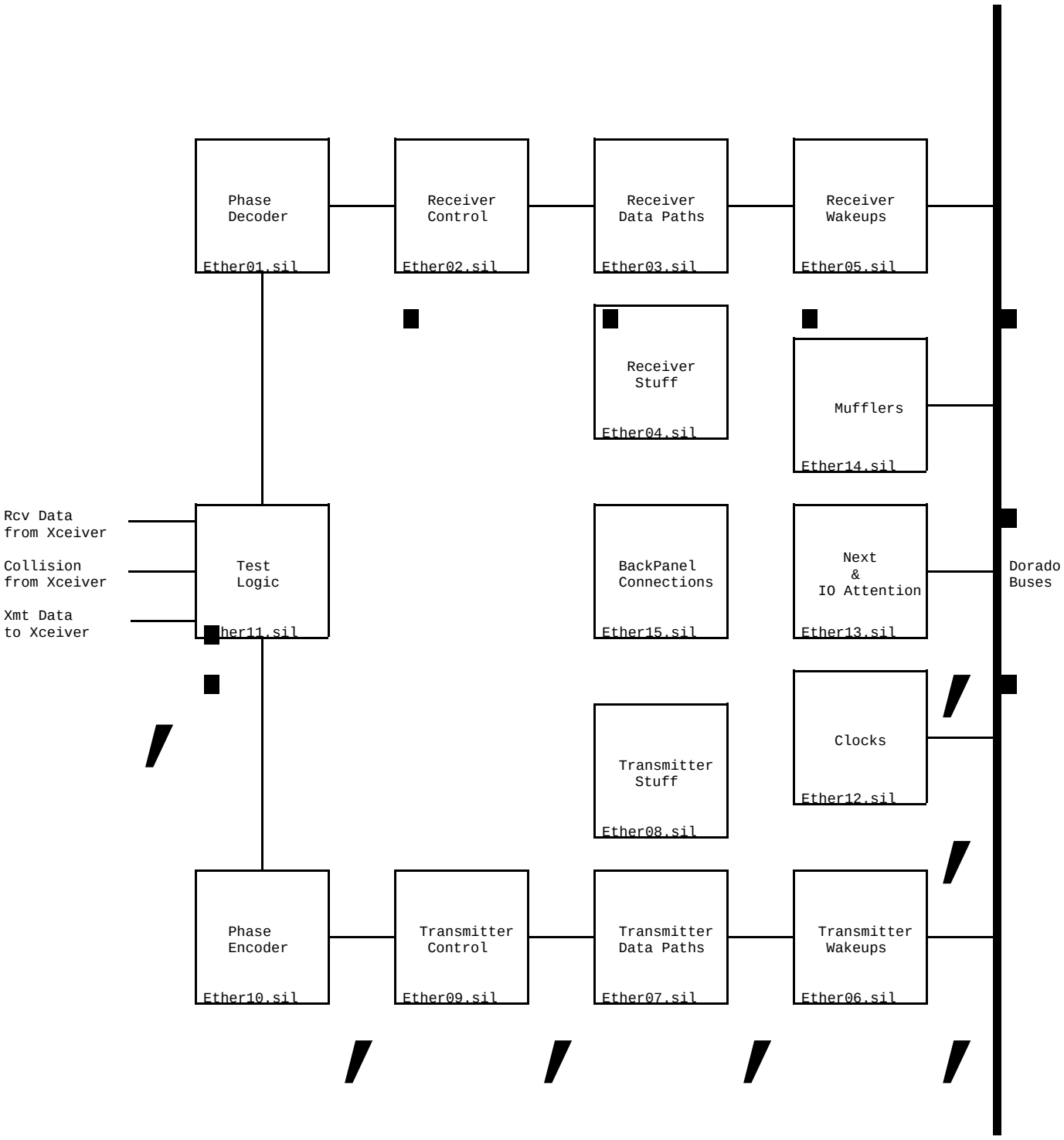
DAISEY CHAIN CABLE

AMP 204746-1 Cal-Comp

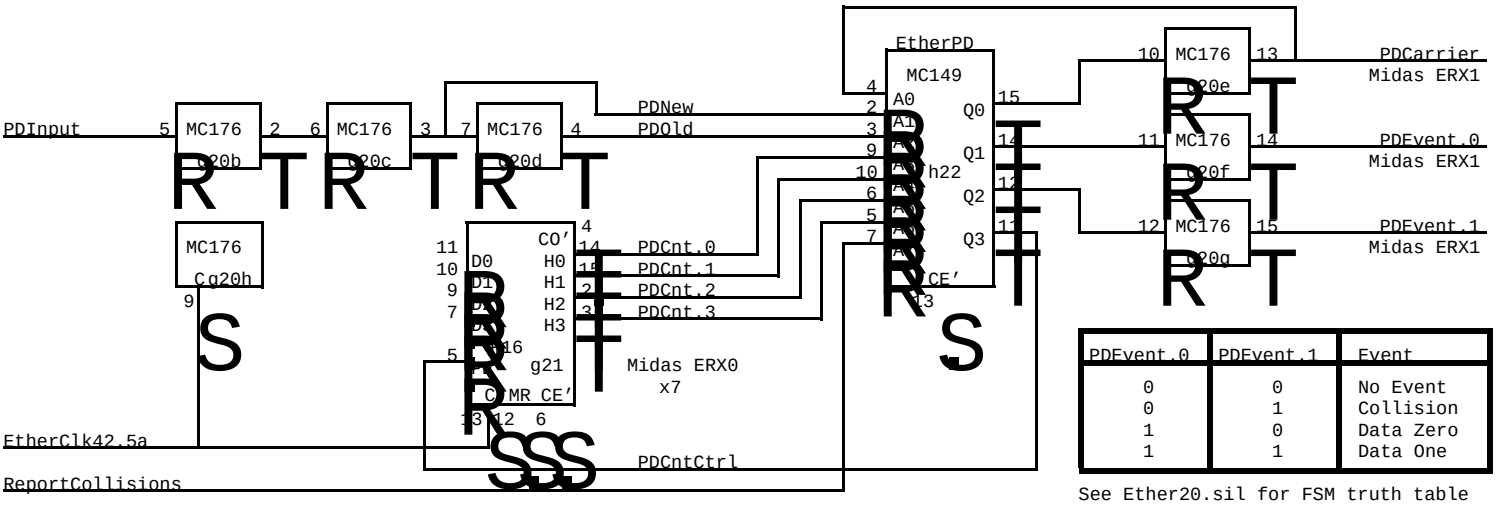
Assembly 12424



XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Dorado to Trident Cables	TriconD17.sil	Roger Bates	Cf	7/08/79	23b



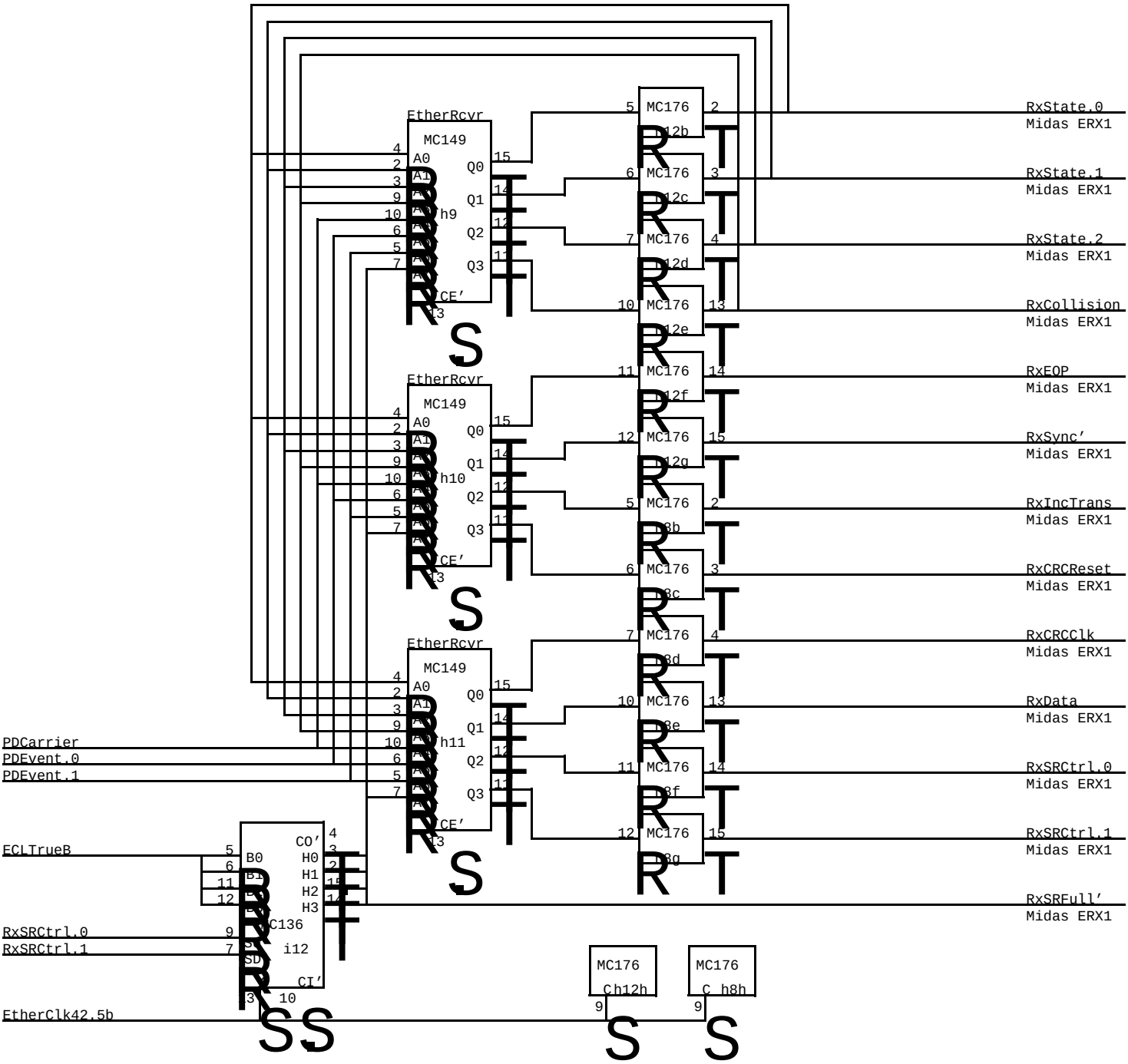
See DskEth*.sil for IOA, IOB, Muffler Control and Board Clocks



PDEvent.0	PDEvent.1	Event
0	0	No Event
0	1	Collision
1	0	Data Zero
1	1	Data One

See Ether20.sil for FSM truth table

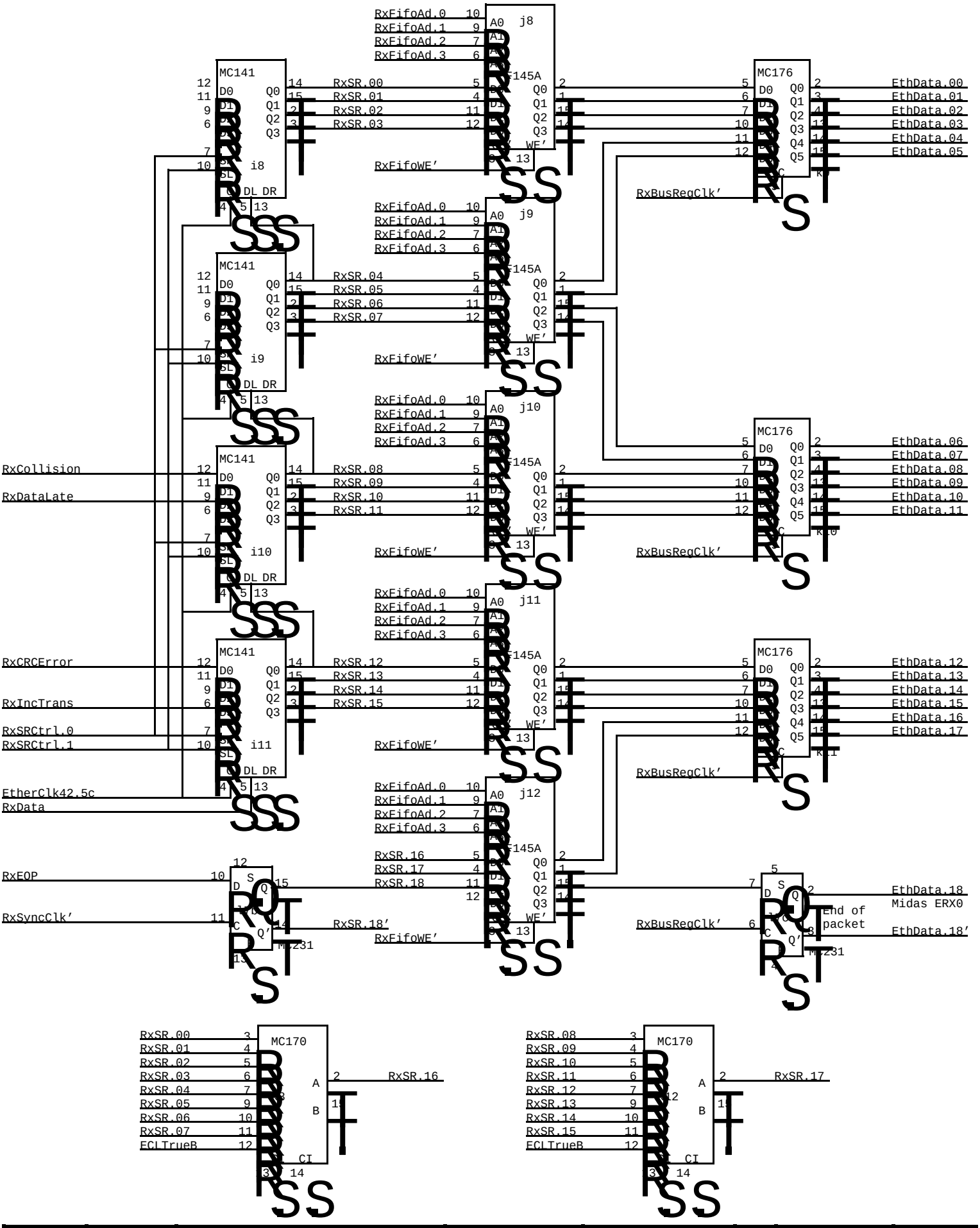
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Phase Decoder	Ether01.sil	David Boggs	Cf	7/08/79	25



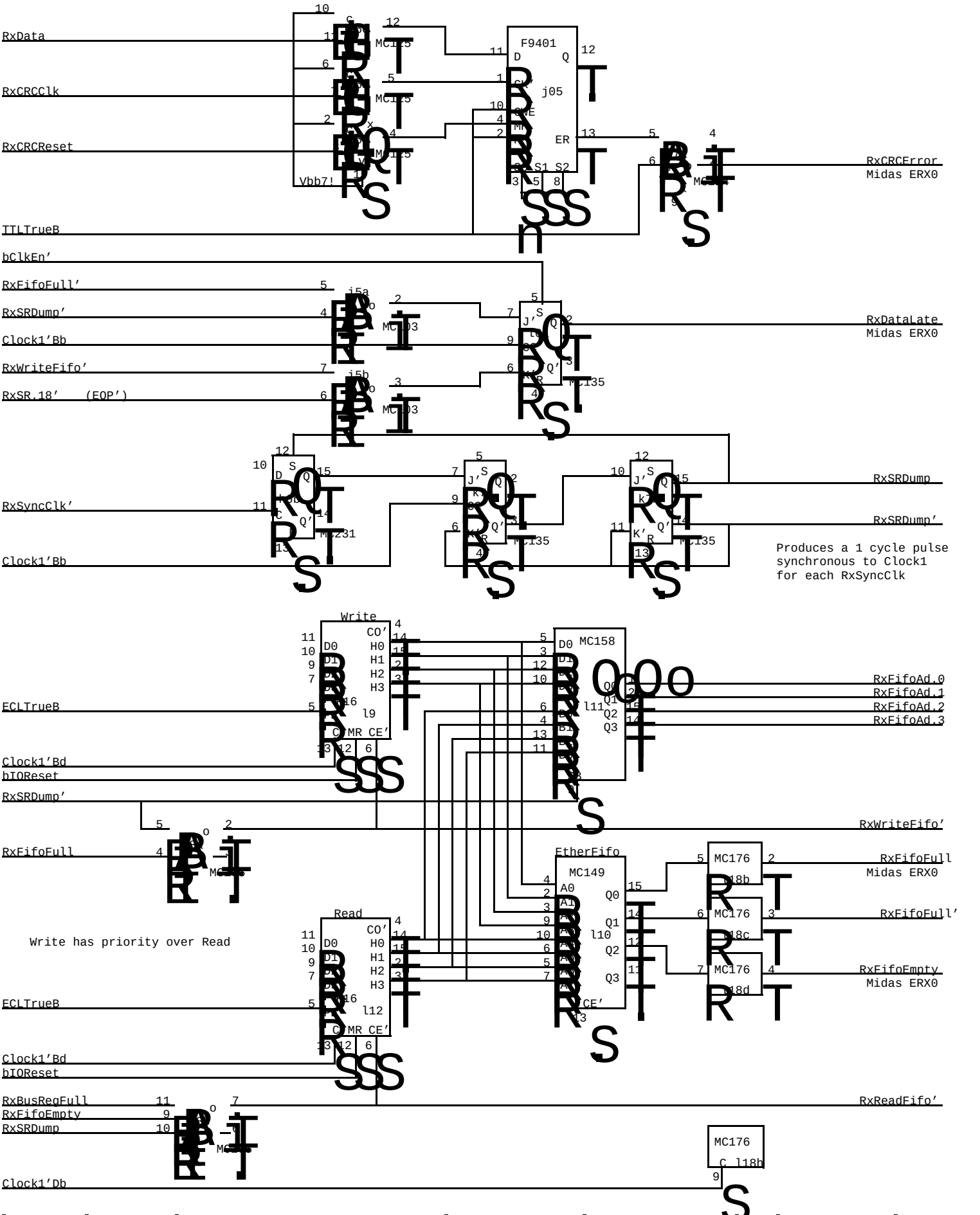
See Ether18.sil for timing diagrams

The slowest Dorado clock speed at which the receiver works is 85 ns (T0 to T1)

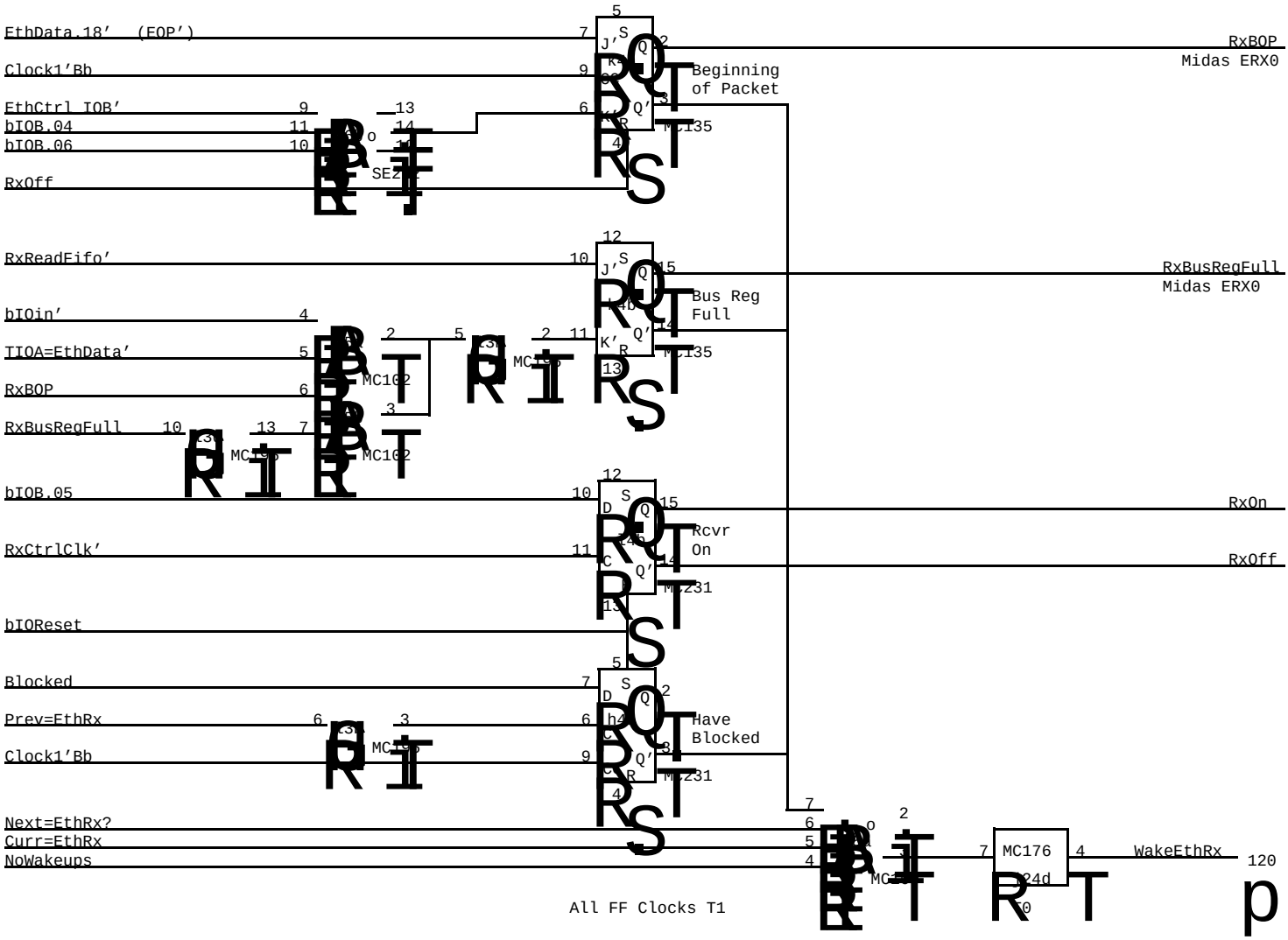
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Receiver Control	Ether02.sil	David Boggs	Cf	9/24/79	26



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Receiver Data Paths	Ether03.sil	David Boggs	Cf	7/08/79	27

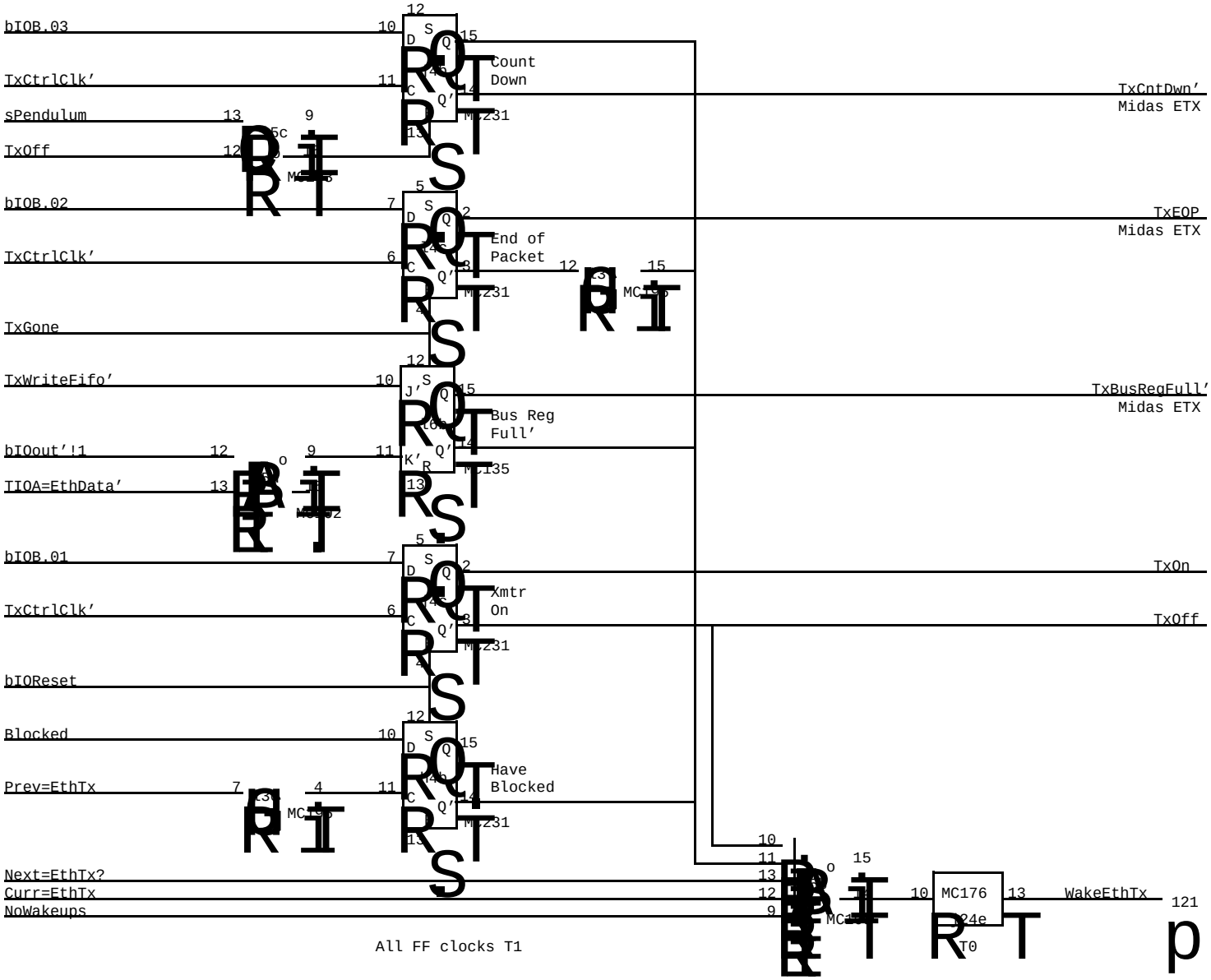


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Receiver Stuff	Ether04.sil	David Boggs	Cf	7/08/79	28



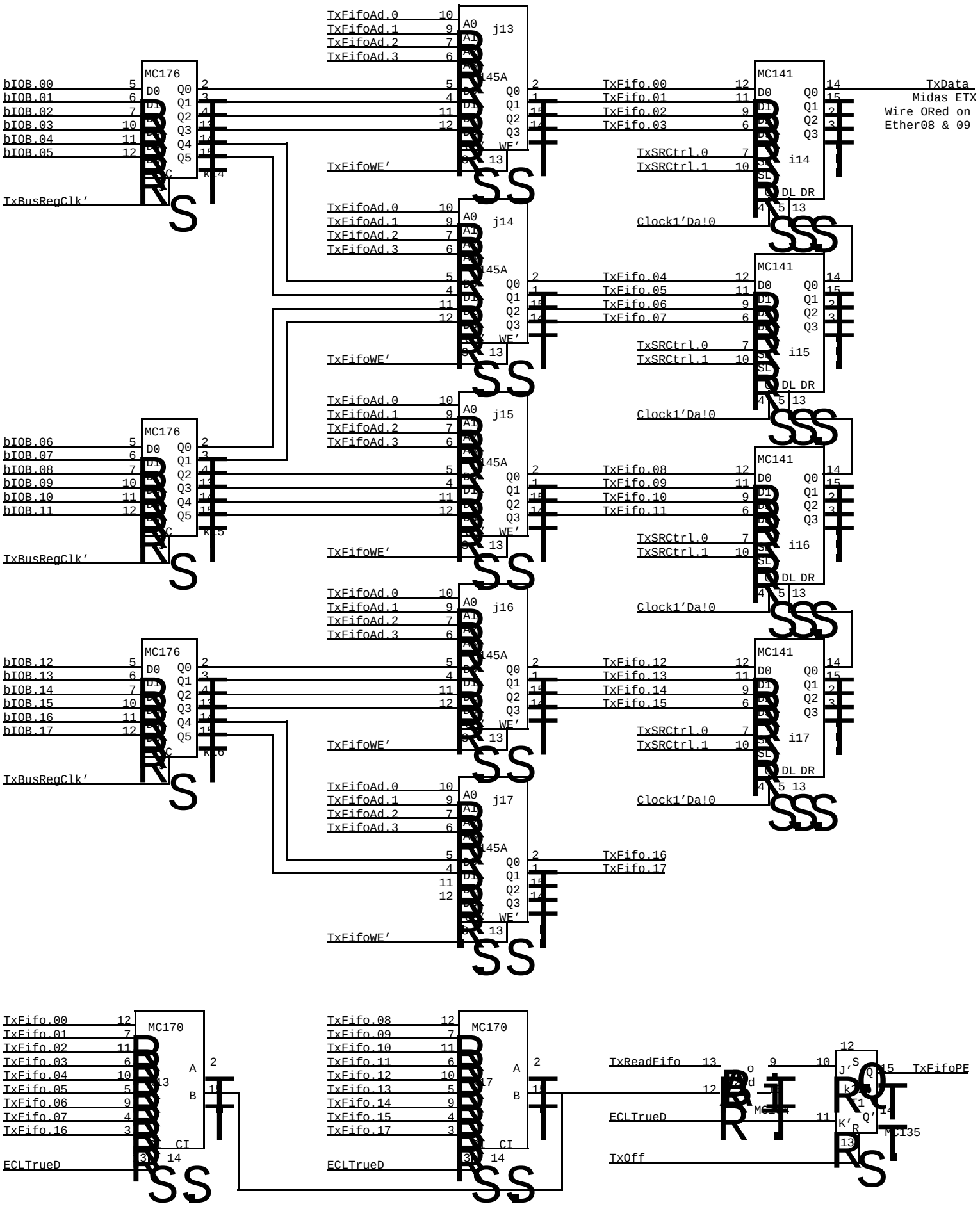
See Ether21 & 22.sil for wakeup timing diagrams

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Receiver Wakeups	Ether05.sil	David Boggs	Cf	7/08/79	29

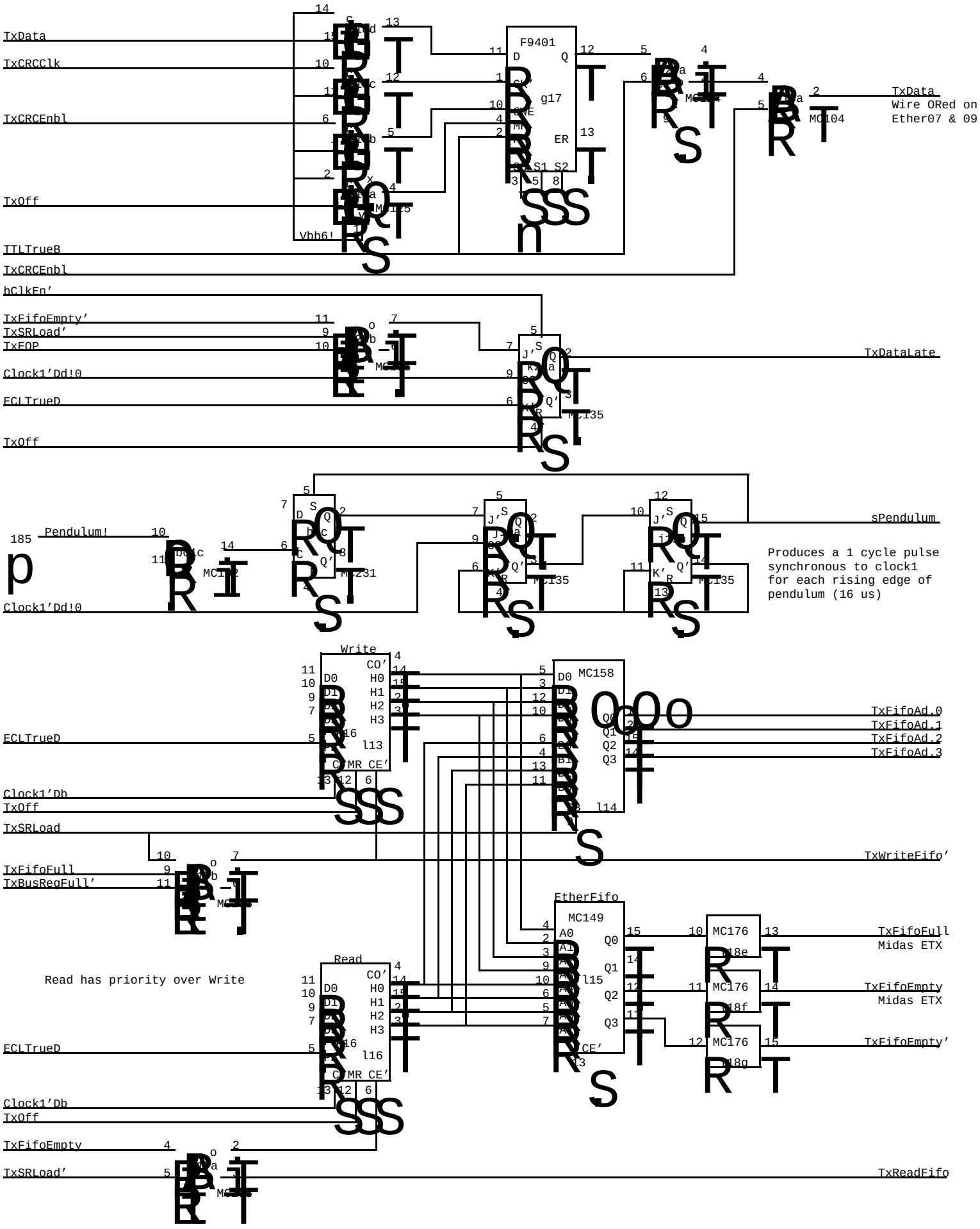


See Ether21 & 22.sil for wakeup timing diagrams

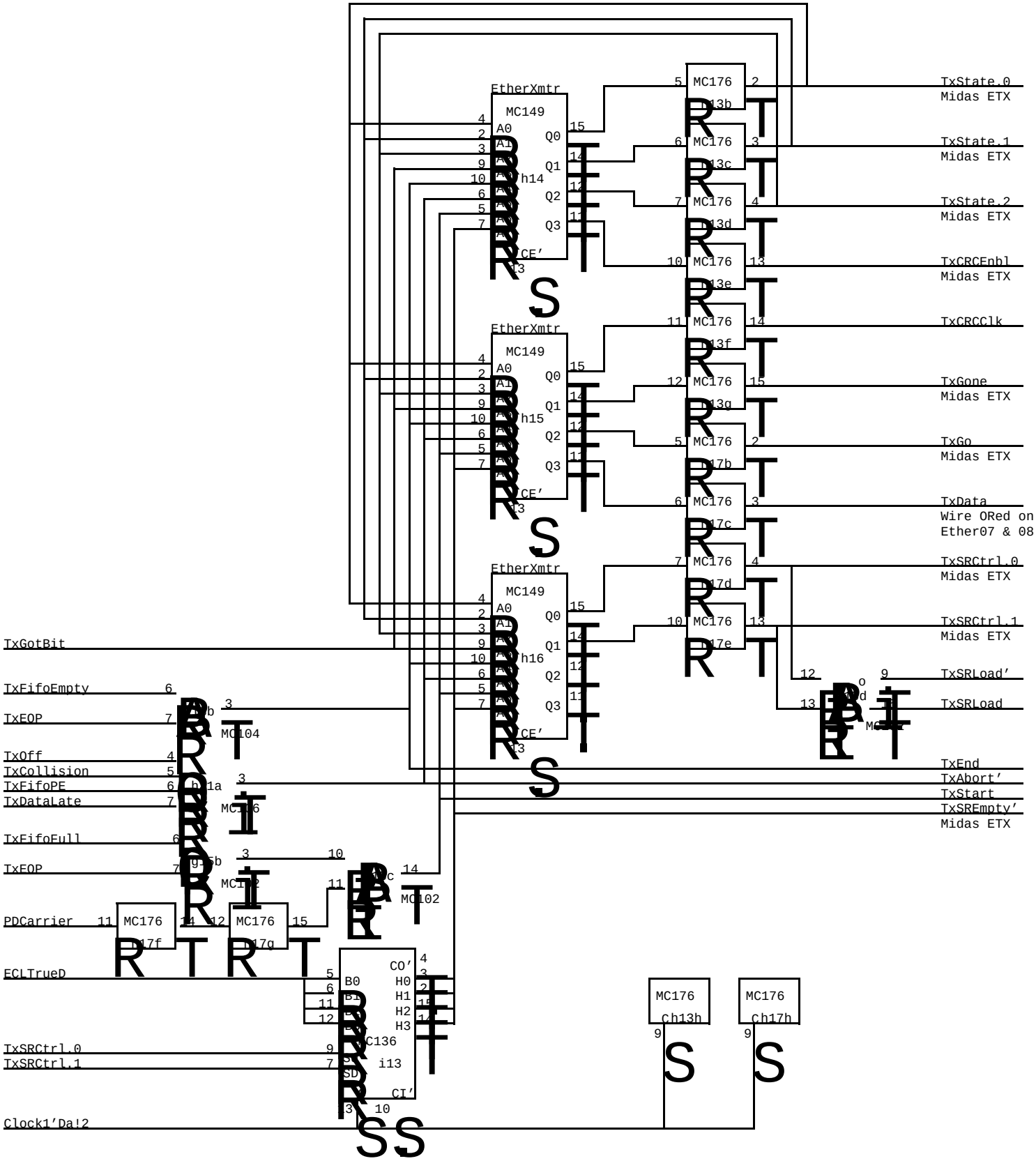
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Transmitter Wakeups	Ether06.sil	David Boggs	Cf	7/08/79	30



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Transmitter Data Paths	Ether07.sil	David Boggs	Cf	7/08/79	31

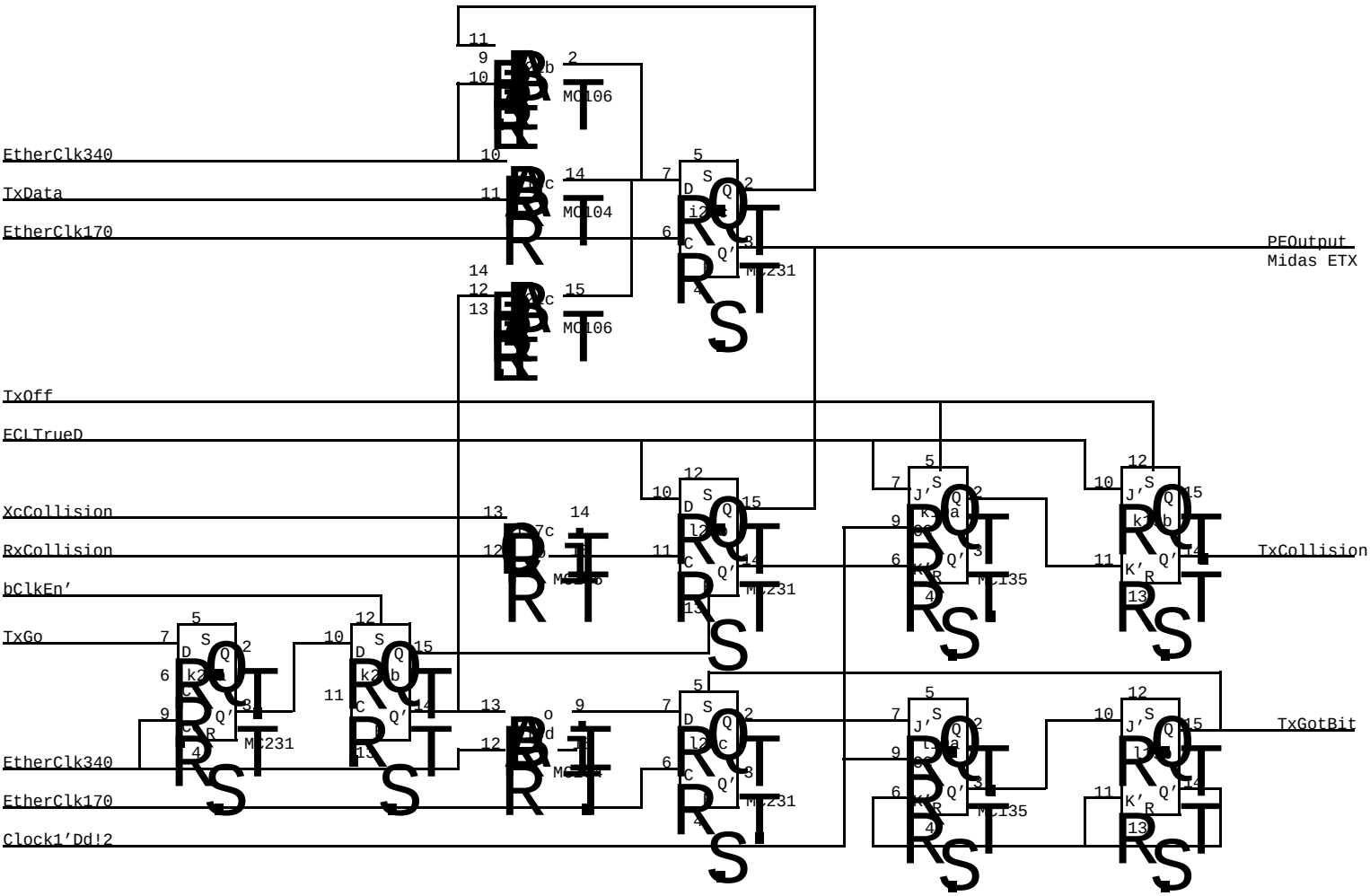


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Transmitter Stuff	Ether08.sil	David Boggs	Cf	7/08/79	32



See Ether17.sil for timing diagrams

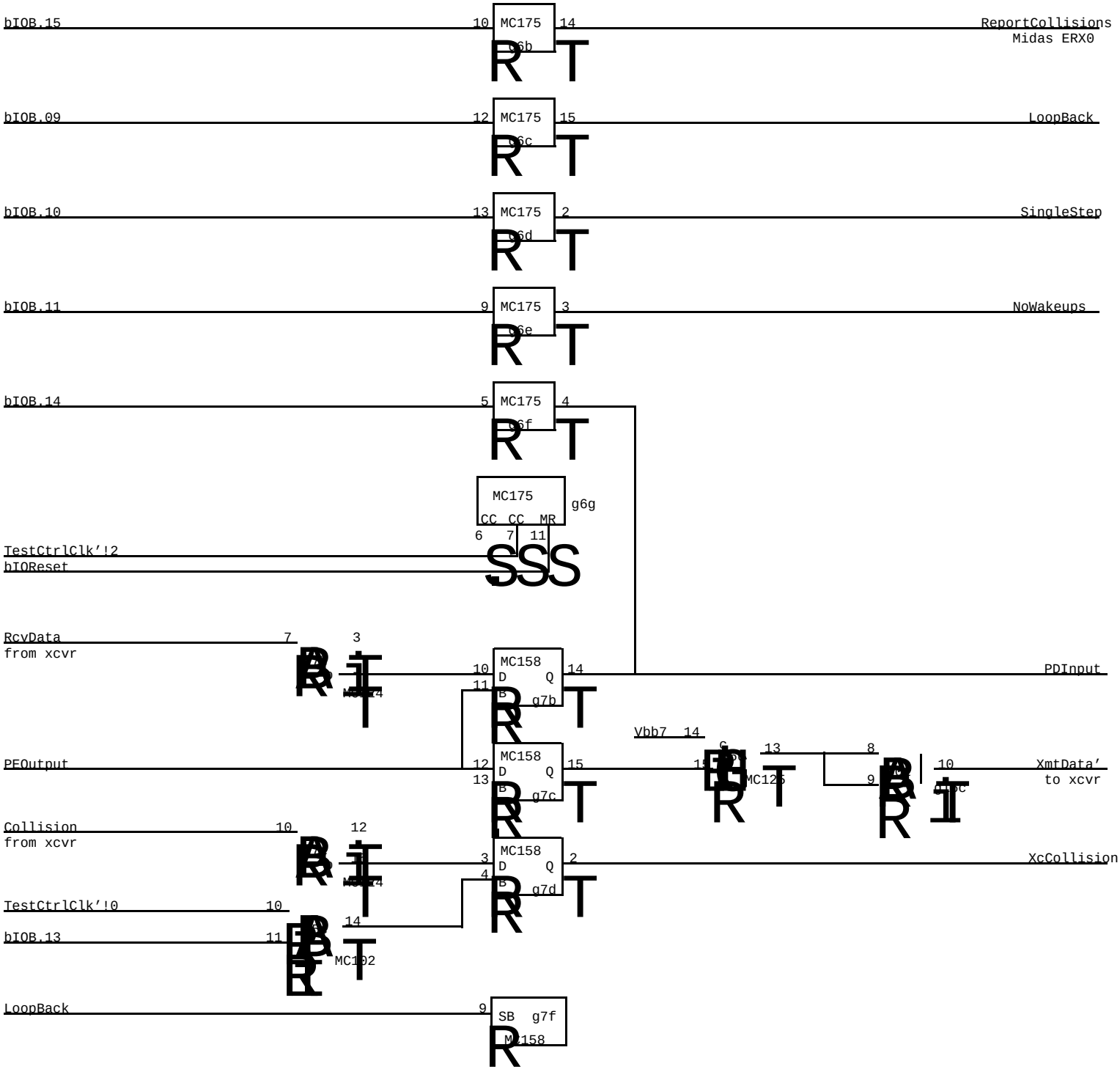
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Transmitter Control	Ether09.sil	David Boggs	Cf	9/24/79	33



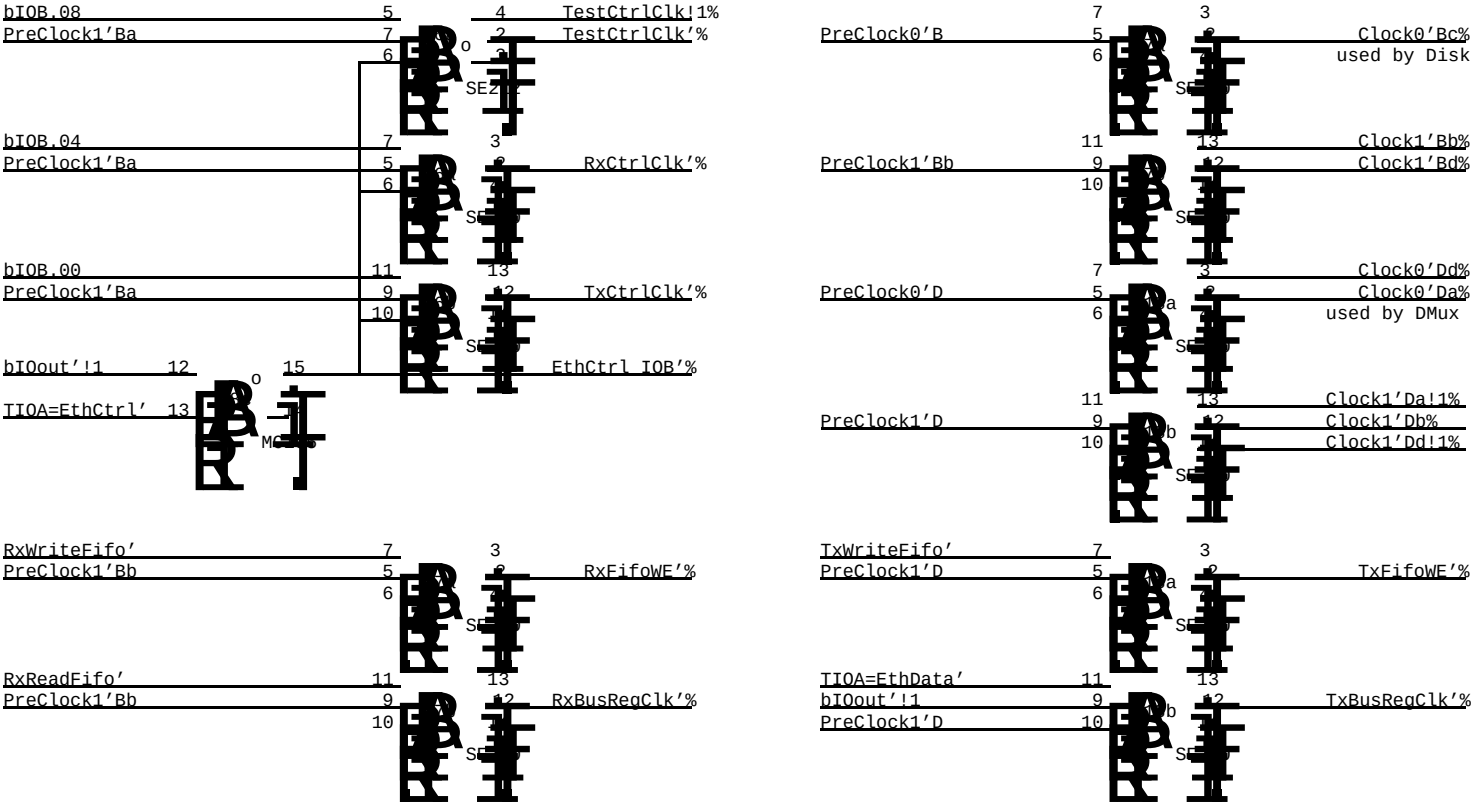
See Ether19.sil for timing diagrams

The slowest Dorado clock speed at which the transmitter works is 42.5 ns (T0 to T1)

525 ns < length of jam < 915 ns

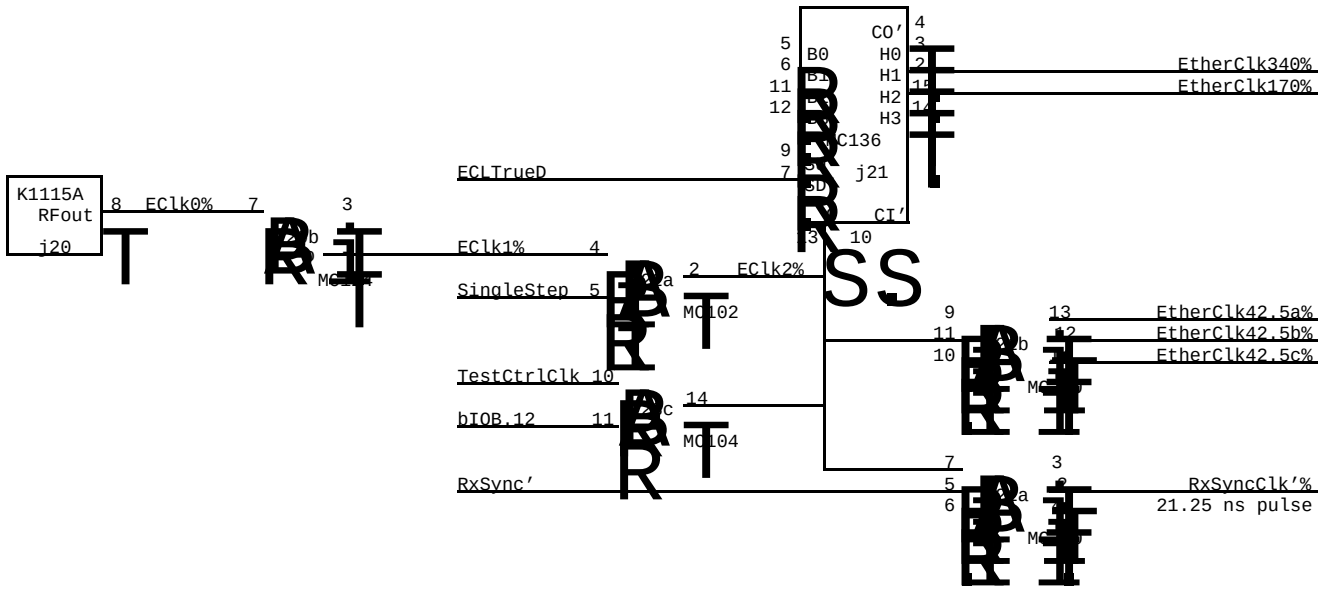


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Test Logic	Ether11.sil	David Boggs	Cf	2/09/82	35

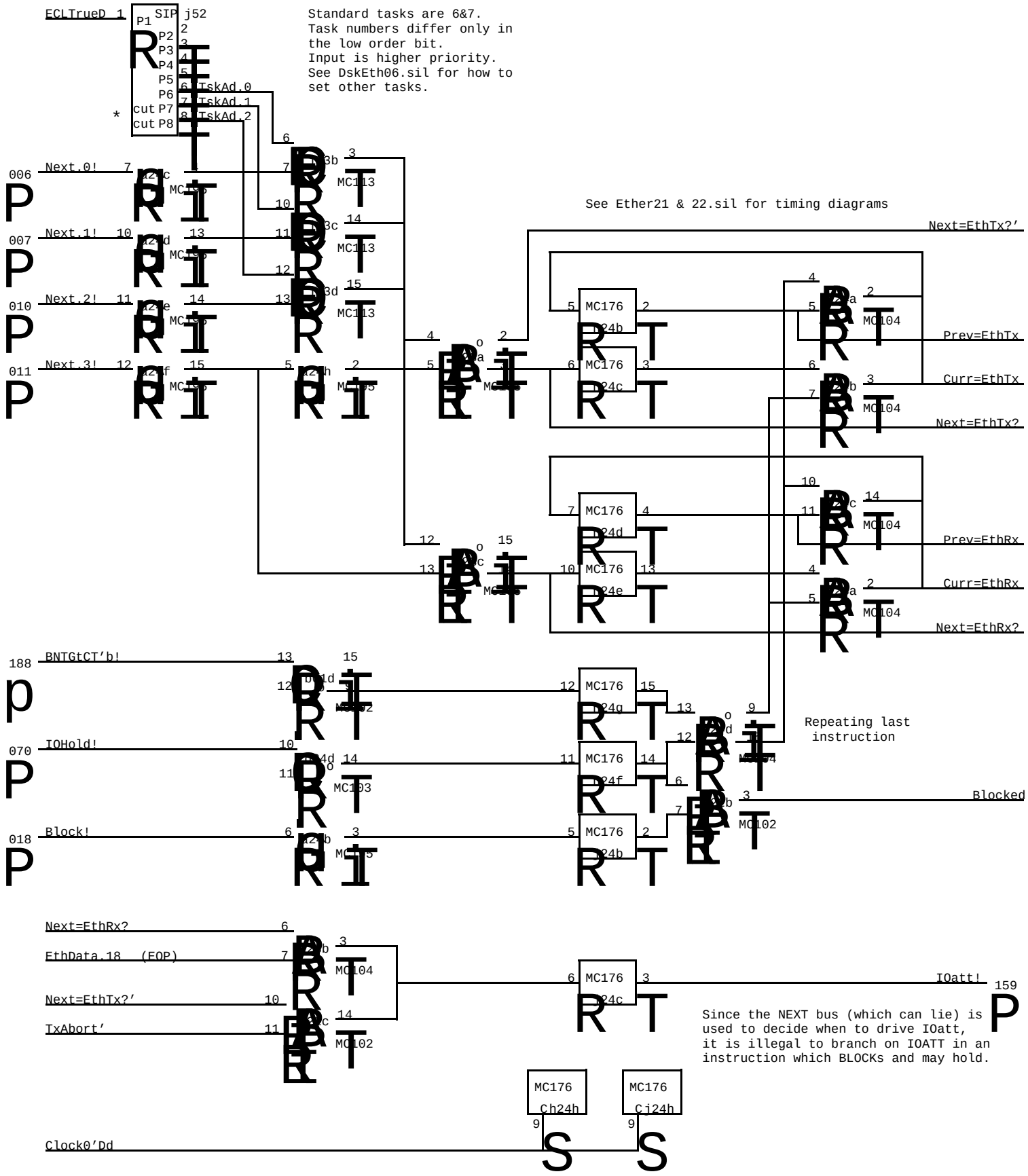


Dorado Synchronous Clocks

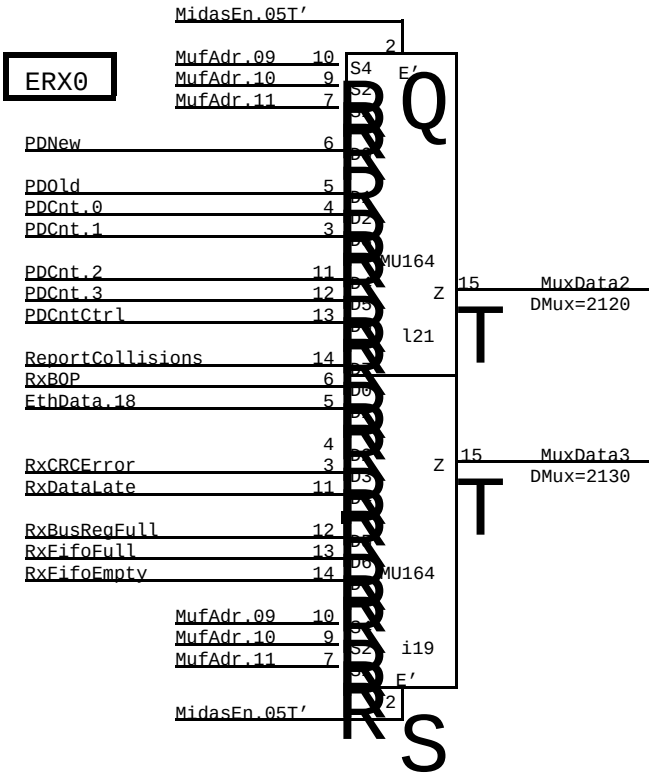
Free-running Ether Clocks

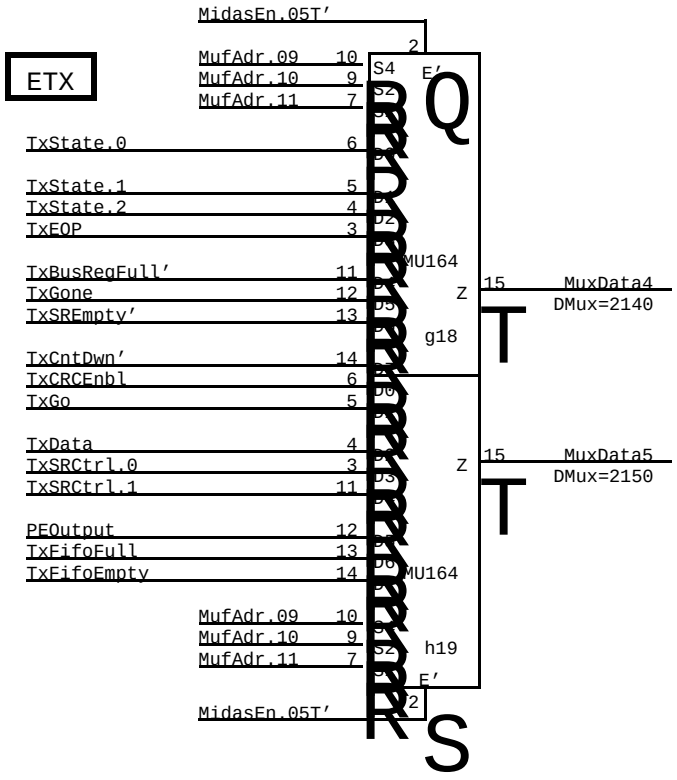


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Clocks	Ether12.sil	David Boggs	Cf	9/24/79	36

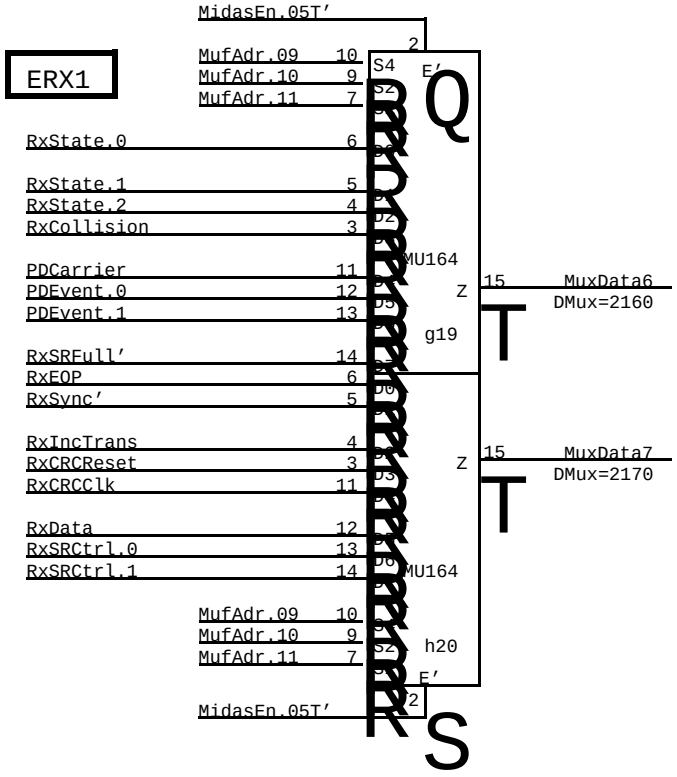


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Next & IOAttention	Ether13.sil	David Boggs	Cf	7/08/79	37

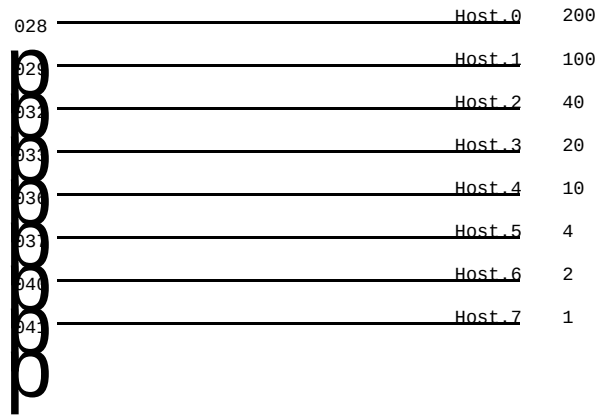


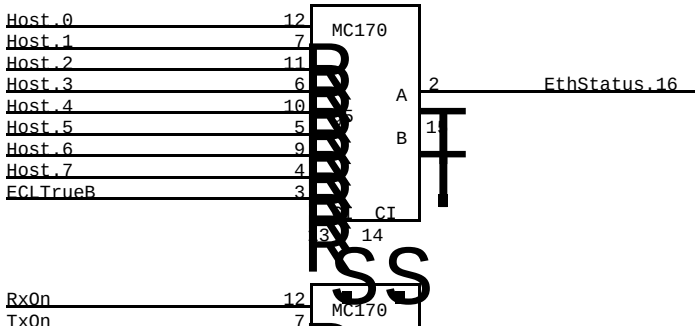


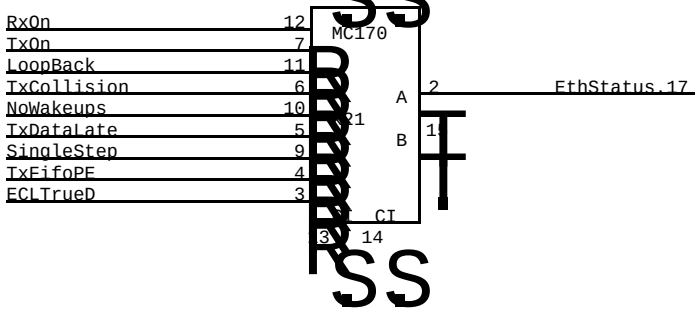
See DskEth01.sil for muffler control logic.
DMux addresses 2000-2117 are used by the disk.

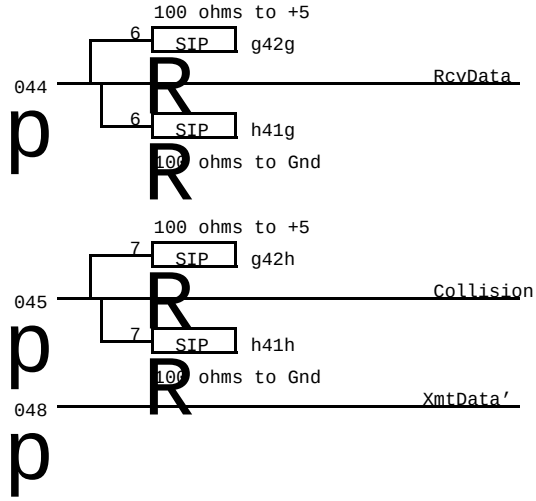


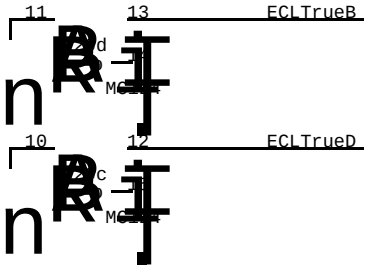
To set a host address bit to 1
pull it up to gnd through 91 ohms.

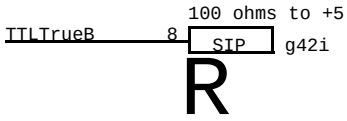




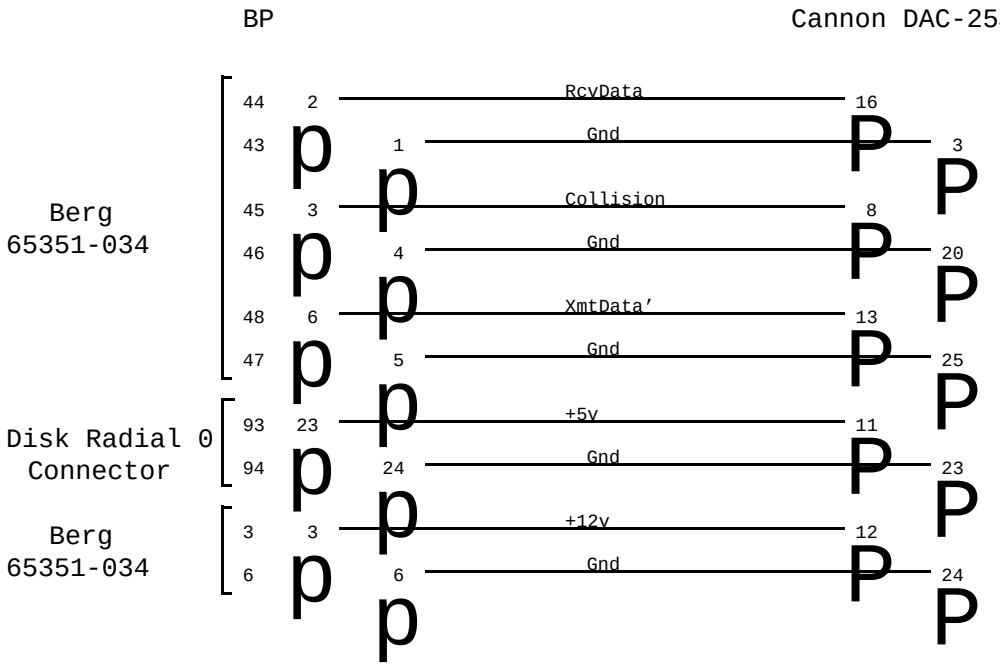






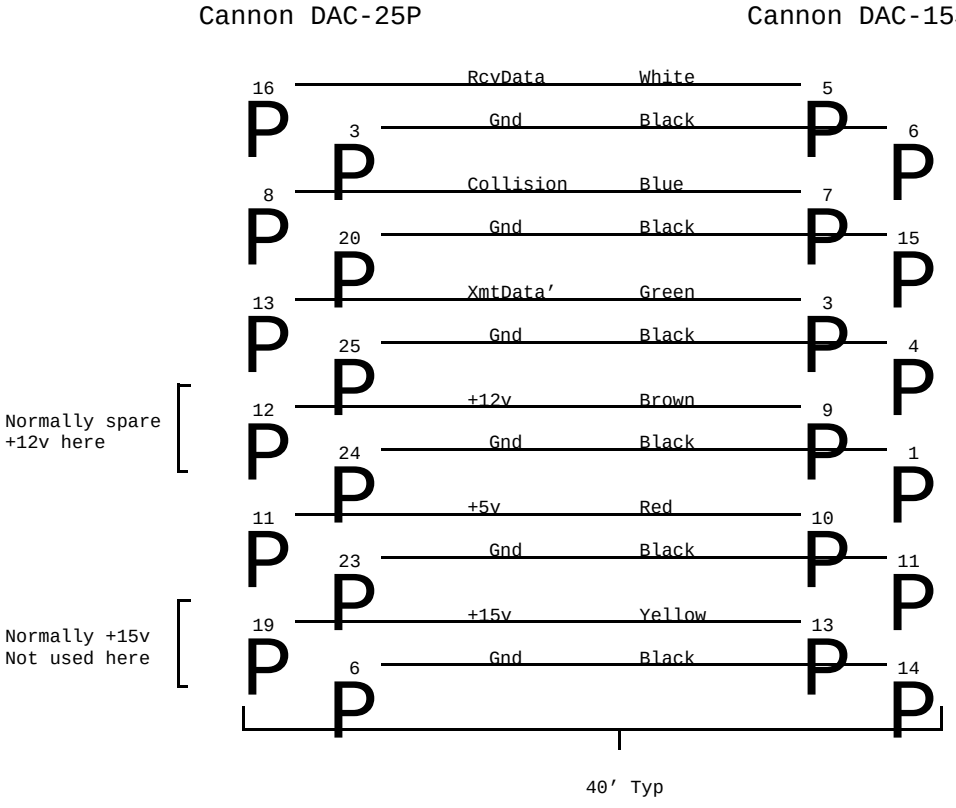


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BackPanel Connections	Ether15.sil	David Boggs	Cf	9/24/79	39



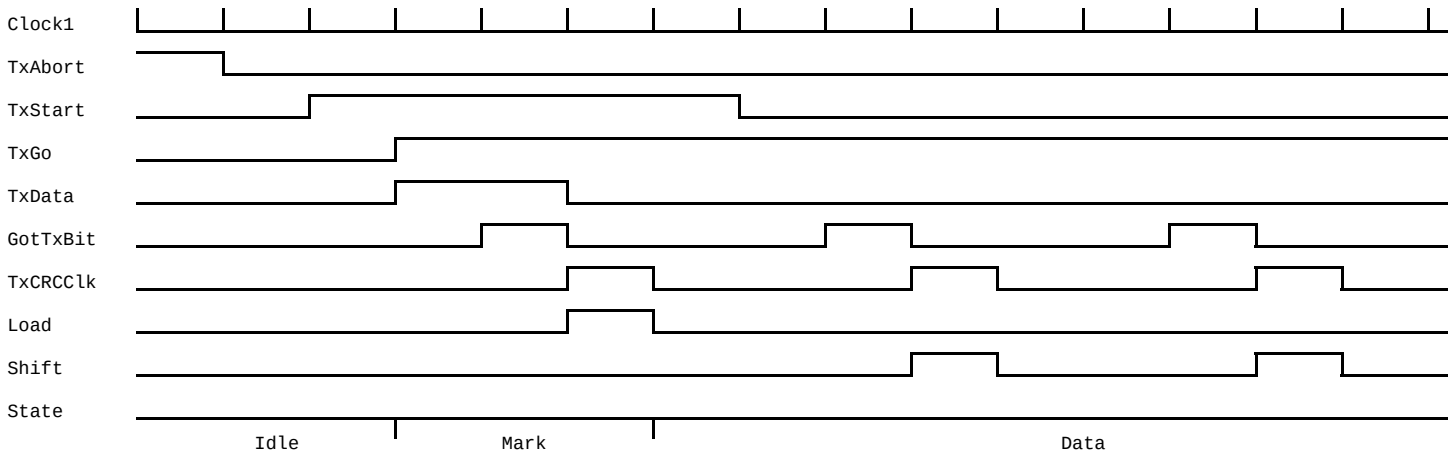
Internal Cable

External Cable

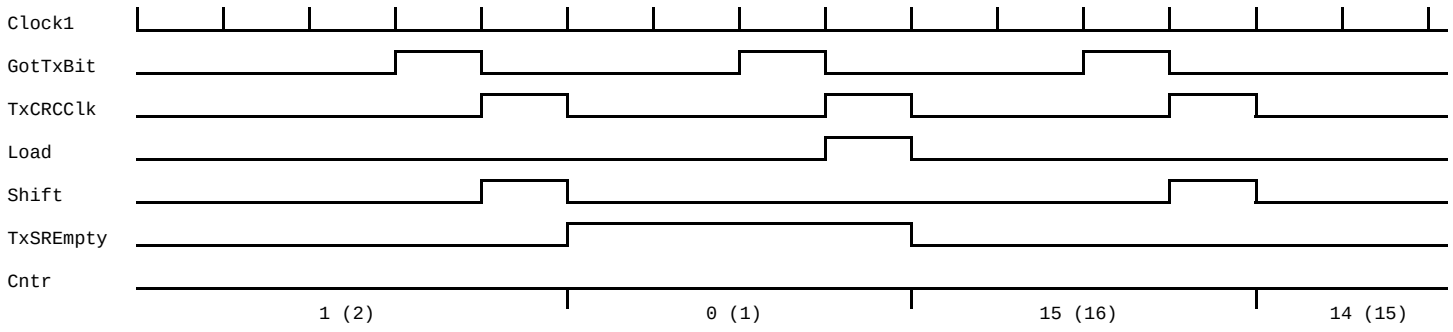


This is a standard Alto II
Ethernet external cable
part # 216411

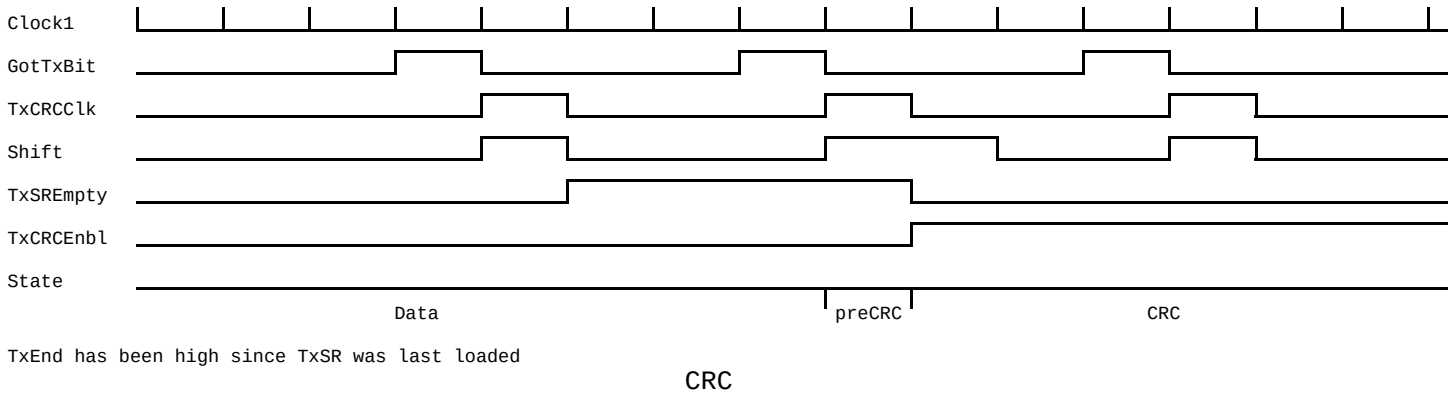
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Ethernet Cables	Ether16.sil	David Boggs	Cf	7/08/79	40



Startup

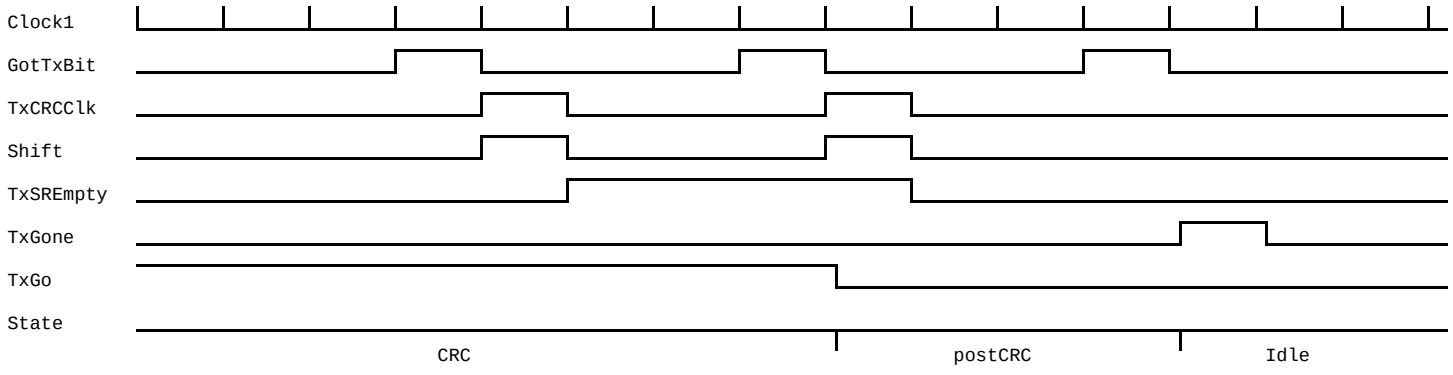


Loading Tx Shift Register



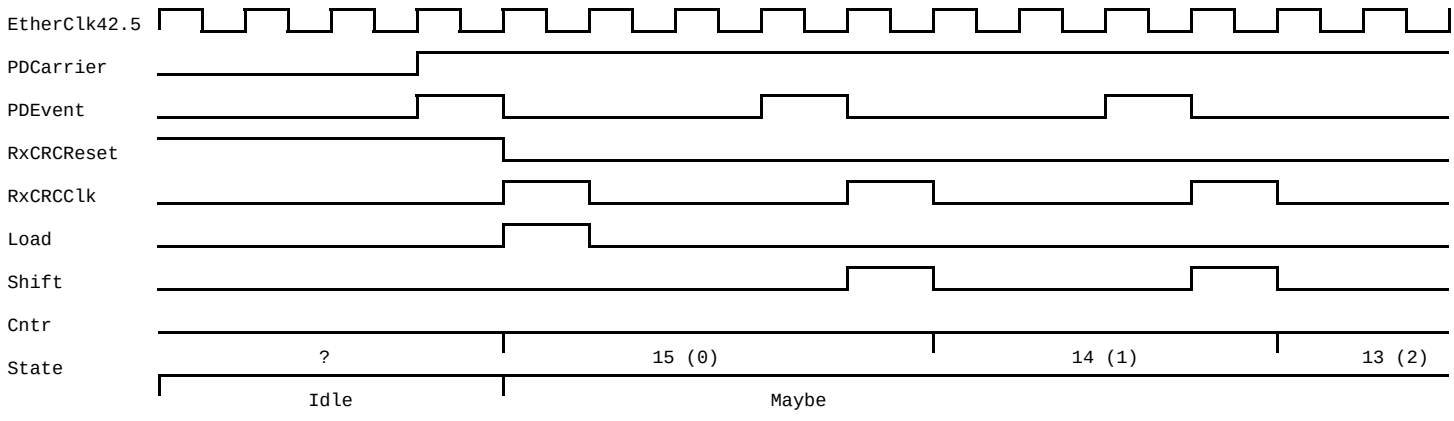
TxEnd has been high since TxSR was last loaded

CRC

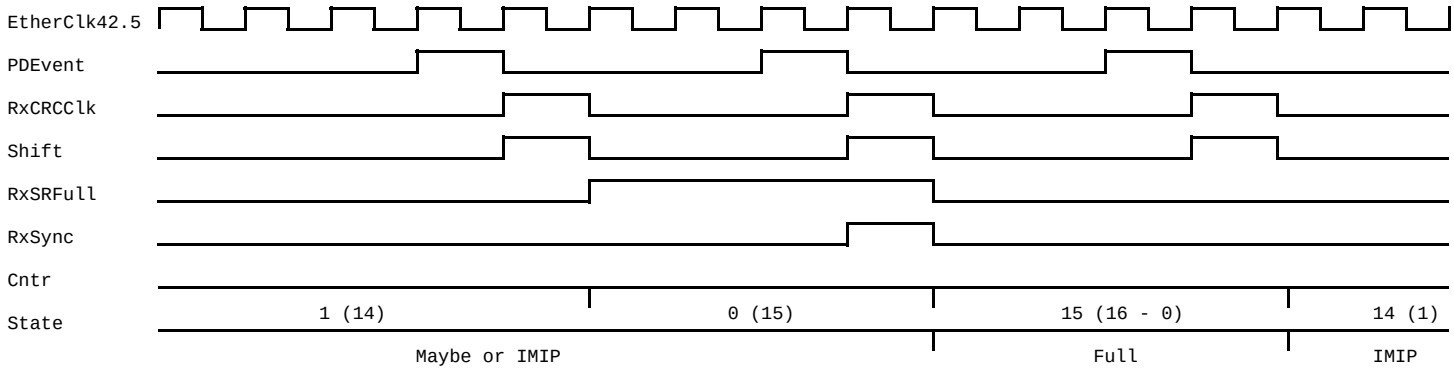


ShutDown

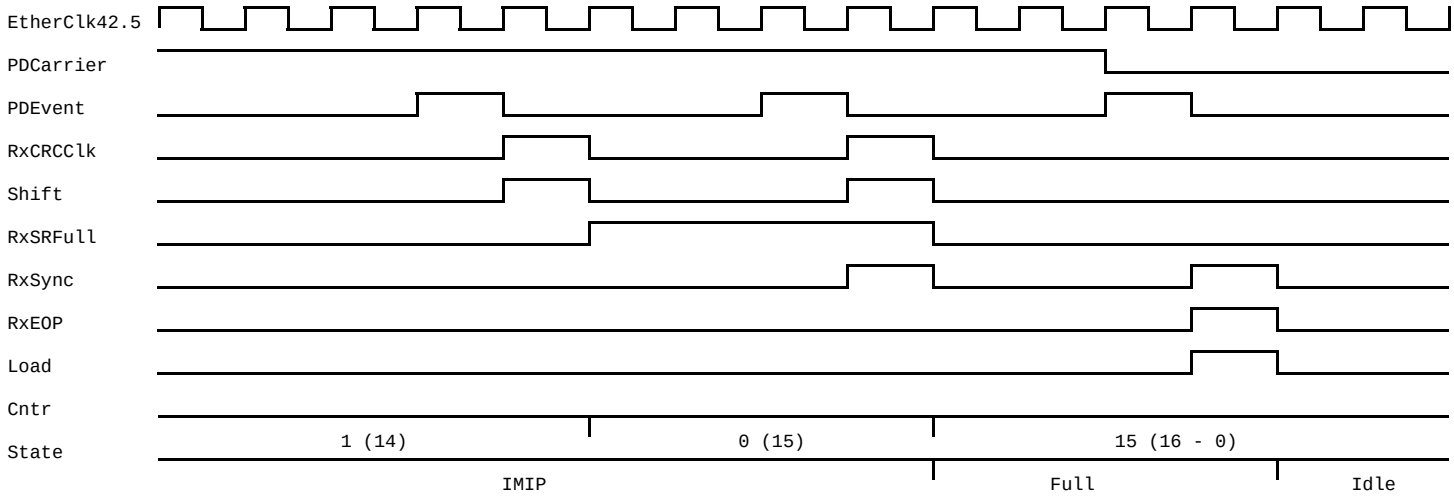
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Transmitter Timing	Ether17.sil	David Boggs	Cf	7/08/79	41



Startup



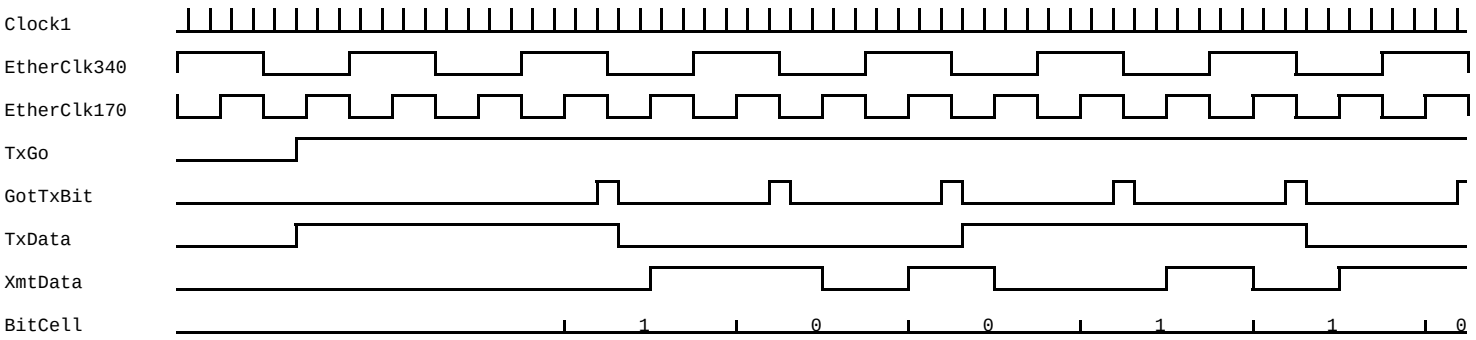
Dumping Rx Shift Register



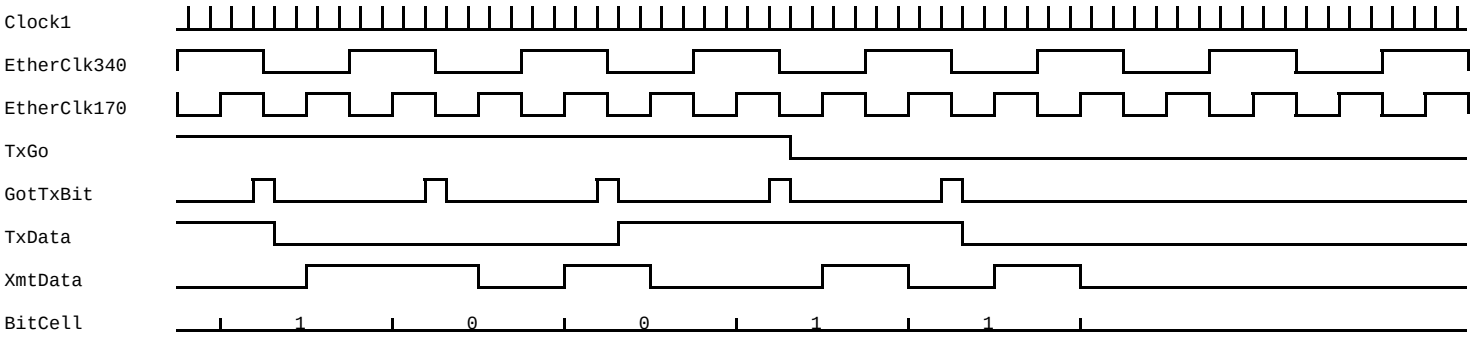
ShutDown

Cntr notation is <cntr value>(<# occupied postions>)
Phase decoder events are encoded in PDEvent.x
Shift and Load are encoded in RxSRCtrl.x
state is encoded in RxState.x
shift also decrements Cntr

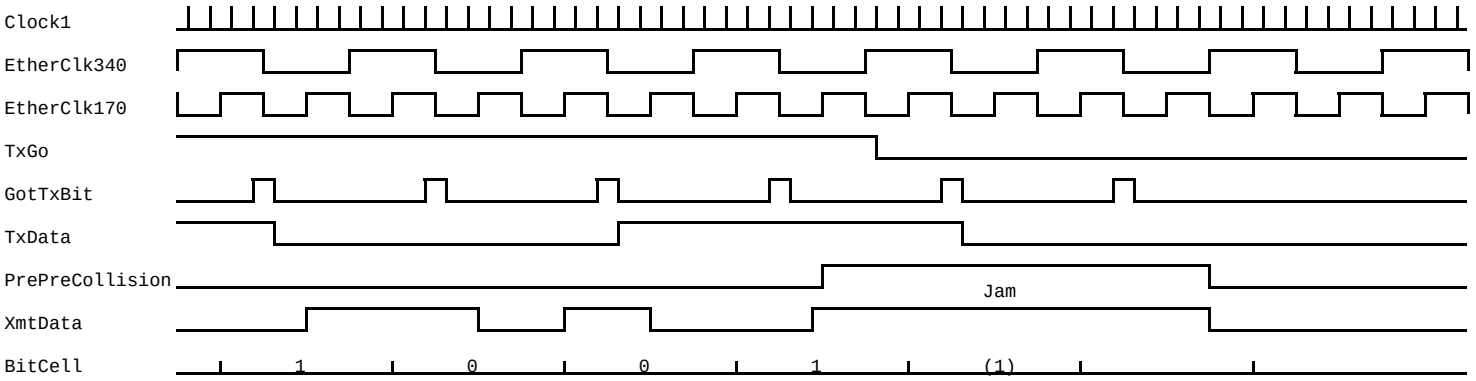
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Receiver Timing	Ether18.sil	David Boggs	Cf	7/08/79	42



Startup



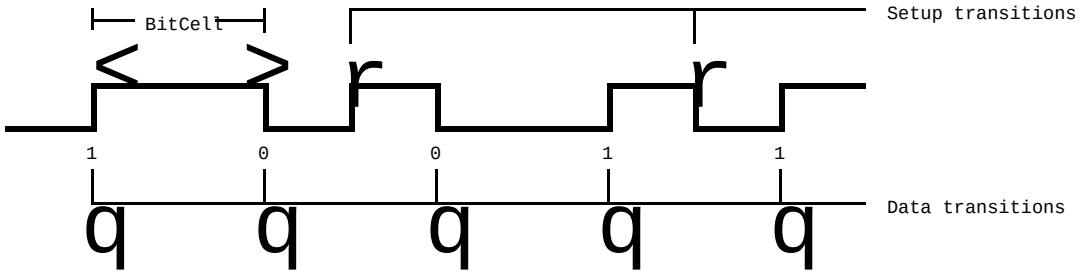
Shutdown



PrePreCollision is the output of the first stage of the Collision synchronizer

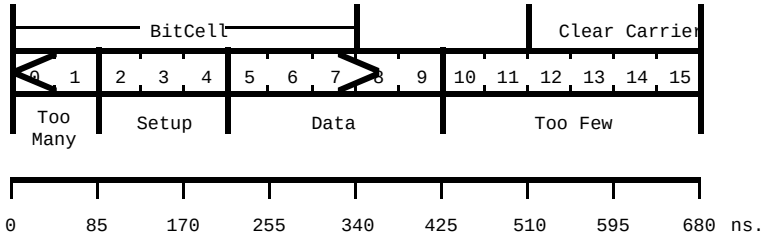
Collision

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Phase Encoder Timing	Ether19.sil	David Boggs	Cf	7/08/79	43



A bitcell is nominally 340 ns.

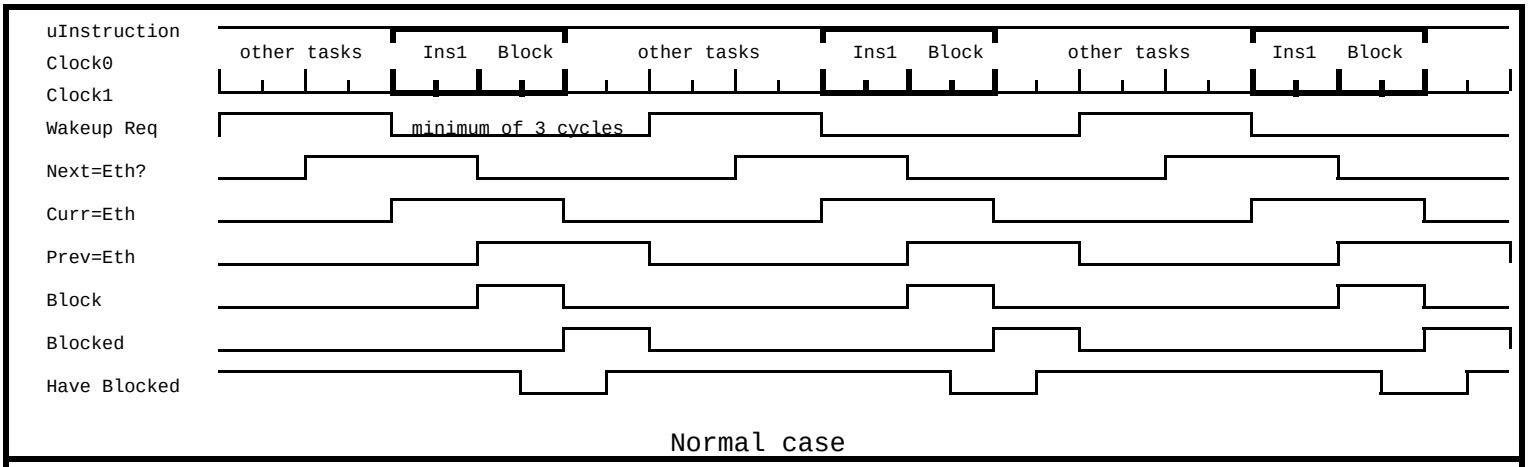
A sample is nominally 42.5 ns.



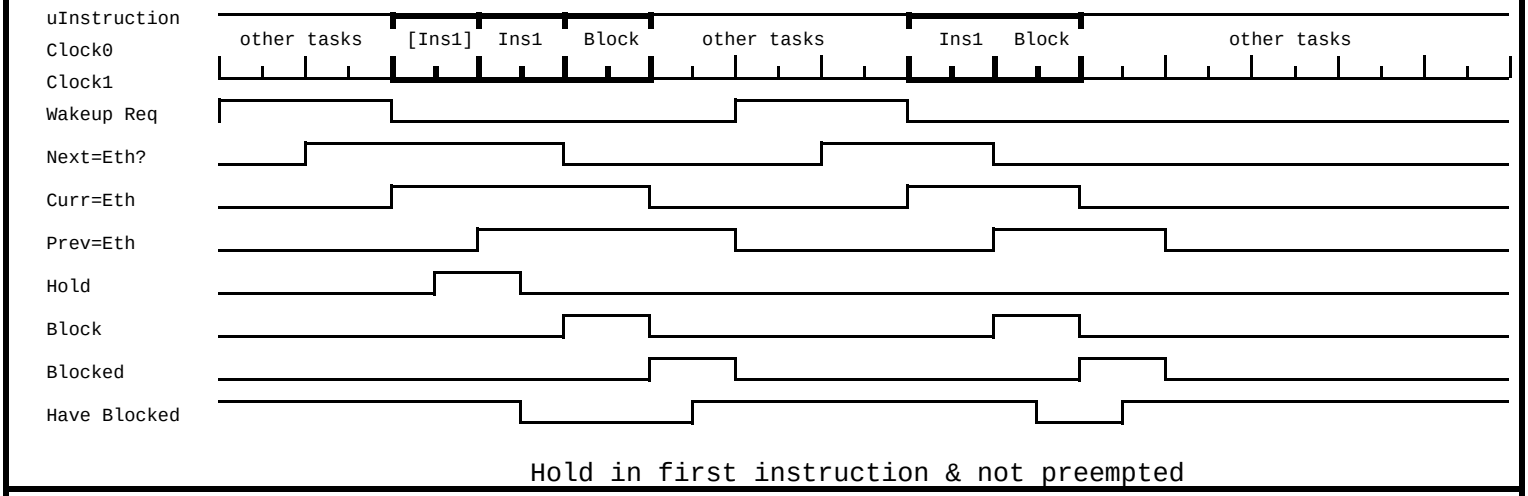
Inputs				Outputs			Comment
Carrier	Old	New	Cnt	Carrier	Event	CntCtrl	
Low	Low	Low	d/c	Low	NoEvent	Count	Idle
Low	Low	High	d/c	High	One	Reset	Start of packet (start bit)
Low	High	Low	d/c	High	Collision	Reset	Impossible
Low	High	High	d/c	Low	NoEvent	Count	Impossible
High	Low	High	0-1	High	Collision	Count	Too many transitions
High	High	Low	0-1	High	Collision	Count	Too many transitions
High	Low	High	2-4	High	NoEvent	Count	Setup transition (zero next)
High	High	Low	2-4	High	NoEvent	Count	Setup transition (one next)
High	Low	High	5-9	High	One	Reset	Data transition
High	High	Low	5-9	High	Zero	Reset	Data transition
High	Low	High	10-15	High	Collision	Reset	Too few transitions
High	High	Low	10-15	High	Collision	Reset	Too few transitions
High	Low	Low	0-11	High	NoEvent	Count	Active
High	High	High	0-11	High	NoEvent	Count	Active
High	Low	Low	12-15	Low	Collision	Reset	End of packet
High	High	High	12-15	High	Collision	Reset	Jam

"Impossible" conditions can happen right after power up.

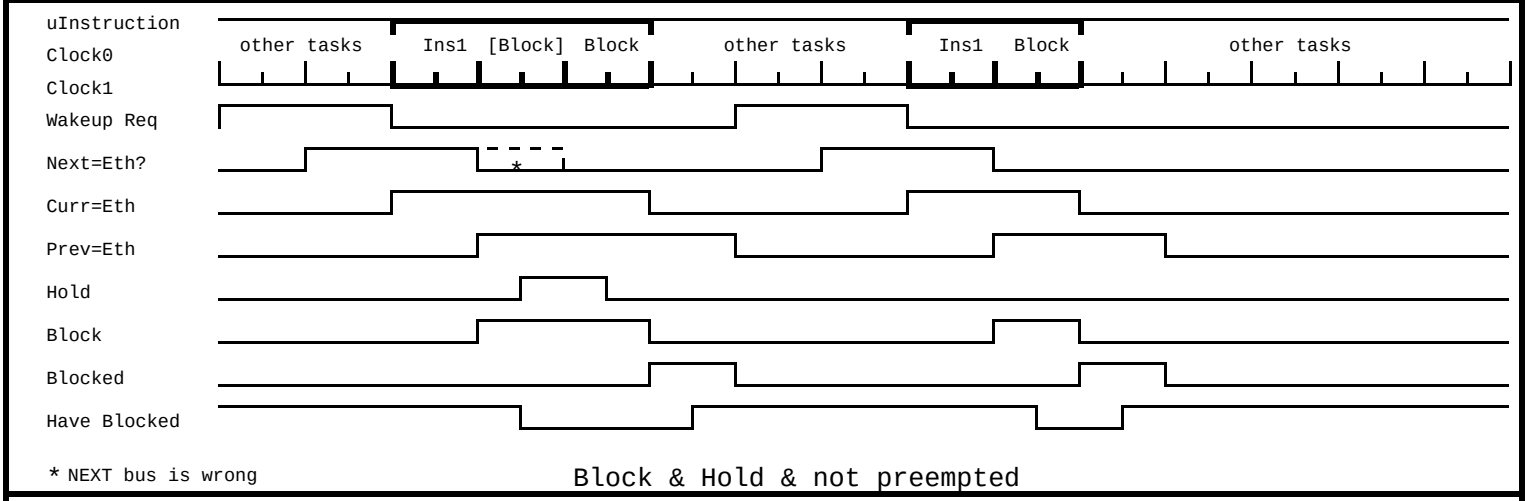
d/c means "don't care".



Normal case

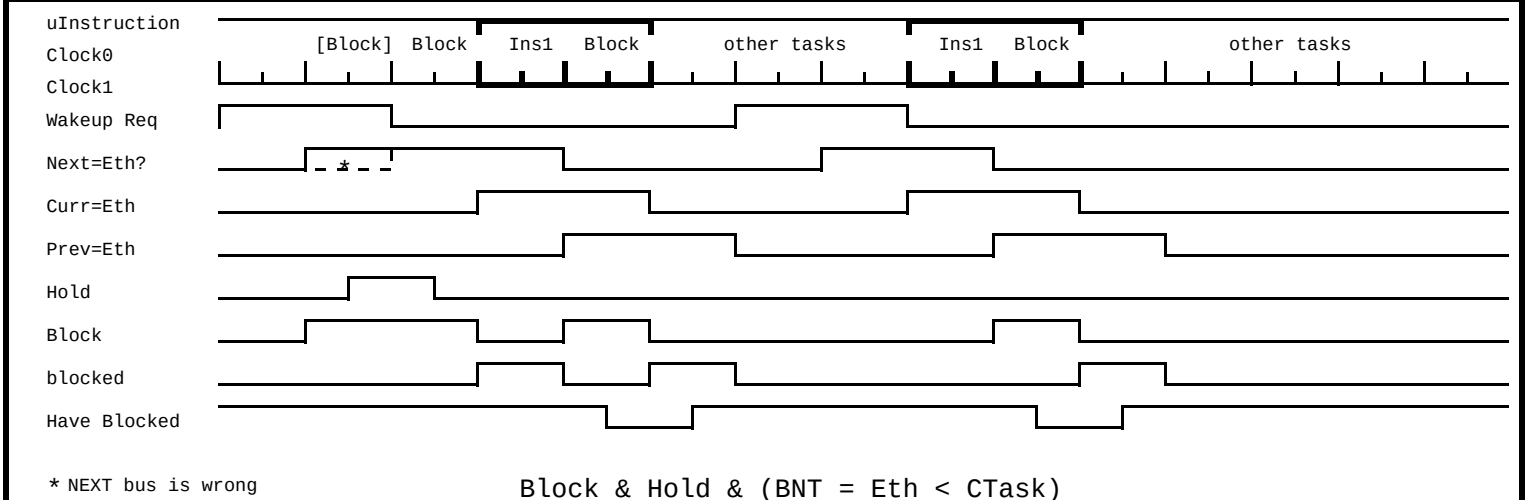


Hold in first instruction & not preempted



* NEXT bus is wrong

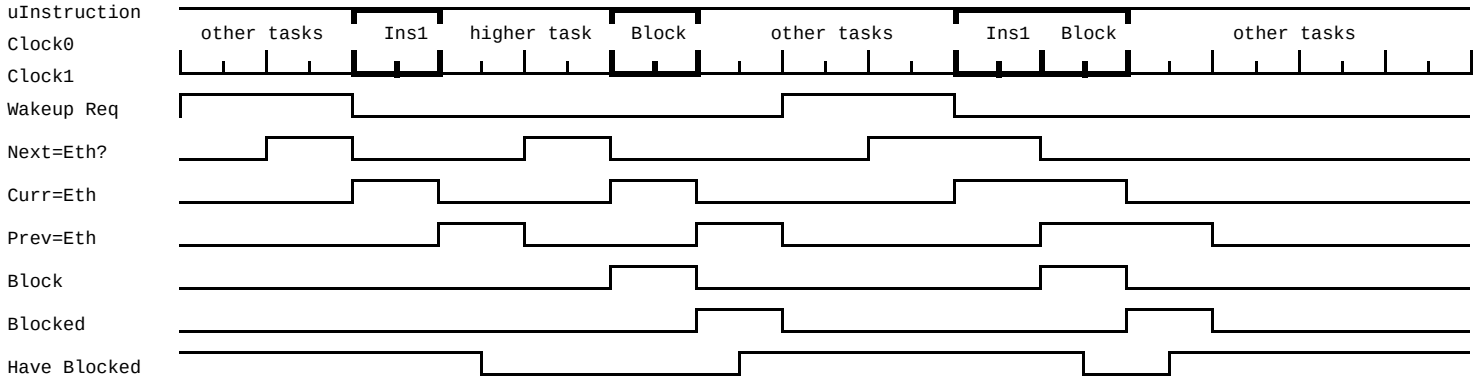
Block & Hold & not preempted



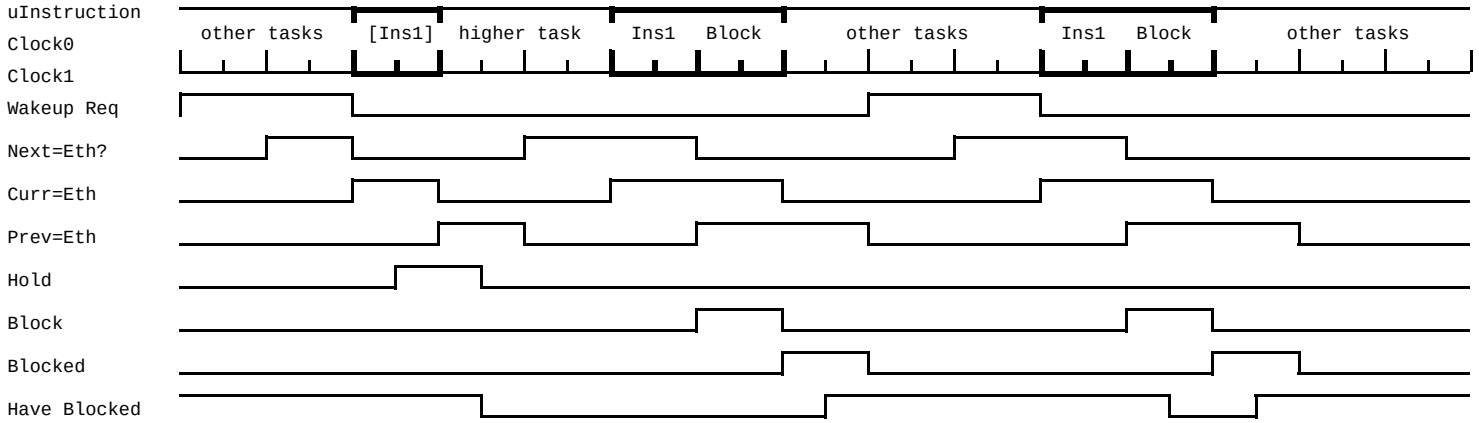
* NEXT bus is wrong

Block & Hold & (BNT = Eth < CTask)

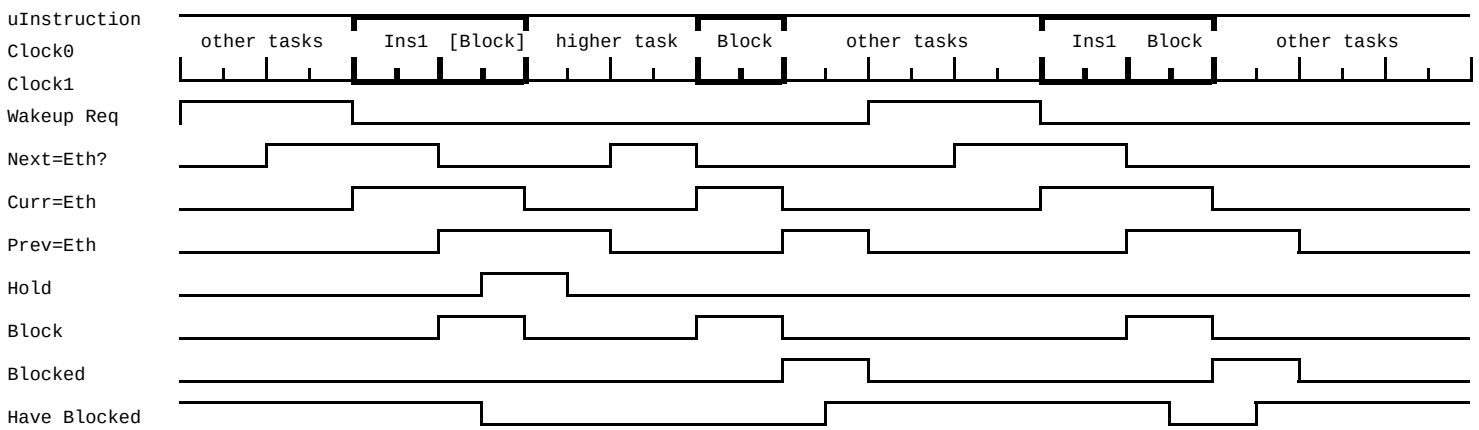
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Wakeup Timing	Ether21.sil	David Boggs	Cf	7/08/79	45



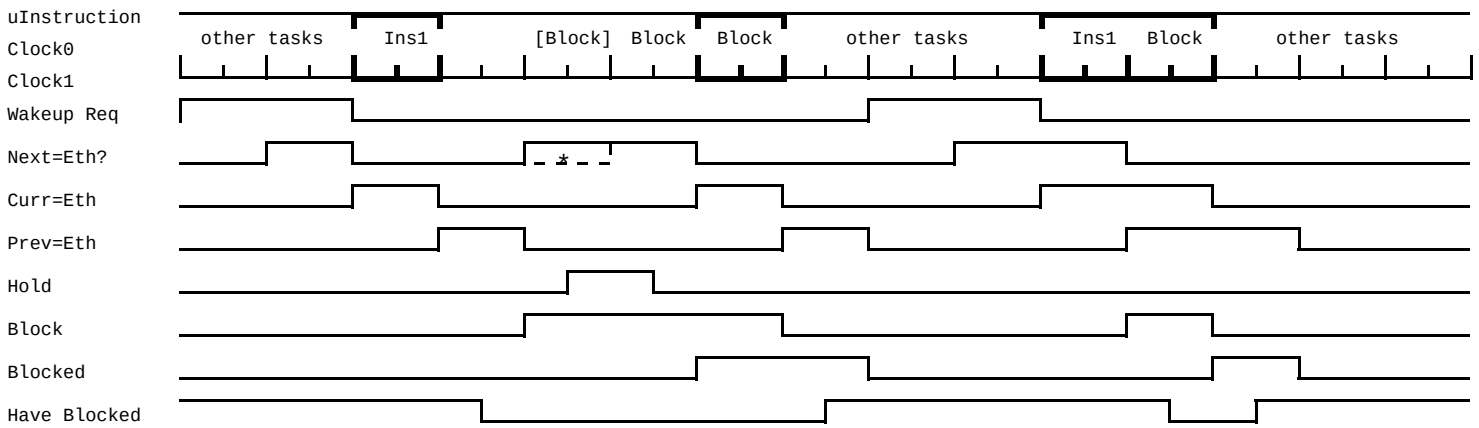
Preemption after first instruction



Hold in first instruction & then preempted



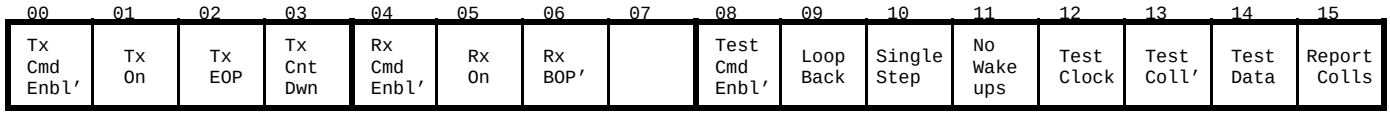
Block & Hold & then preempted



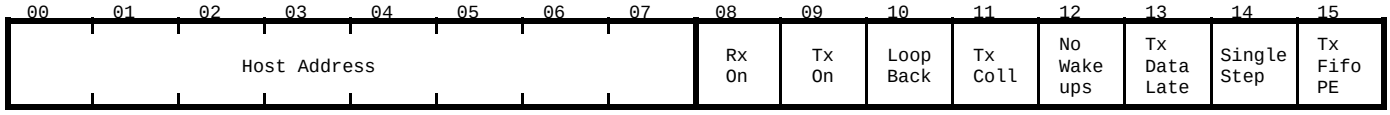
* NEXT bus is wrong

Block & Hold & (BNT = Eth < CTask) while Eth is preempted

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Wakeup Timing	Ether22.sil	David Boggs	Cf	7/08/79	46



Output



028 029 032 033 036 037 040 041

p p p p p p p p Input

The host address is set by jumpers on the right backplane.

To set a bit to one, pull it up to ground through 91 ohms.