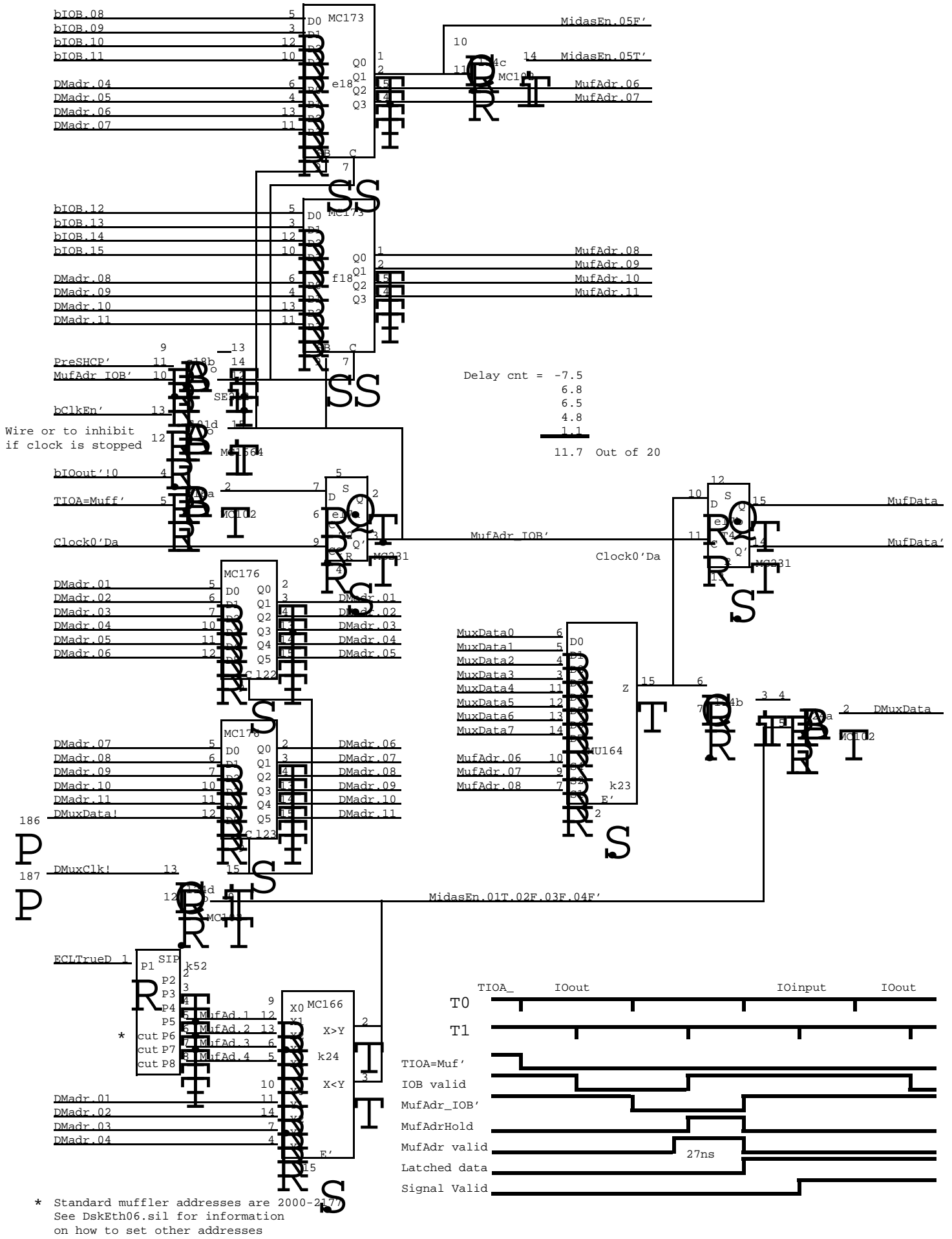
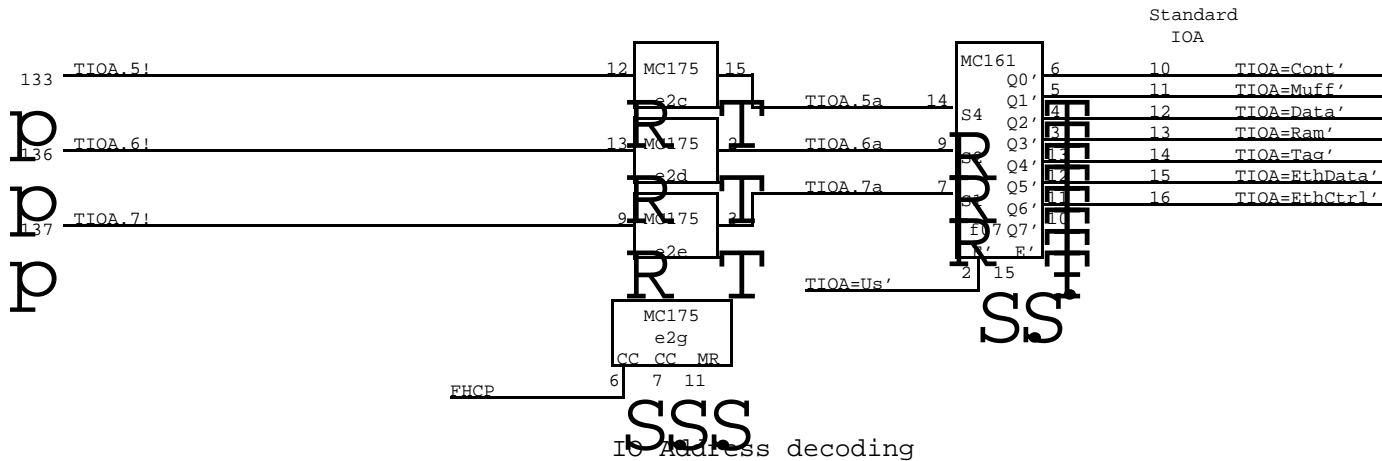
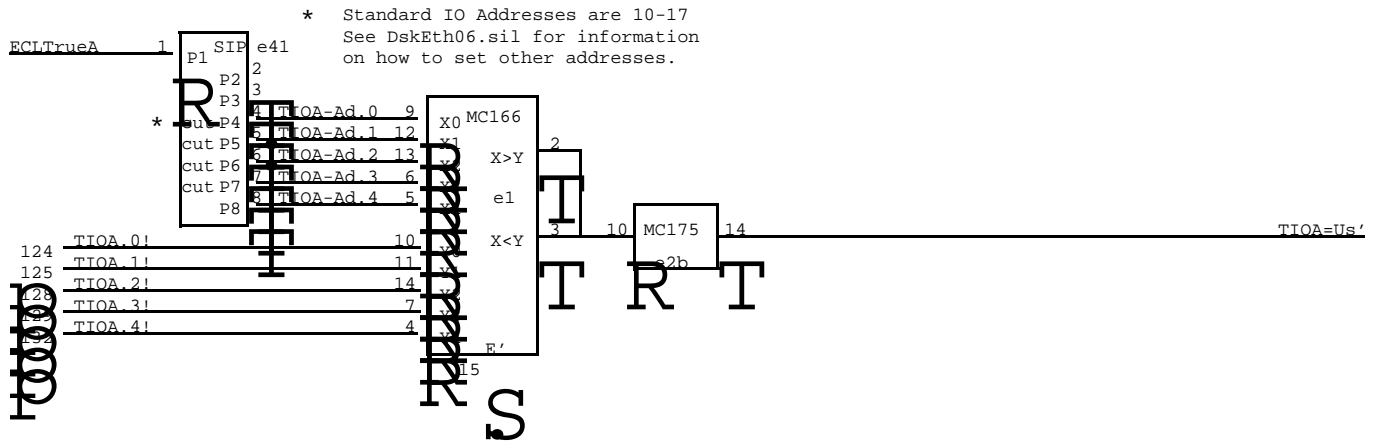


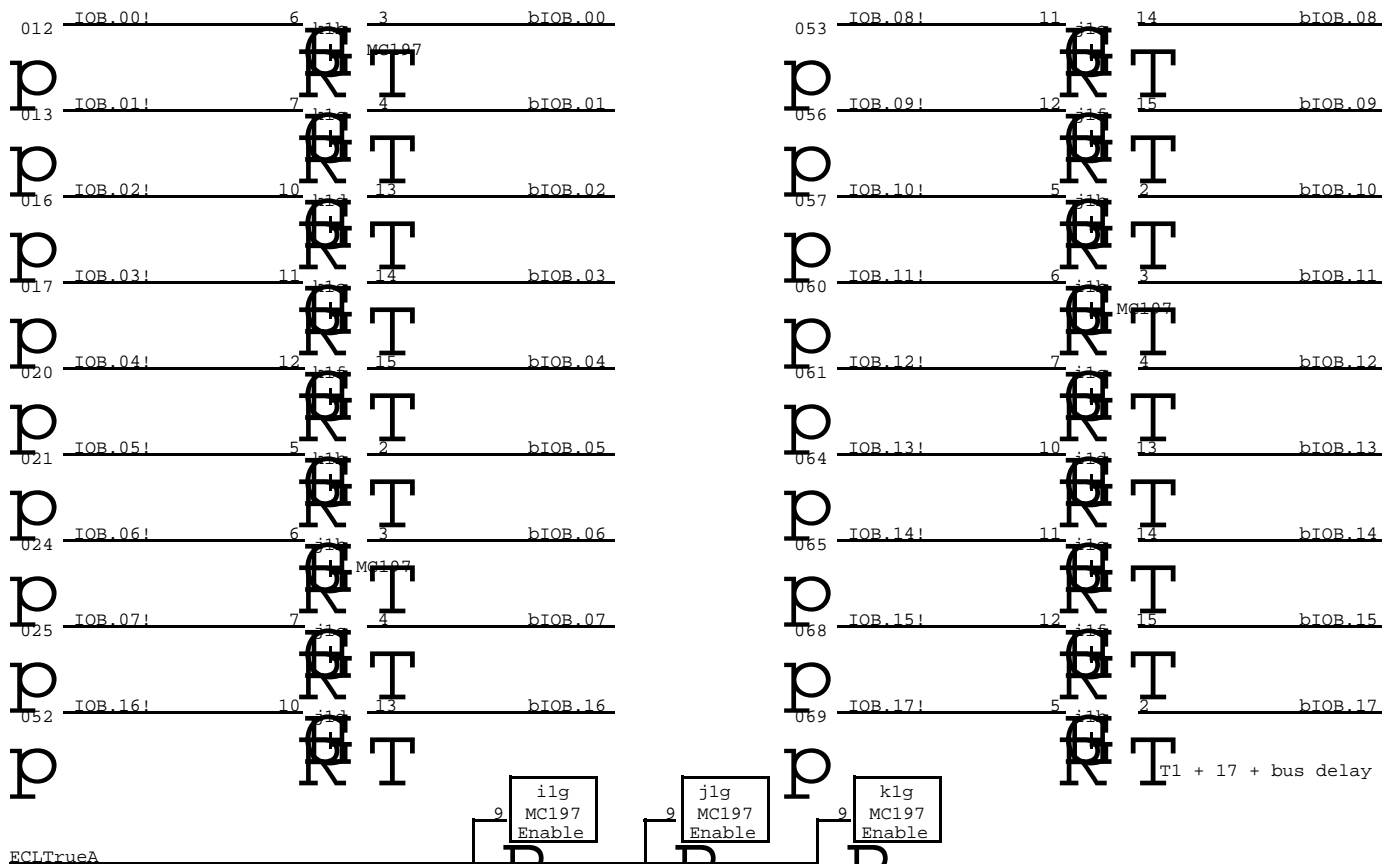
1) Drawings of common logic	01
Midas Muffler Control	01
IOA and IOB	02
Clocks and Temp sense	04
Layout	05
Configuration	06
2) Drawings for TriconD disk Controller	07
State Control Register	08
Format Ram, Counter and Proms	09
Tag Register	10
Disk Drive Control	11
FIFO	13
Error Correction Shift Register	15
Task Wake-Up and IOB parity check	16
Mufflers	18
Clocks	19
I/O pins and Termination	20
Timing Diagram	21
Cable Assembly Drawings	22
3) Drawings for Ethernet Controller	23
Receiver	24
Transmitter	29
Test Logic	34
Clocks	35
Next Bus and IOattention	36
Mufflers	37
Cable I/O and termination	38
Timing Diagrams	40



* Standard muffler addresses are 2000-2177
 See DskEth06.sil for information
 on how to set other addresses

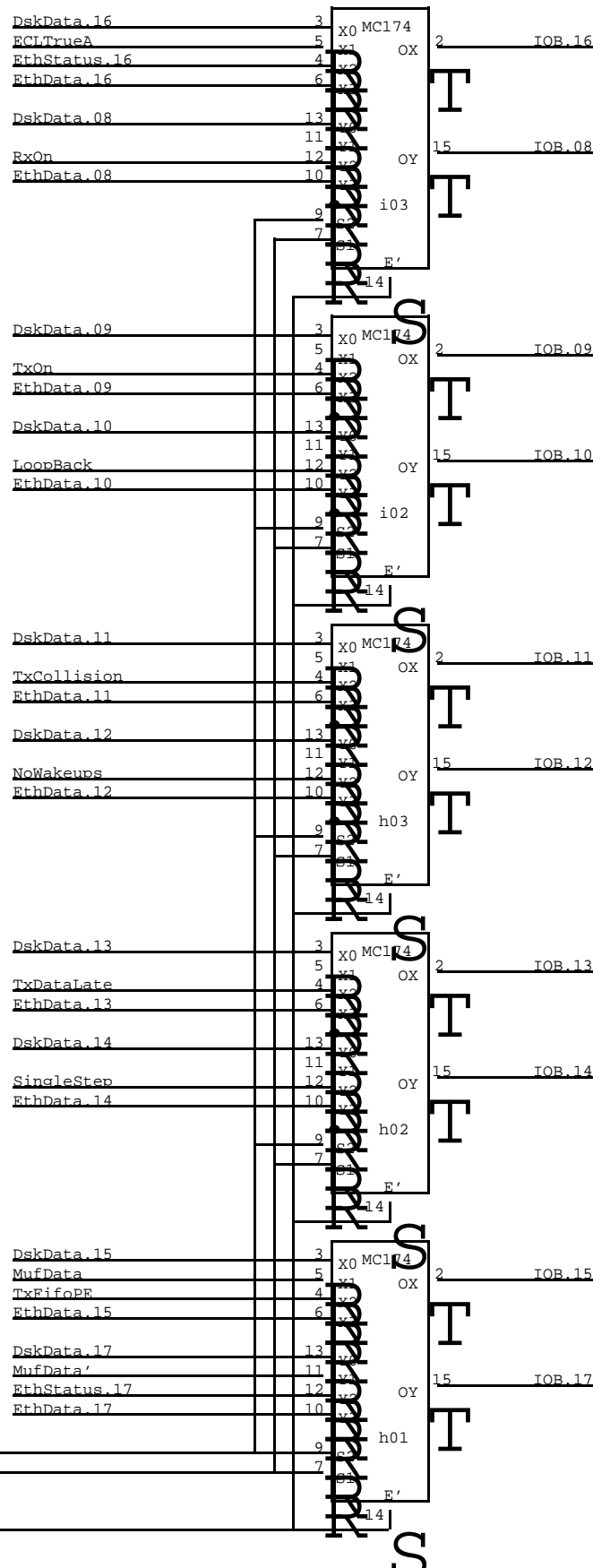
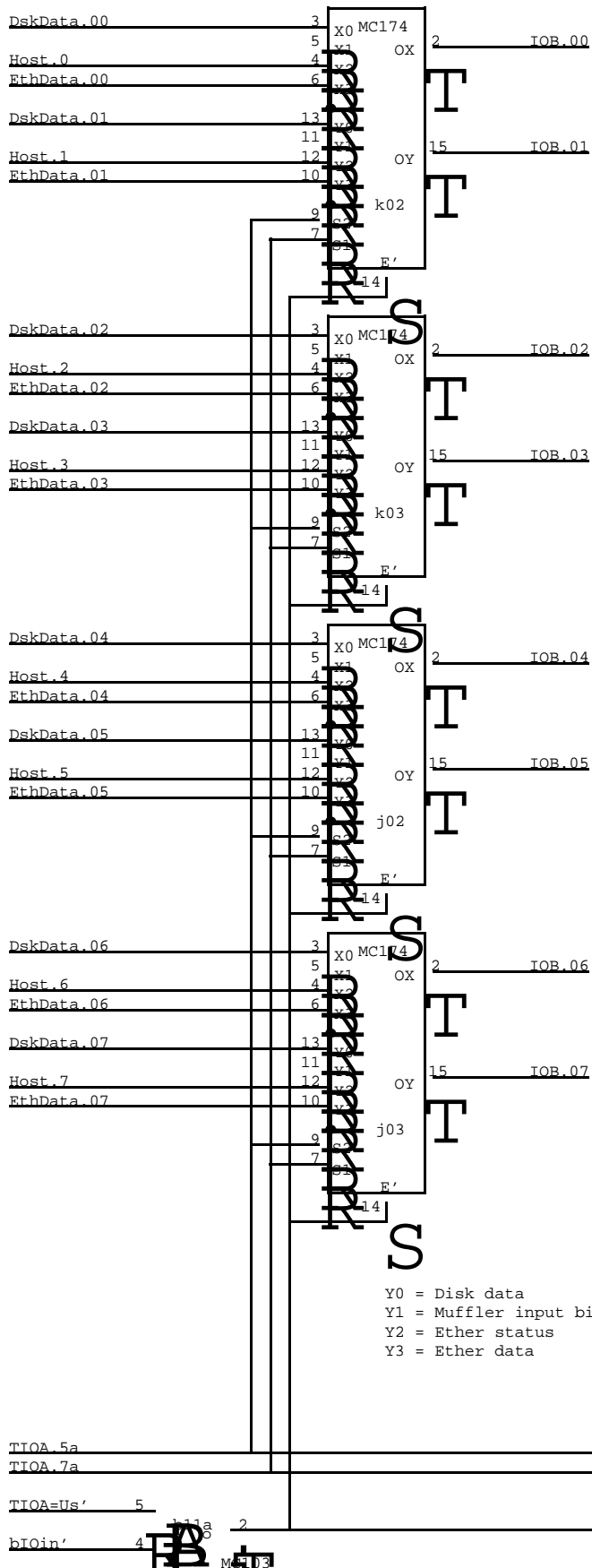


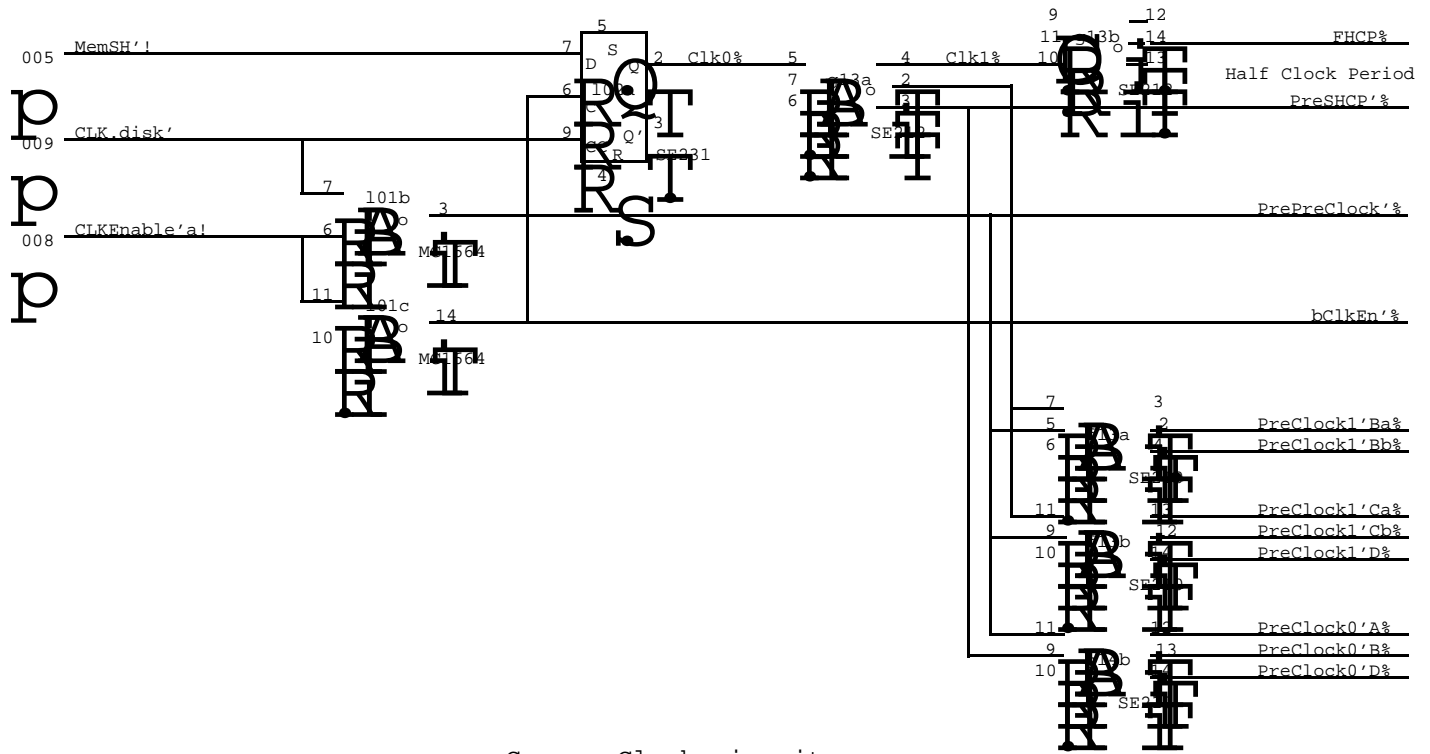
IOB receivers



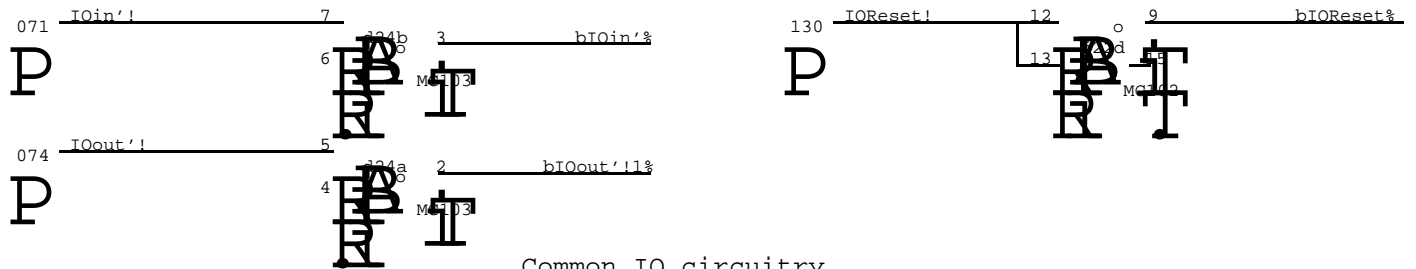
NOTE: IOB data received by this board is tested as part of the disk controller (Pg 18). Both the disk and the Ethernet check the data parity after it has gone through the respective FIFO's.

XEROX PARC	Project Dorado	Drawing IOA & IOB	File DskEth02.sil	Designer Bates/Boggs	Rev Da	Date 7/19/79	Page 02
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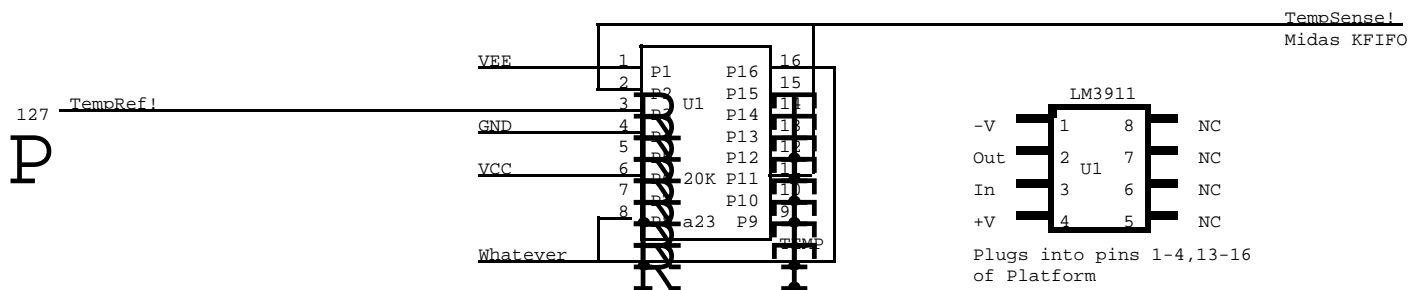




Common Clock circuitry



Common IO circuitry

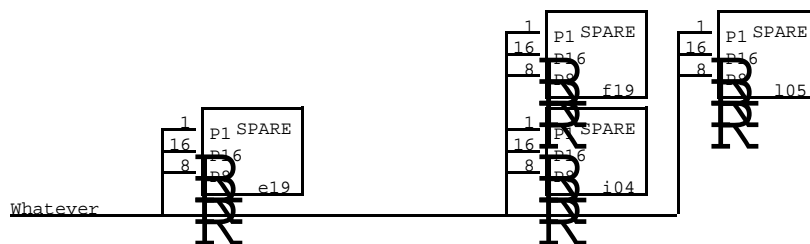


Temperature Sensor

Power connections are as follows:

Stitch-Weld:1 & 16 are GND
 8 is -5

Multiwire: 16 is GND
 8 is -5
 except in locations
 a18, g03, and g16
 which are uncommitted



Spare Socket locations for Multiwire

XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	Dorado	Clocks & IO Signals	DskEth04.sil	Bates/Boggs	Da	2/09/82	04

Cut SIP legs at k52 to set the Muffler addresses for the board.

* Standard addresses are 2000-2177.

Muff Addr	P5	P6	P7	P8
0000-0177	cut	cut	cut	cut
0200-0377	cut	cut	cut	
0400-0577	cut	cut		cut
0600-0777	cut	cut		
1000-1177	cut		cut	cut
1200-1377	cut		cut	
1400-1577	cut			cut
1600-1777	cut			
* 2000-2177		cut	cut	cut
2200-2377		cut	cut	
2400-2577		cut		cut
2600-2777		cut		
3000-3177			cut	cut
3200-3377			cut	
3400-3577				cut
3600-3777				

Cut SIP legs at e41 to set the IOA bus addresses for the board.

* Standard addresses are 10-17.

IOA	P4	P5	P6	P7	P8
000-007	cut	cut	cut	cut	cut
* 010-017	cut	cut	cut	cut	
020-027	cut	cut	cut		cut
030-037	cut	cut	cut		
040-047	cut	cut		cut	cut
050-057	cut	cut		cut	
060-067	cut	cut			cut
070-077	cut	cut			
100-107	cut		cut	cut	cut
110-117	cut		cut	cut	
120-127	cut		cut		cut
130-137	cut		cut		
140-147	cut			cut	cut
150-157	cut			cut	
160-167	cut				cut
170-177	cut				
200-207		cut	cut	cut	cut
210-217		cut	cut	cut	
220-227		cut	cut		cut
230-237		cut	cut	cut	
240-247		cut		cut	cut
250-257		cut			
260-267		cut			cut
270-277		cut			
300-307			cut	cut	cut
310-317			cut	cut	
320-327			cut		cut
330-337			cut		
340-347				cut	cut
350-357				cut	
360-367					cut
370-377					

Cut SIP legs at j52 to set the Task numbers for the Ethernet.

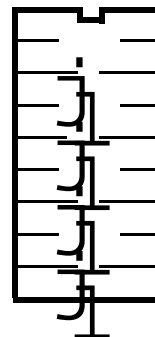
* Standard tasks are 6 & 7.

Tasks	P6	P7	P8
2 & 3			cut
4 & 5		cut	
* 6 & 7		cut	cut
8 & 9	cut		
10 & 11	cut		cut
12 & 13	cut	cut	
14 & 15	cut	cut	cut

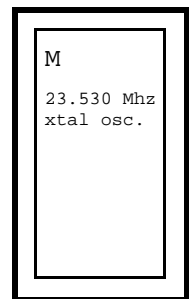
The EtherFifo ROMs are identical and interchangeable. The DiskRead, EtherRcvr and EtherXmtr ROMs are not.

Name	Type	#	Location
DskEth			
Disk			
DiskRead	SG139	2	a20 a21
DiskTag	MC149	1	d21
DiskUnits	S288	1	d05
DiskFifo	MC149	1	b14
Ether			
EtherPD	MC149	1	h22
EtherRcvr	MC149	3	h09 h10 h11
EtherFifo	MC149	2	l10 l15
EtherXmtr	MC149	3	h14 h15 h16

PLAT at a04



K1115A at j20



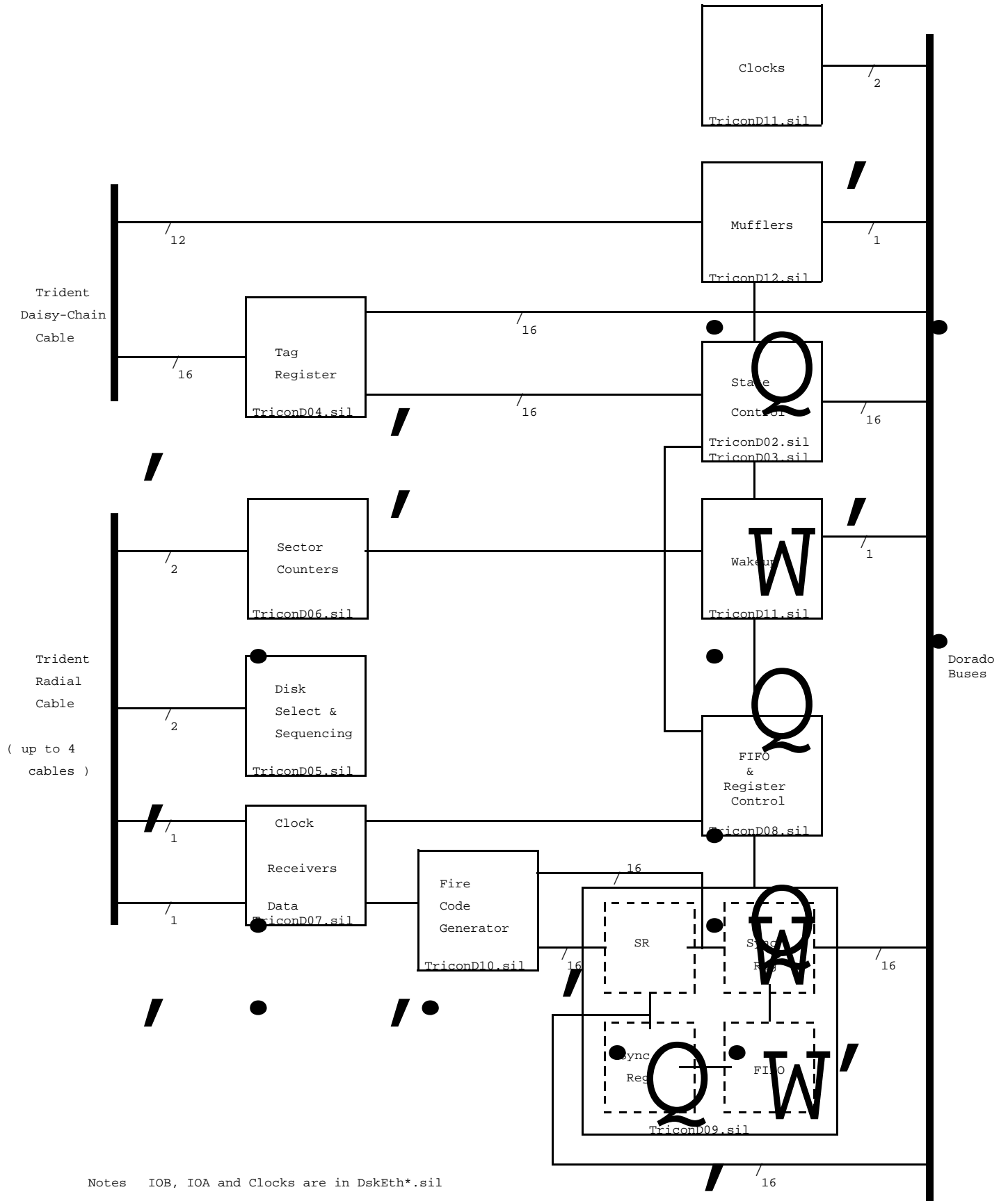
"DoradoProms DskEth" gets all proms for the DskEth board.

"DoradoProms Disk" gets all proms for the Trident half of the board. All capacitors 330pf

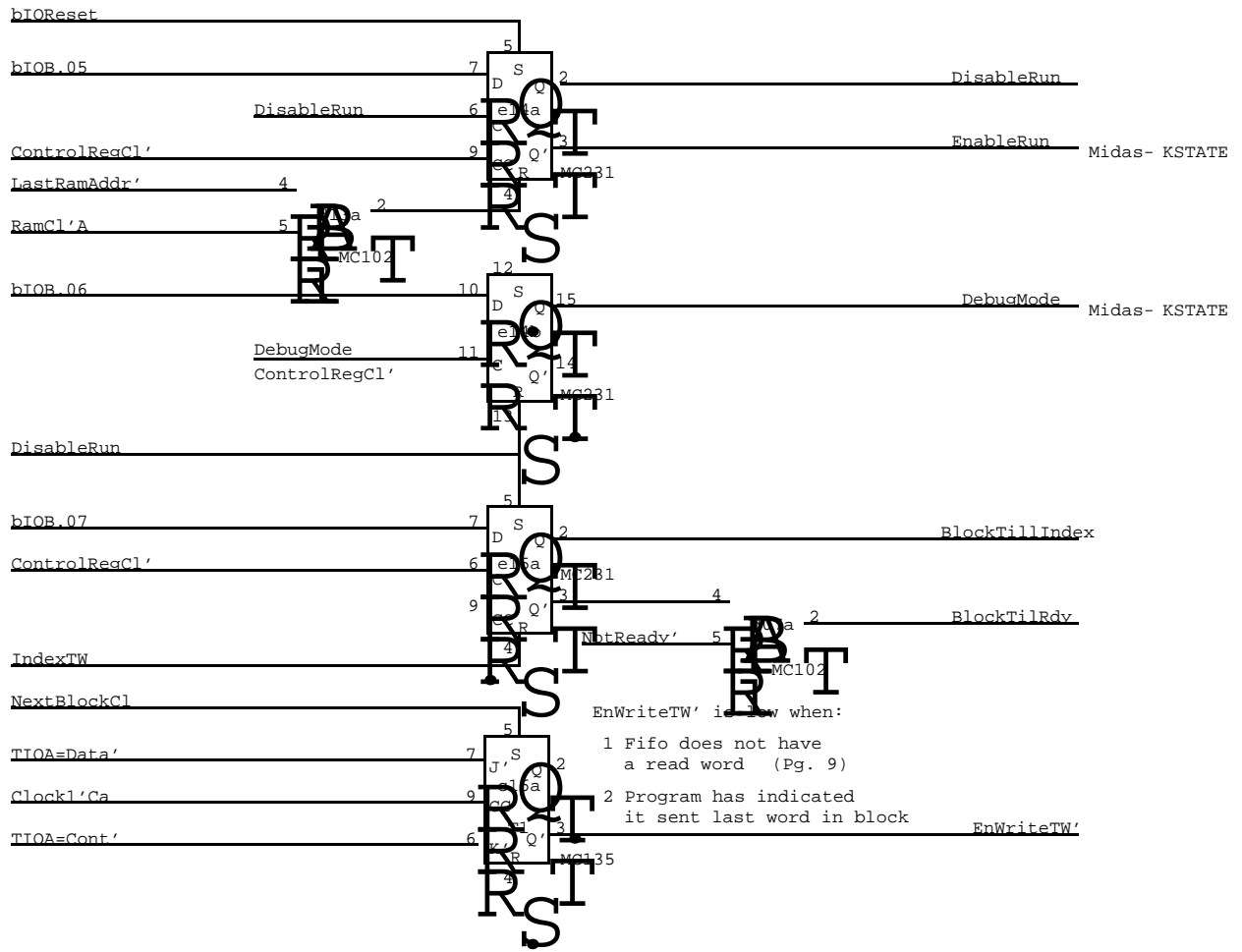
"DoradoProms Ether" gets all proms for the Ethernet half of the board.

All resistors 27K

Logo is near pin 1. This is a 14 pin pkg. Board pins 8 & 9 aren't used. Remove bypass cap above pin 1

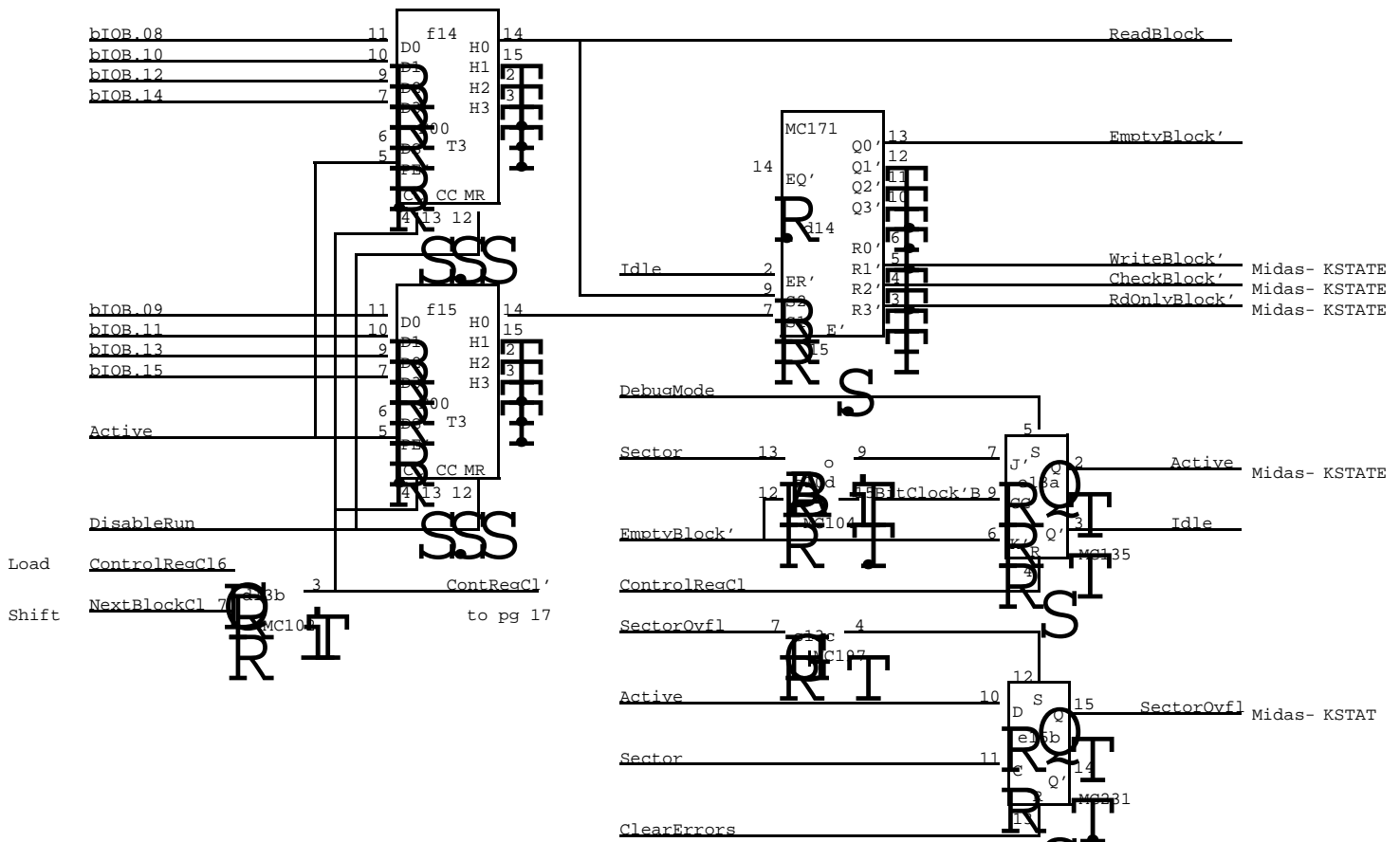


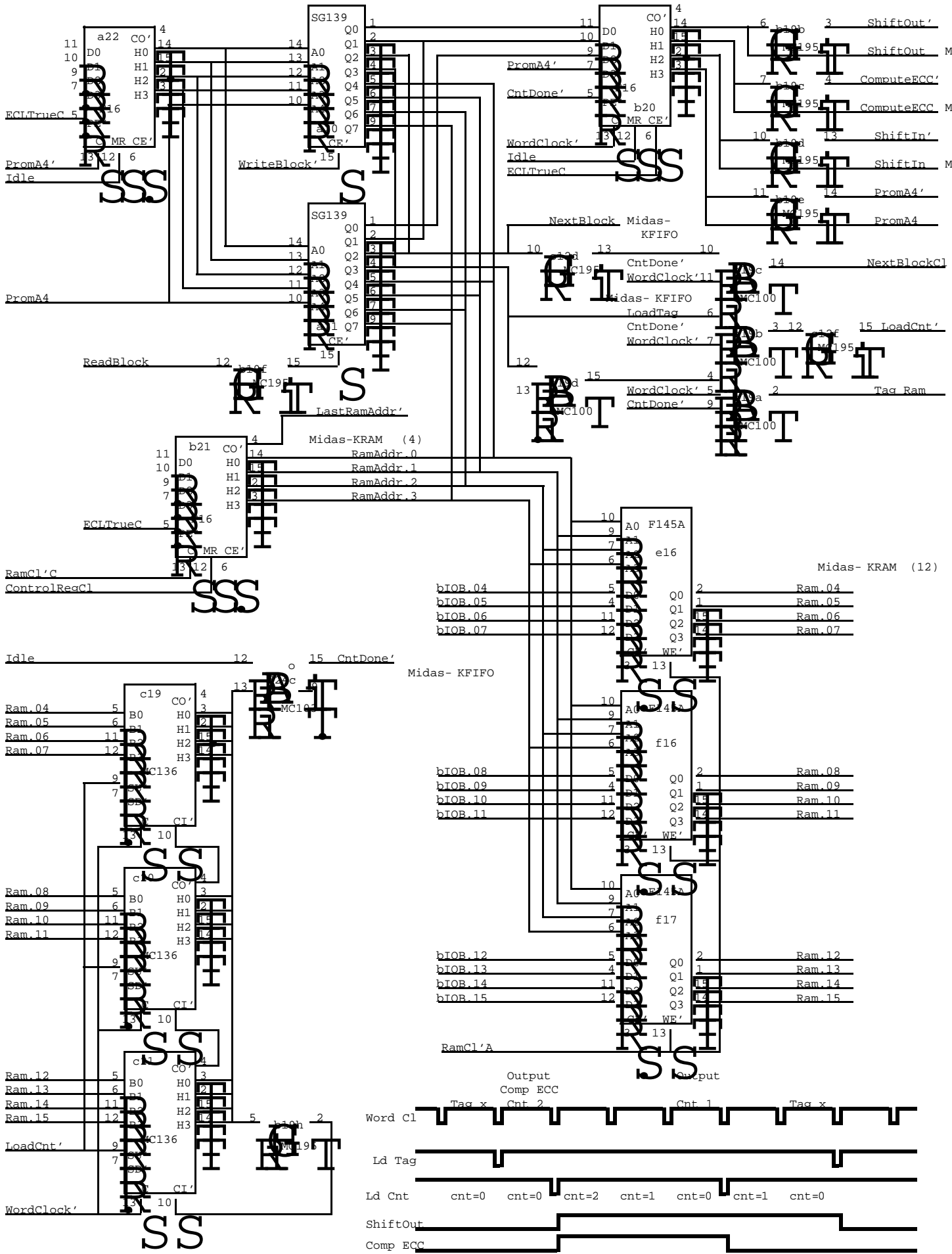
Notes IOB, IOA and Clocks are in DskEth*.sil



EnWriteTW' is low when:

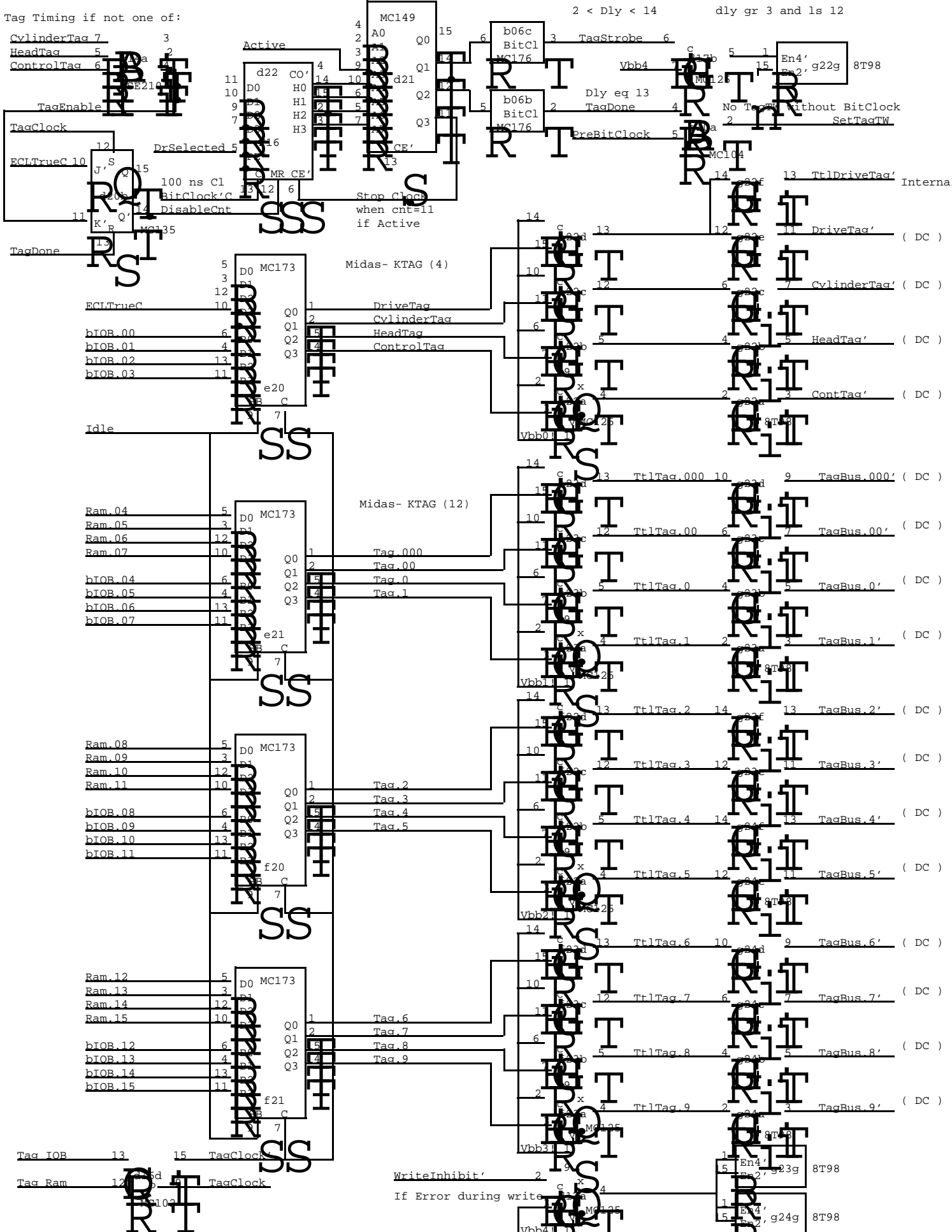
- 1 Fifo does not have a read word (Pg. 9)
- 2 Program has indicated it sent last word in block



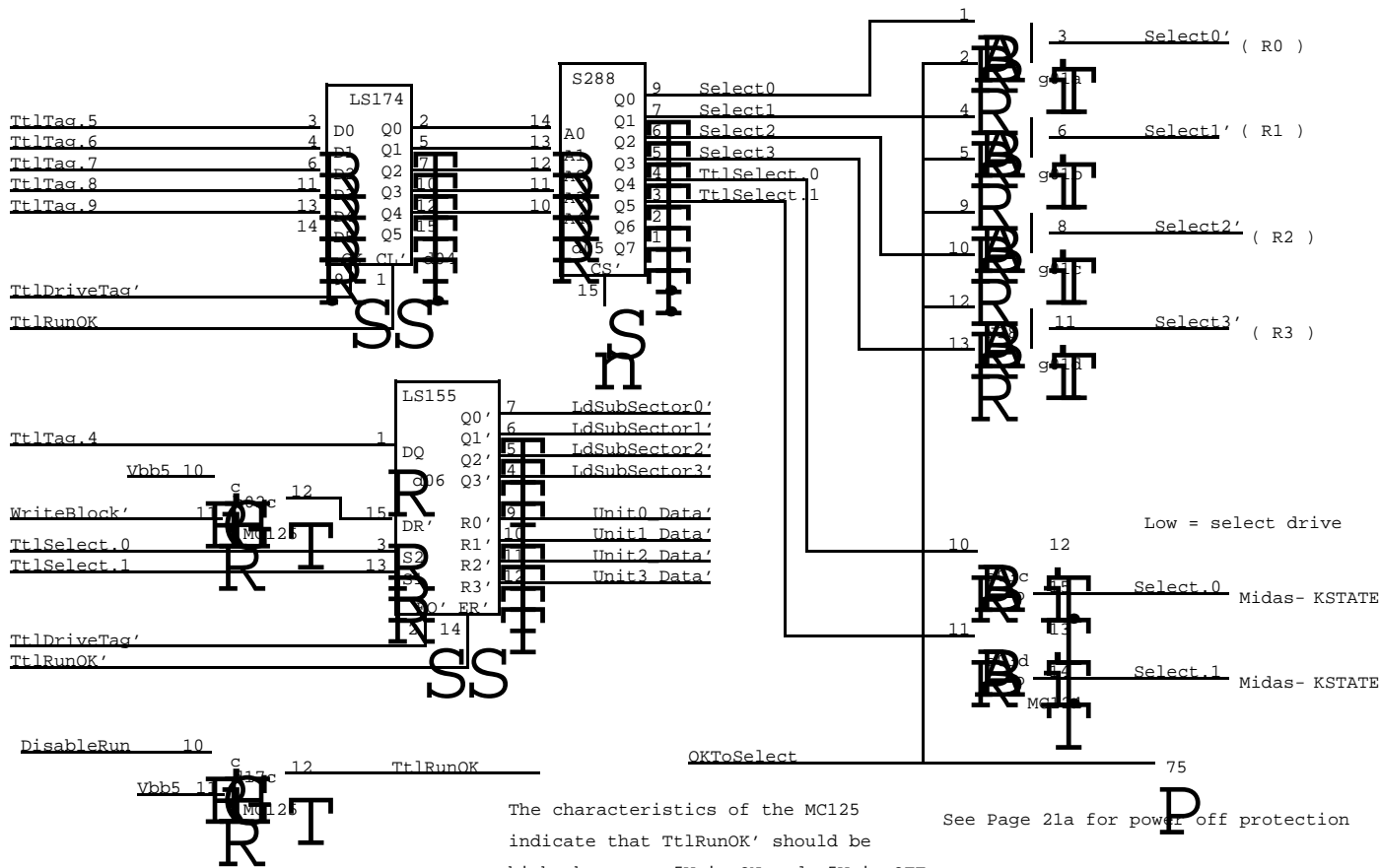


No Tag Timing if not one of:

2 < Dly < 14 dly gr 3 and ls 12

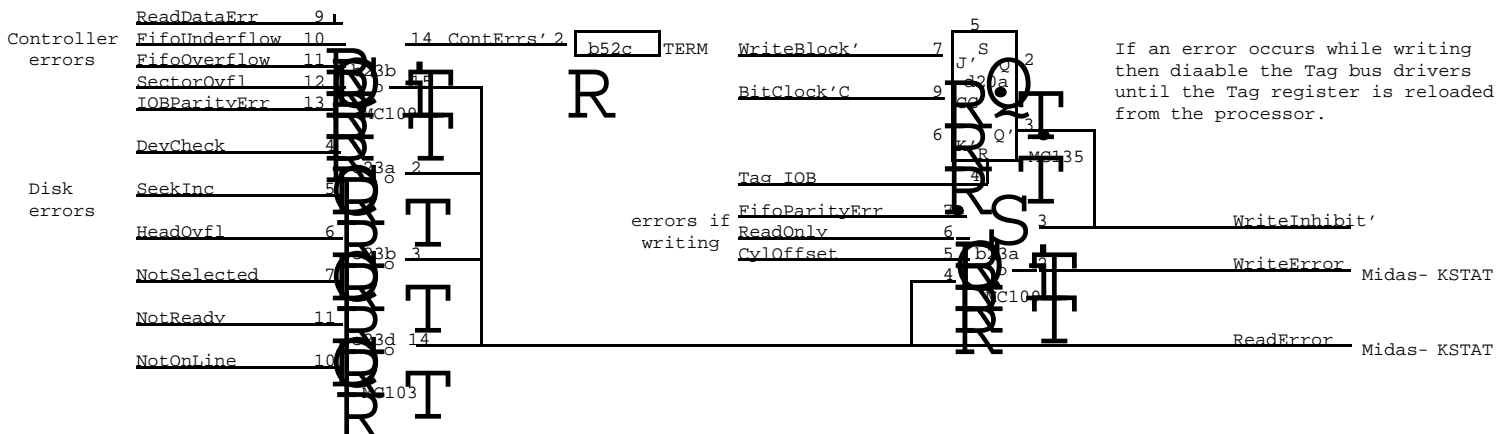
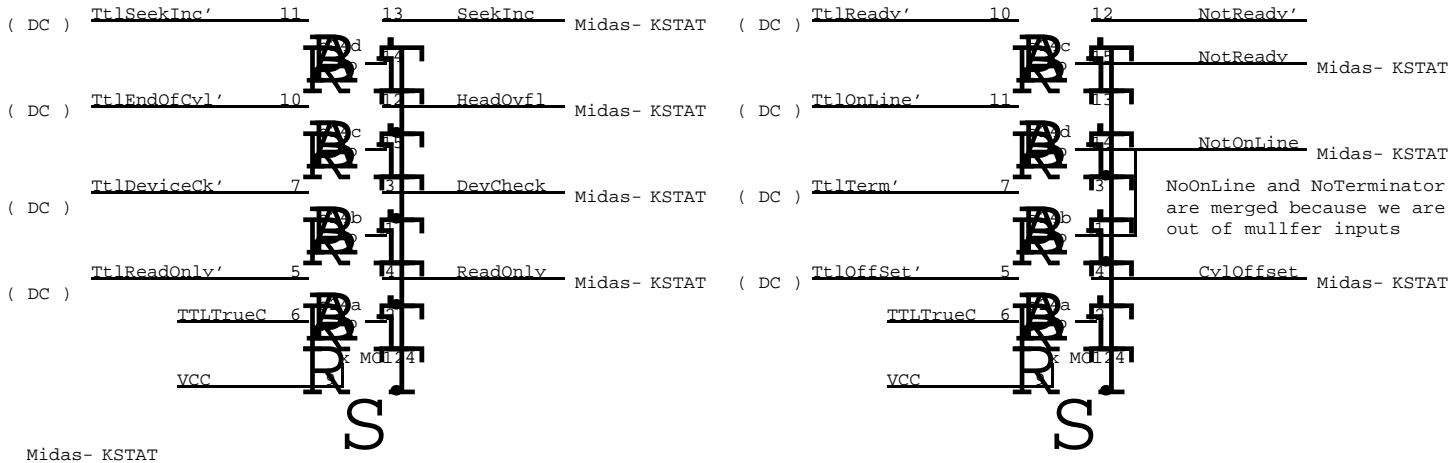


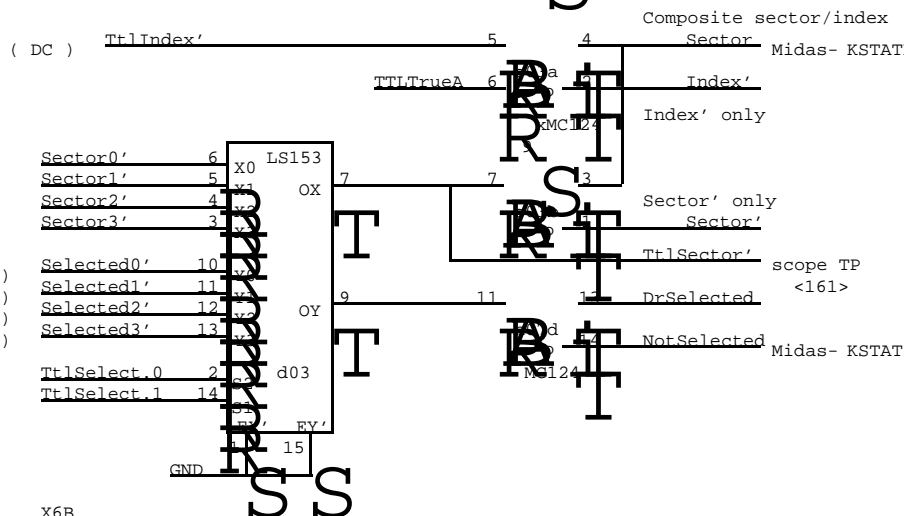
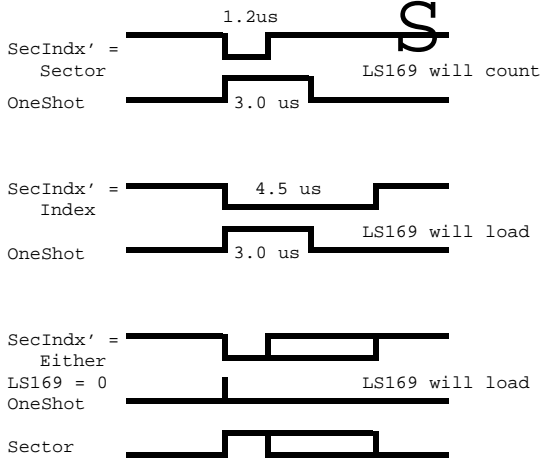
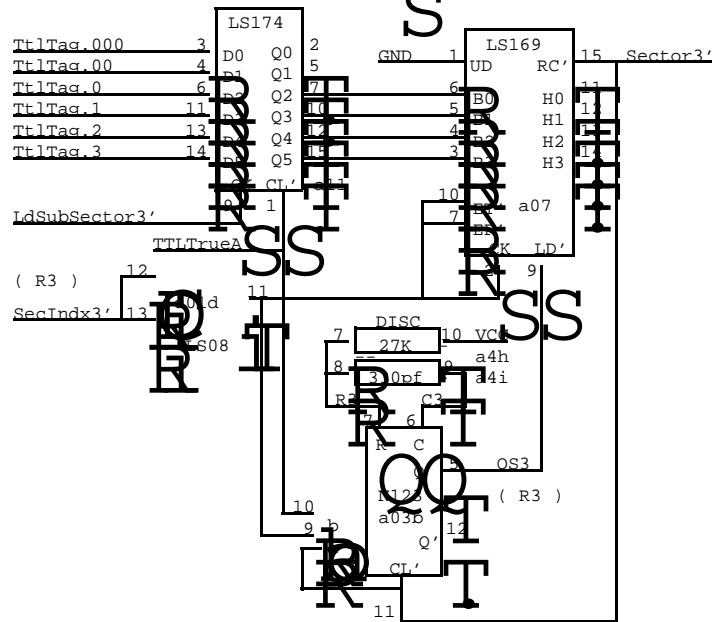
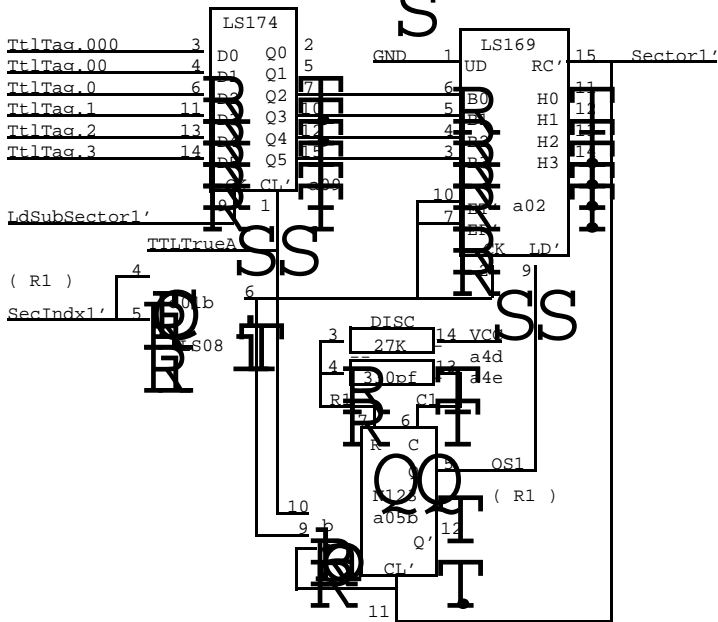
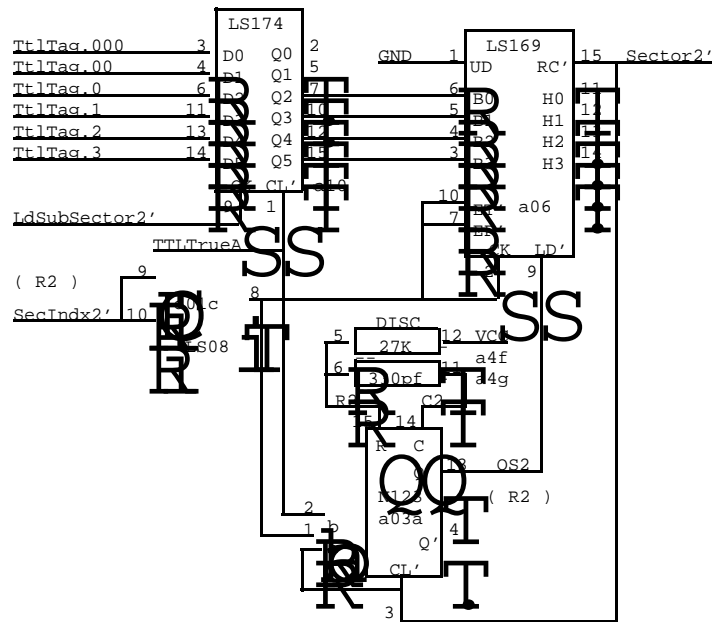
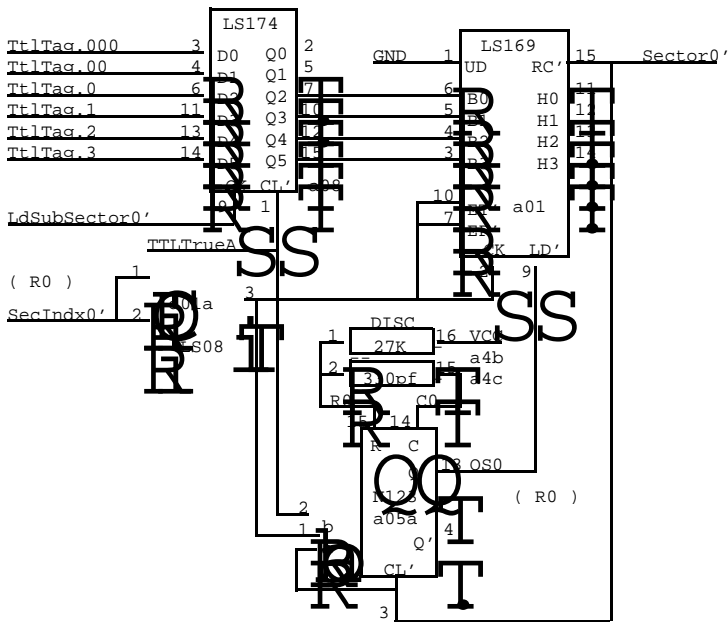
XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	Dorado	TAG register & Bus Drivers	TriconD04.si	Roger Bates	Da	7/23/79	10



The characteristics of the MC125 indicate that TtlRunOK' should be high whenever +5V is ON and -5V is OFF.

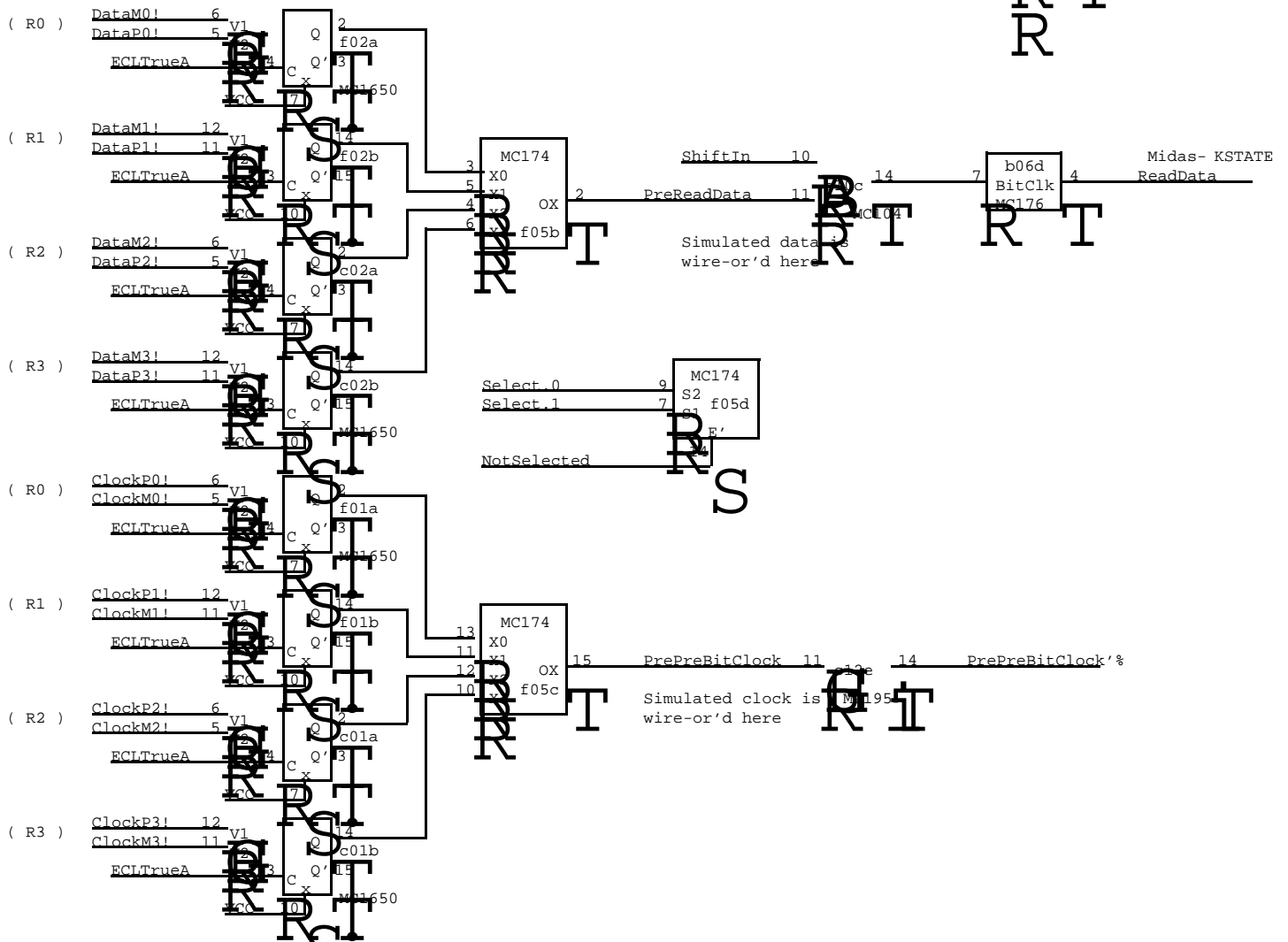
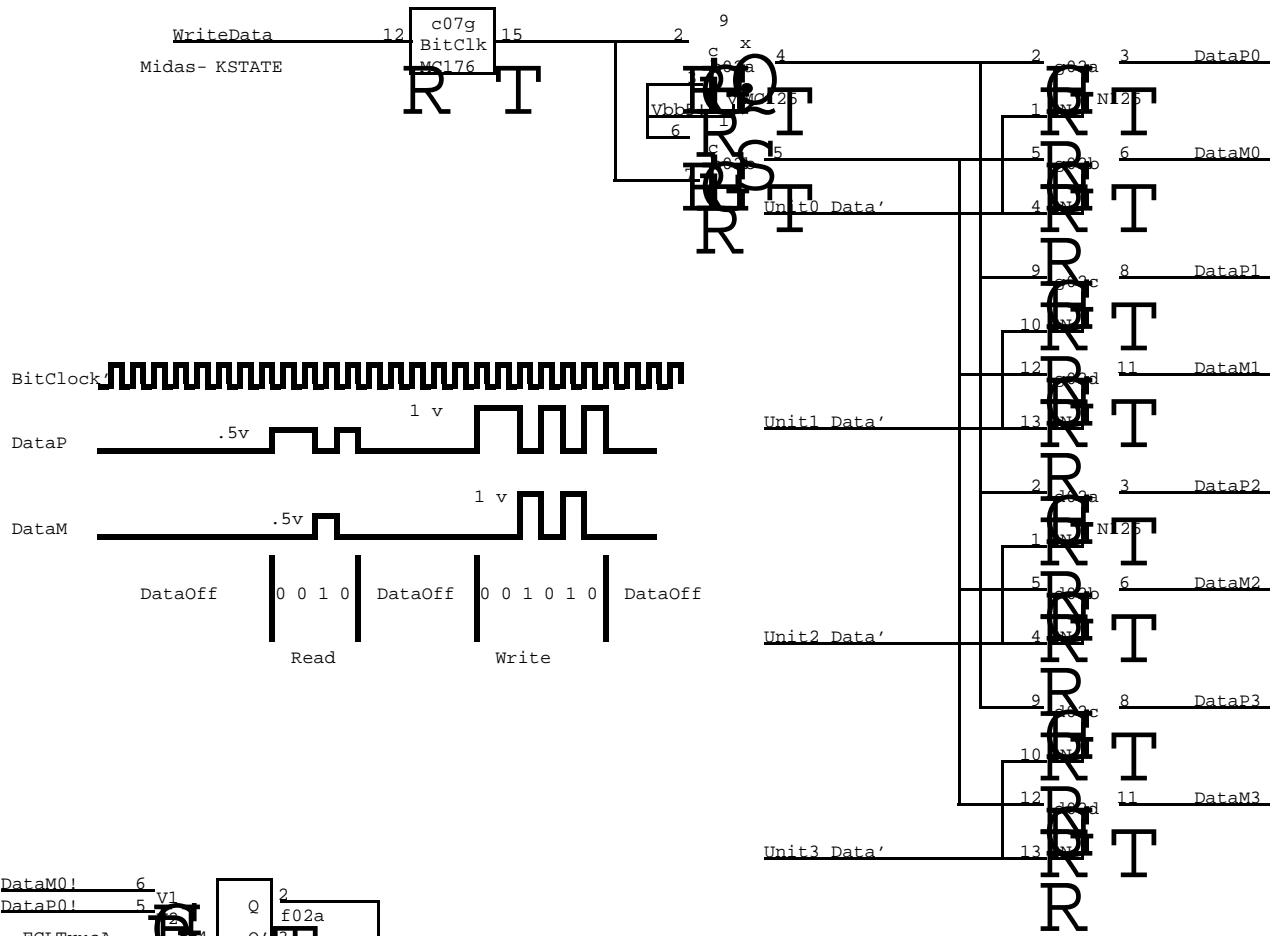
See Page 21a for power off protection

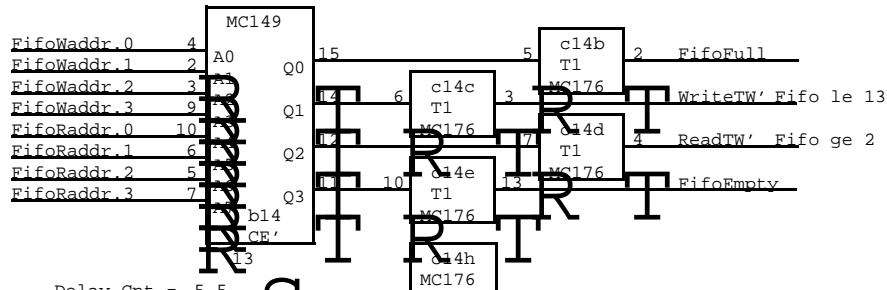
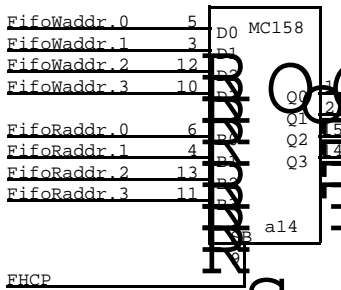




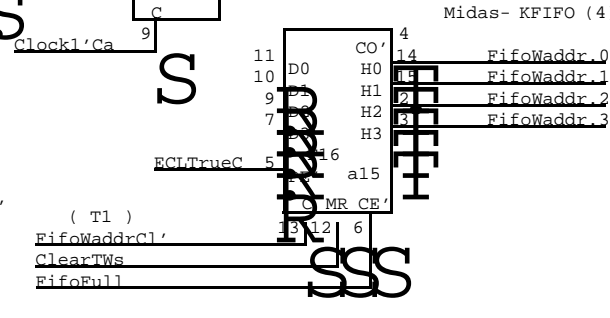
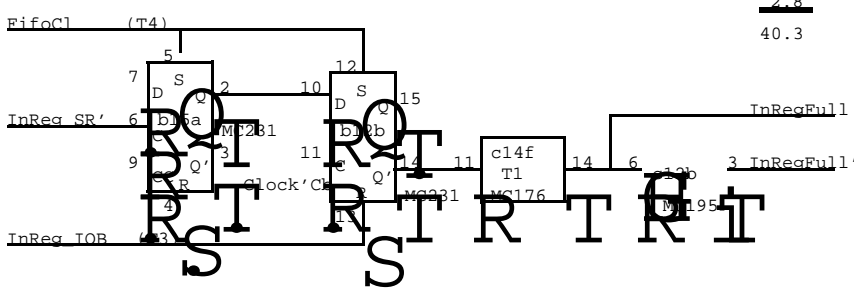
The above sector counters require the TRIDENT X6A disk to have its sector counters set to provide 4 - 11 117 "sub-sector" pulses per revolution. This is done by setting the disk jumpers as follows:

- X6B
- 2 - 13
- 3 - 12
- 4 - 11
- 5 - 10
- 6 - 09

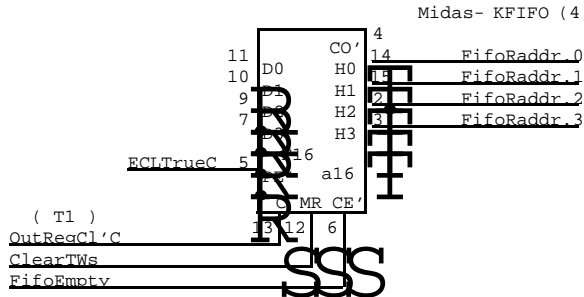
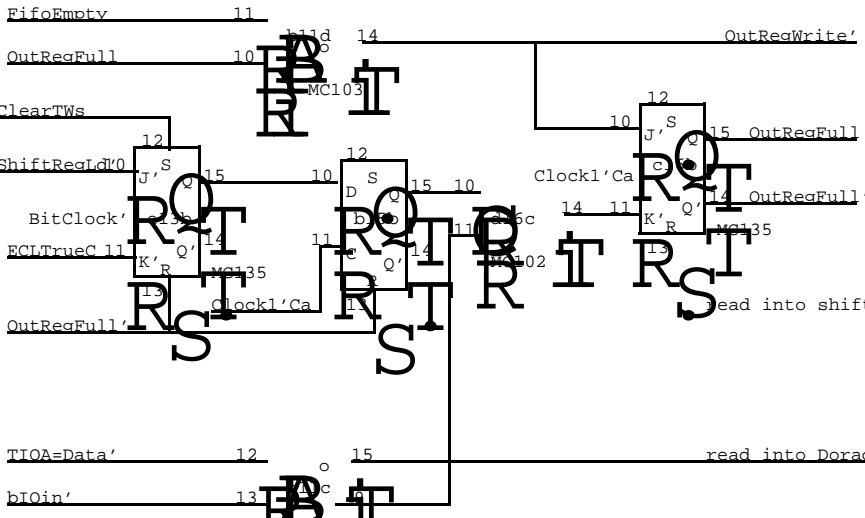
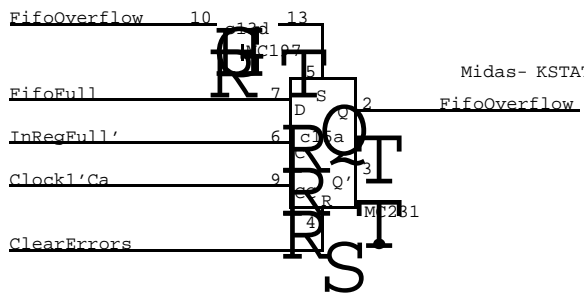
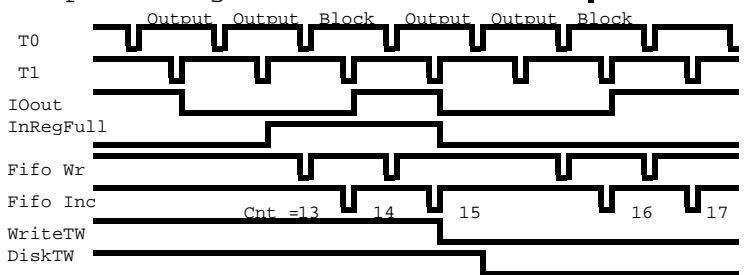




Delay Cnt = 5.5
32
2.8
40.3

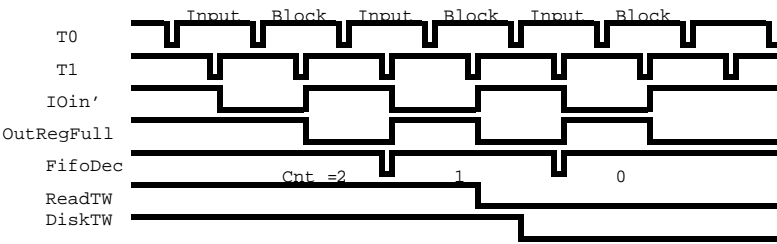


Output timing

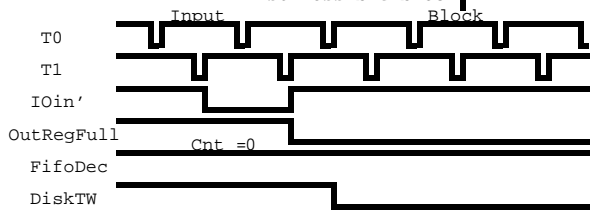


Input timing

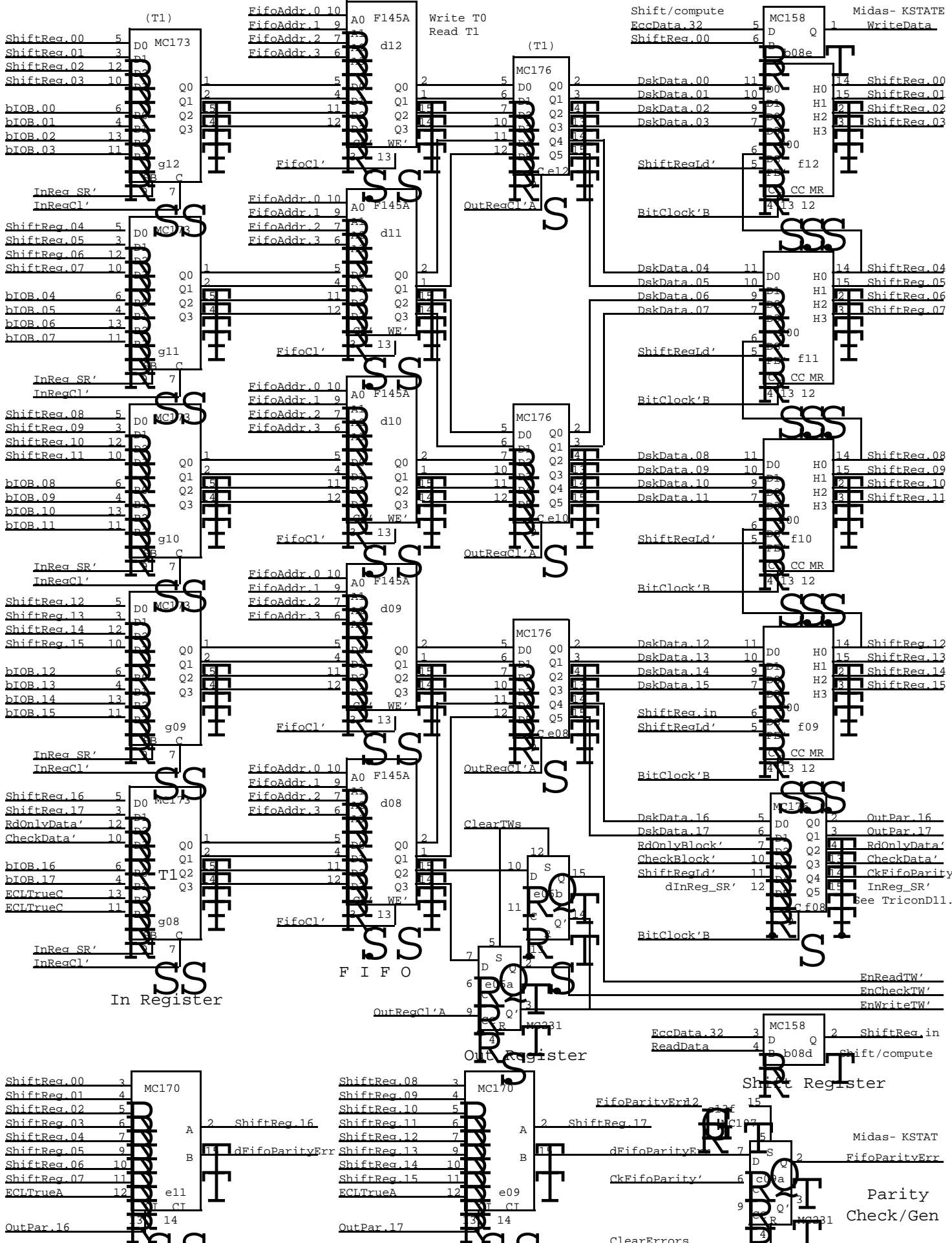
"Read"



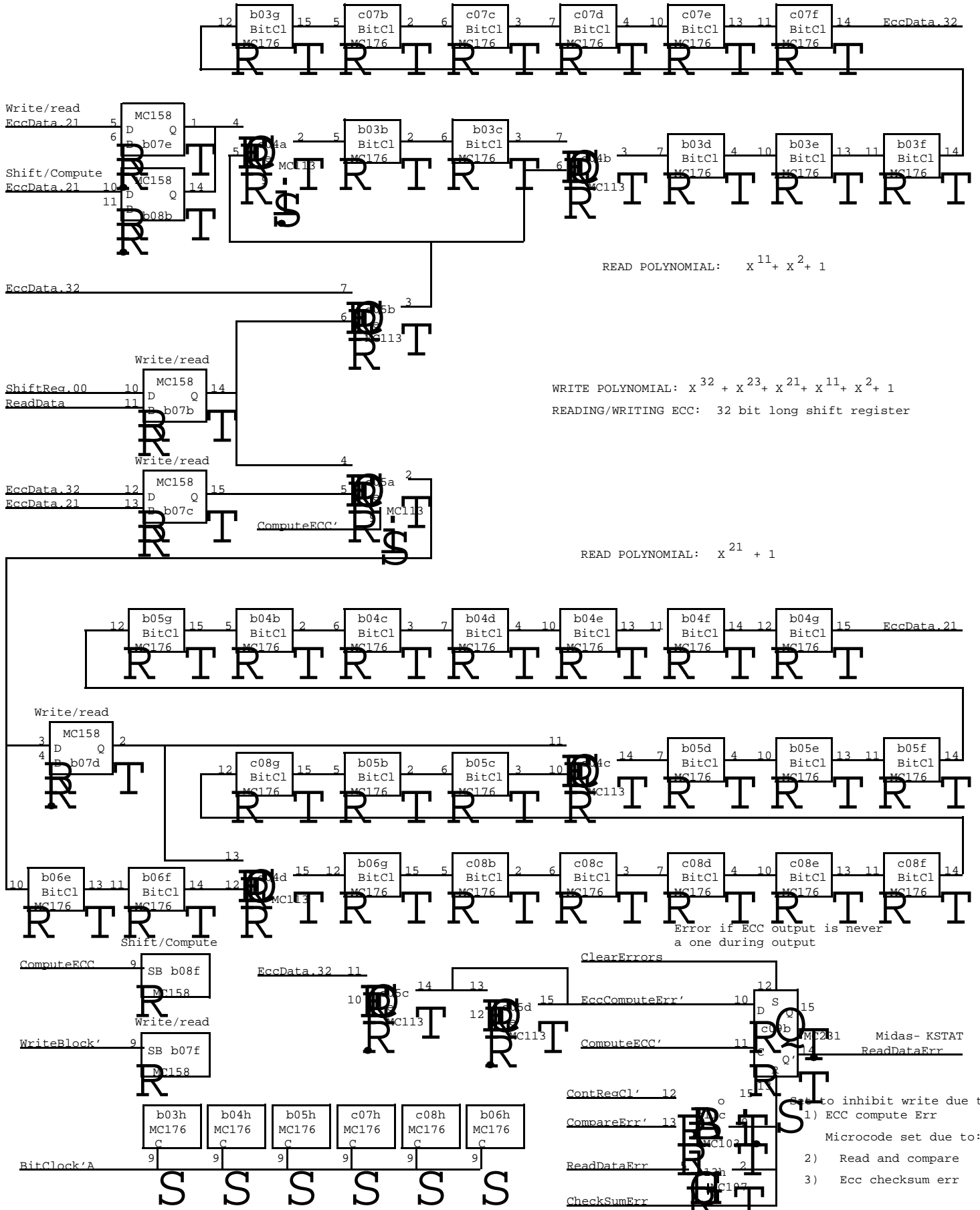
"Compare"

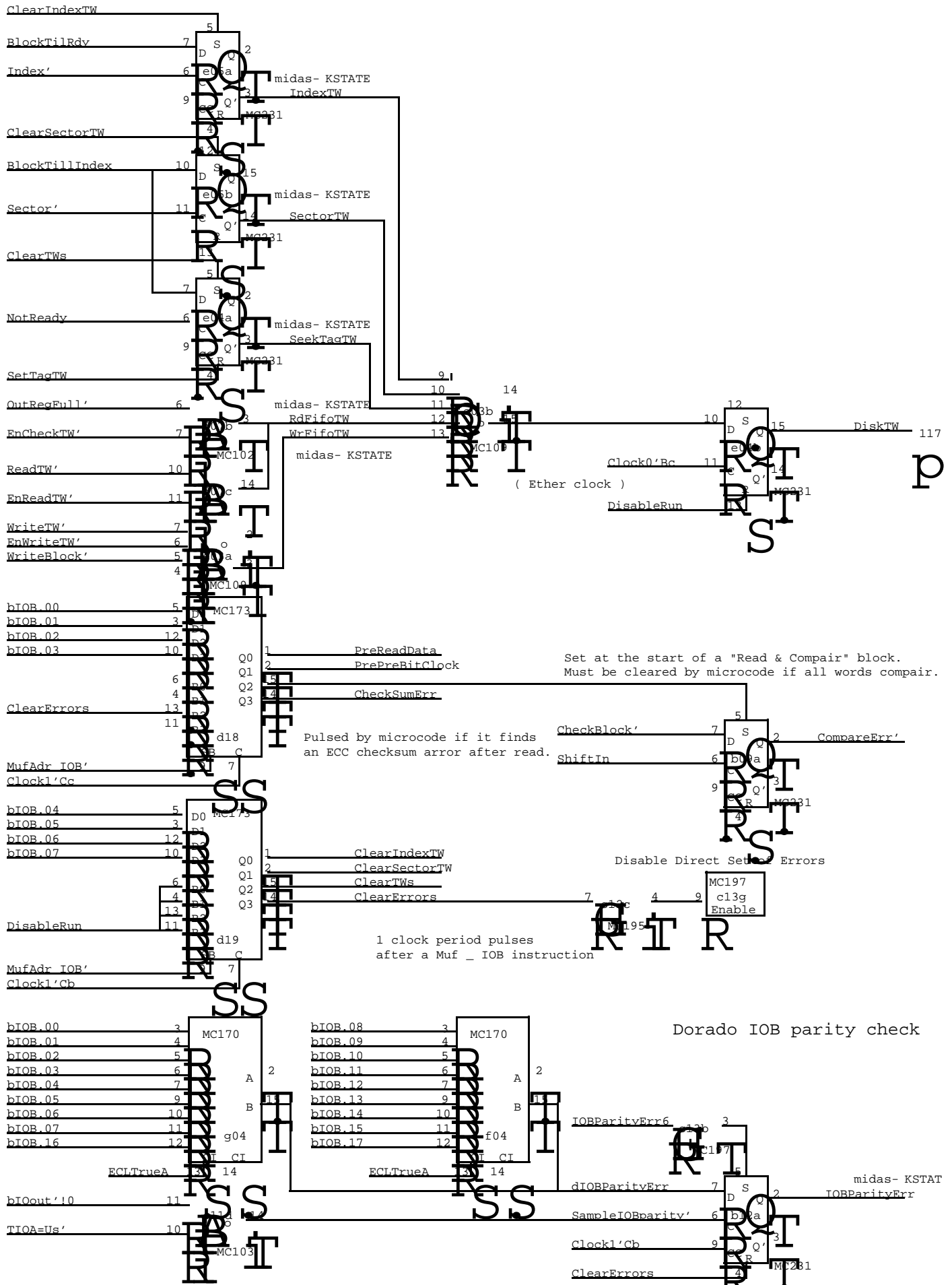


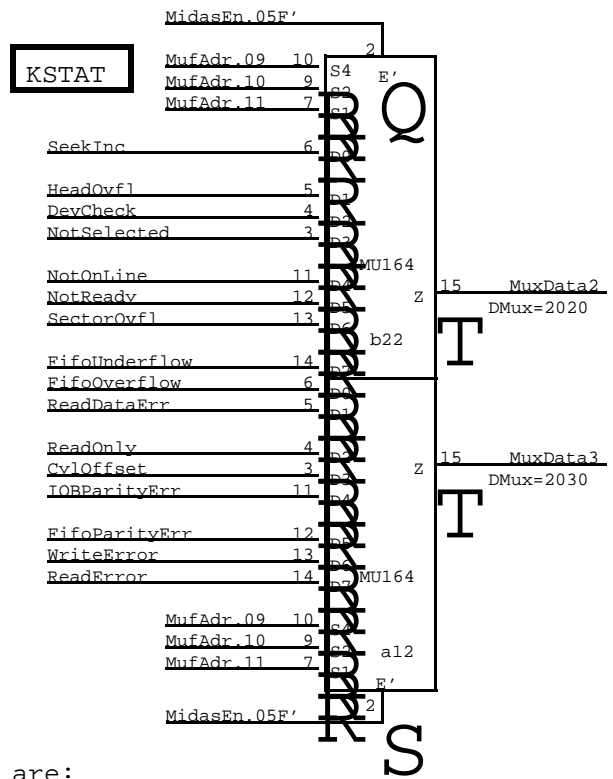
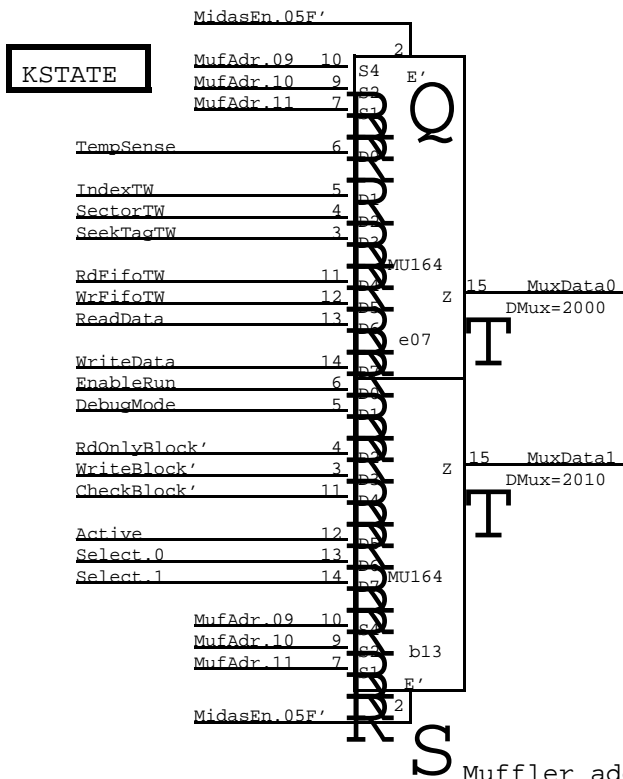
XEROX PARC	Project Dorado	Drawing F I F O Control	File TriconD08.si	Designer Roger Bates	Rev Da	Date 9/24/79	Page 14
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POLYNOMIAL DIVIDER FOR FIRE CODE GENERATION



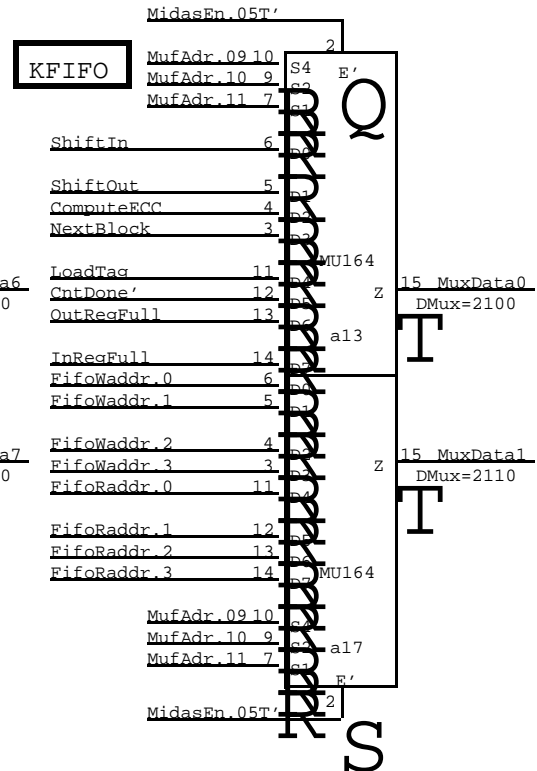
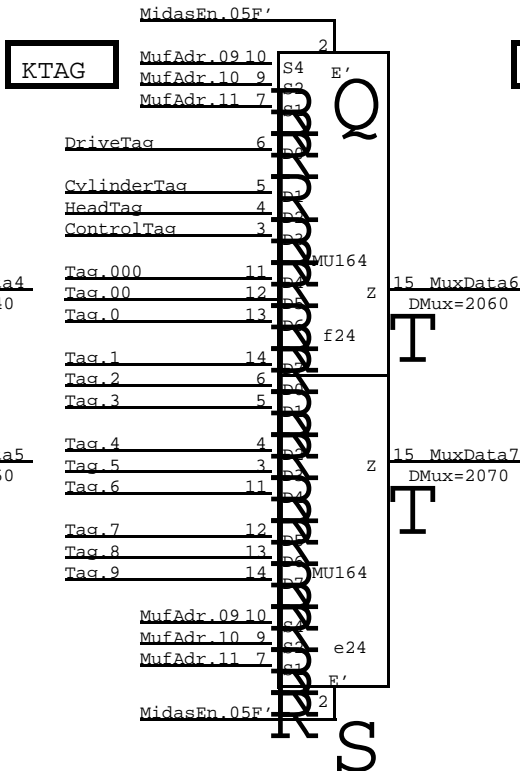
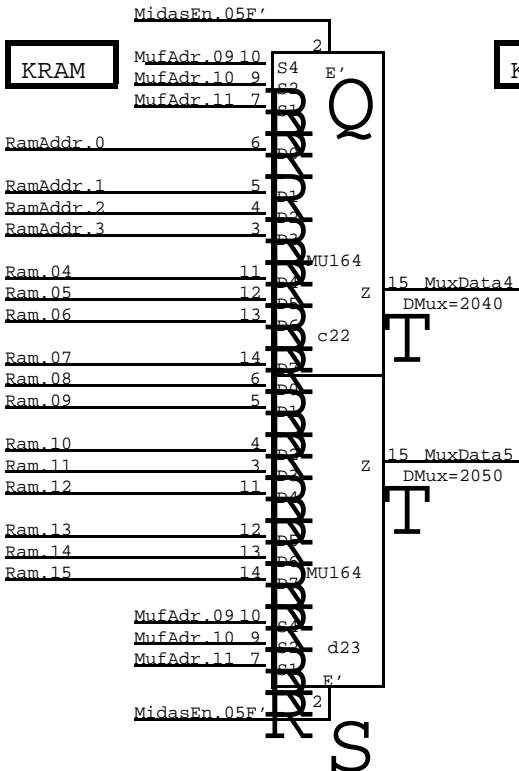


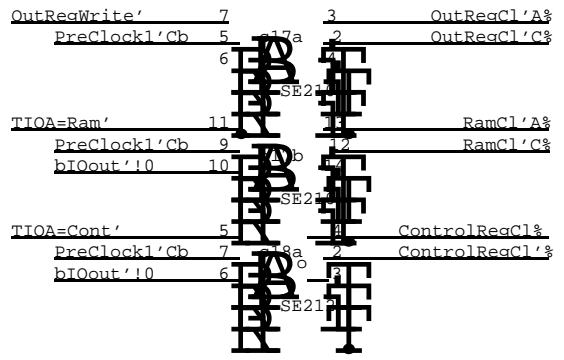
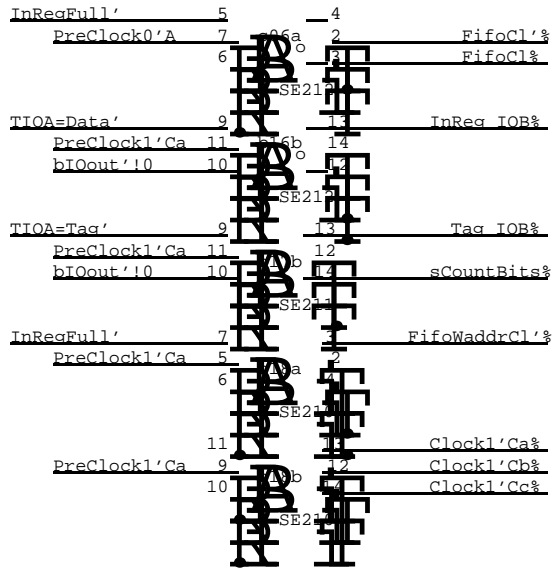
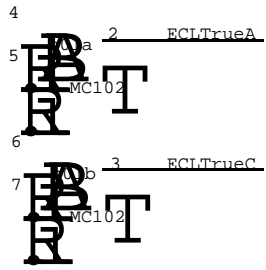


Muffler addresses are:

Value listed for Program input
Value plus 2000 for Midas input

Values from 120 to 177 are
used by the Ethernet

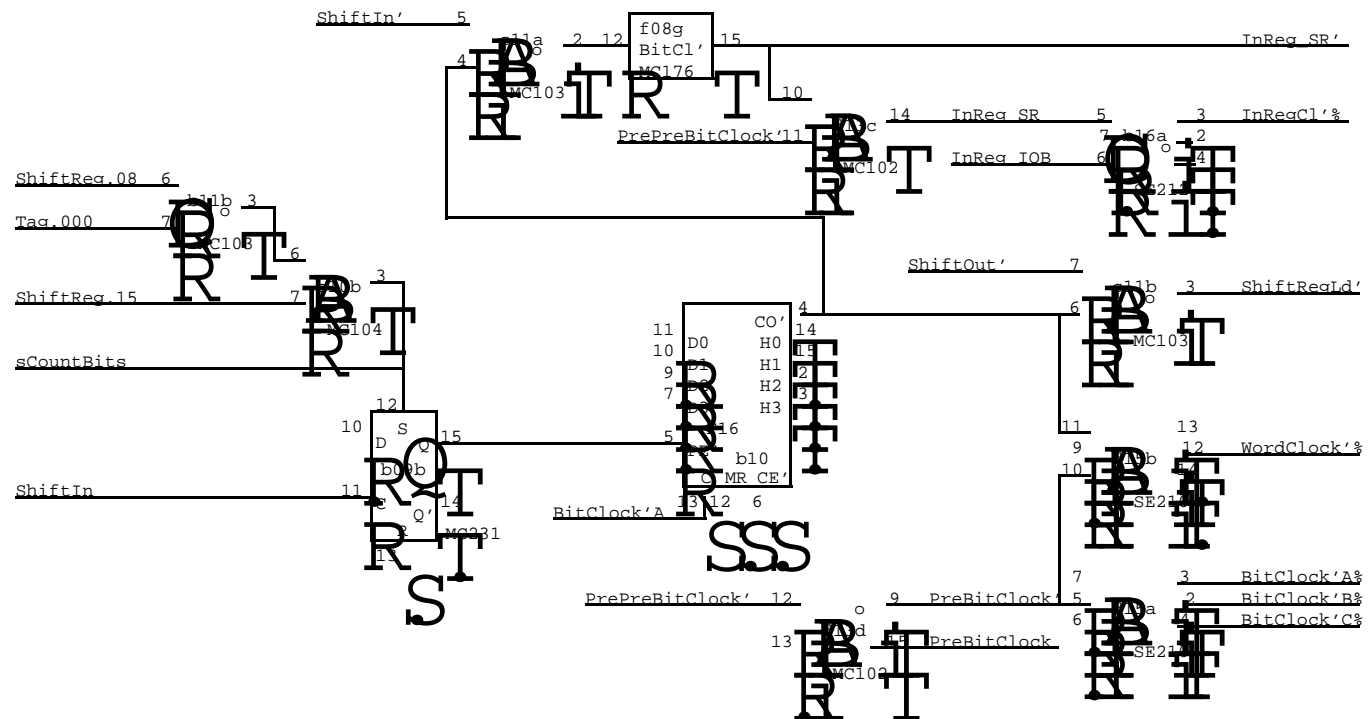




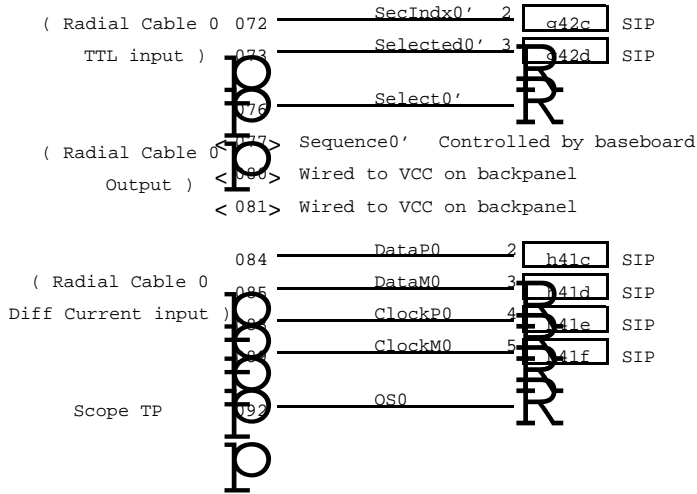
System Clocks

Disk Clocks

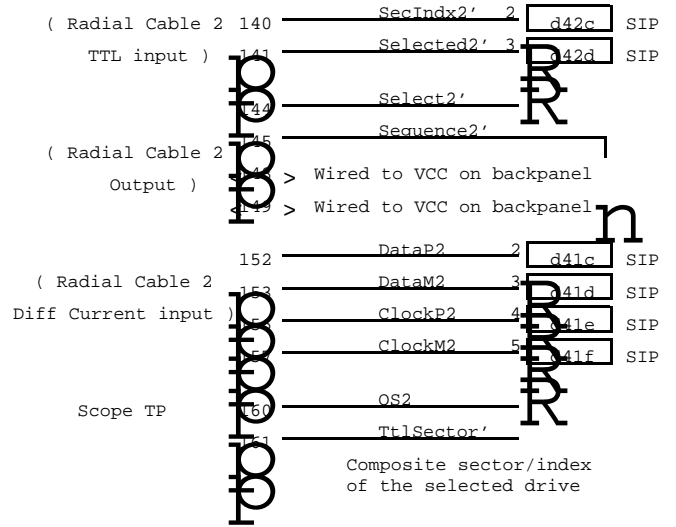
Delay reading of shift register
by 1 bit for correct bit alignment



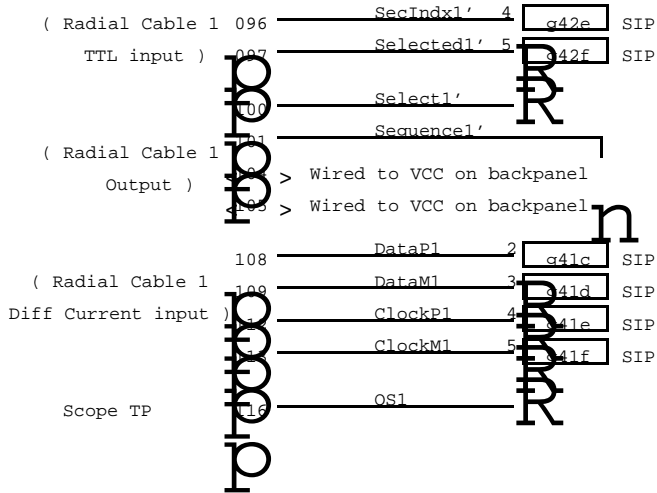
Radial Cable for Drive 0



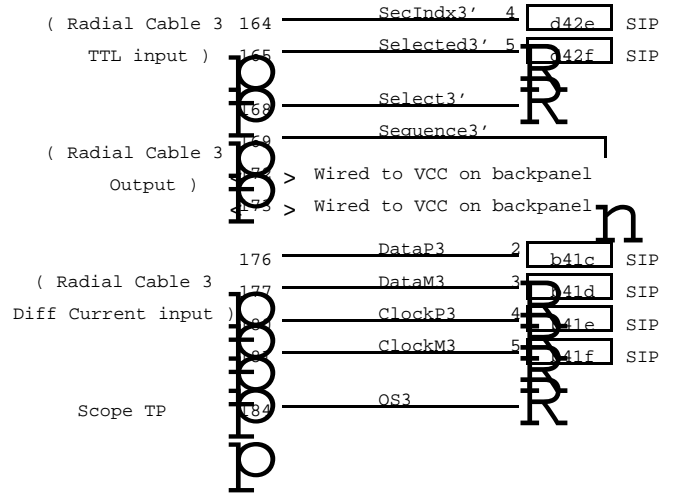
Radial Cable for Drive 2



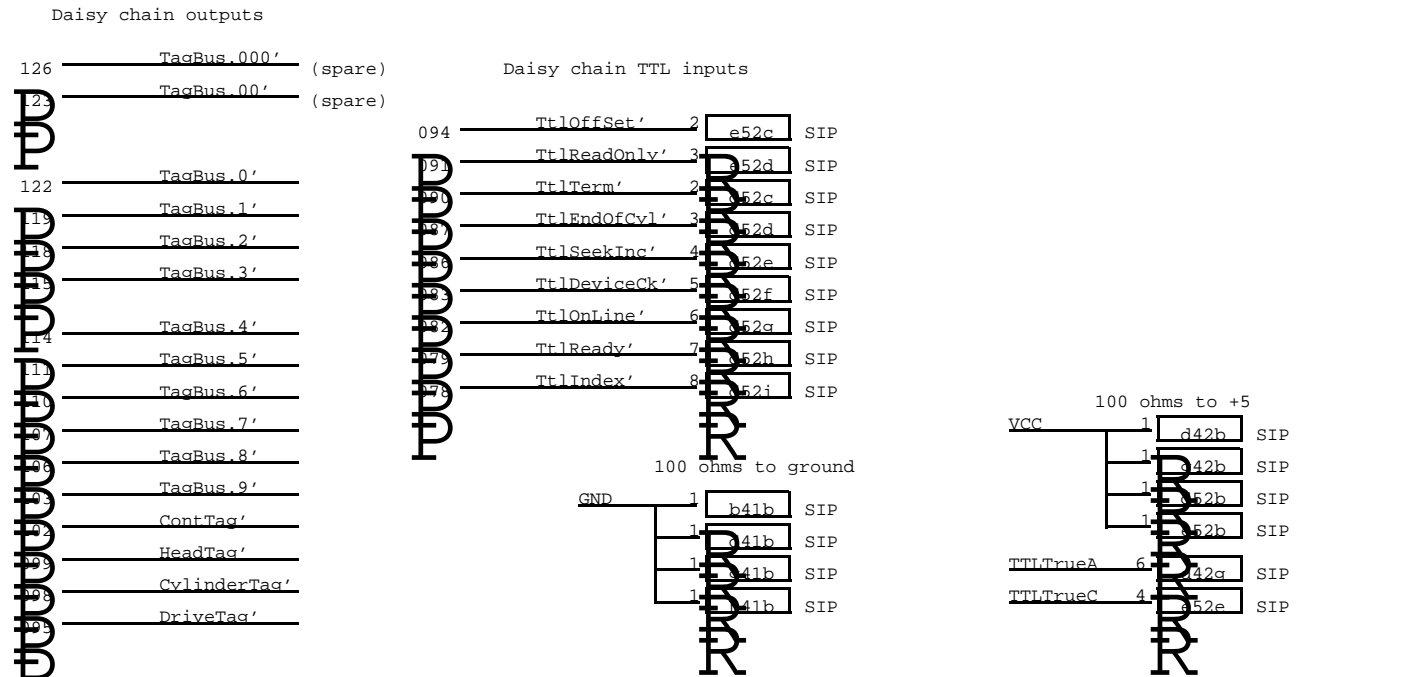
Radial Cable for Drive 1



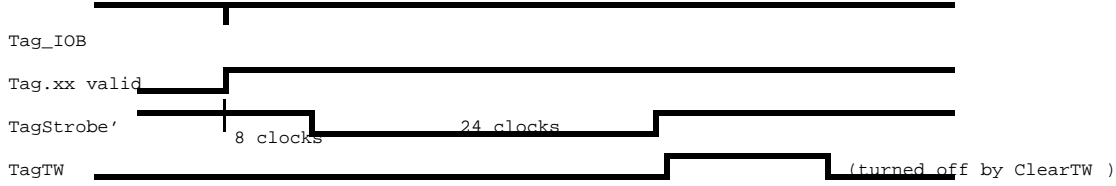
Radial Cable for Drive 3



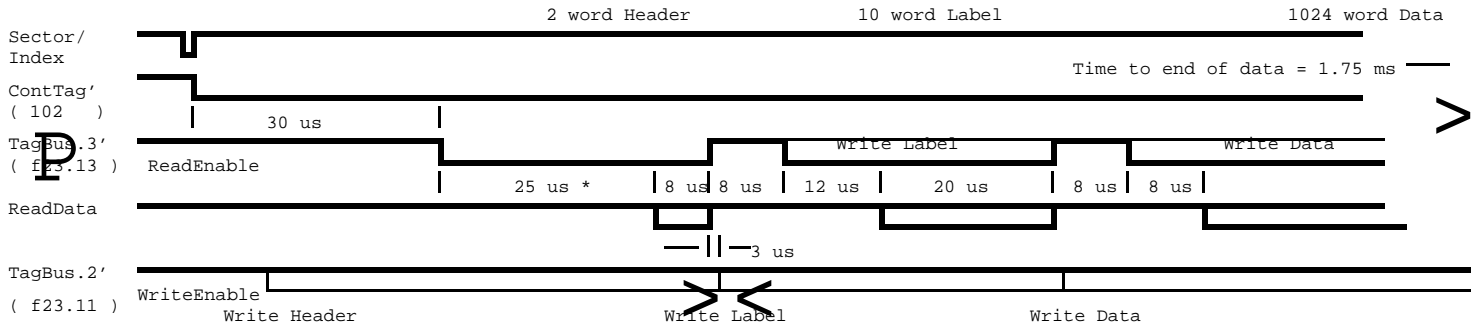
Daisy Chain Cable



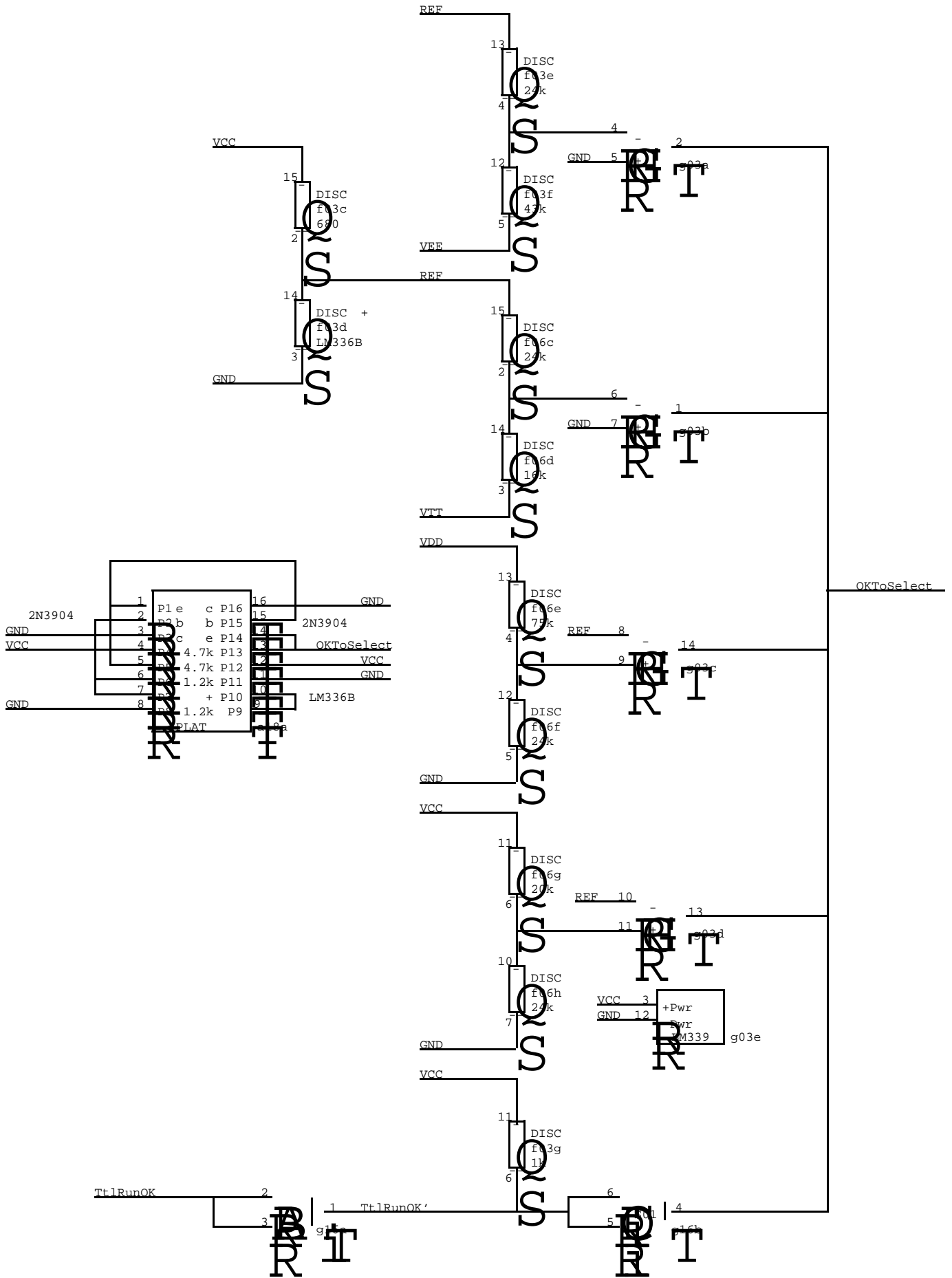
Head or Cylinder Tag Instruction



Read or Write Instruction



* This value is for reading a pack on the same drive that Headers were written. It may vary by +/- 15 us on other drives.

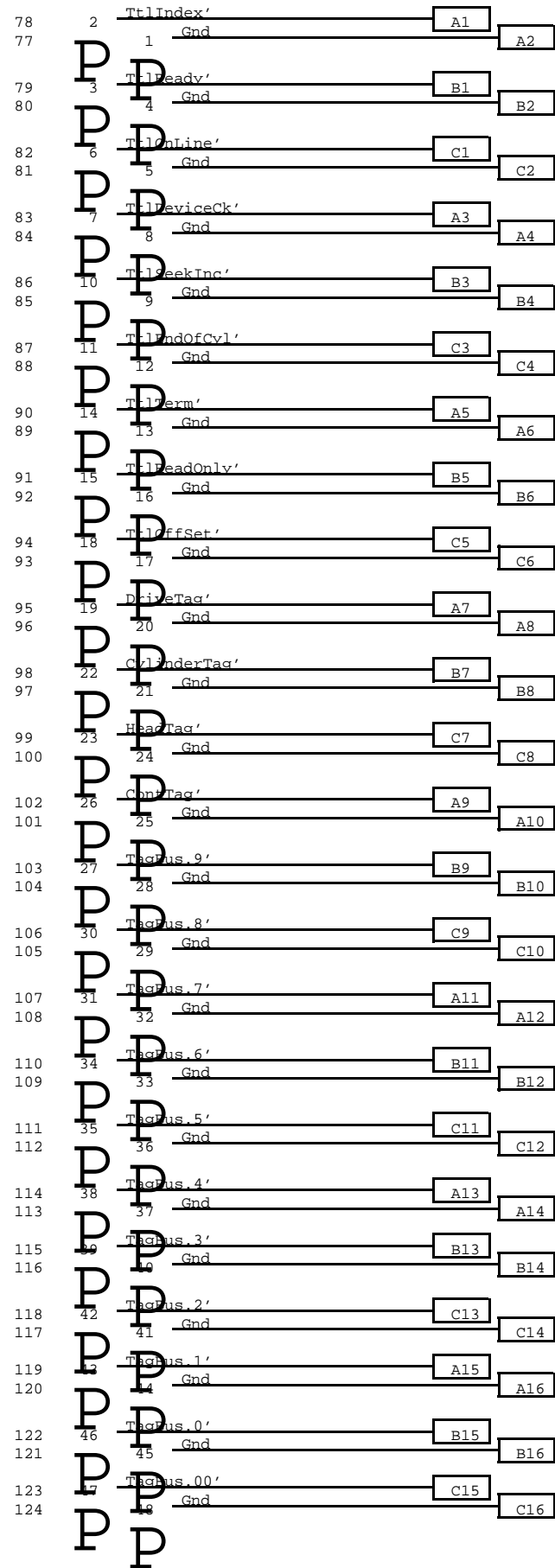
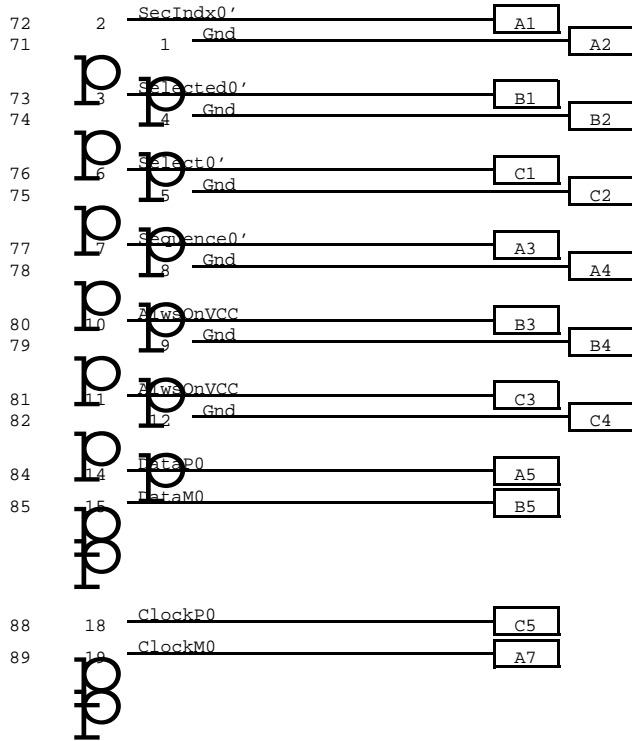


Radial Cable for Drive 0

DAISEY CHAIN CABLE

AMP 204733-1

AMP 204729-1



Radial Cable for Drive 0

DAISEY CHAIN CABLE

AMP 204746-1

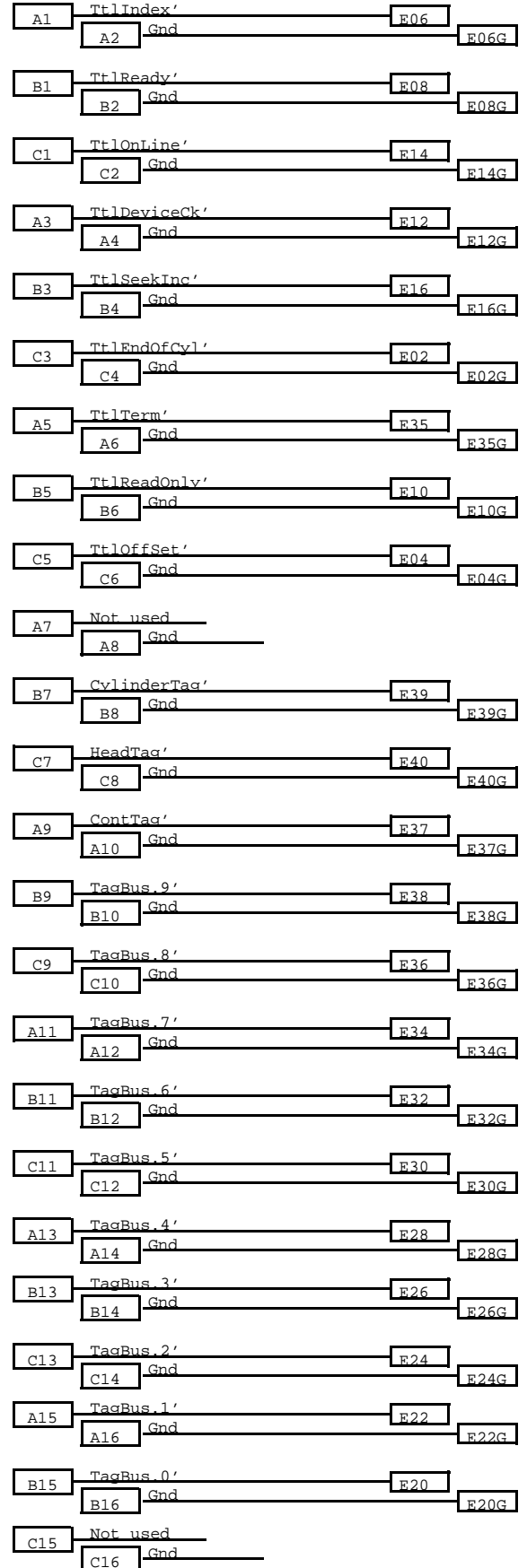
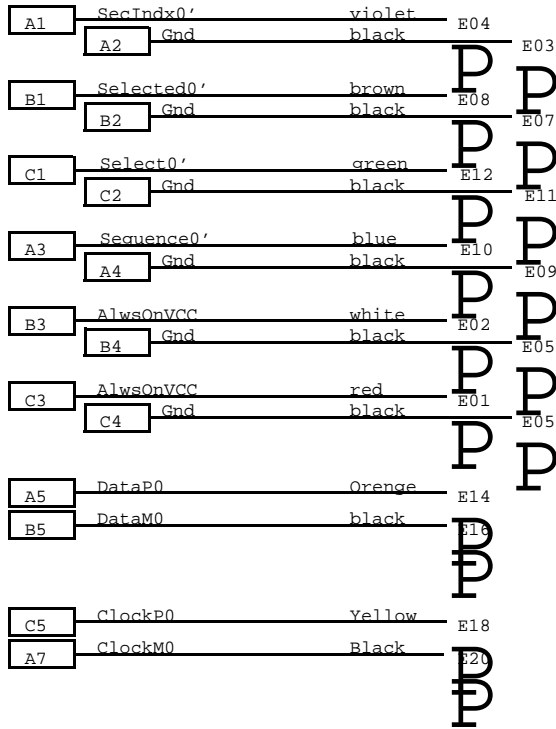
Cal-Comp

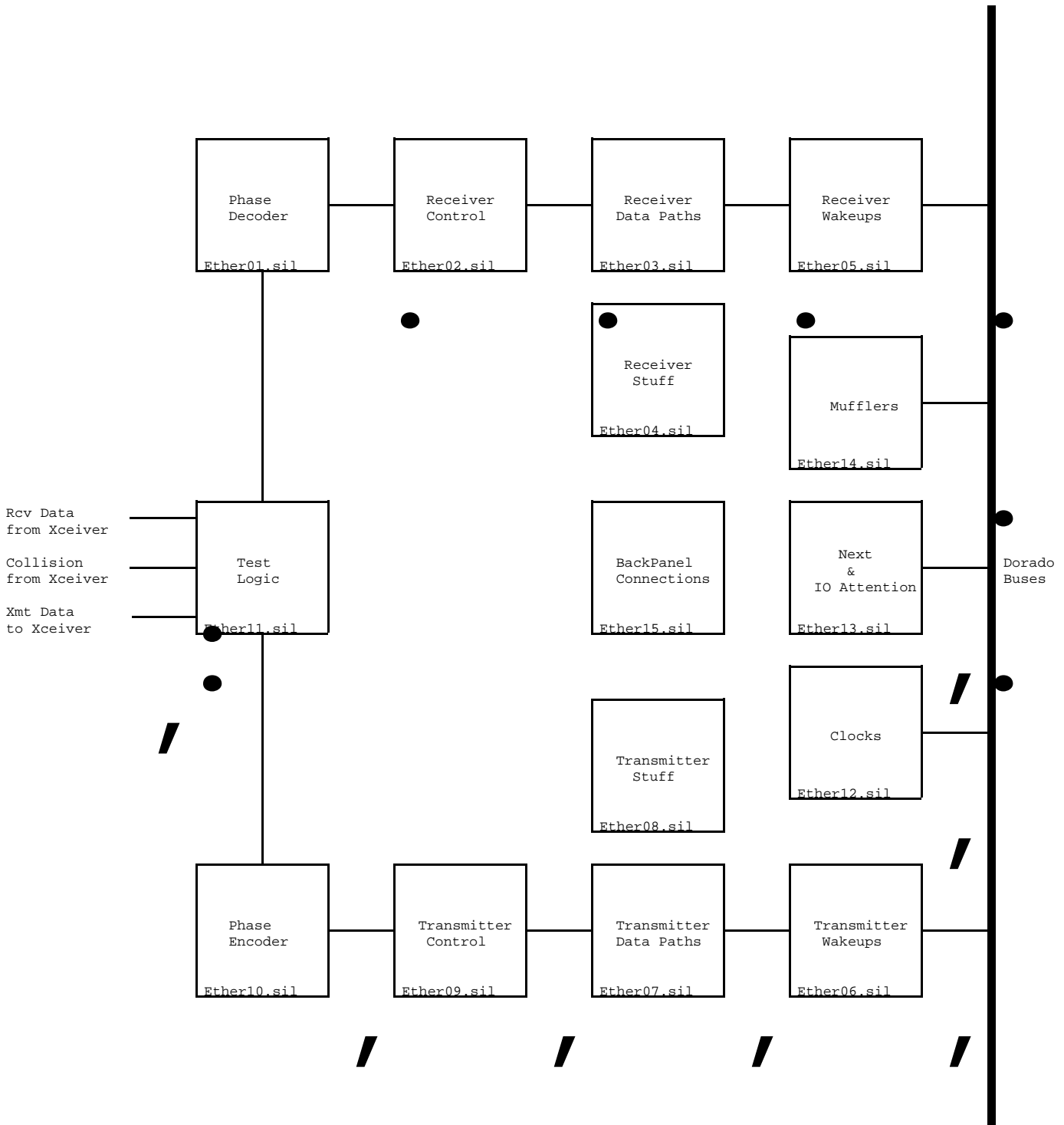
Assembly 12424

Cal-Comp

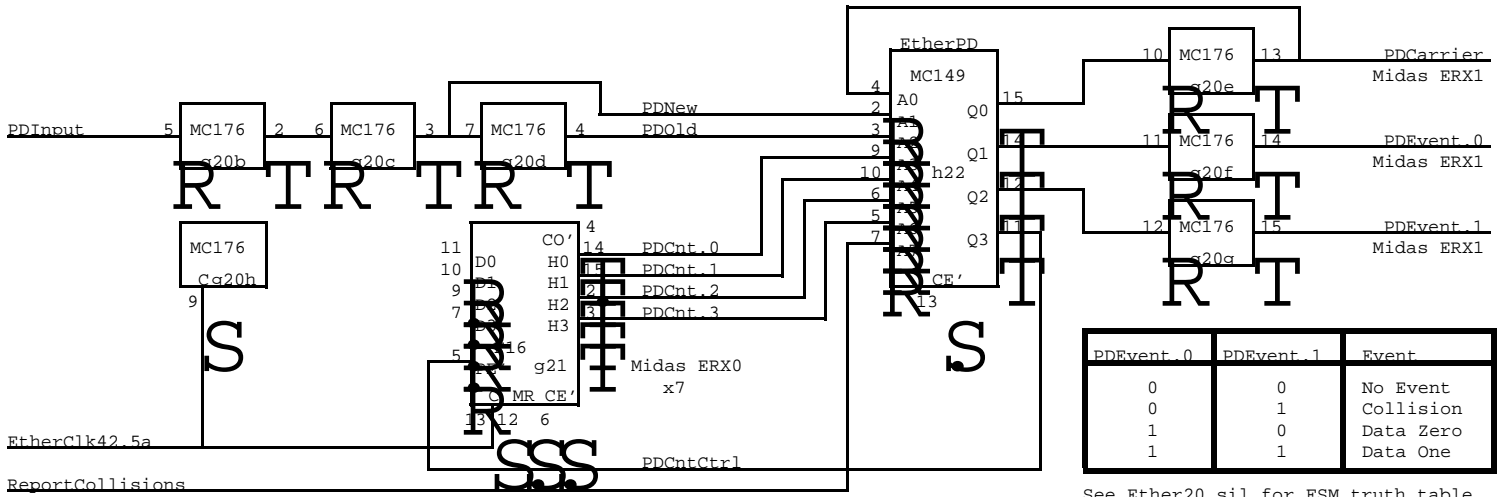
AMP 204742-1

Assembly 12433

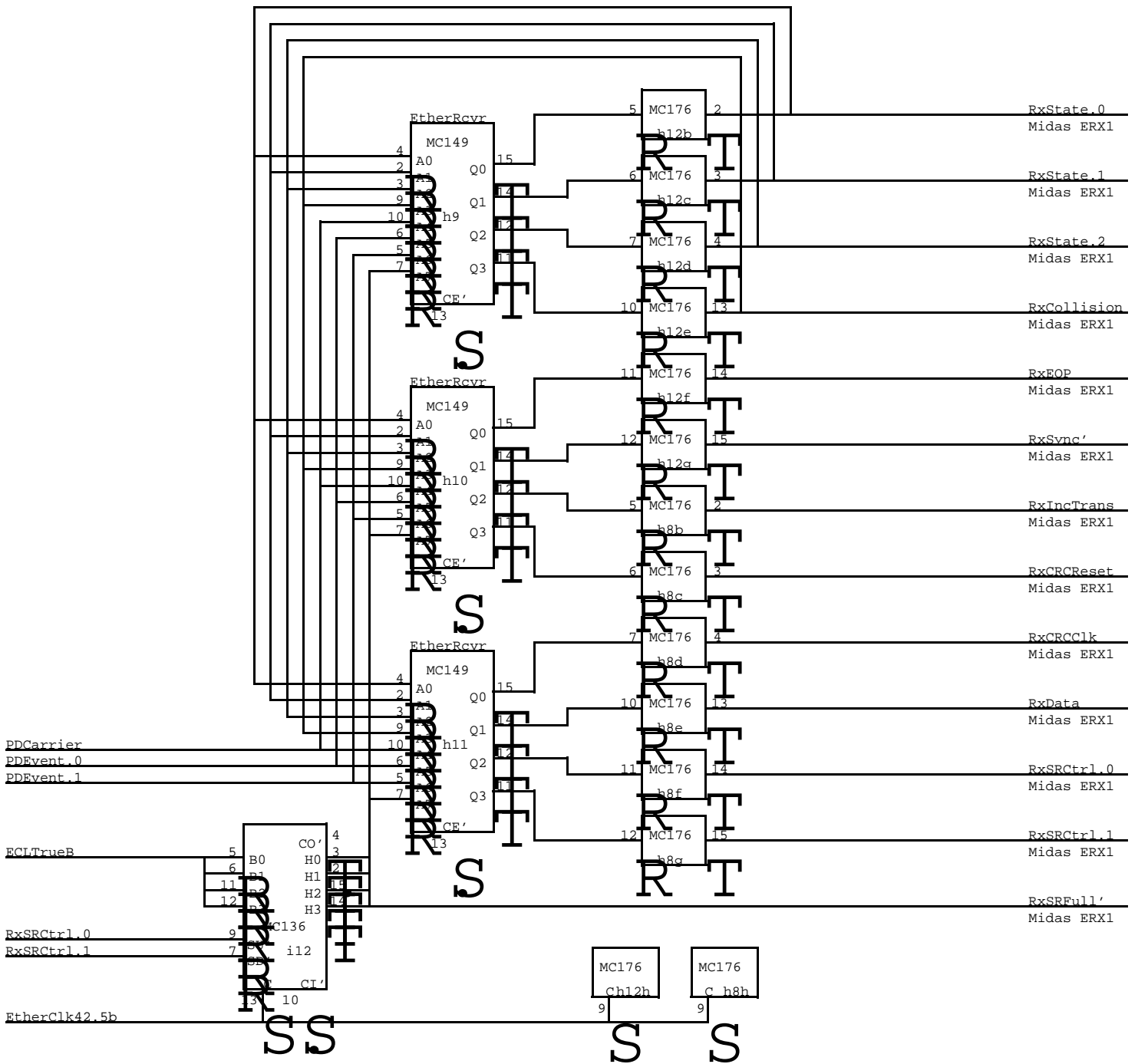




See DskEth*.sil for IOA, IOB, Muffler Control and Board Clocks



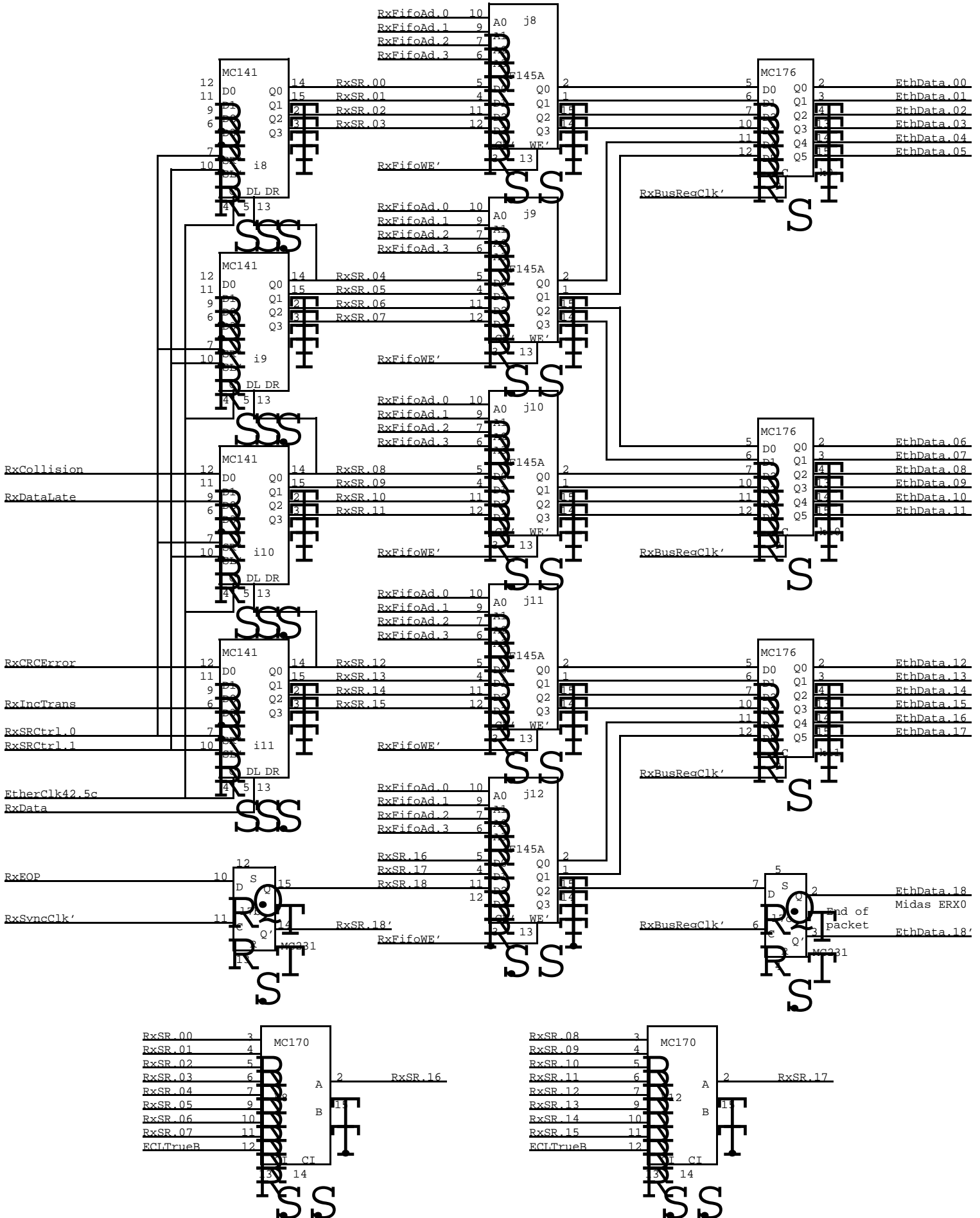
See Ether20.sil for FSM truth table

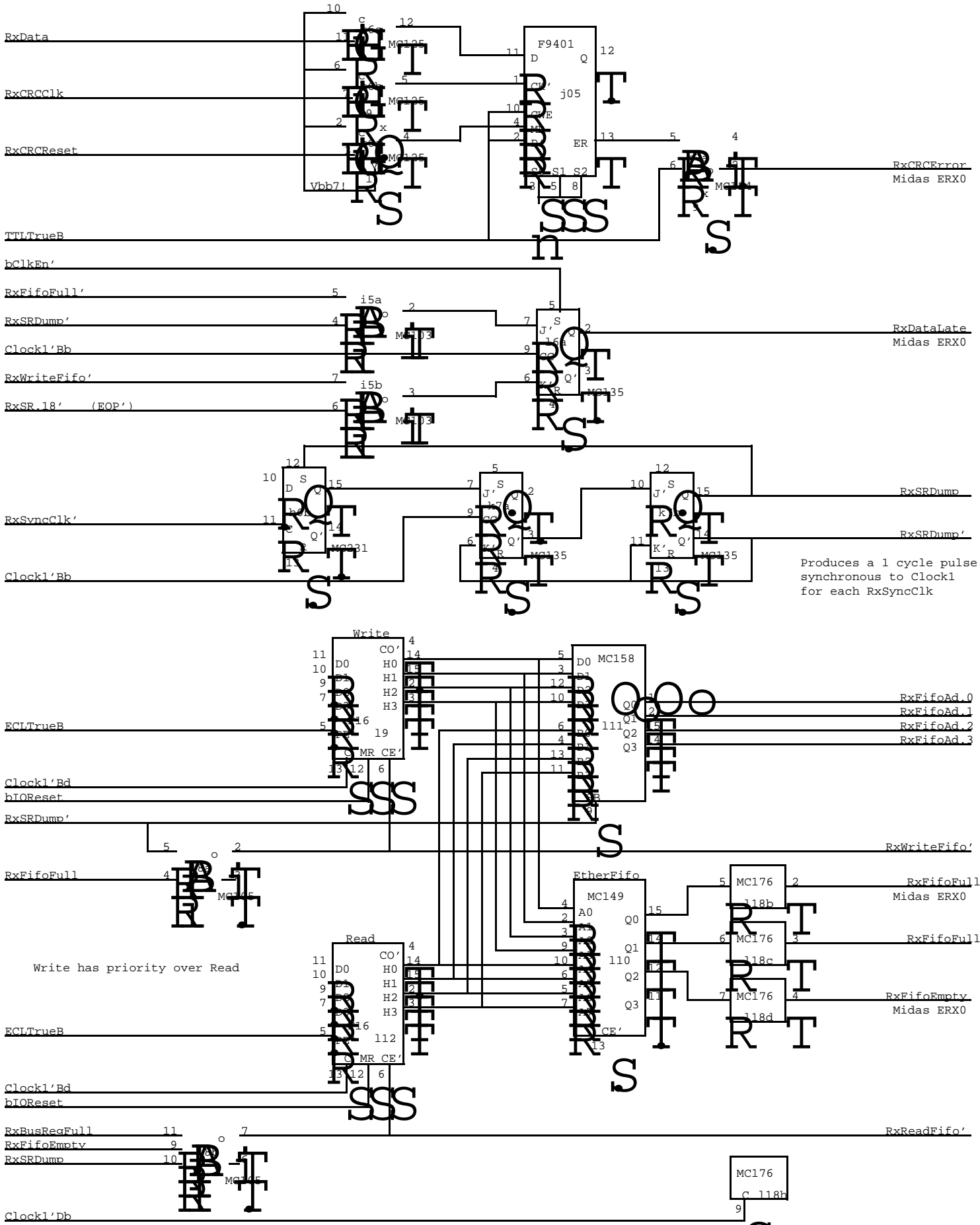


See Ether18.sil for timing diagrams

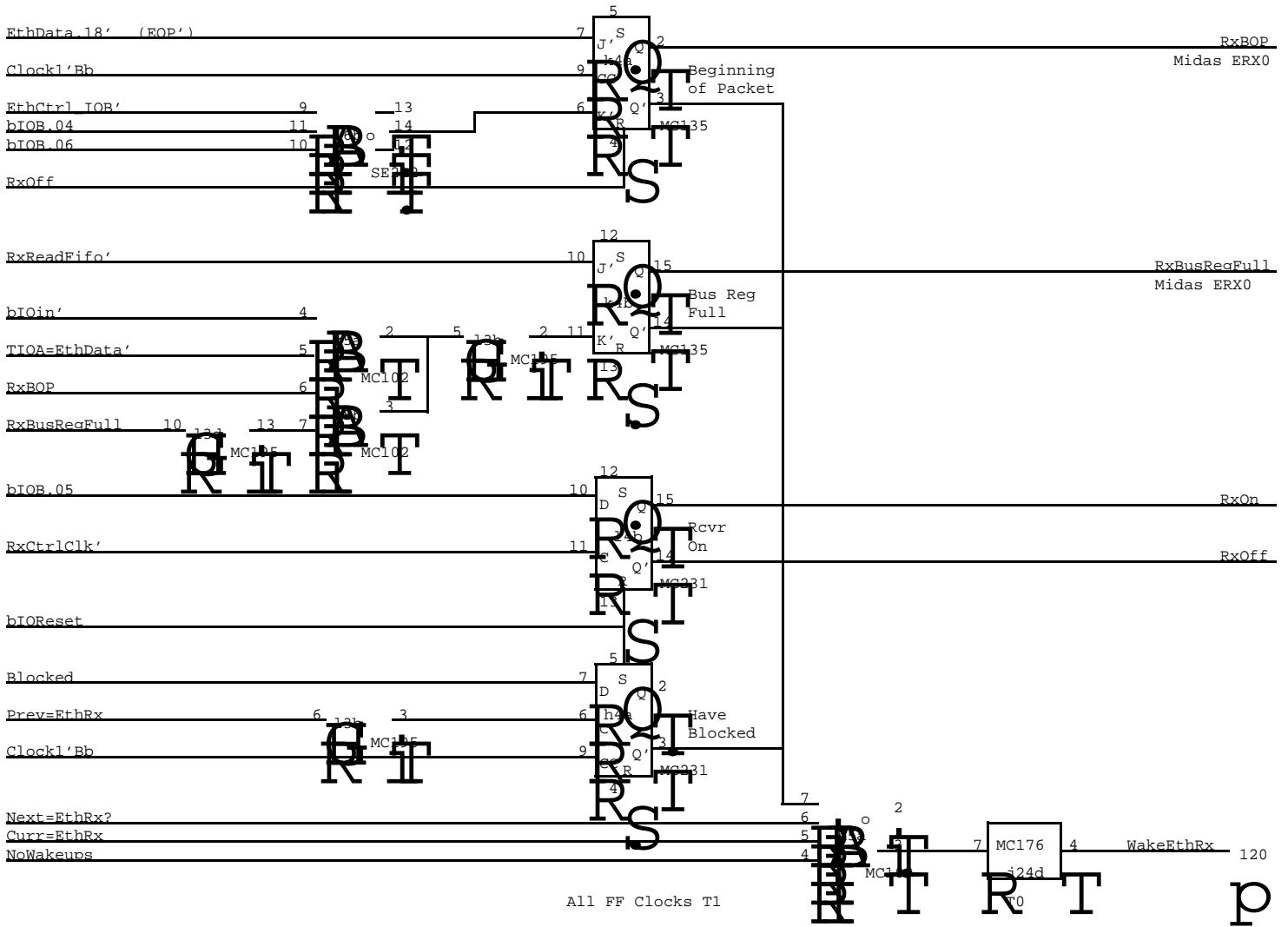
The slowest Dorado clock speed at which the receiver works is 85 ns (T0 to T1)

XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	Dorado	Receiver Control	Ether02.sil	David Boggs	Da	9/24/79	26



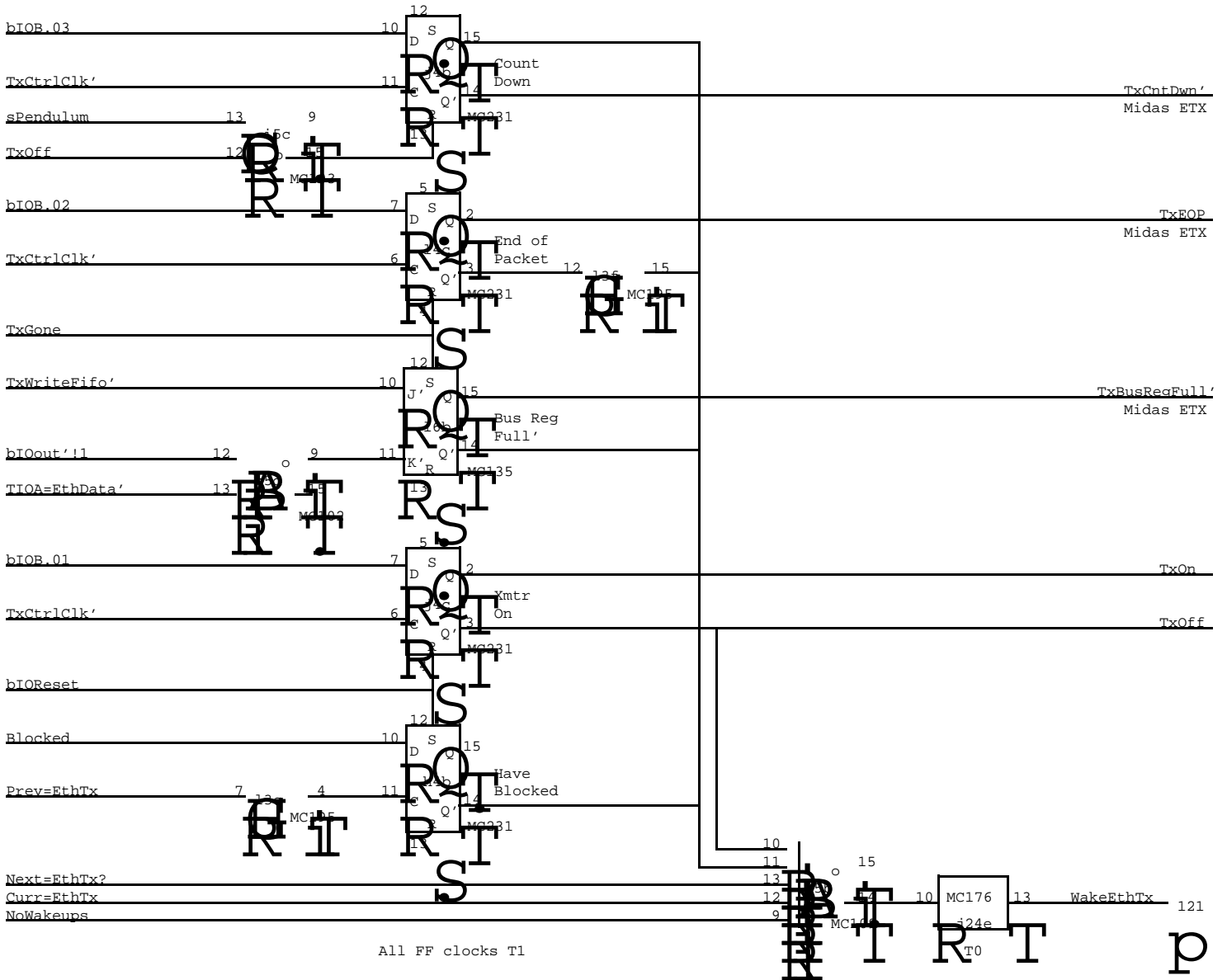


XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	Dorado	Receiver Stuff	Ether04.sil	David Boggs	Da	7/08/79	28

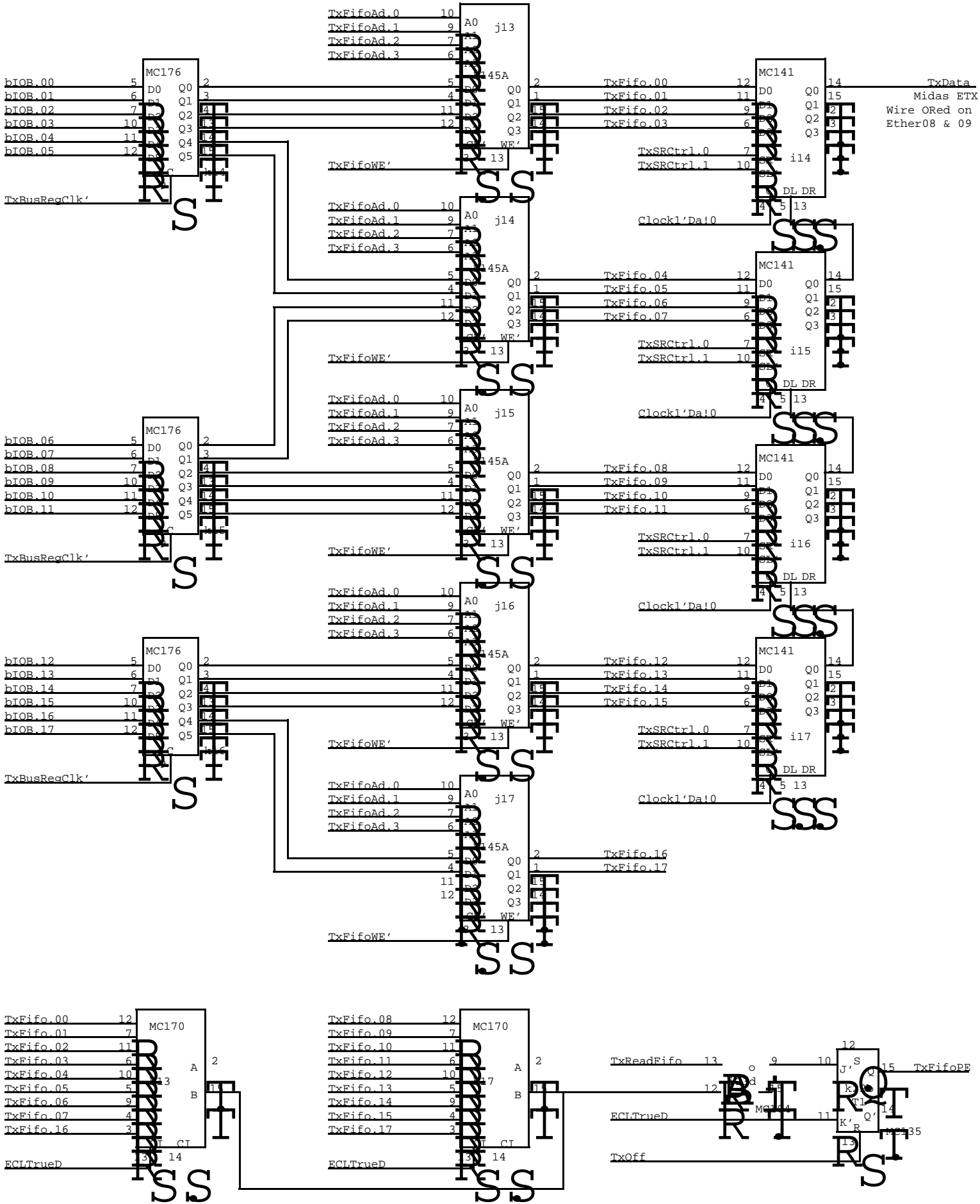


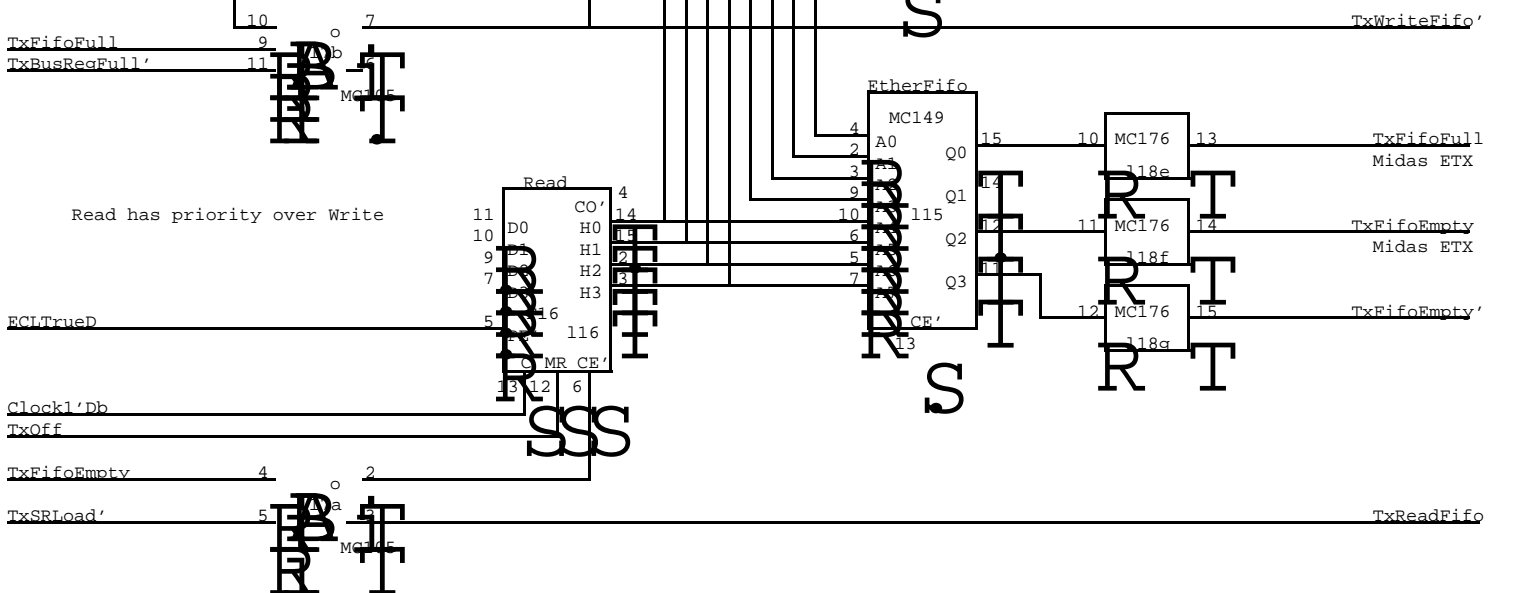
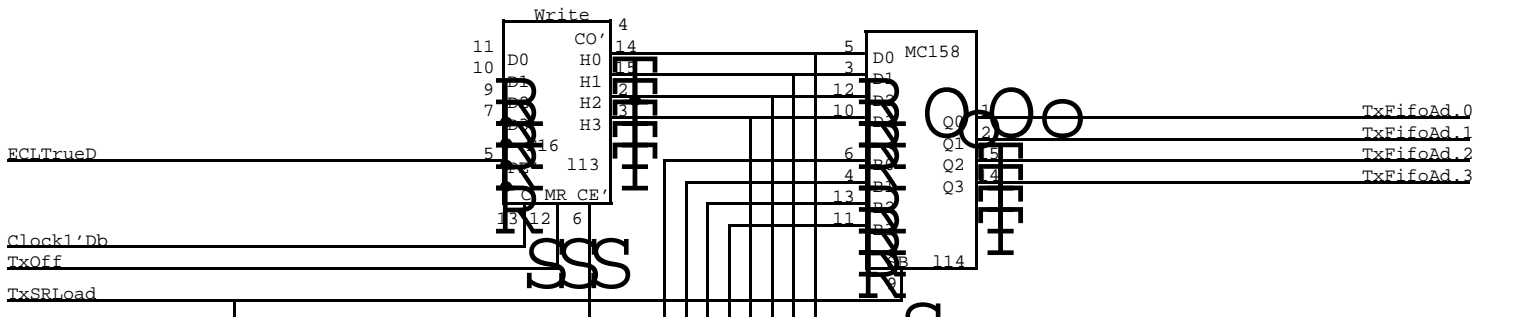
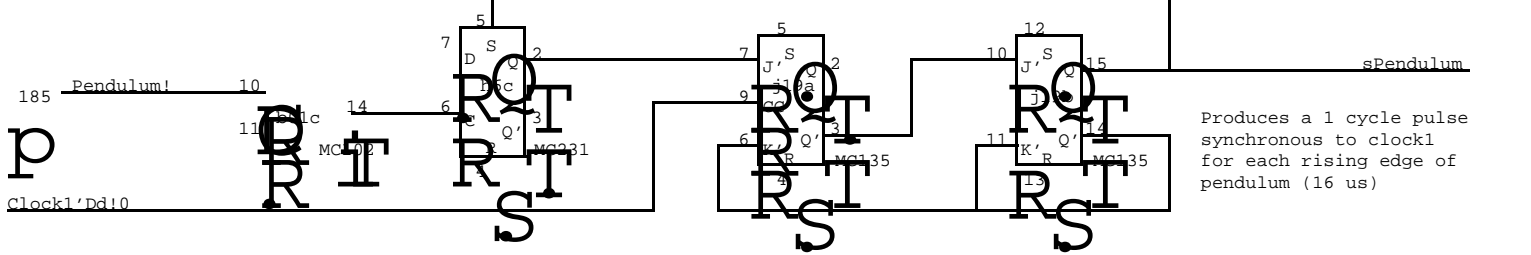
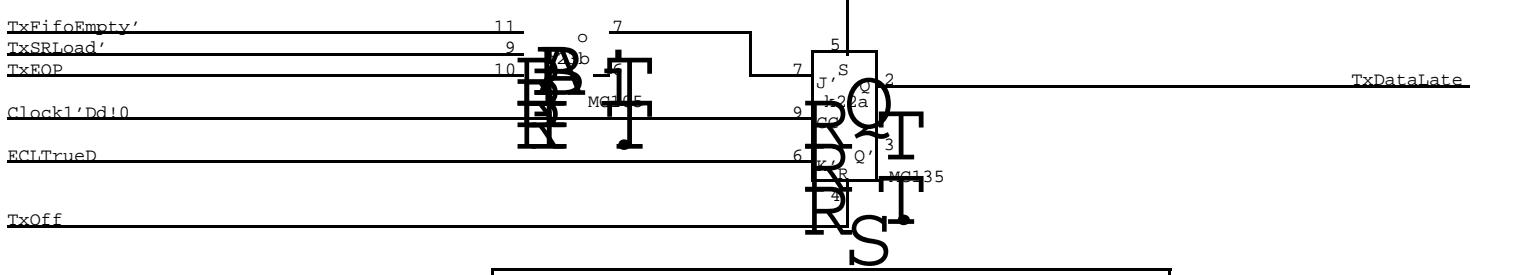
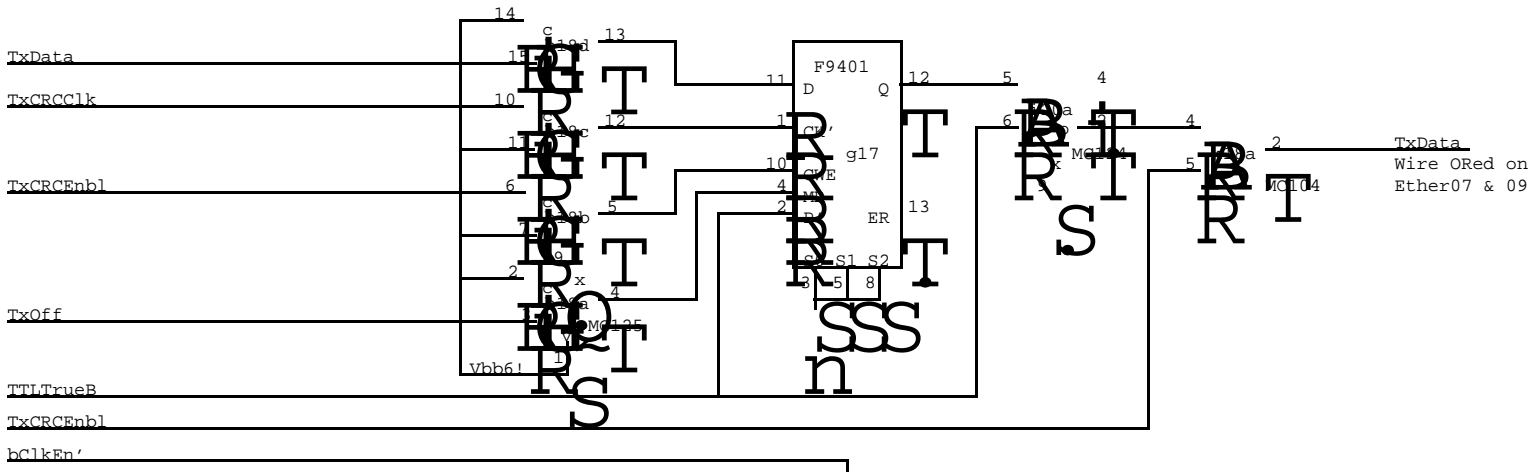
See Ether21 & 22.sil for wakeup timing diagrams

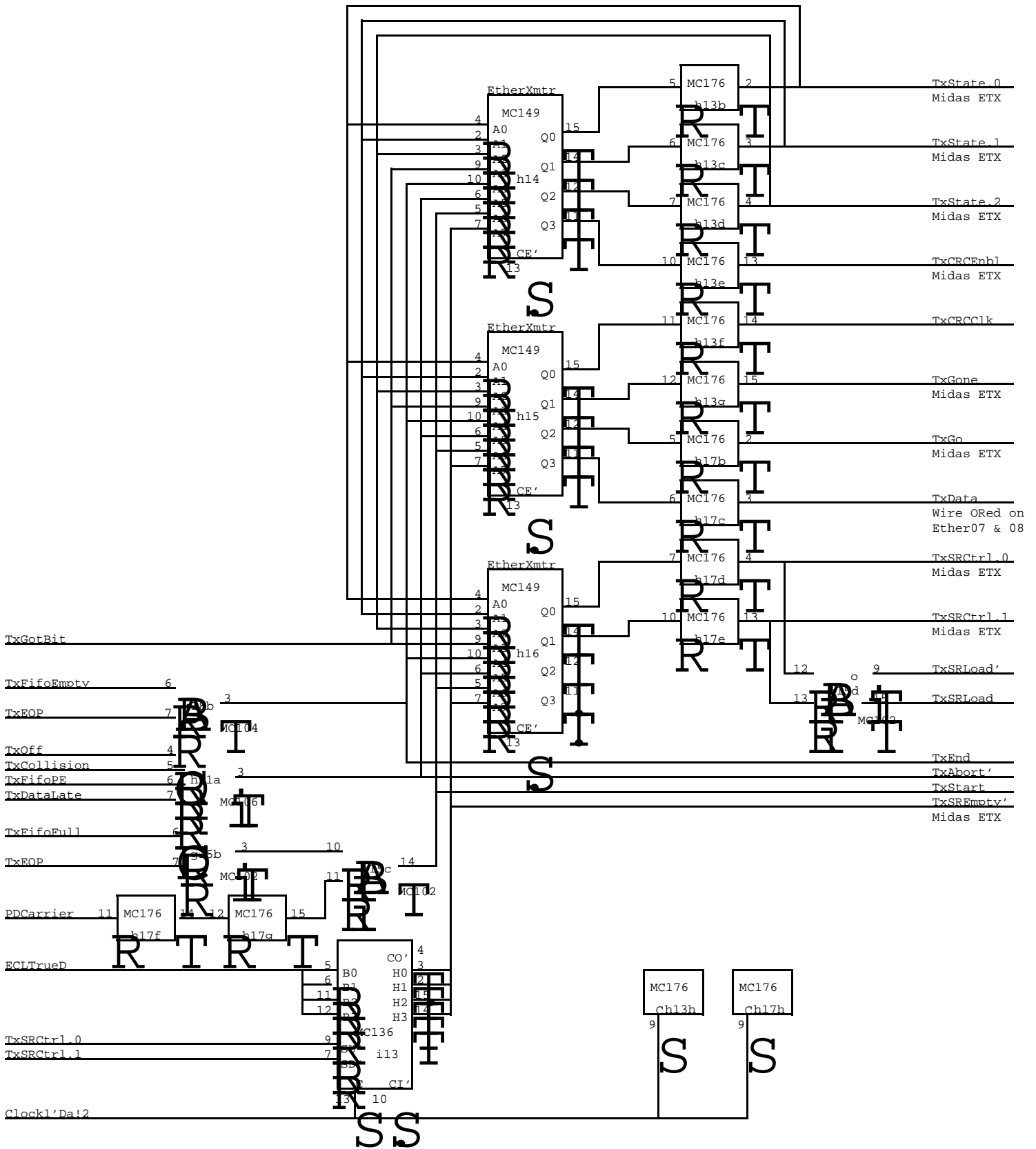
XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	Dorado	Receiver Wakeups	Ether05.sil	David Boggs	Da	7/08/79	29



See Ether21 & 22.sil for wakeup timing diagrams

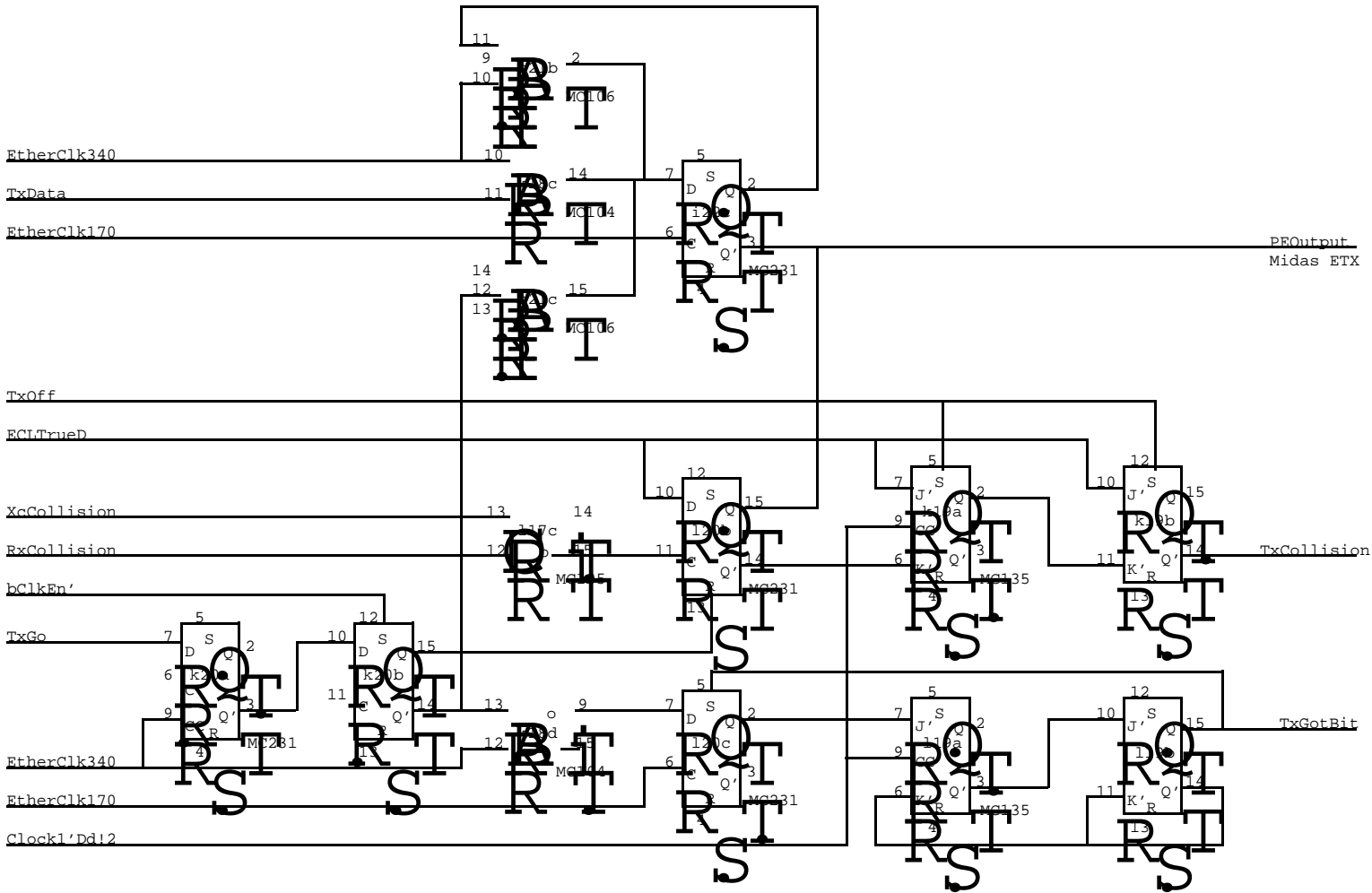






See Ether17.sil for timing diagrams

XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	Dorado	Transmitter Control	Ether09.sil	David Boggs	Da	9/24/79	33

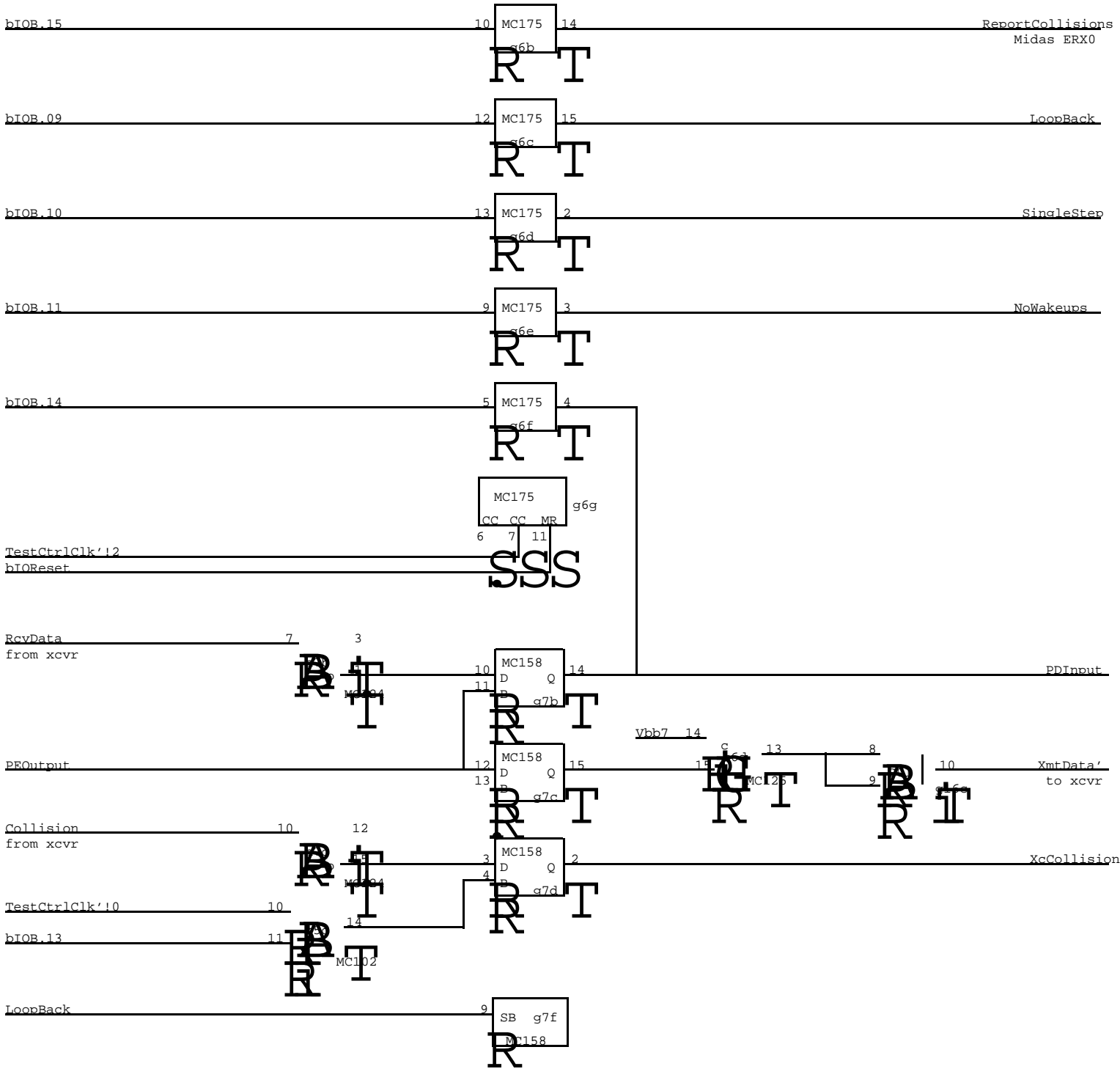


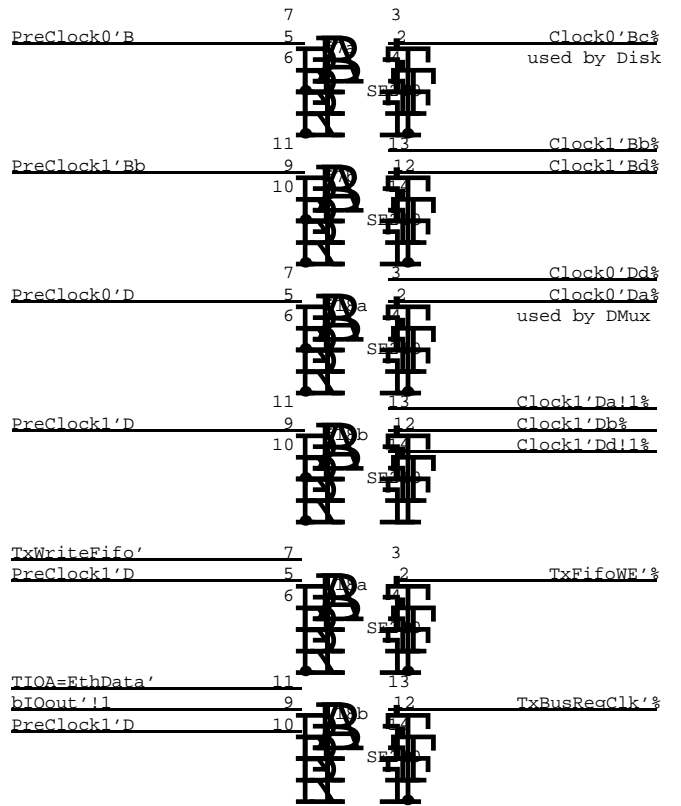
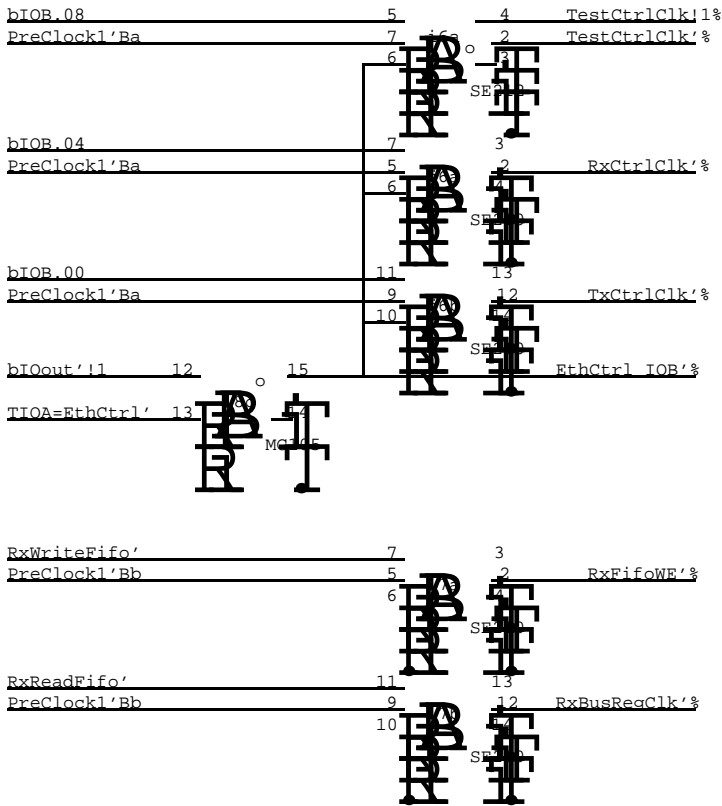
See Ether19.sil for timing diagrams

The slowest Dorado clock speed at which the transmitter works is 42.5 ns (T0 to T1)

525 ns < length of jam < 915 ns

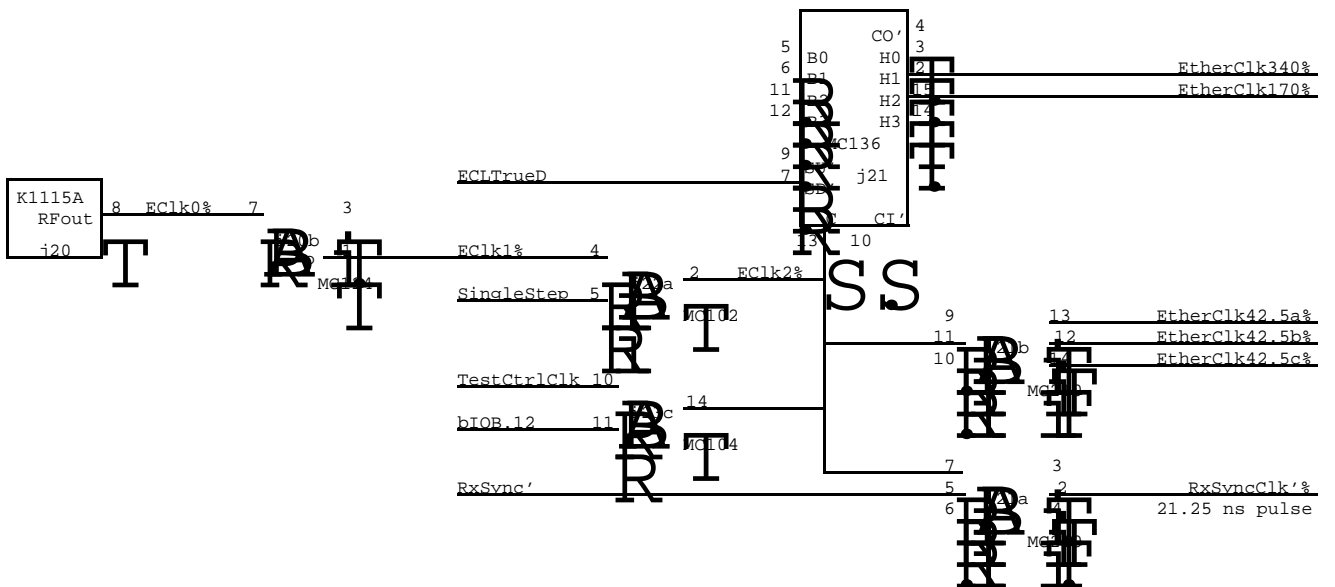
XEROX PARC	Project Dorado	Drawing Phase Encoder	File Ether10.sil	Designer David Boggs	Rev Da	Date 9/24/79	Page 34
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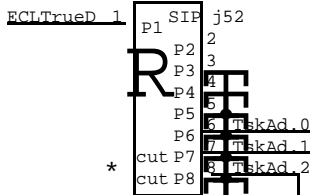


Dorado Synchronous Clocks

Free-running Ether Clocks

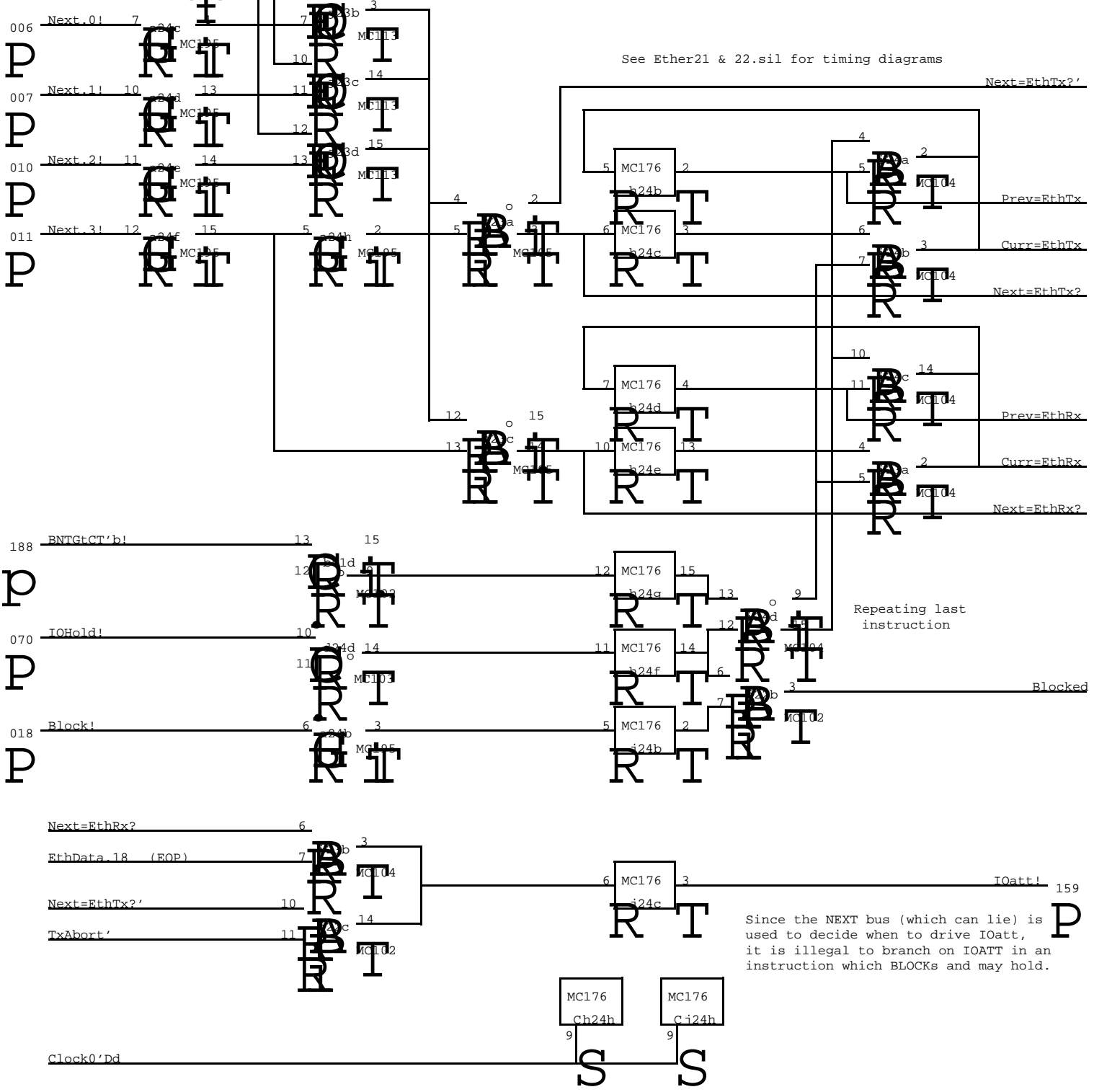


XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	Dorado	Clocks	Ether12.sil	David Boggs	Da	9/24/79	36

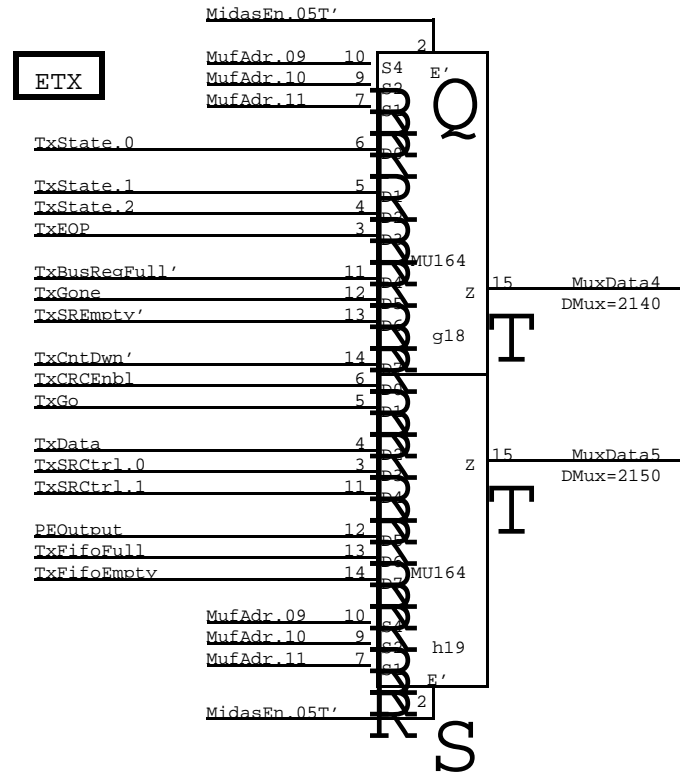
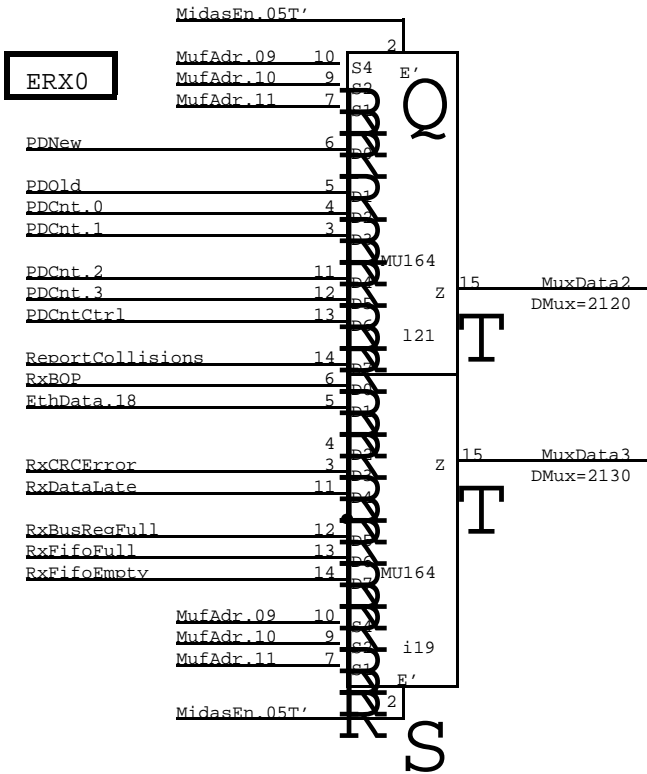


Standard tasks are 6&7.
 Task numbers differ only in
 the low order bit.
 Input is higher priority.
 See DskEth06.sil for how to
 set other tasks.

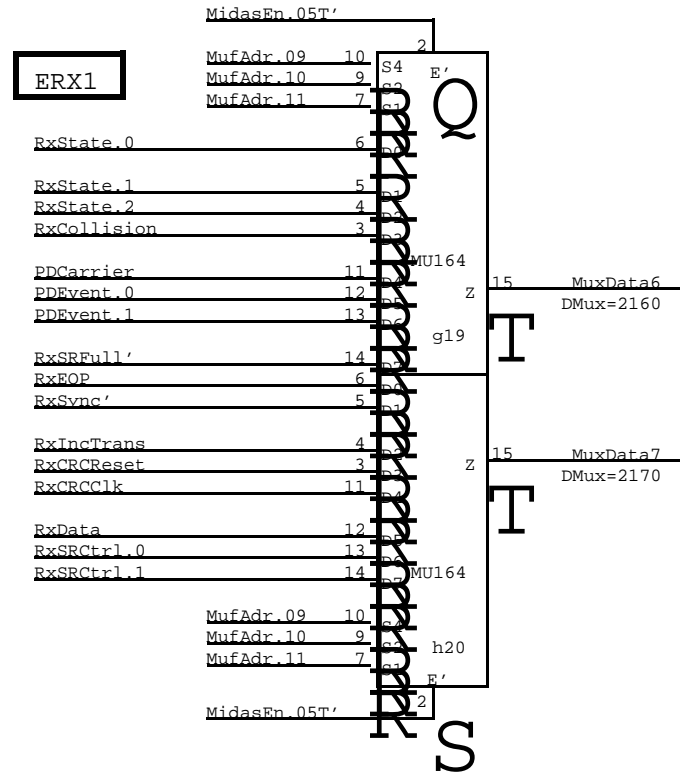
See Ether21 & 22.sil for timing diagrams



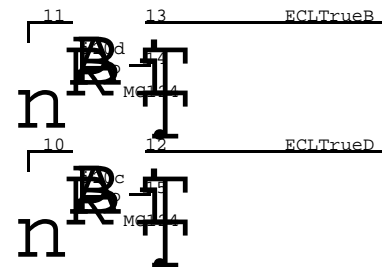
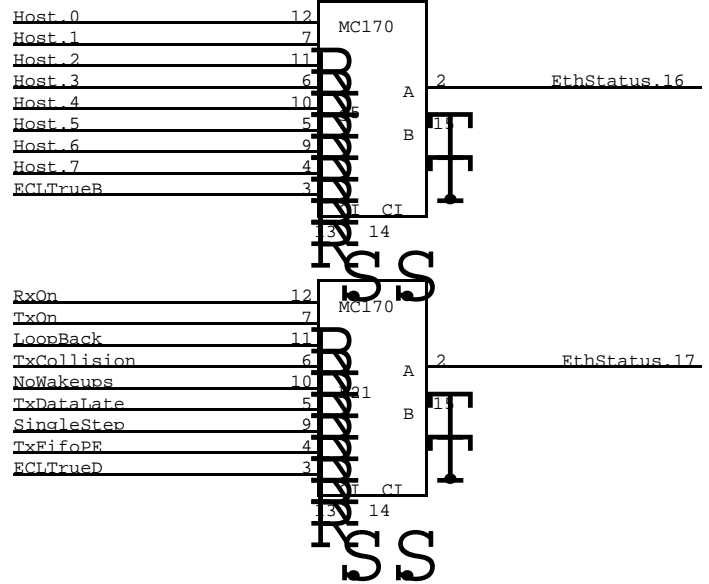
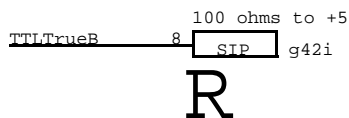
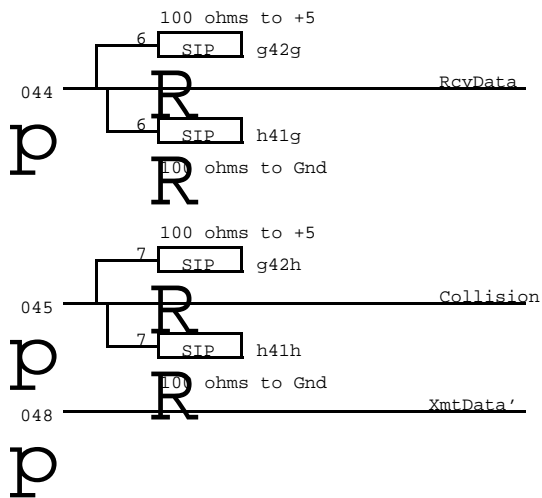
Since the NEXT bus (which can lie) is
 used to decide when to drive IOatt,
 it is illegal to branch on IOATT in an
 instruction which BLOCKs and may hold.



See DskEth01.sil for muffler control logic.
DMux addresses 2000-2117 are used by the disk.

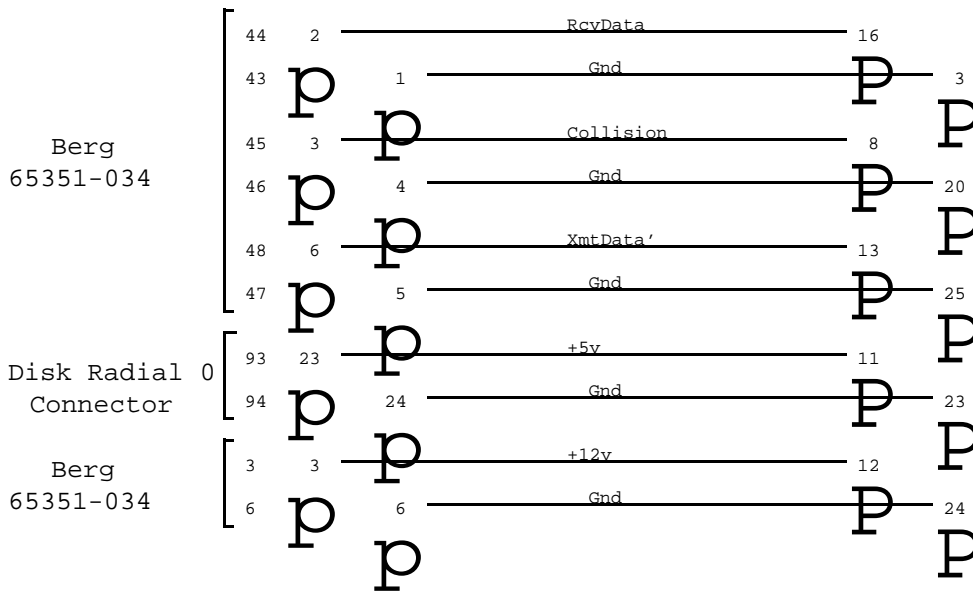


To set a host address bit to 1
pull it up to gnd through 91 ohms.



BP

Cannon DAC-25S

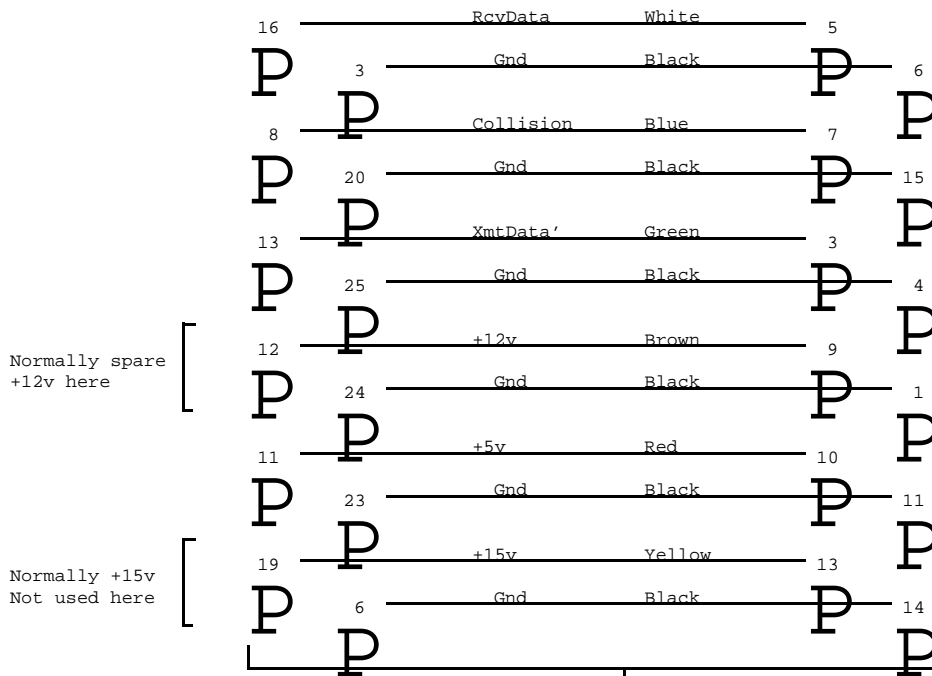


Internal Cable

External Cable

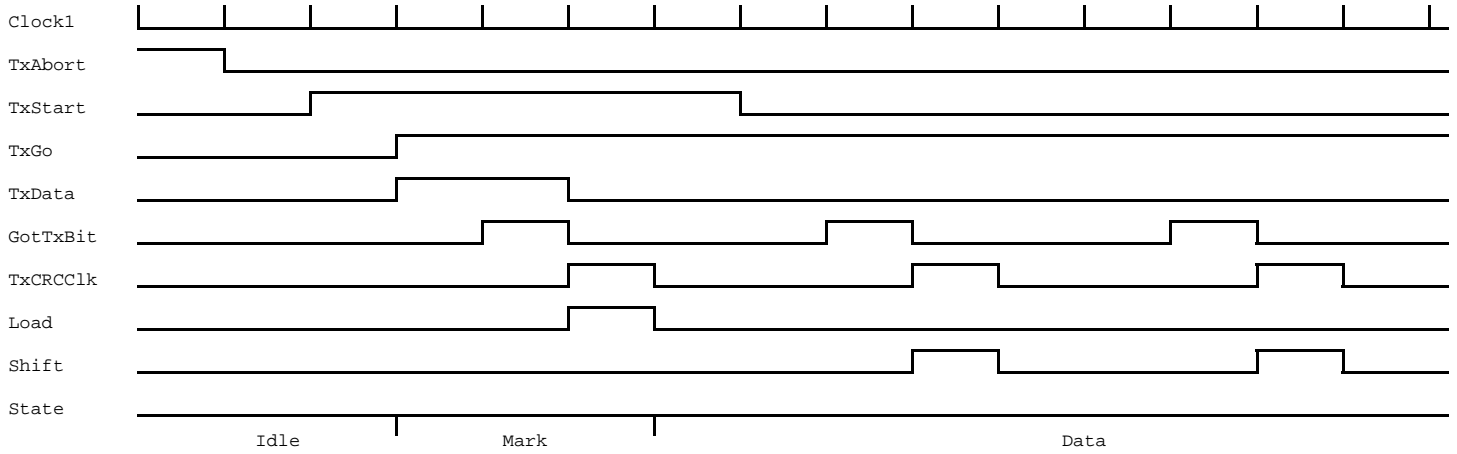
Cannon DAC-25P

Cannon DAC-15S

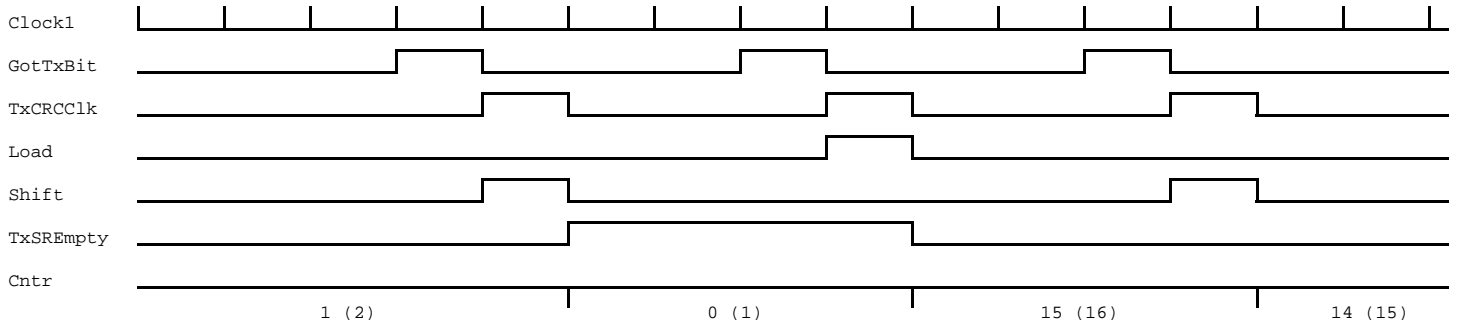


40' Typ

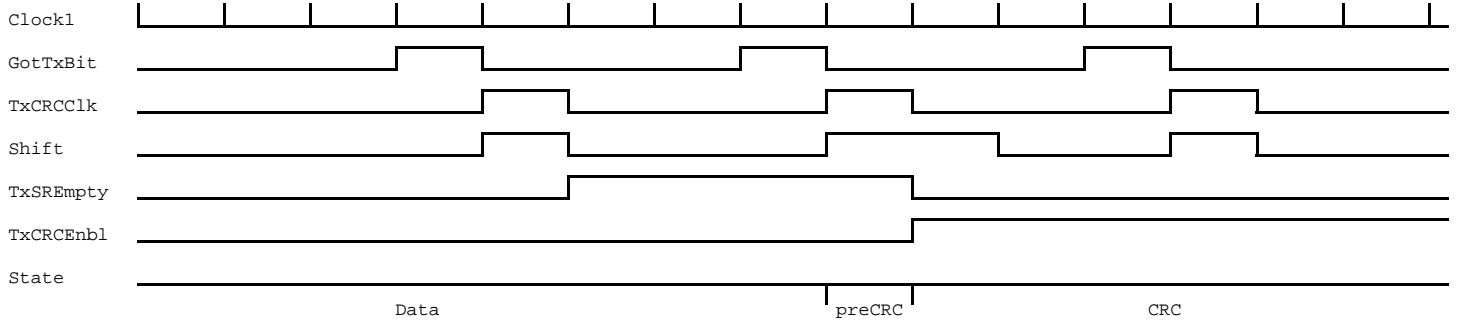
This is a standard Alto II Ethernet external cable part # 216411



Startup

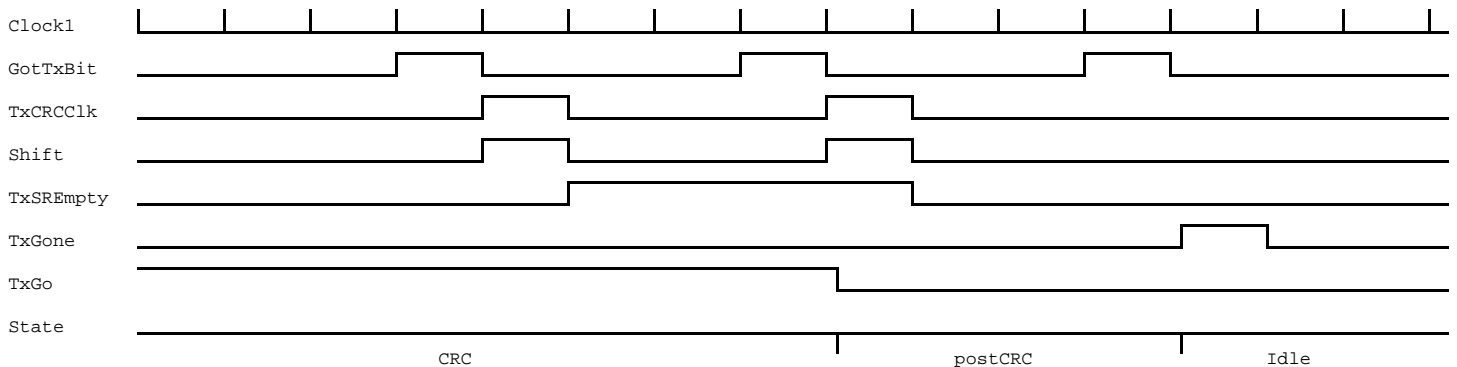


Loading Tx Shift Register

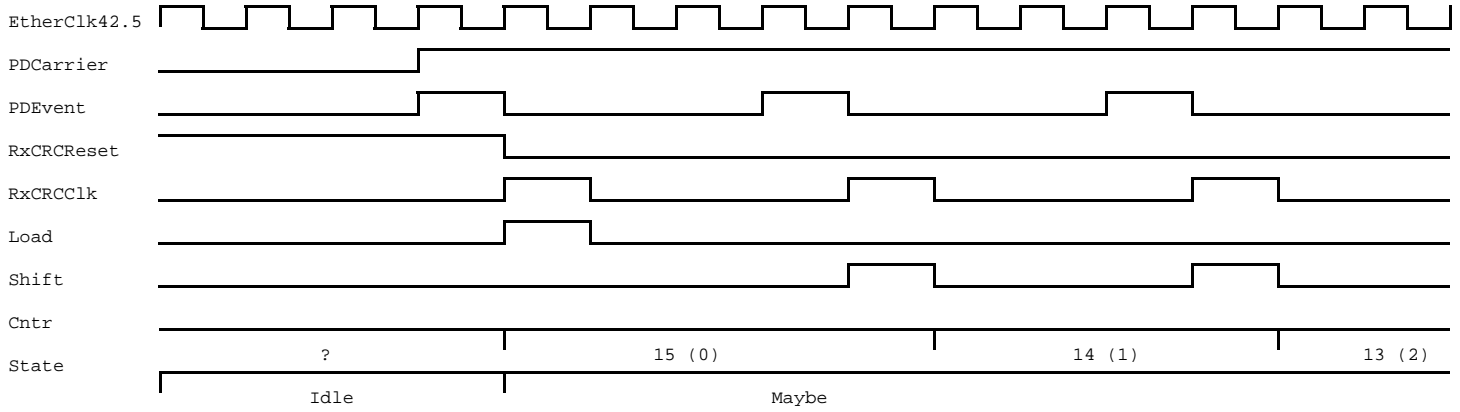


TxEnd has been high since TxSR was last loaded

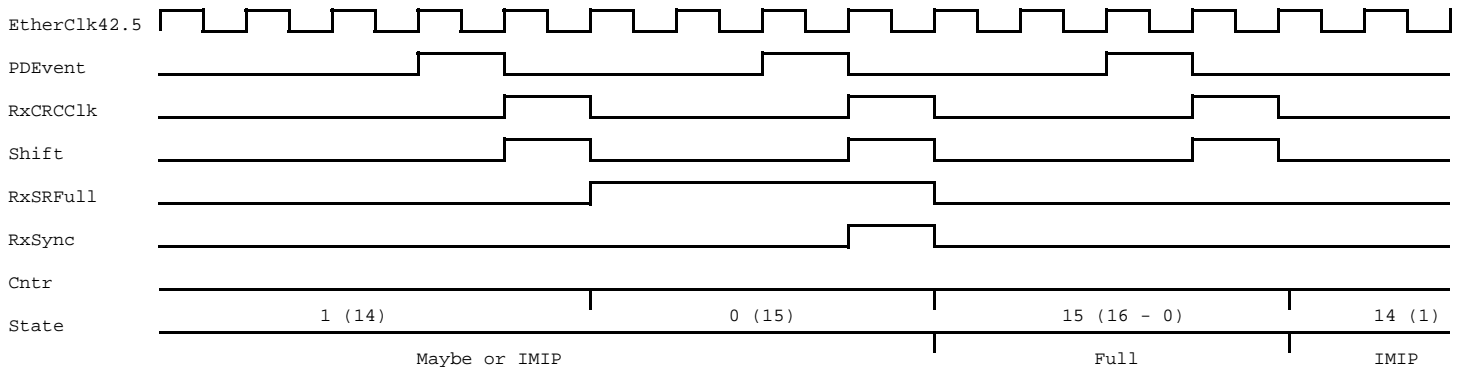
CRC



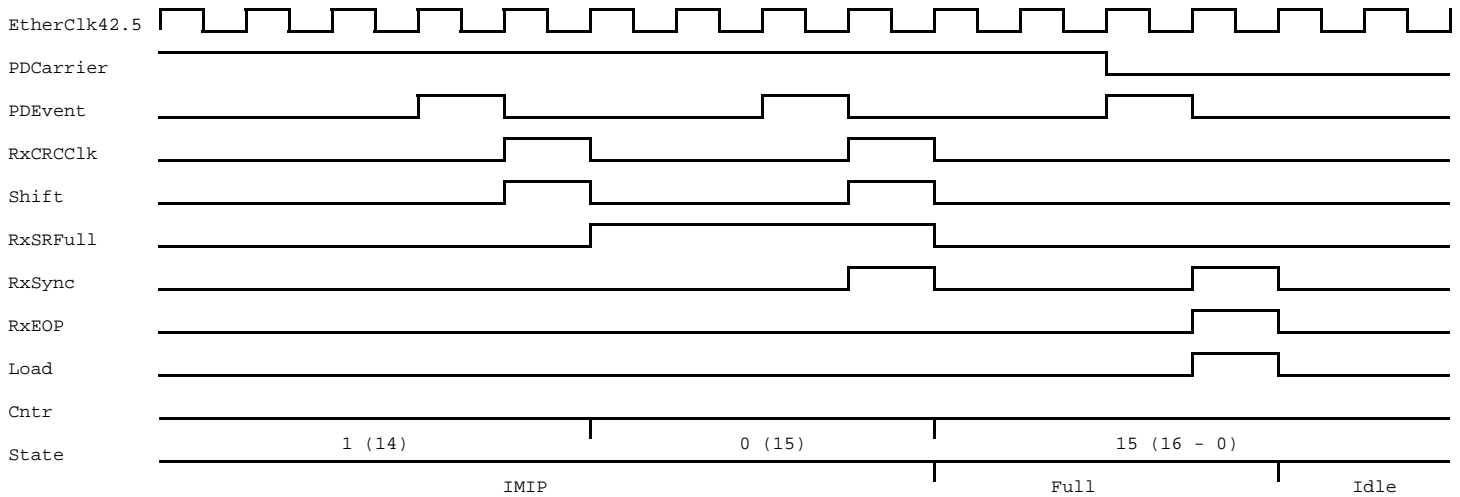
ShutDown



Startup

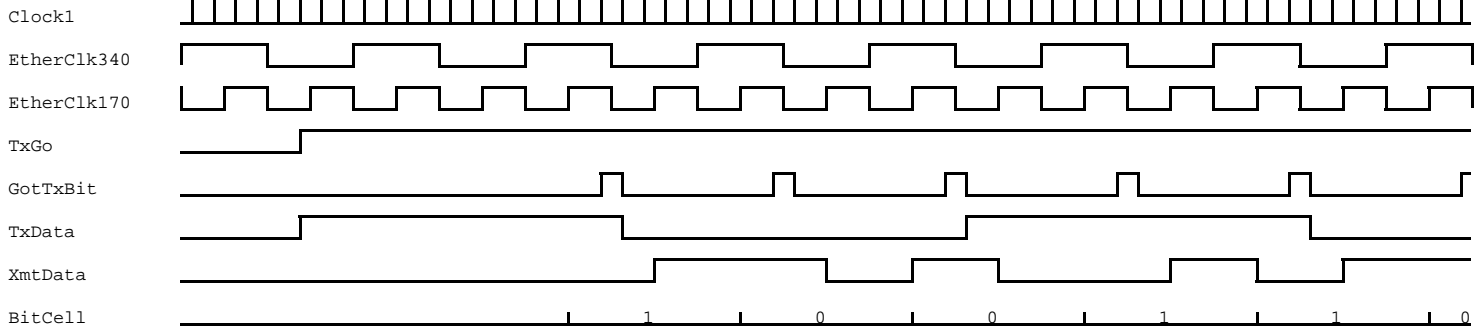


Dumping Rx Shift Register

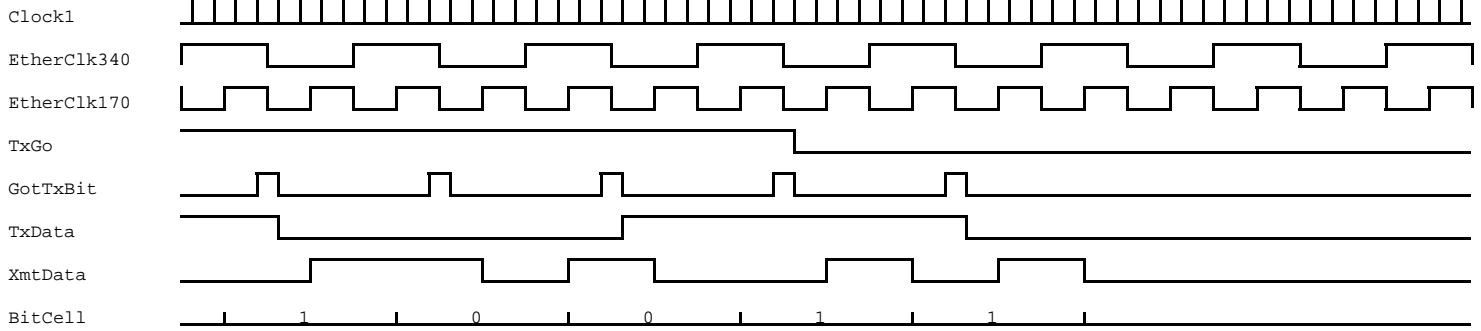


ShutDown

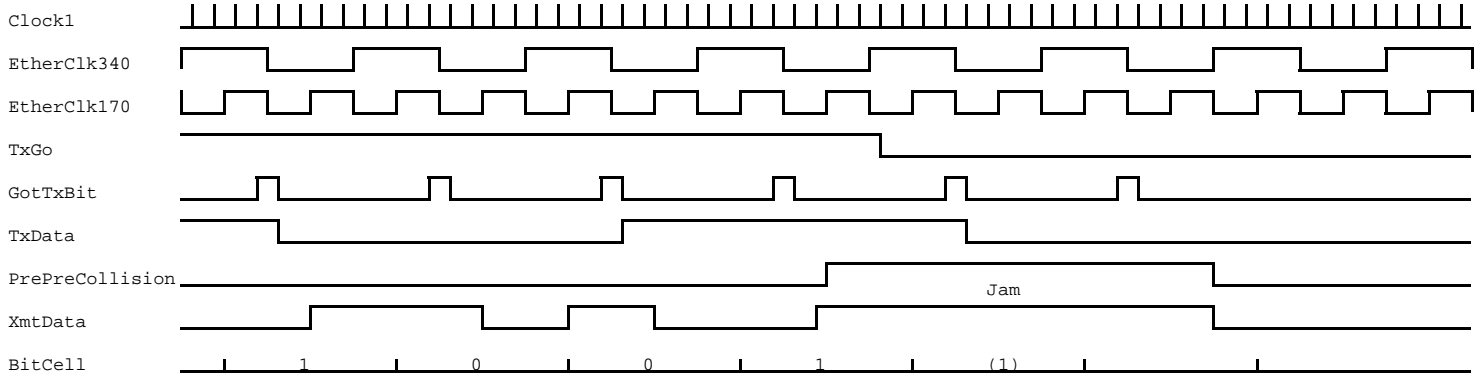
Cntr notation is <cntr value><# occupied postions>
 Phase decoder events are encoded in PDEvent.x
 Shift and Load are encoded in RxSRCtrl.x
 state is encoded in RxState.x
 shift also decrements Cntr



Startup

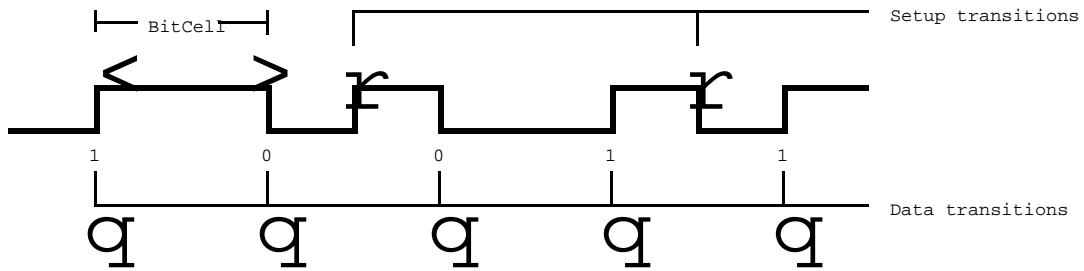


Shutdown

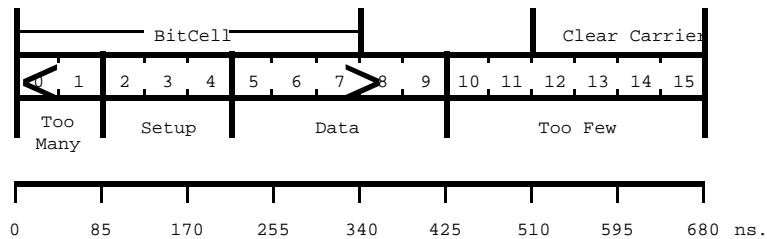


PrePreCollision is the output of the first stage of the Collision synchronizer

Collision

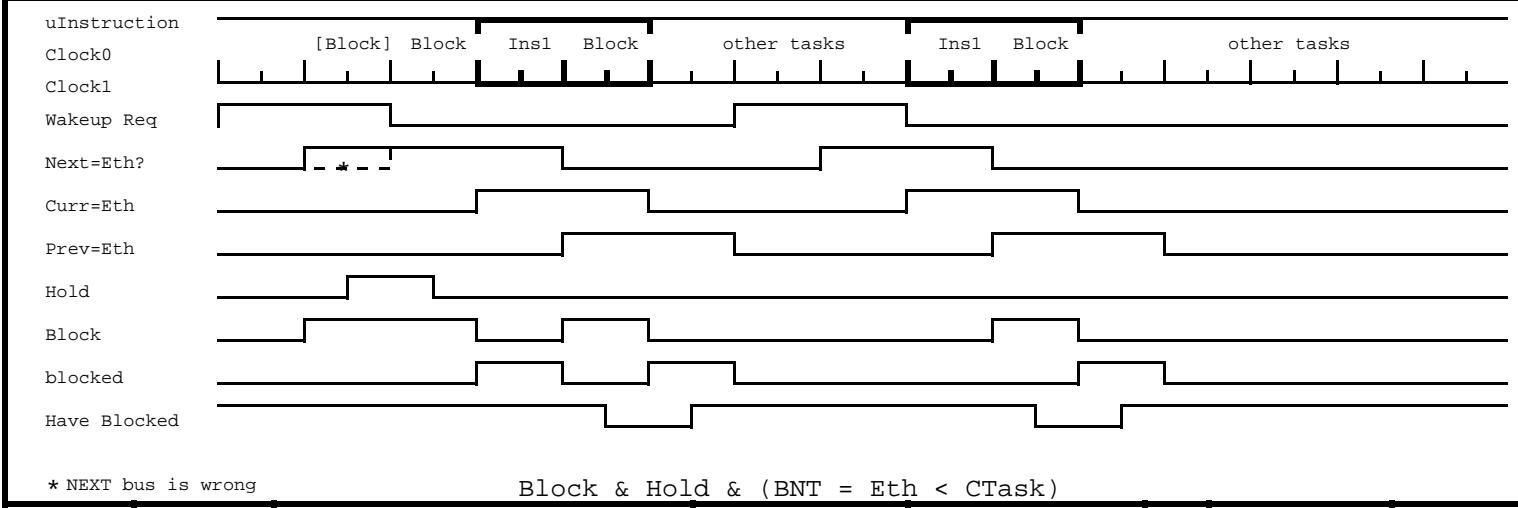
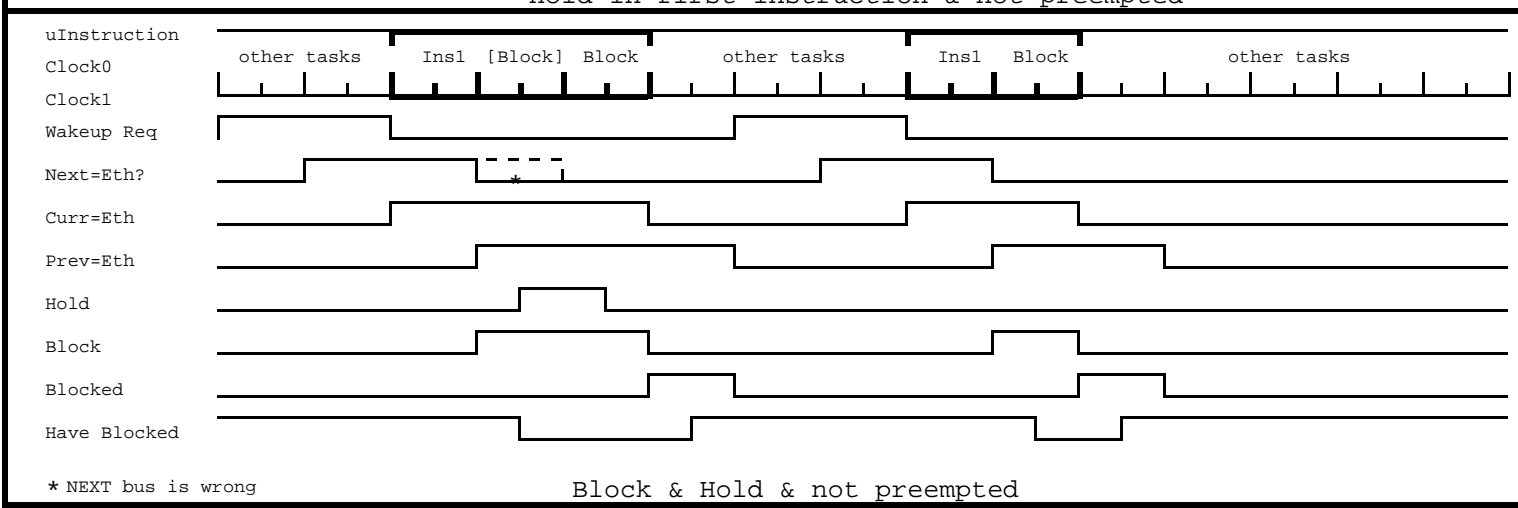
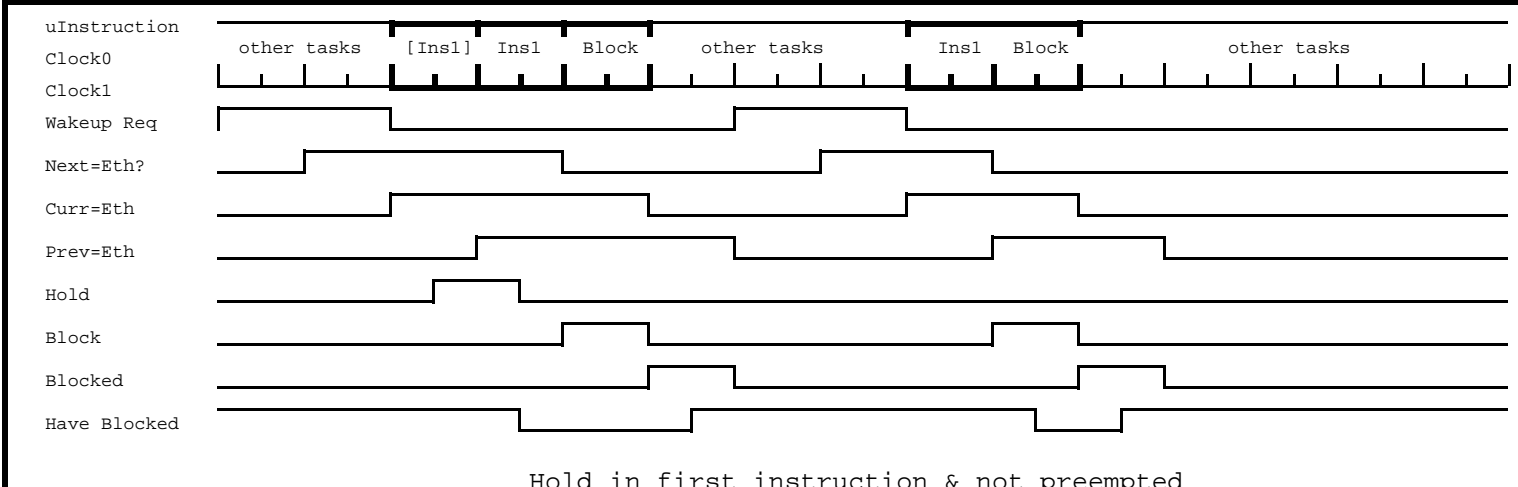
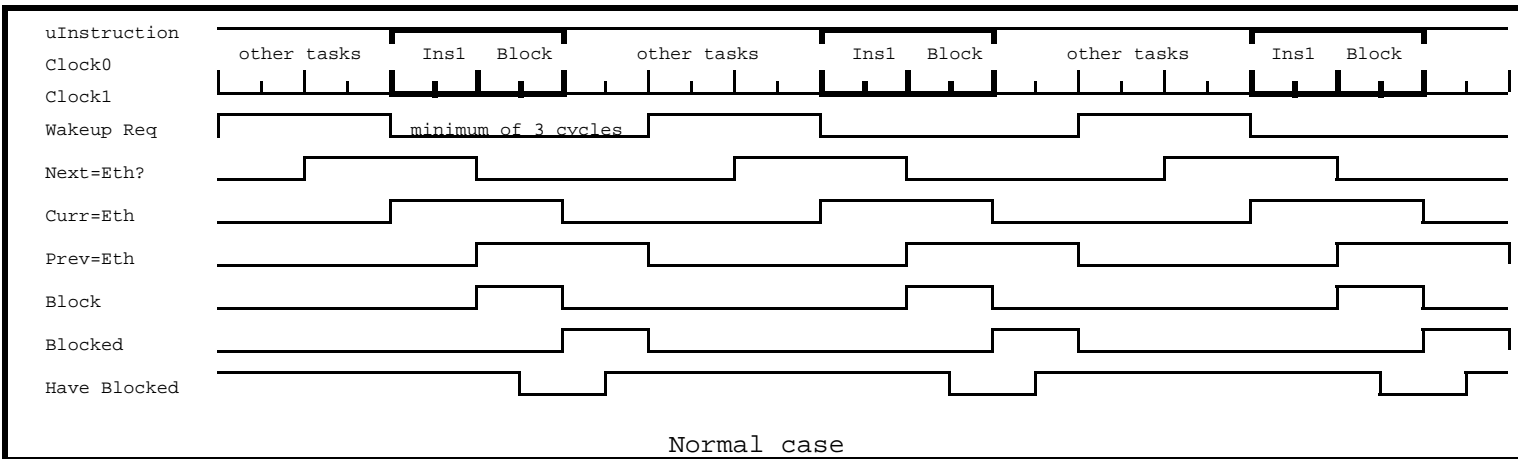


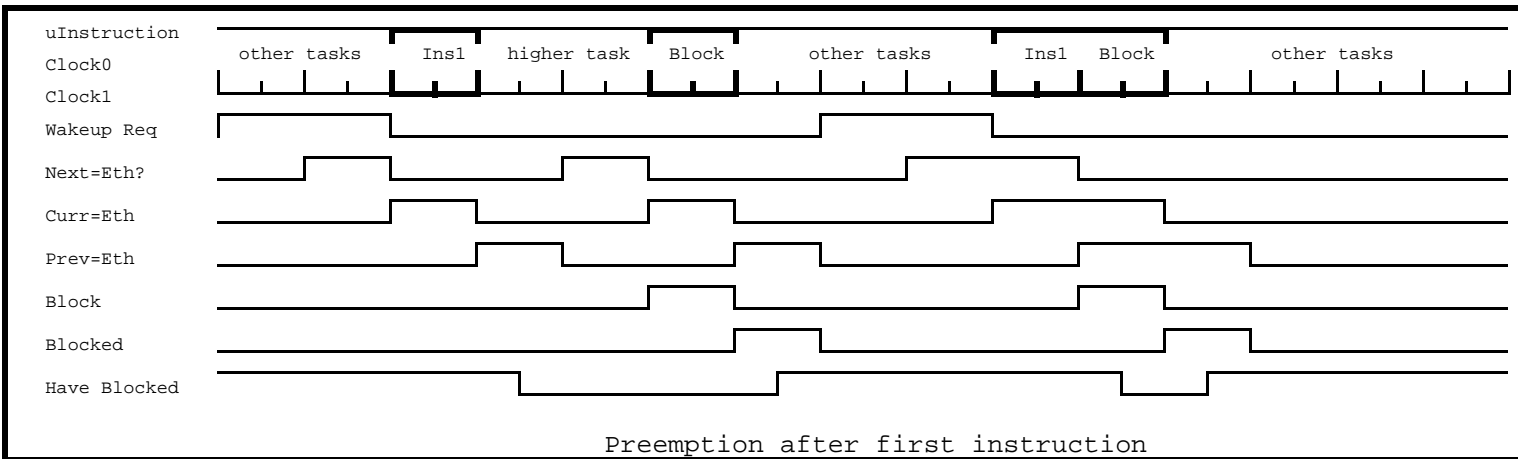
A bitcell is nominally 340 ns.
 A sample is nominally 42.5 ns.



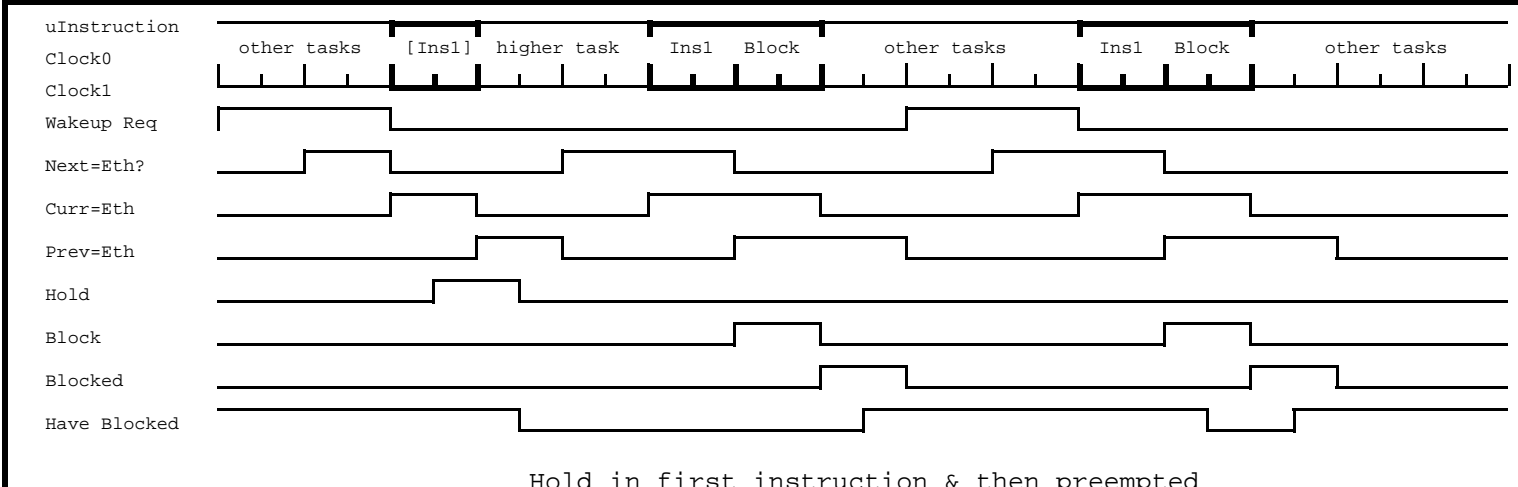
Inputs				Outputs			Comment
Carrier	Old	New	Cnt	Carrier	Event	CntCtrl	
Low	Low	Low	d/c	Low	NoEvent	Count	Idle
Low	Low	High	d/c	High	One	Reset	Start of packet (start bit)
Low	High	Low	d/c	High	Collision	Reset	Impossible
Low	High	High	d/c	Low	NoEvent	Count	Impossible
High	Low	High	0-1	High	Collision	Count	Too many transitions
High	High	Low	0-1	High	Collision	Count	Too many transitions
High	Low	High	2-4	High	NoEvent	Count	Setup transition (zero next)
High	High	Low	2-4	High	NoEvent	Count	Setup transition (one next)
High	Low	High	5-9	High	One	Reset	Data transition
High	High	Low	5-9	High	Zero	Reset	Data transition
High	Low	High	10-15	High	Collision	Reset	Too few transitions
High	High	Low	10-15	High	Collision	Reset	Too few transitions
High	Low	Low	0-11	High	NoEvent	Count	Active
High	High	High	0-11	High	NoEvent	Count	Active
High	Low	Low	12-15	Low	Collision	Reset	End of packet
High	High	High	12-15	High	Collision	Reset	Jam

"Impossible" conditions can happen right after power up.
 d/c means "don't care".

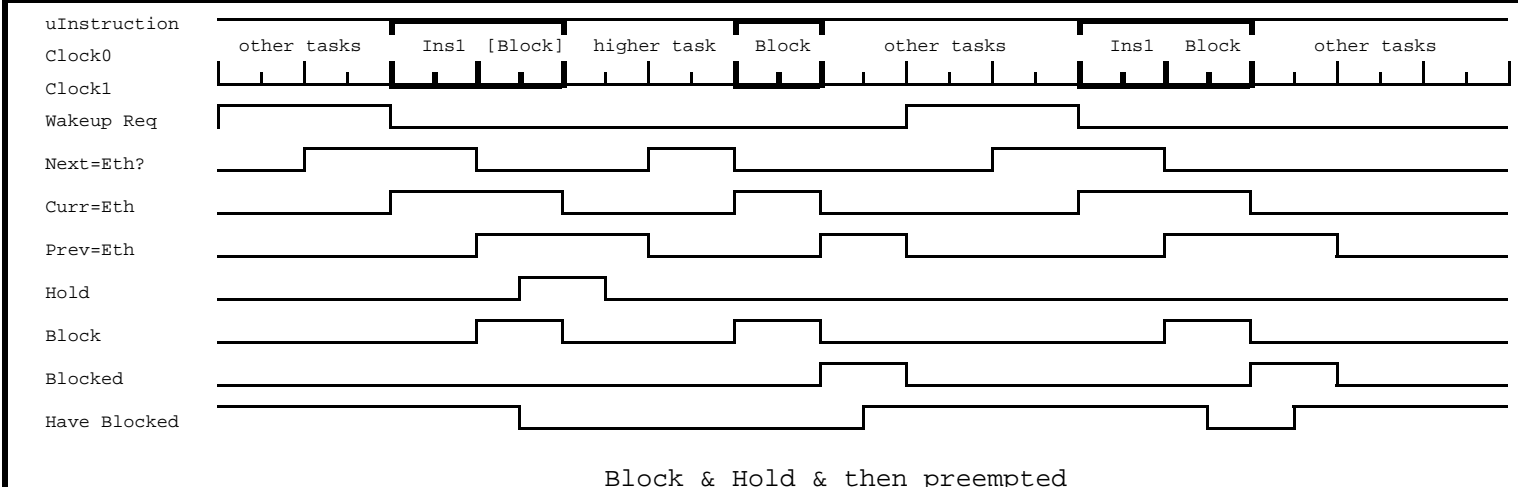




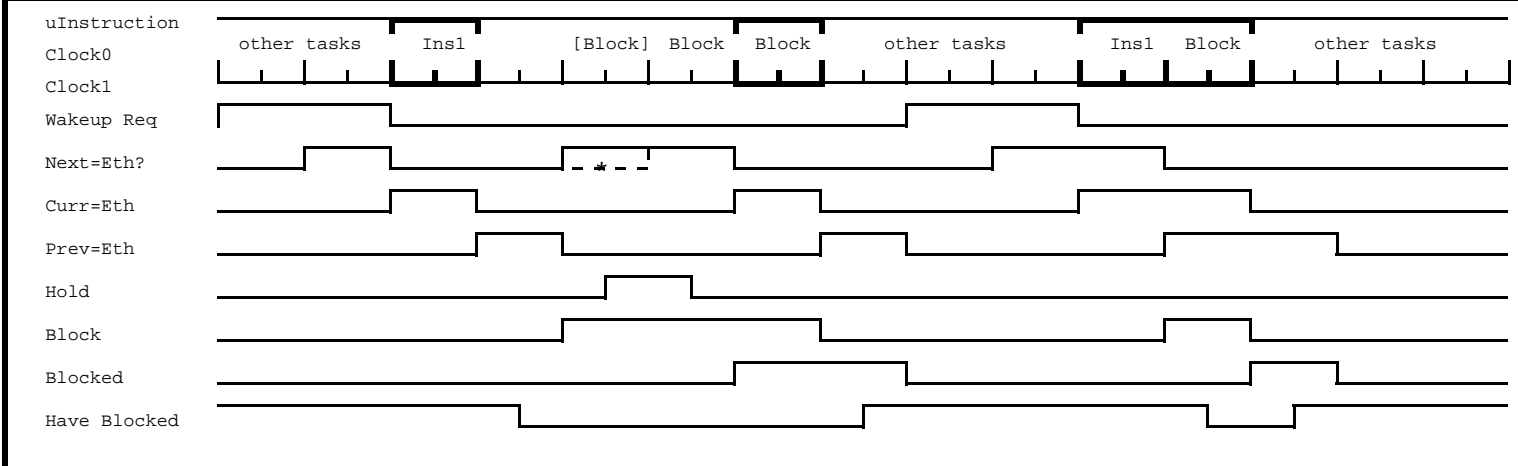
Preemption after first instruction



Hold in first instruction & then preempted



Block & Hold & then preempted



* NEXT bus is wrong Block & Hold & (BNT = Eth < CTask) while Eth is preempted

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Tx Cmd Enbl'	Tx On	Tx EOP	Tx Cnt Dwn	Rx Cmd Enbl'	Rx On	Rx BOP'		Test Cmd Enbl'	Loop Back	Single Step	No Wake ups	Test Clock	Test Coll'	Test Data	Report Colls

Output

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Host Address								Rx On	Tx On	Loop Back	Tx Coll	No Wake ups	Tx Data Late	Single Step	Tx Fifo PE



The host address is set by jumpers on the right backplane.
To set a bit to one, pull it up to ground through 91 ohms.