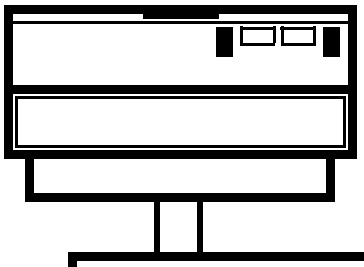
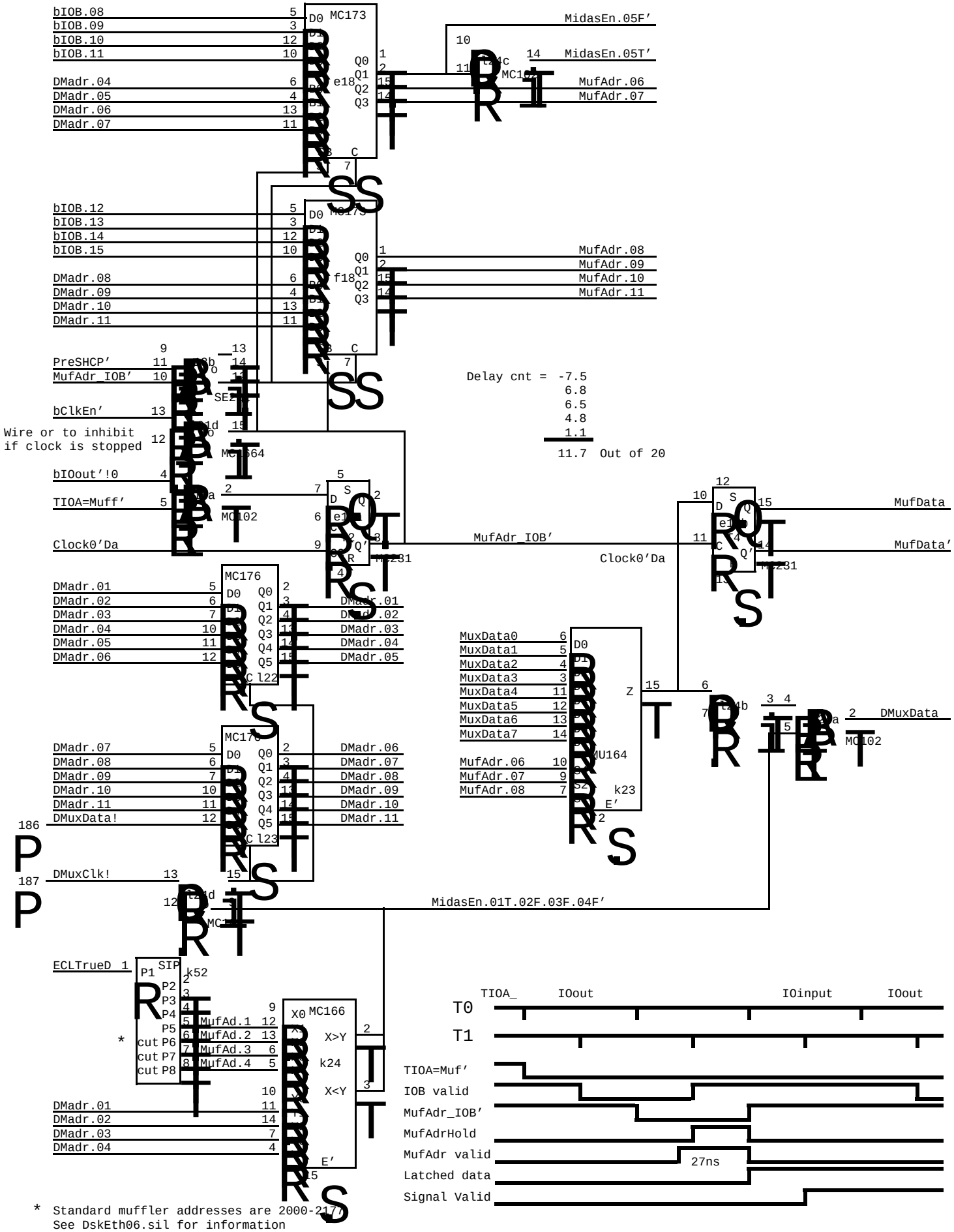


# DORADO SCHEMATICS

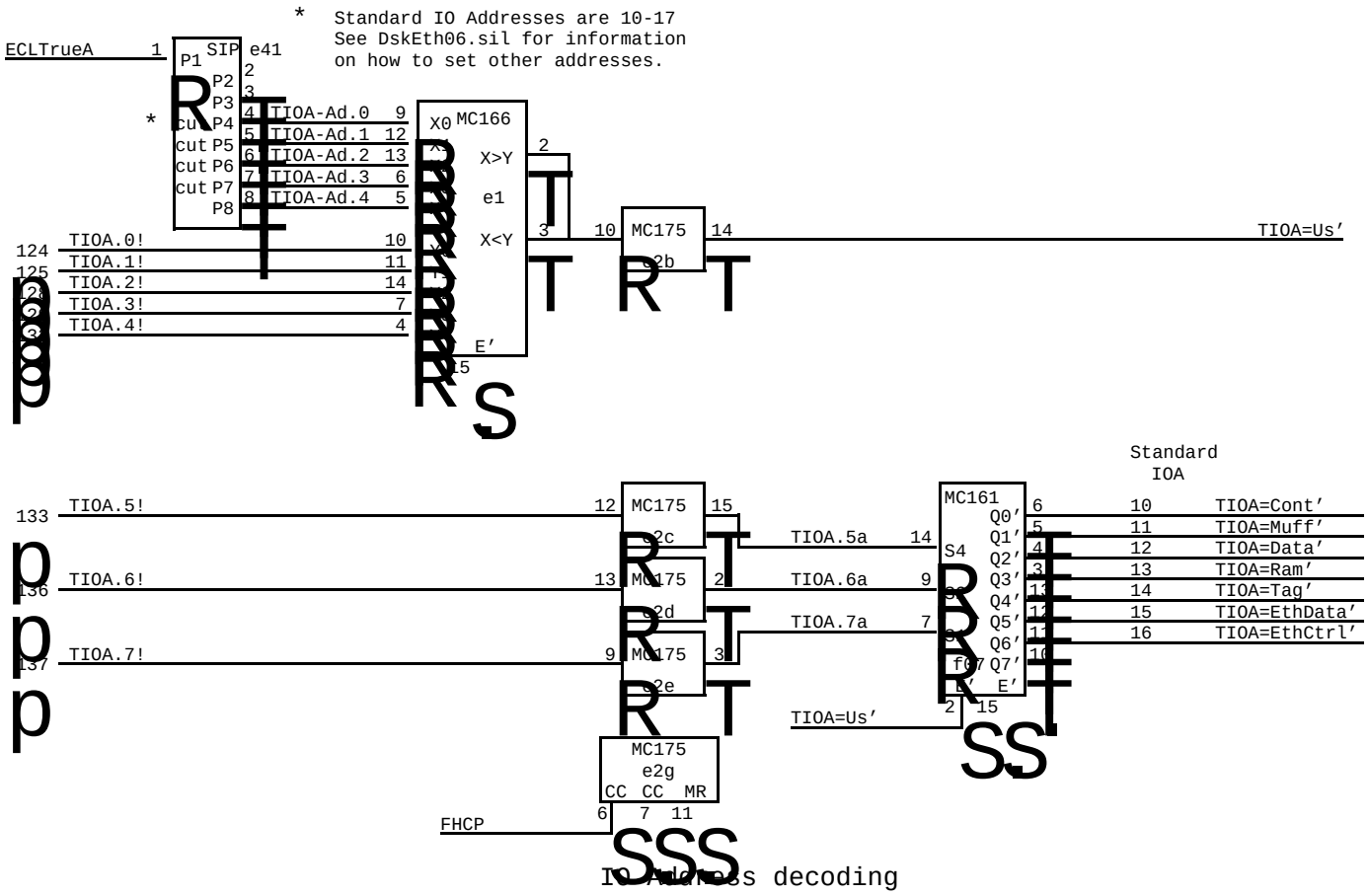
## I/O HARDWARE

## DISK and ETHERNET



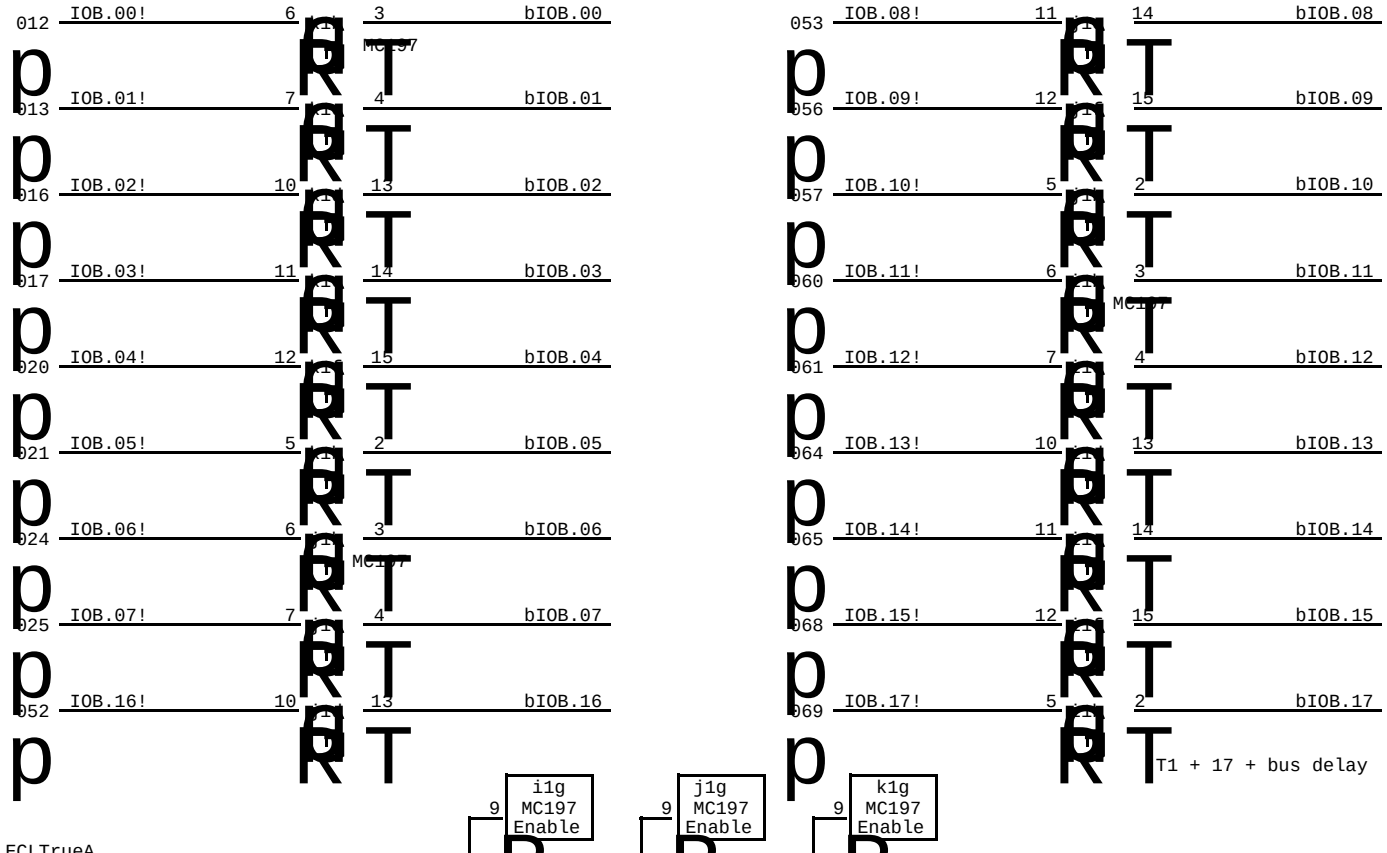

* Standard muffler addresses are 2000-2177
See DskEth06.sil for information
on how to set other addresses

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | DMux Control | DskEth01.sil | Roger Bates | Ce | 7/19/79 | 01 |



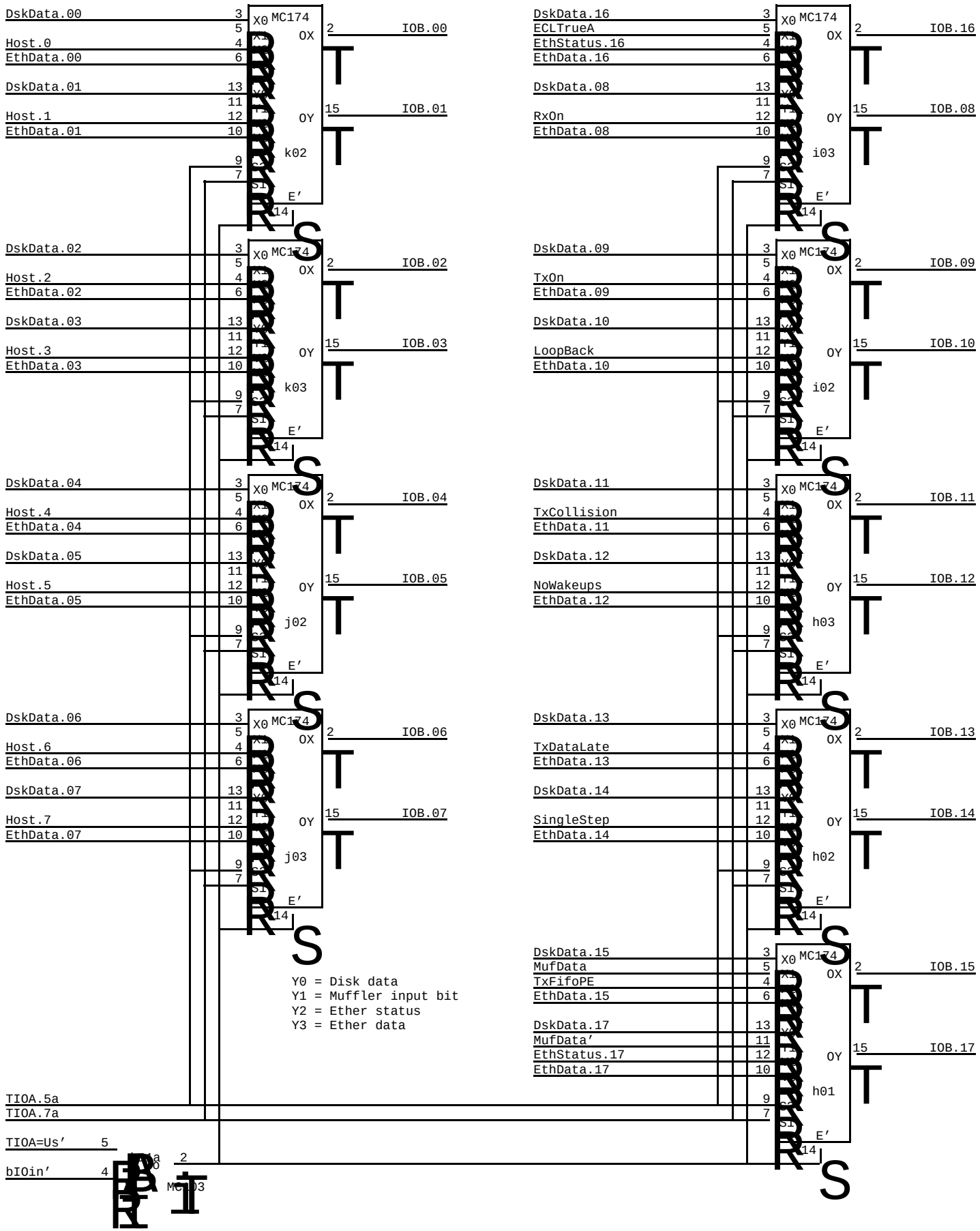

IO Address decoding

IOB receivers

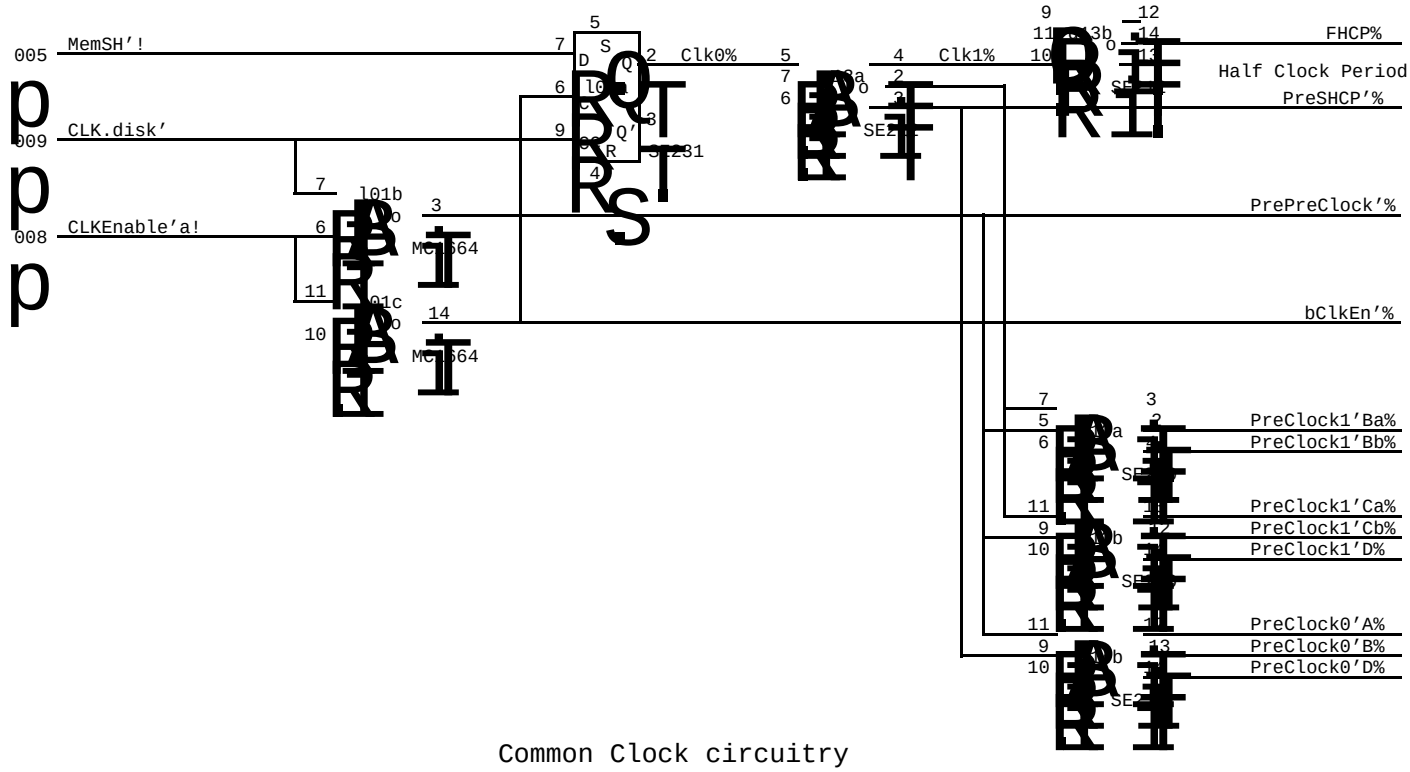



NOTE: IOB data received by this board is tested as part of the disk controller (Pg 18)
Both the disk and the Ethernet check the data parity after it has gone
through the respective FIFO's.

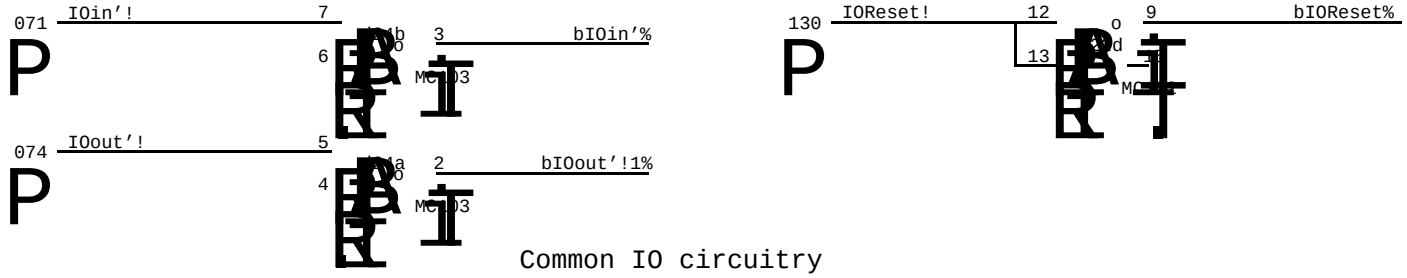
| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | IOA & IOB | DskEth02.sil | Bates/Boggs | Ce | 7/19/79 | 02 |



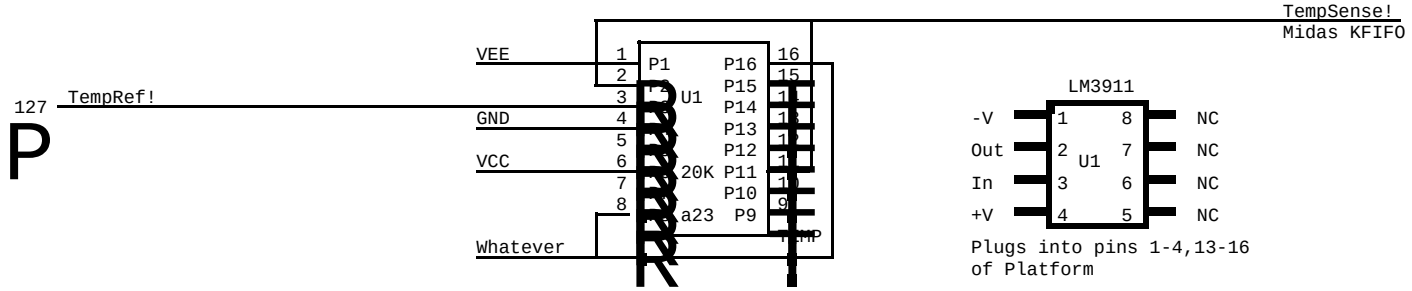

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | IOB data Select/Drivers | DskEth03.sil | Bates/Boggs | Ce | 9/24/79 | 03 |




Common Clock circuitry




Common IO circuitry



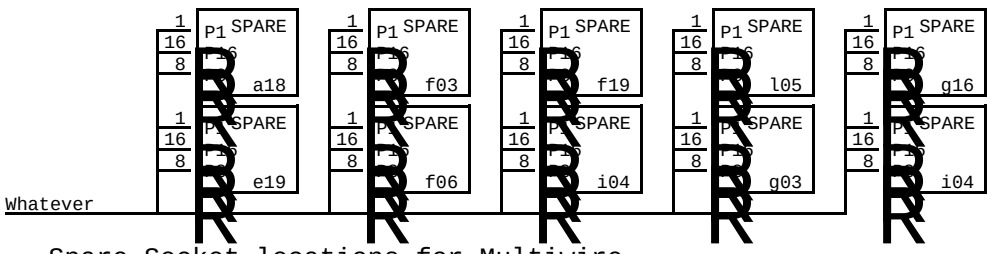

Temperature Sensor

Power connections are as follows:

Stitch-Weld: 1 & 16 are GND
8 is -5

Multiwire: 16 is GND
8 is -5

except in locations
a18, g03, and g16
which are uncommitted




Spare Socket locations for Multiwire

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Clocks & IO Signals | DskEth04.sil | Bates/Boggs | Ce | 7/23/79 | 04 |


| | A | B | C | D | E | F | G | H | I | J | K | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Sec Cnt LS169 X | 9,13 MC102 IIII | Disk IO MC1650 IIII | Sec Cnt LS08 | IOA MC166 X | Disk IO MC1650 IIII | Dr Cont 8T98 IIIIII | IOB MC174 X | IOB MC197 IIIIII | IOB MC197 IIIIII | IOB MC197 IIIIII | Clock,13 MC1664 ,III |
| 41 | | SIP | | | SIP | SIP | | SIP | | | | |
| 2 | Sec Cnt LS169 X | MC125 III, | Disk IO MC1650 IIII | Disk IO N125 IIII | TIOA MC175 IIII, | Disk IO MC1650 IIII | Disk IO N125 IIII | IOB MC174 X | MC174 X | MC174 X | IOB MC174 X | Clock SE231 I, |
| 3 | Sec Cnt N123 II | ECC MC176 IIIIII | MC124 IIII | Sec Cnt LS153 X | TW MC109 II | | | IOB MC174 X | IOB MC174 X | IOB MC174 X | IOB MC174 X | 5,6,12 MC195 III,II |
| 42 | | | | | | | SIP | | | | | |
| 4 | Sec Cnt PLAT X | ECC MC176 IIIIII | ECC MC113 IIII | Dr Cont LS174 X | TW MC231 II | IOB MC170 X | IOB MC170 X | Rx TW MC231 II | | Tx TW MC231 II | Rx Tw MC135 II | 5,6 MC231 II |
| 5 | Sec Cnt N123 II | ECC MC176 IIIIII | ECC MC113 IIII | Dr Cont S288 X | TW MC231 II | Disk IO MC174 X | Host MC170 X | TW Com MC109 II | 4,5 MC103 III, | Rx CRC F9401 X | 5,11 MC102 IIII | |
| 43 | | | | | | | | | | | | |
| 6 | Sec Cnt LS169 X | ECC MC176 IIIIII | Clock,8 SE212 II | Dr Cont LS155 X | TW Bit Cl MC231 II | | Test MC175 IIIII | 4,8 MC231 II | Clock SE212 II | Clock SE210 II | RxCRC,11 MC125 IIII | 6,4 MC135 II |
| 7 | Sec Cnt LS169 X | ECC MC158 IIII | ECC MC176 IIIIII | MC102 III, | Muf MU164 X | TIOA MC161 X | Test MC158 III, | 1,4,10 MC124 IIII | Clock SE210 II | Clock SE210 II | RxSR Dmp MC135 II | Rx EOP MC231 II |
| 44 | | | | | | | | | | | | |
| 8 | Sec Cnt LS174 X | ECC,9 MC158 IIII | ECC MC176 IIIIII | FIFO F145A X | Out Reg MC176 X | Sh Reg MC176 X | In Reg MC173 X | Rx FSM MC176 IIIIII | Rx SR MC141 X | Rx Fifo F145A X | Rx Par MC170 X | 4,12 MC105 III |
| 9 | Sec Cnt LS174 X | Out Reg MC231 II | MC231 II | FIFO F145A X | Out Reg MC170 X | Sh Reg F00 X | In Reg MC173 X | Rx FSM MCM149 X | Rx SR MC141 X | Rx Fifo F145A X | Rx Reg MC176 X | Rx Write F16 X |
| 45 | | | | | | | | | | | | |
| 10 | Sec Cnt LS174 X | Bit Cl F16 X | MC104 IIII | FIFO F145A X | Out Reg MC176 X | Sh Reg F00 X | In Reg MC173 X | Rx FSM MCM149 X | Rx SR MC141 X | Rx Fifo F145A X | Rx Reg MC176 X | Rx Fifo MCM149 X |
| 11 | Sec Cnt LS174 X | MC103 IIII | MC103 IIII | FIFO F145A X | Out Reg MC170 X | Sh Reg F00 X | In Reg MC173 X | Rx FSM MCM149 X | Rx SR MC141 X | Rx Fifo F145A X | Rx Reg MC176 X | Rx Fifo MC158 X |
| 46 | | | | | | | | | | | | |
| 12 | Muf MU164 X | MC231 II | MC195 IIIII, | FIFO F145A X | Out Reg MC176 X | Sh Reg F00 X | In Reg MC173 X | Rx FSM MC176 IIIIII | Rx FSM MC136 X | Rx Fifo F145A X | Rx Par MC170 X | Rx Read F16 X |
| 13 | Muf MU164 X | Muf MU164 X | Errors MC197 IIIIII | MC102 IIII | Cont MC135 II | Clock SE210 II | Clock SE212 II | Tx FSM MC176 IIIIII | Tx FSM MC136 X | Tx Fifo F145A X | Tx Par MC170 X | Tx Write F16 X |
| 47 | | | | | | | | | | | | |
| 14 | Fifo Cnt MC158 X | Fifo Cnt MCM149 X | Fifo Cnt,4 MC176 IIIII, | Cont MC171 X | Cont MC231 II | Cont F00 X | Clock SE210 II | Tx FSM MCM149 X | Tx SR MC141 X | Tx Fifo F145A X | Tx Reg MC176 X | Tx Fifo MC158 X |
| 48 | | | | | | | | | | | | |
| 15 | Fifo Cnt F16 X | Fifo Cnt MC231 II | Fifo Cnt MC231 II | Bit Cl SE210 II | Cont MC231 II | Cont F00 X | Tx FSM MC102 ,III | Tx FSM MCM149 X | Tx SR MC141 X | Tx Fifo F145A X | Tx Reg MC176 X | Tx Fifo MCM149 X |
| 16 | Fifo Cnt F16 X | Clock SE212 II | Cont MC135 II | Fifo Cnt,2 MC102 I,II | Ram MC145A X | Ram MC145A X | | Tx FSM MCM149 X | Tx SR MC141 X | Tx Fifo F145A X | Tx Reg MC176 X | Tx Read F16 X |
| 17 | Muf MU164 X | Clock SE211 II | Clock SE210 II | TAG MC125 III, | Muf MC231 II | Ram MC145A X | Tx CRC F9401 X | Tx FSM MC176 IIIIII | Tx SR MC141 X | Tx Fifo F145A X | Tx Par MC170 X | 8,10 MC105 III |
| 49 | | | | | | | | | | | | |
| 18 | | Clock SE210 II | Clock SE212 II | Muf MC173 X | Muf MC173 X | Muf MC173 X | ETX MU164 X | Tx CRC MC125 IIII | Clock SE210 II | Clock SE210 II | 9,10 MC104 IIII | FIFOs MC176 IIIIII |
| 19 | 3,5 MC100 IIII | MC195 IIIIII | CNT MC136 X | Disk Muf MC173 X | | | ERX MU164 X | ETX MU164 X | EFIFO MU164 X | Pend MC135 II | Coll MC135 II | GotBit MC135 II |
| 50 | | | | | | | | | | | | |
| 20 | Ram MC139 X | Ram F16 II | CNT MC136 X | TAG MC135 II | TAG MC173 X | TAG MC173 X | Rx PD MC176 X | ERX MU164 X | 8,12 MC124 IIII | Ether Clk K1115A X | TxGo MC231 II | Tx PE MC231 II |
| 21 | Ram MC139 X | Ram F16 X | CNT MC136 X | TAG MCM149 X | TAG MC173 X | TAG MC173 X | Rx PD F16 X | 9, PE MC106 III | Ether Clk MC210 II | Ether Clk MC136 X | Status MC170 X | EFIFO MU164 X |
| 51 | | | | | | | | | | | | |
| 22 | Ram F16 X | Muf MU164 X | Muf MU164 X | TAG F16 X | TAG MC125 IIII | TAG MC125 IIII | TAG 8T98 IIIII, | Rx PD MCM149 X | 10 MC231 I, | 7,10.11.13 MC102 IIII | 7, 8 MC135 II | Muf MC176 X |
| 23 | Temp LM3911 X | Dr Stat MC109 II | Dr Stat MC103 II,I | Muf MU164 X | TAG MC125 IIII | TAG MC125 IIII | TAG 8T98 IIIIII | Next,8 MC105 III | Next,7,12 MC104 IIII | Next MC113 ,III | Muf MU164 X | Muf MC176 X |
| 52 | | | | | SIP | SIP | | | | SIP | SIP | |
| 24 | Next MC195 IIIIII | Dr Stat MC124 IIII | Dr Stat MC124 IIII | Clock MC103 IIII | Muf MU164 X | Muf MU164 X | TAG 8T98 IIIIII | Next MC176 IIIIII | Next MC104 IIII | 5,6,13 MC176 IIII,, | Muf MC166 X | Muf MC102 IIII |

| | |
|---|---|
| 31 | chips common to Disk & Ether |
| 137 | chips specific to Disk |
| 111 | chips specific to Ether |
| 9 | spare chip positions |
| 288 | total chip positions |

| XEROX PARC | Project | Reference | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Stitch-Weld board Layout | DskEth05.sil | Bates/Boggs | Ce | 9/24/79 | 05 |

Cut SIP legs at k52 to set the
Muffler addresses for the board.
* Standard addresses are 2000-2177.

| | Muff Addr | P5 | P6 | P7 | P8 |
|---|---|---|---|---|---|
| | 0000-0177 | cut | cut | cut | cut |
| | 0200-0377 | cut | cut | cut | |
| | 0400-0577 | cut | cut | | cut |
| | 0600-0777 | cut | cut | | |
| | 1000-1177 | cut | | cut | cut |
| | 1200-1377 | cut | | cut | |
| | 1400-1577 | cut | | | cut |
| | 1600-1777 | cut | | | |
| * | 2000-2177 | | cut | cut | cut |
| | 2200-2377 | | cut | cut | |
| | 2400-2577 | | cut | | cut |
| | 2600-2777 | | cut | | |
| | 3000-3177 | | | cut | cut |
| | 3200-3377 | | | cut | |
| | 3400-3577 | | | | cut |
| | 3600-3777 | | | | |

Cut SIP legs at j52 to set the
Task numbers for the Ethernet.
* Standard tasks are 6 & 7.

| | Tasks | P6 | P7 | P8 |
|---|---|---|---|---|
| | 2 & 3 | | | cut |
| | 4 & 5 | | cut | |
| * | 6 & 7 | | cut | cut |
| | 8 & 9 | cut | | |
| | 10 & 11 | cut | | cut |
| | 12 & 13 | cut | cut | |
| | 14 & 15 | cut | cut | cut |

Cut SIP legs at e41 to set the
IOA bus addresses for the board.
* Standard addresses are 10-17.

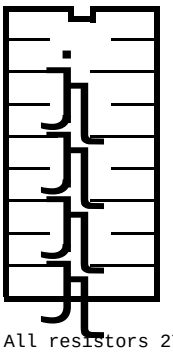
| | IOA | P4 | P5 | P6 | P7 | P8 |
|---|---|---|---|---|---|---|
| | 000-007 | cut | cut | cut | cut | cut |
| * | 010-017 | cut | cut | cut | cut | |
| | 020-027 | cut | cut | cut | | cut |
| | 030-037 | cut | cut | cut | | |
| | 040-047 | cut | cut | | cut | cut |
| | 050-057 | cut | cut | | cut | |
| | 060-067 | cut | cut | | | cut |
| | 070-077 | cut | cut | | | |
| | 100-107 | cut | | cut | cut | cut |
| | 110-117 | cut | | cut | cut | |
| | 120-127 | cut | | cut | | cut |
| | 130-137 | cut | | cut | | |
| | 140-147 | cut | | | cut | cut |
| | 150-157 | cut | | | cut | |
| | 160-167 | cut | | | | cut |
| | 170-177 | cut | | | | |
| | 200-207 | | cut | cut | cut | cut |
| | 210-217 | | cut | cut | cut | |
| | 220-227 | | cut | cut | | cut |
| | 230-237 | | cut | cut | cut | |
| | 240-247 | | cut | | cut | cut |
| | 250-257 | | cut | | | |
| | 260-267 | | cut | | | cut |
| | 270-277 | | cut | | | |
| | 300-307 | | | cut | cut | cut |
| | 310-317 | | | cut | cut | |
| | 320-327 | | | cut | | cut |
| | 330-337 | | | cut | | |
| | 340-347 | | | | cut | cut |
| | 350-357 | | | | cut | |
| | 360-367 | | | | | cut |
| | 370-377 | | | | | |

The EtherFifo ROMs are identical and interchangeable.
The DiskRead, EtherRcvr and EtherXmtr ROMs are not.

| Name | Type | # | Location |
|---|---|---|---|
| DskEth | | | |
| Disk | | | |
| DiskRead | SG139 | 2 | a20 a21 |
| DiskTag | MC149 | 1 | d21 |
| DiskUnits | S288 | 1 | d05 |
| DiskFifo | MC149 | 1 | b14 |
| Ether | | | |
| EtherPD | MC149 | 1 | h22 |
| EtherRcvr | MC149 | 3 | h09 h10 h11 |
| EtherFifo | MC149 | 2 | l10 l15 |
| EtherXmtr | MC149 | 3 | h14 h15 h16 |

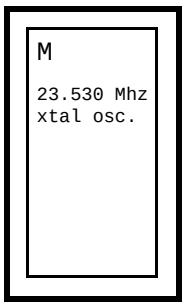
"DoradoProms DskEth" gets all proms for the DskEth board.
"DoradoProms Disk" gets all proms for the Trident half of the board.
"DoradoProms Ether" gets all proms for the Ethernet half of the board.

PLAT at a04

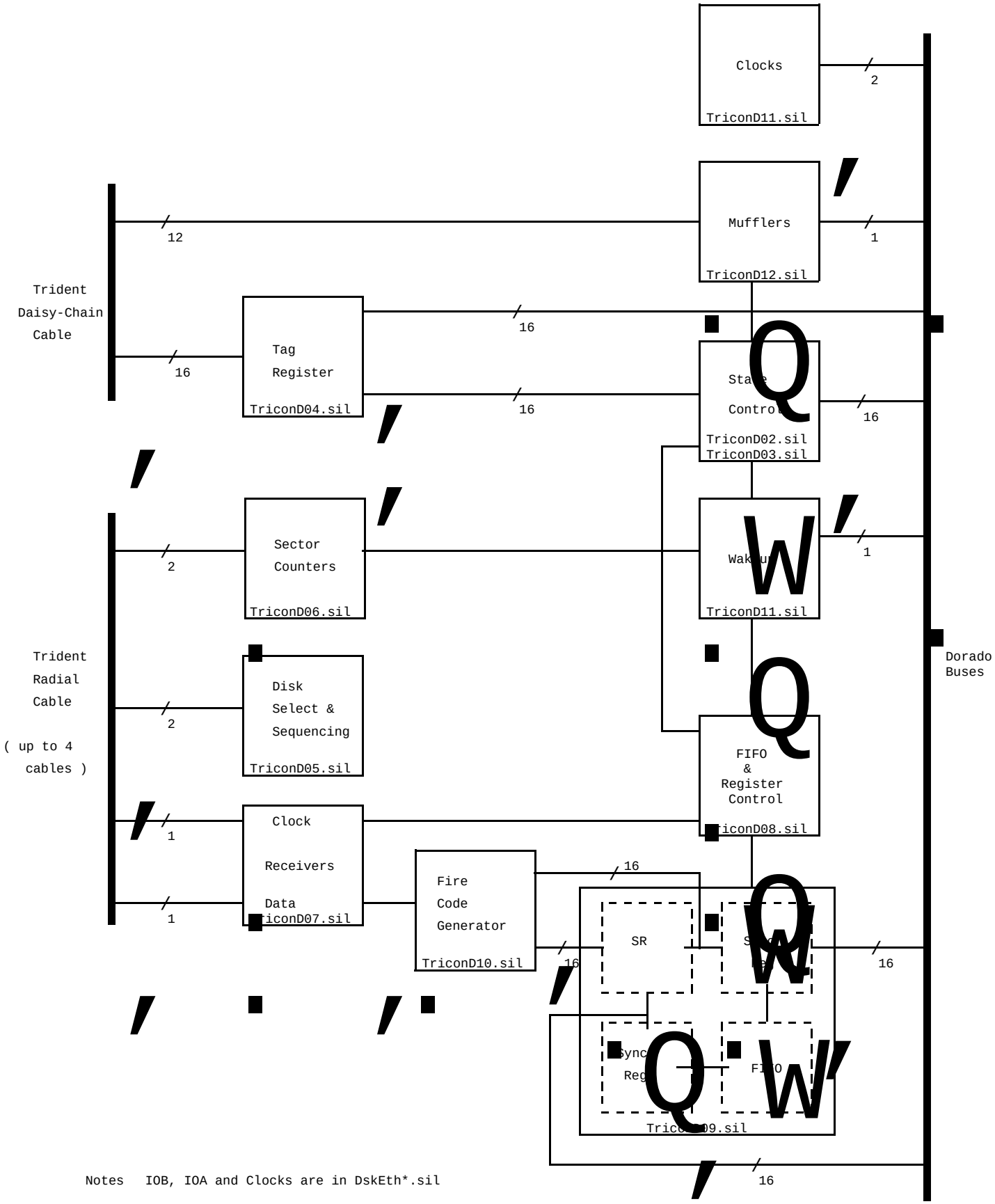


All resistors 27K
All capacitors 330pf

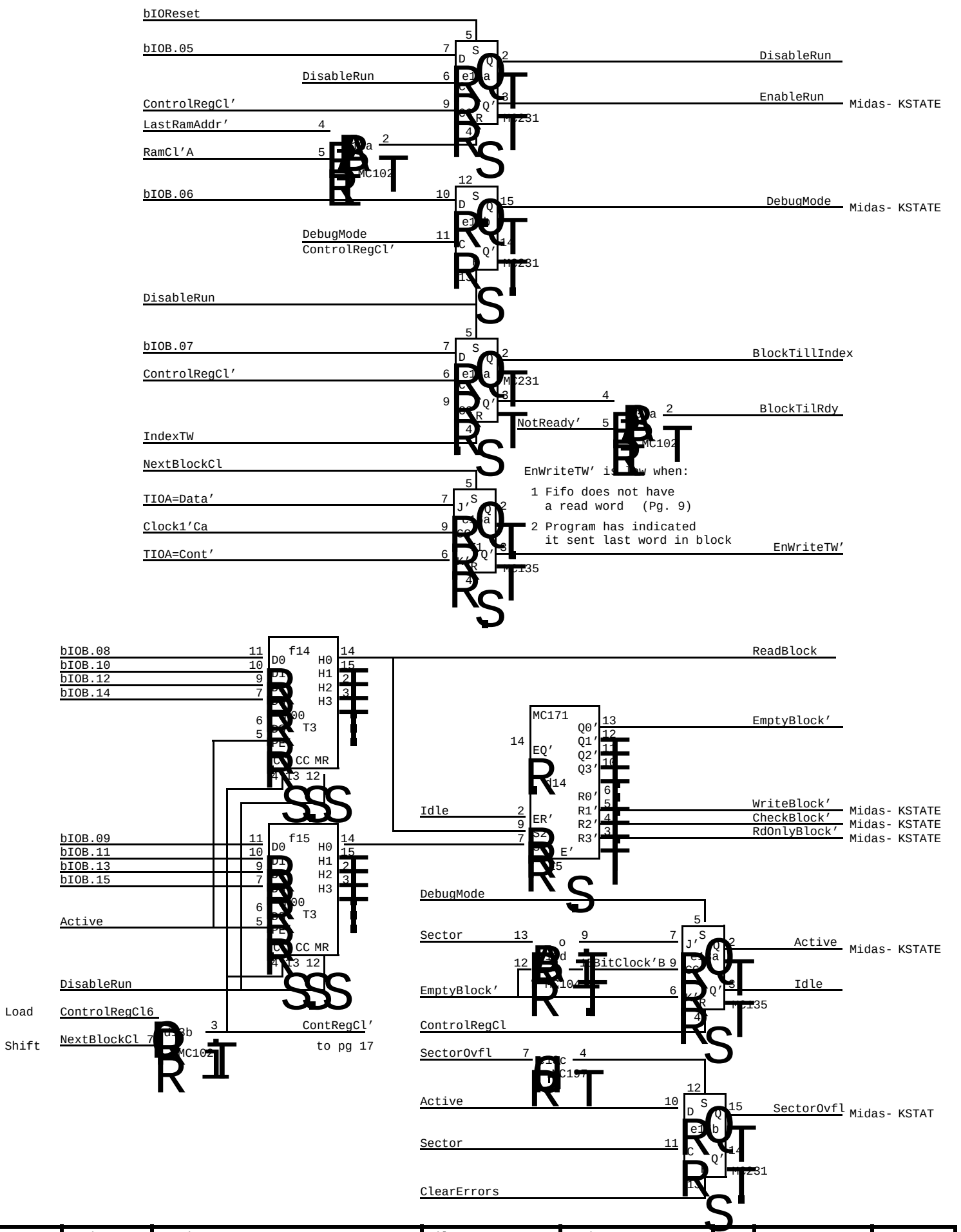
K1115A at j20



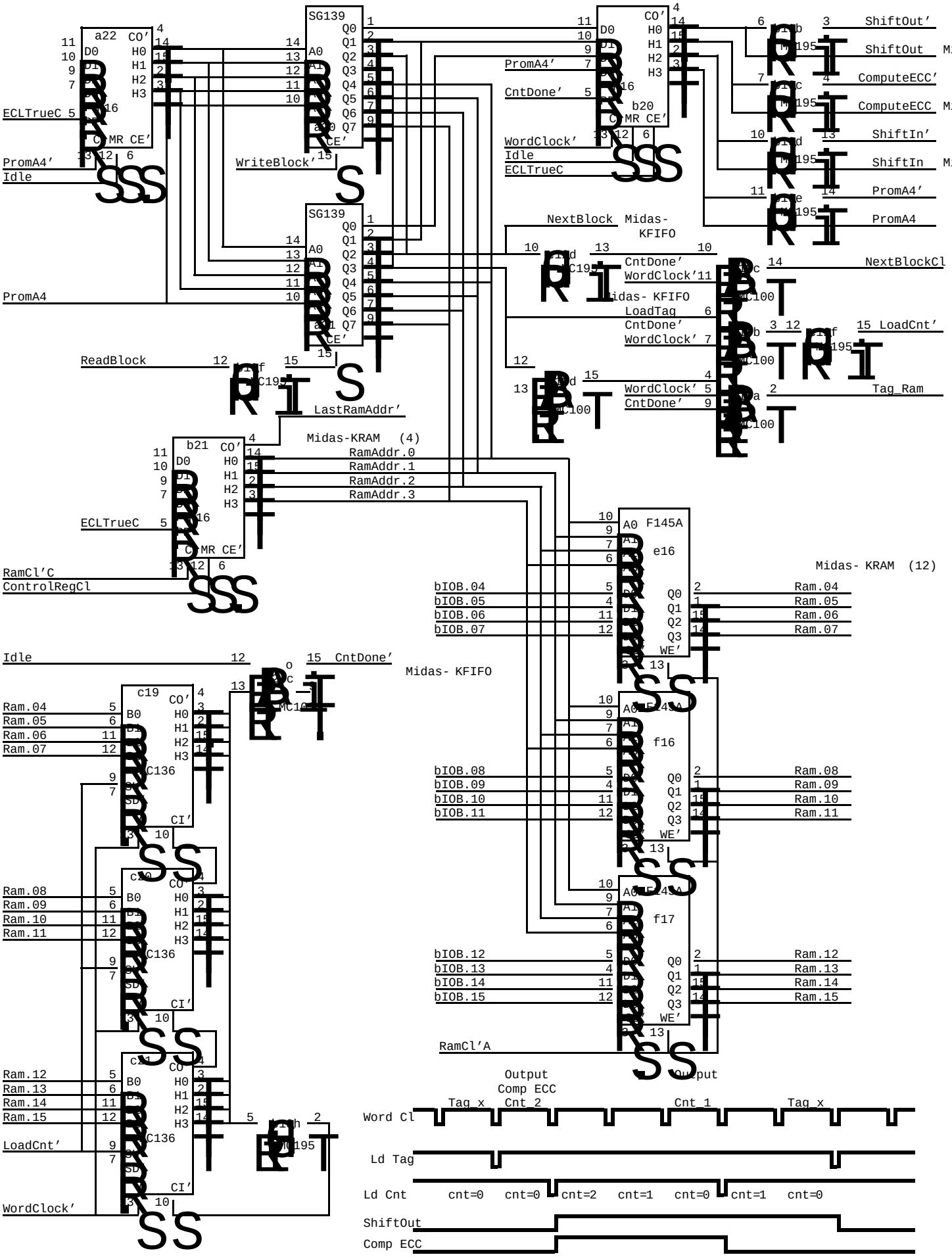

Logo is near pin 1.
This is a 14 pin pkg.
Board pins 8 & 9 aren't used.
Remove bypass cap above pin 1



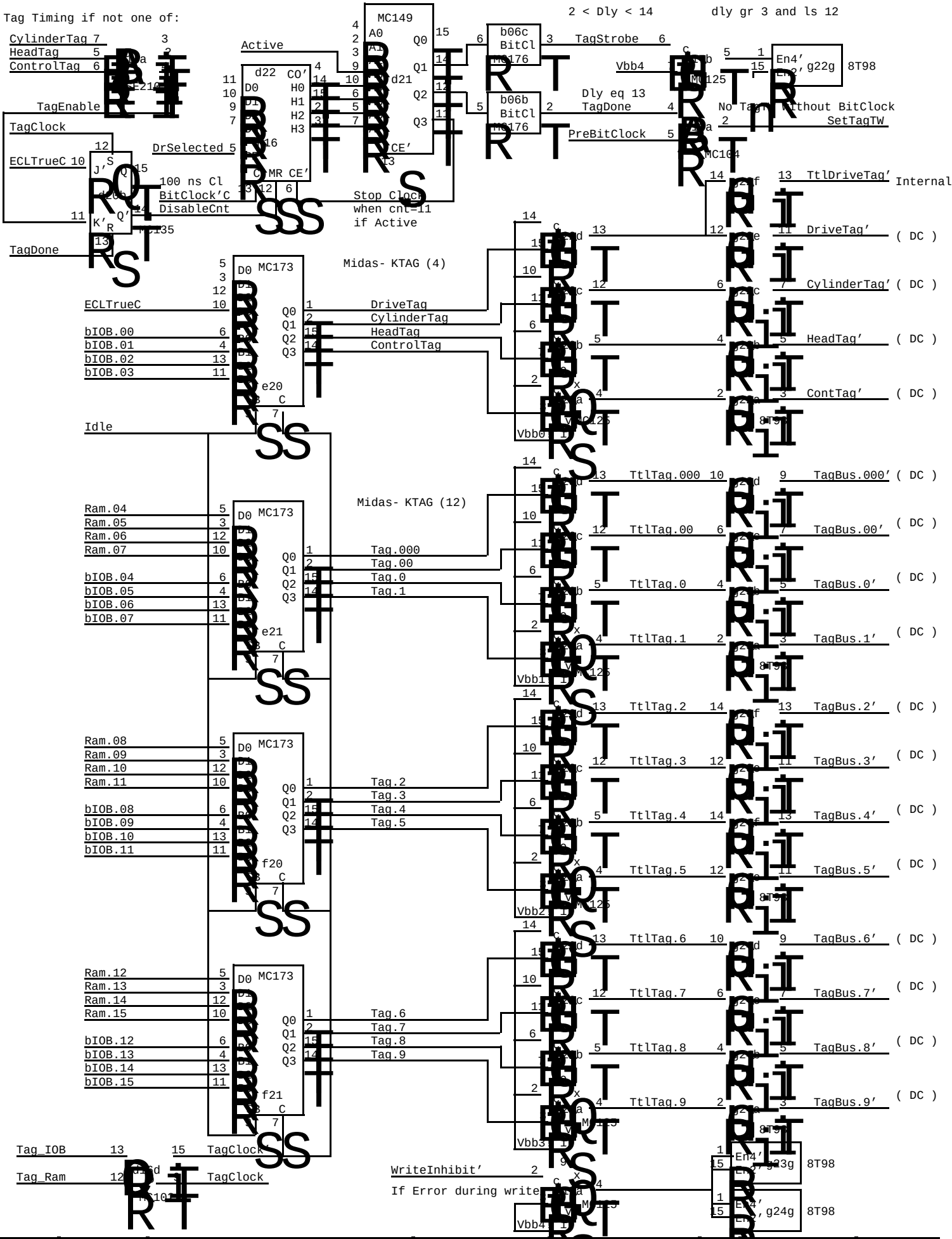

| XEROX PARC | Project | Reference | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Dorado Disc Controller | TriconD01.sil | Roger Bates | Ce | 7/19/79 | 07 |



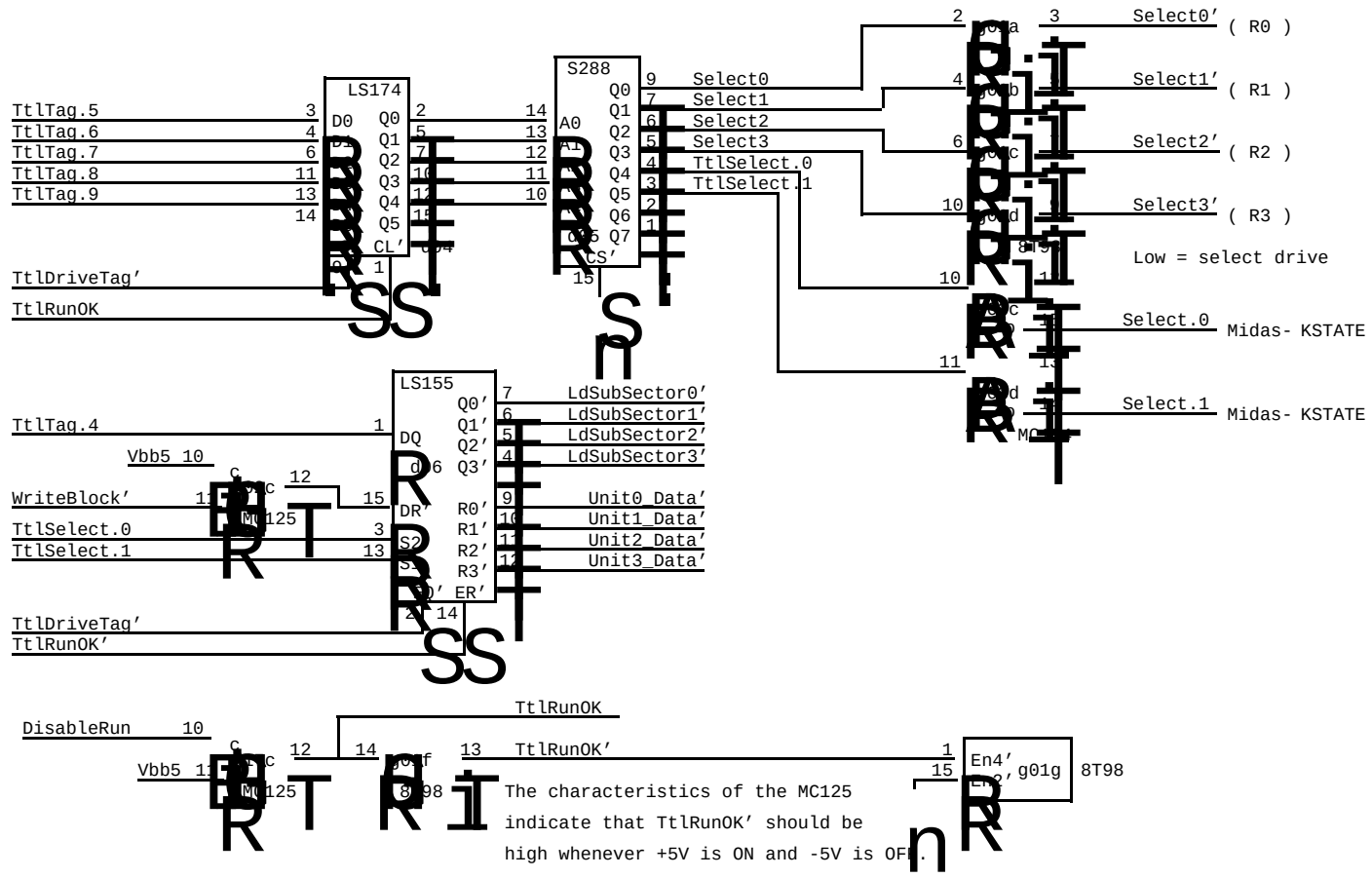

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | State Control Register | TriconD02.sil | Roger Bates | Ce | 9/24/79 | 08 |

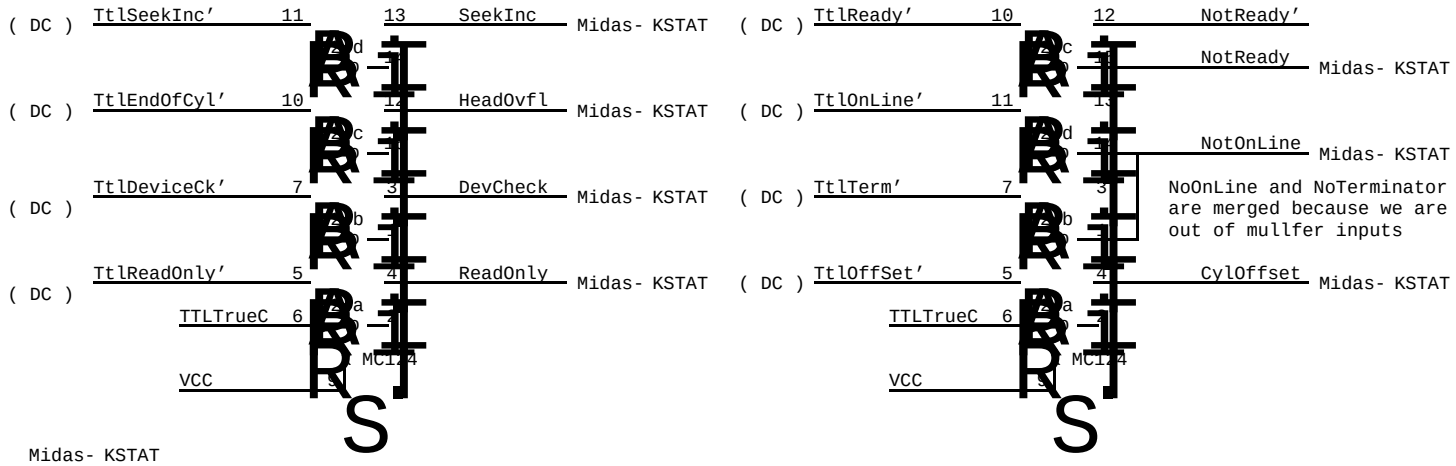


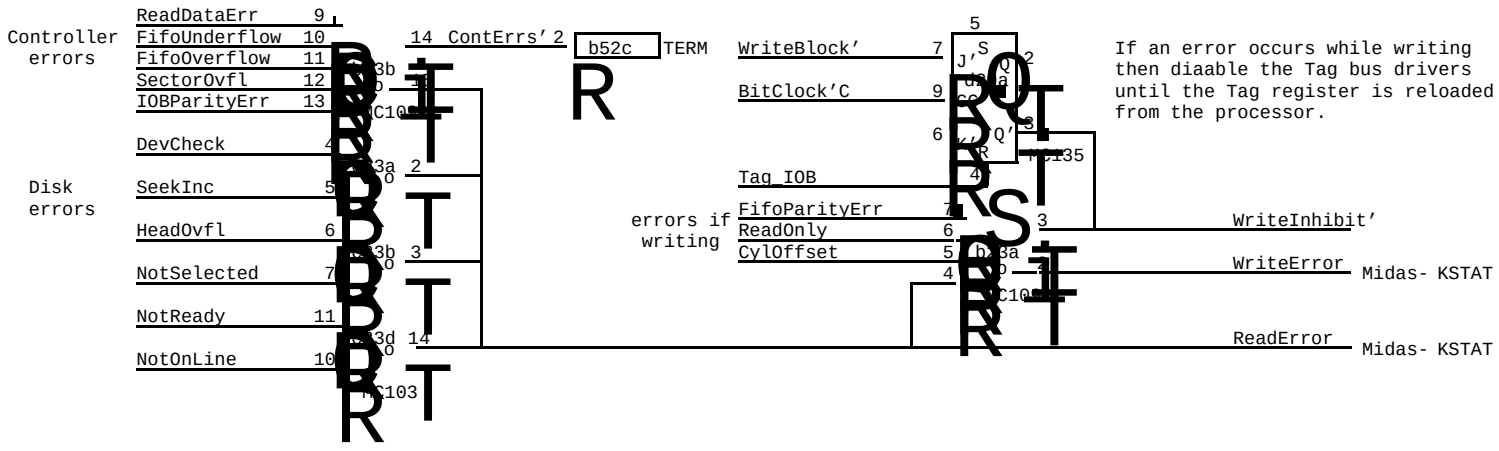

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Control RAM and Format Counter | TriconD03.sil | Roger Bates | Ce | 9/24/79 | 09 |



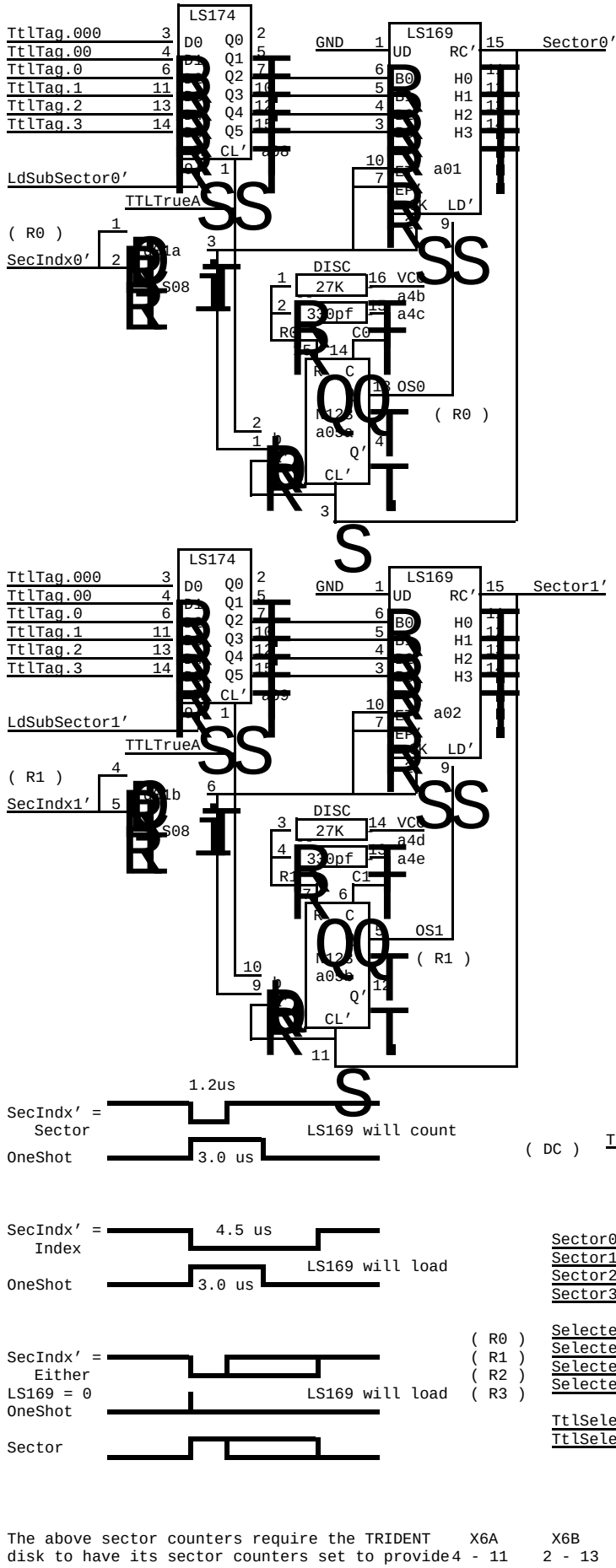

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | TAG register & Bus Drivers | TriconD04.sil | Roger Bates | Ce | 7/23/79 | 10 |



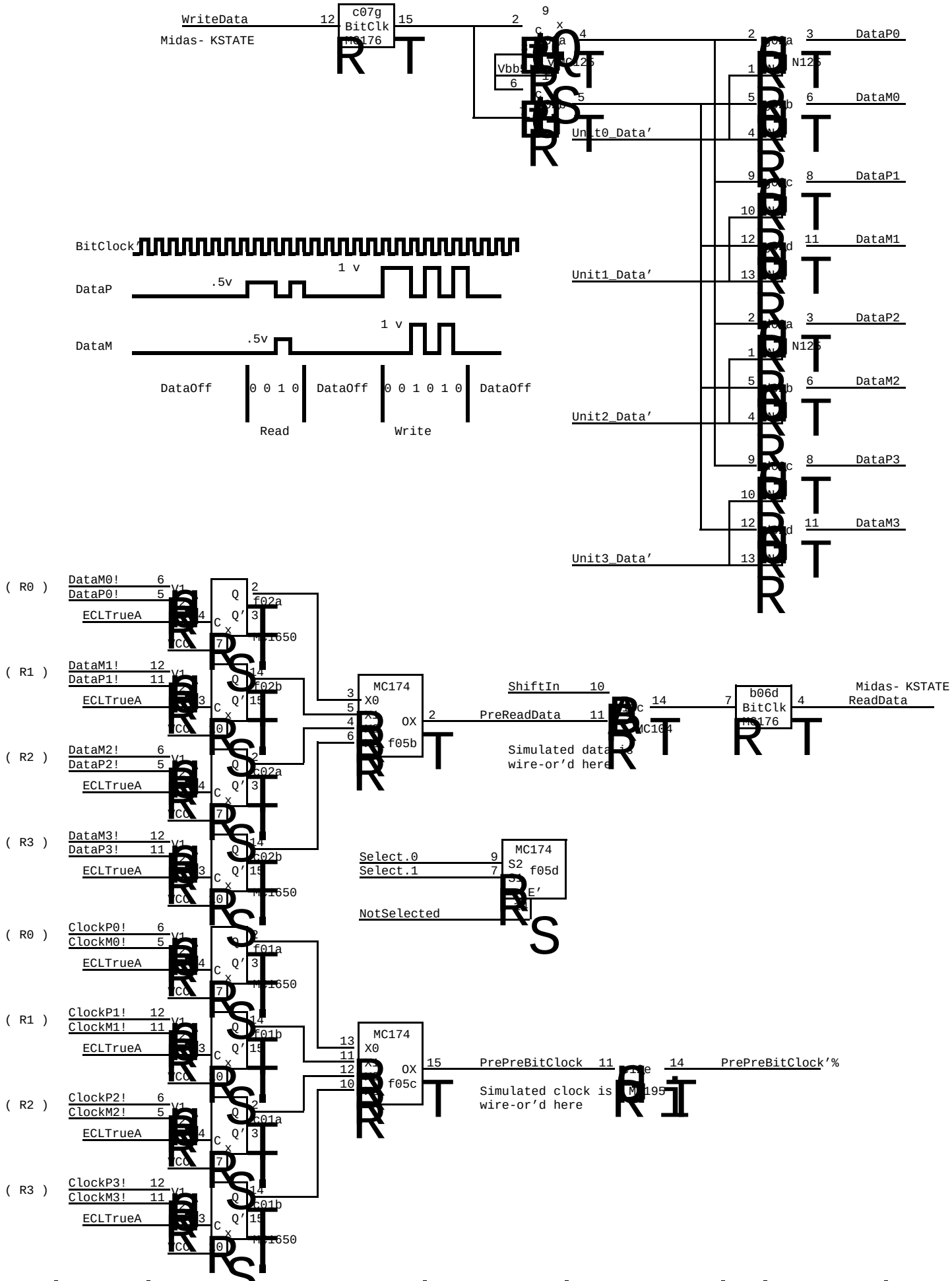

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Disk Drive Control | TriconD05.sil | Roger Bates | Ce | 7/23/79 | 11 |



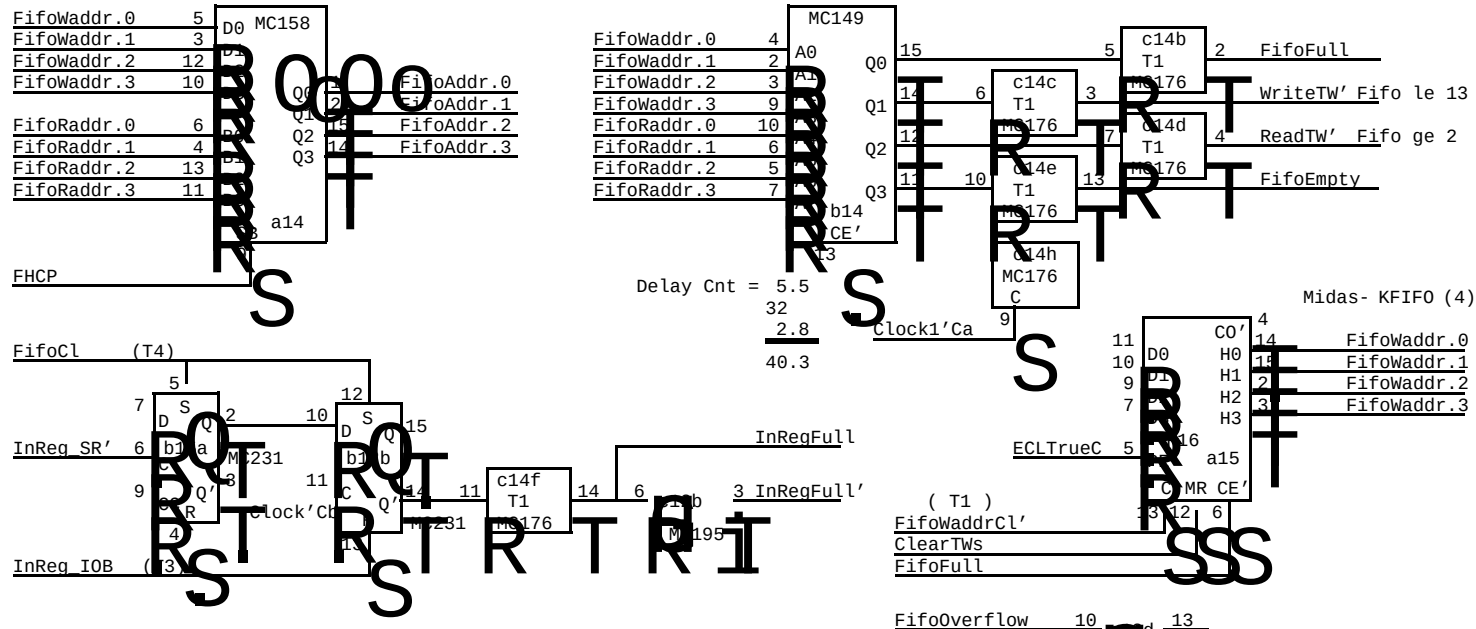

The above sector counters require the TRIDENT disk to have its sector counters set to provide 117 "sub-sector" pulses per revolution. This is done by setting the disk jumpers as follows:

| | X6A | X6B |
|---|---|---|
| | 4 - 11 | 2 - 13 |
| | 5 - 10 | 3 - 12 |
| | | 4 - 11 |
| | | 5 - 10 |
| | | 6 - 09 |

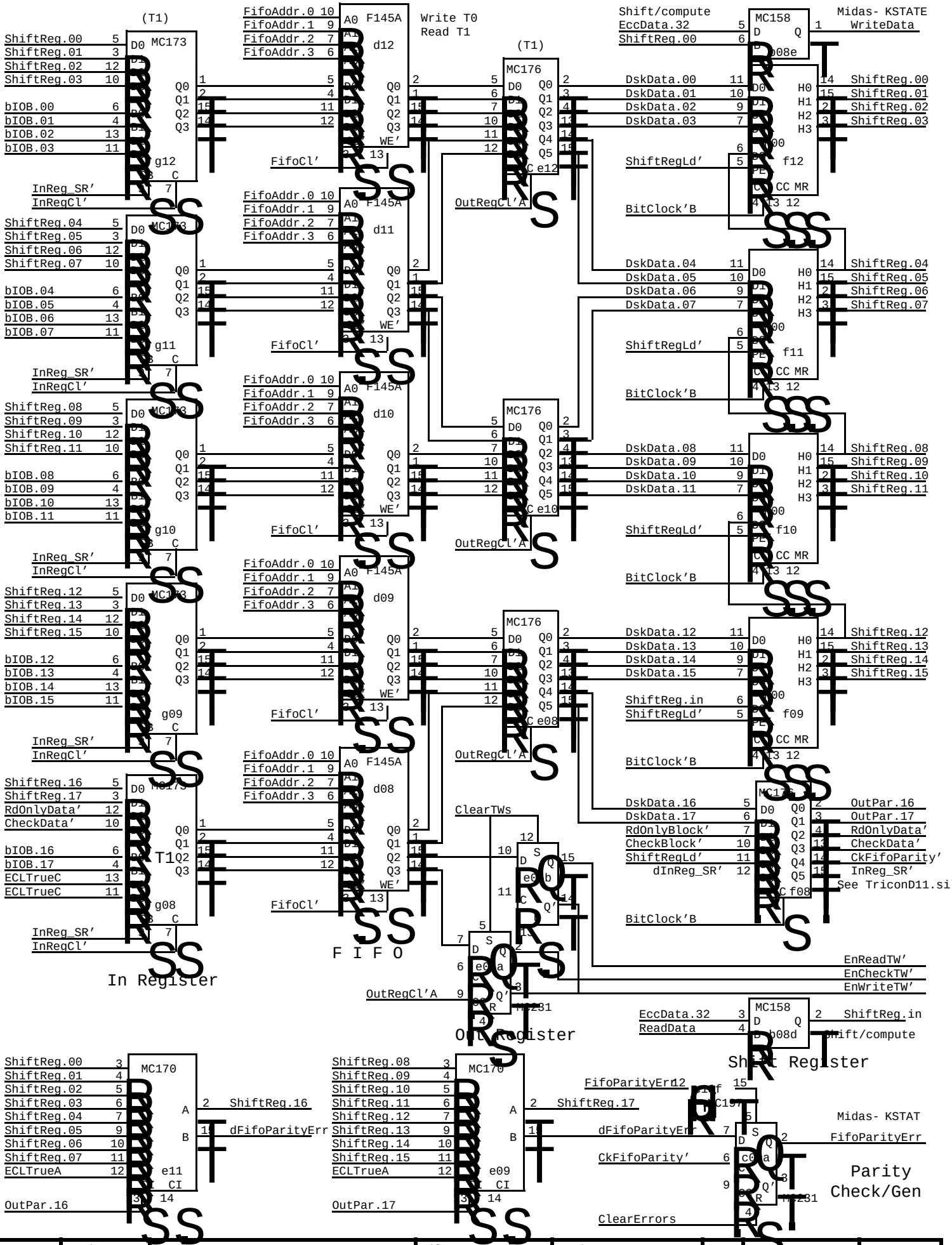
| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Sector Length Counters | TriconD06.sil | Roger Bates | Ce | 7/24/79 | 12 |




| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Clock and Data Input | TriconD07.sil | Roger Bates | Ce | 7/23/79 | 13 |

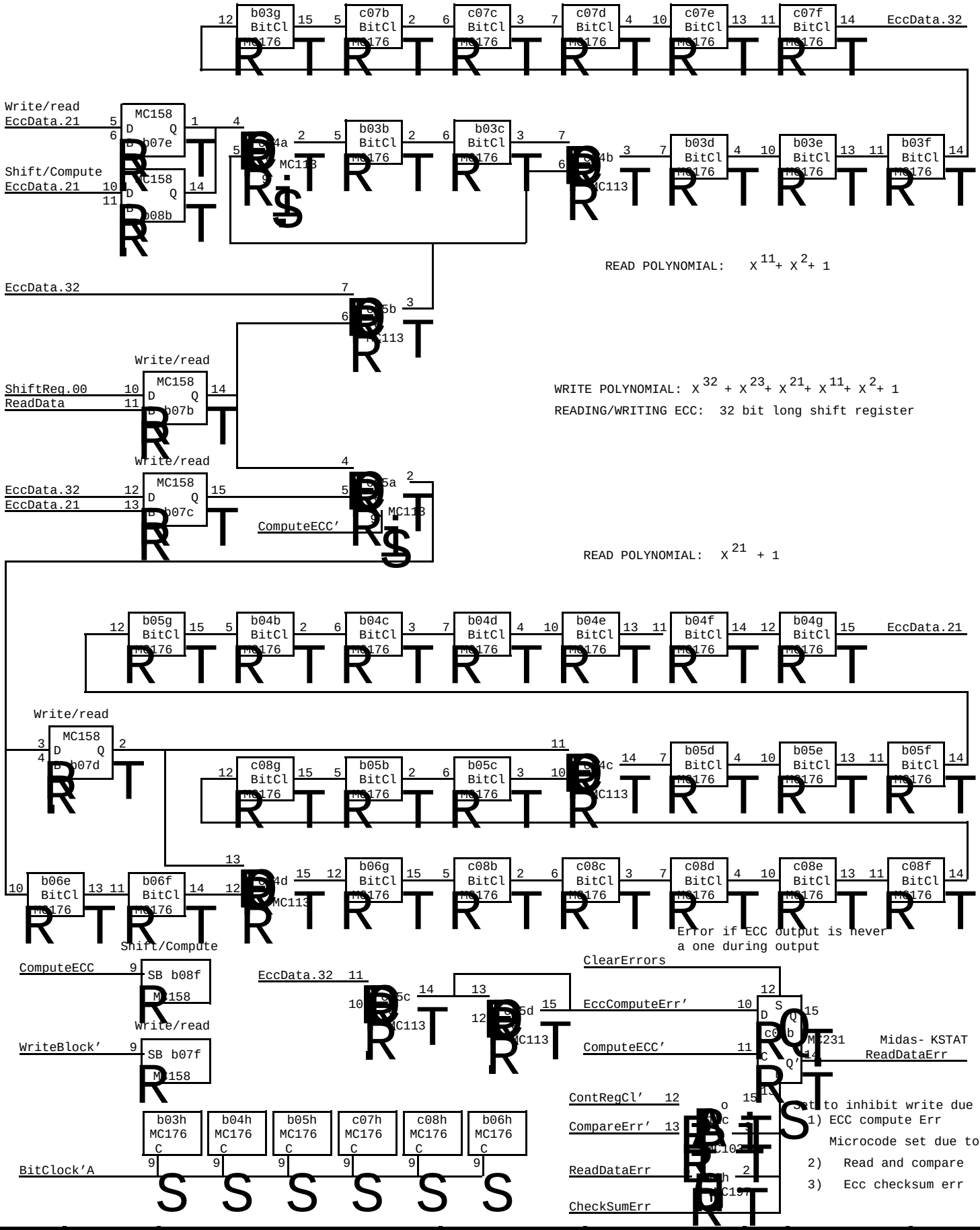



| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | F I F O Control | TriconD08.sil | Roger Bates | Ce | 9/24/79 | 14 |

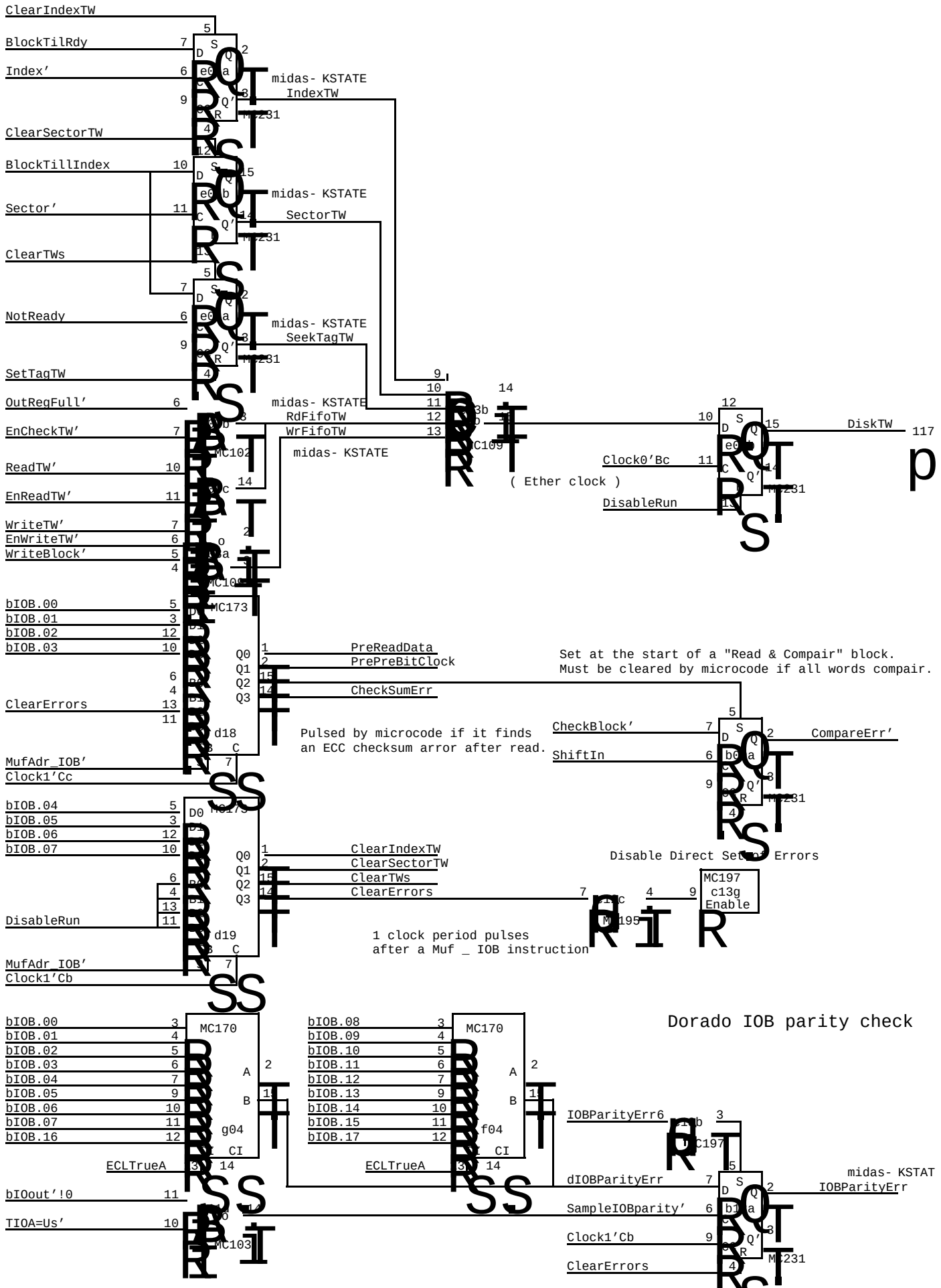



| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | F I F O and Shift Register | TriconD09.sil | Roger Bates | Ce | 7/08/79 | 15 |

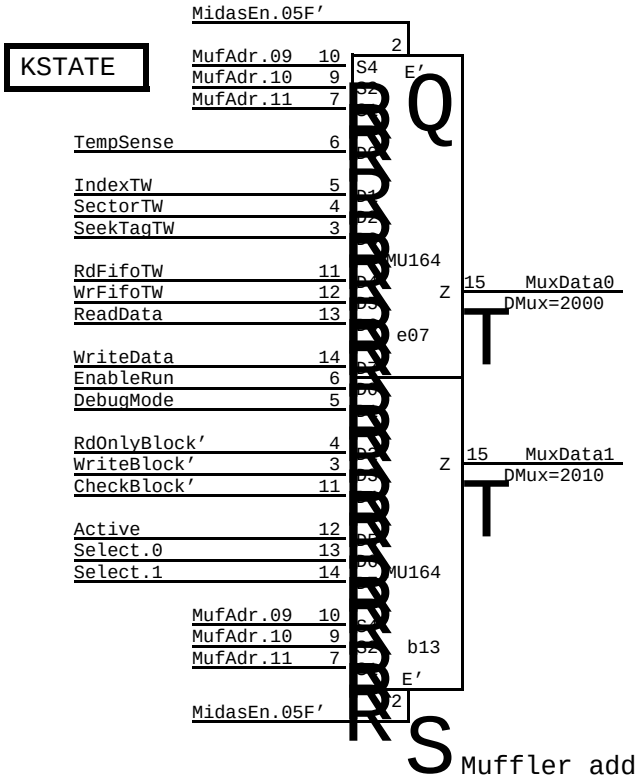
# POLYNOMIAL DIVIDER FOR FIRE CODE GENERATION

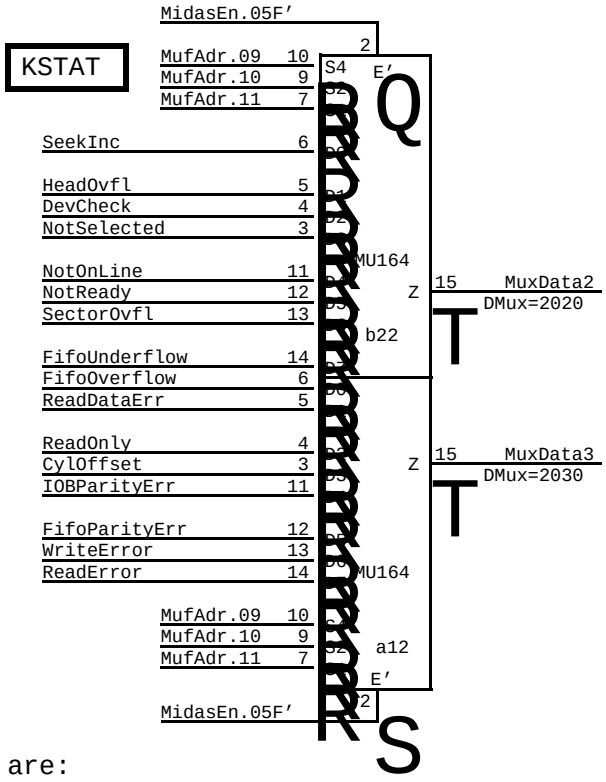



| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Fire Code Generator | TriconD10.sil | Roger Bates | Ce | 7/08/79 | 16 |




| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Buss Parity Task Wake-Up | TriconD11.sil | Roger Bates | Ce | 7/08/79 | 17 |

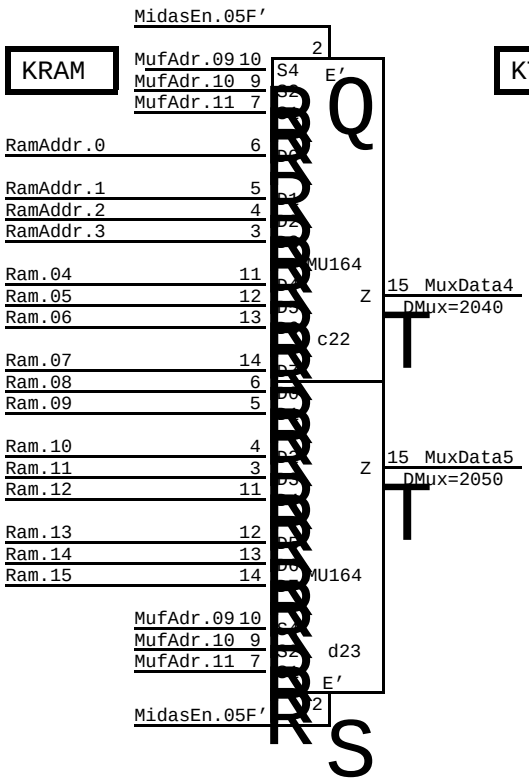


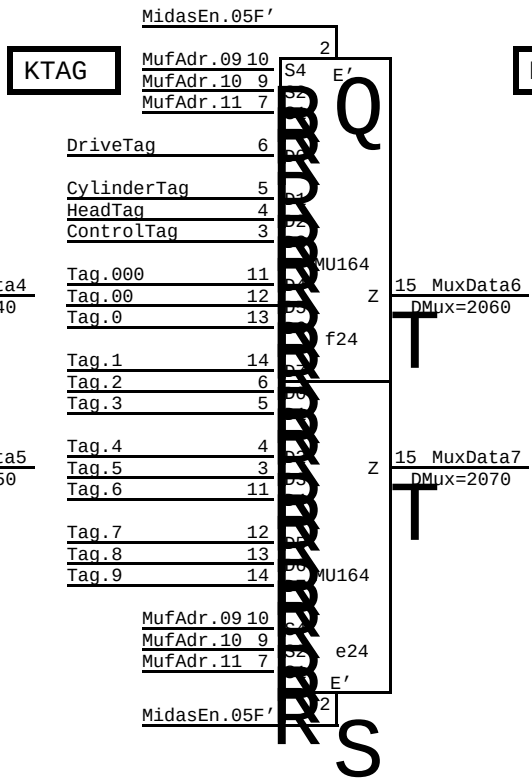



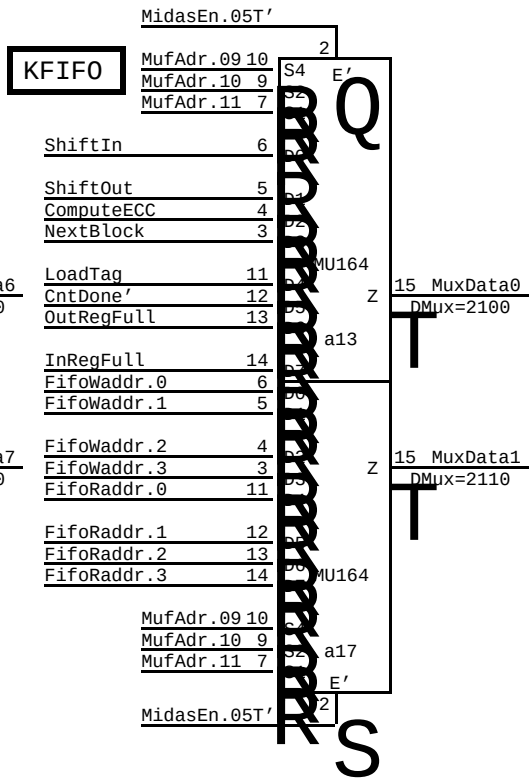

Muffler addresses are:

Value listed for Program input
Value plus 2000 for Midas input

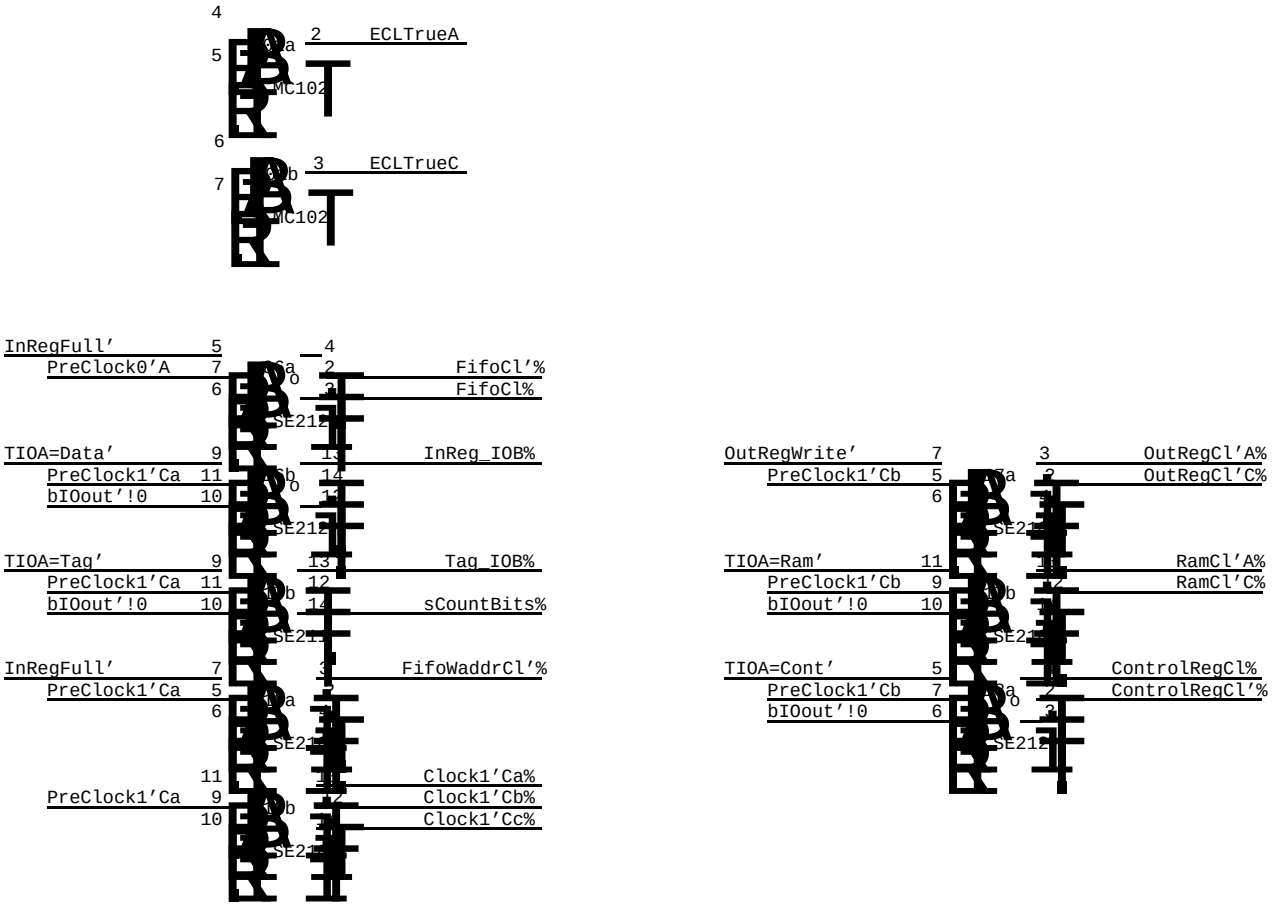
Values from 120 to 177 are
used by the Ethernet



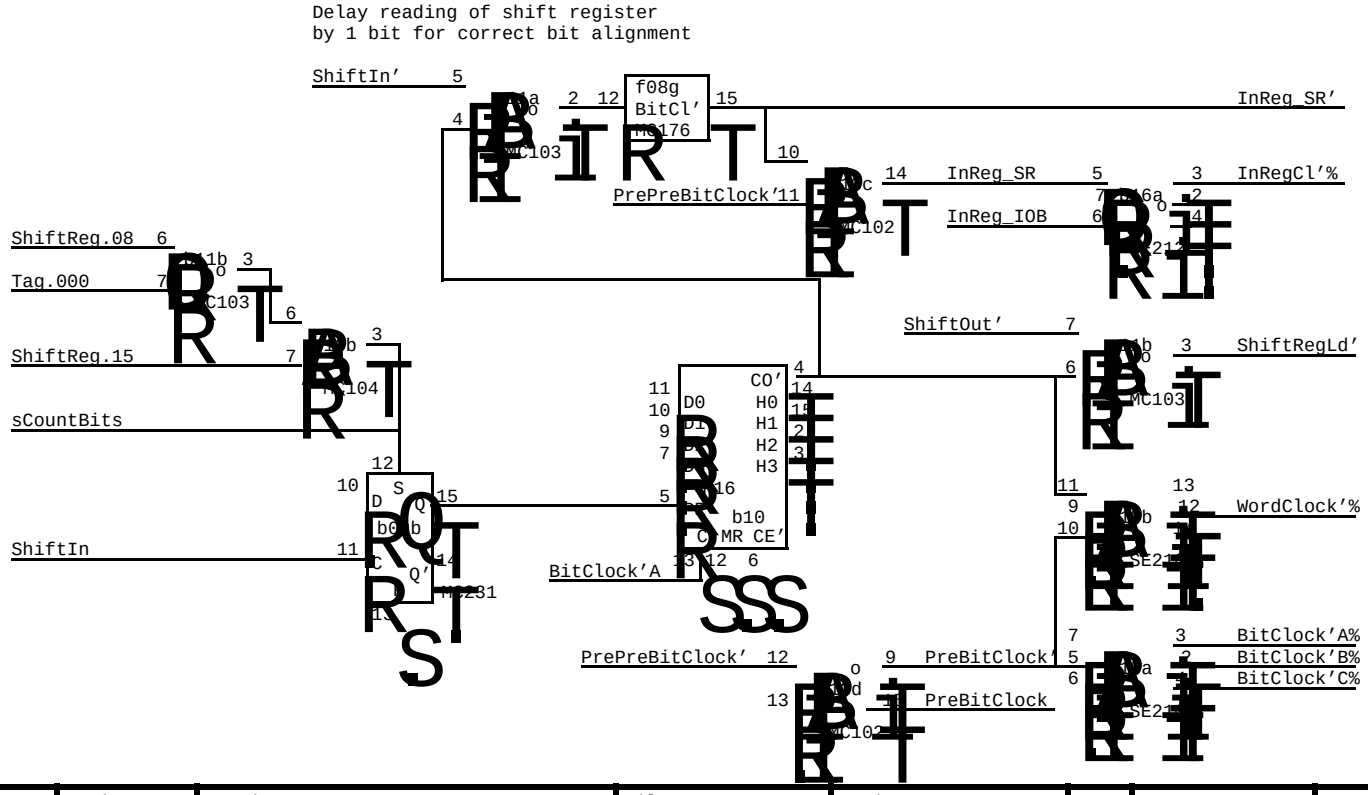

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | DMUX CONTROL | TriconD12.sil | Roger Bates | Ce | 7/08/79 | 18 |



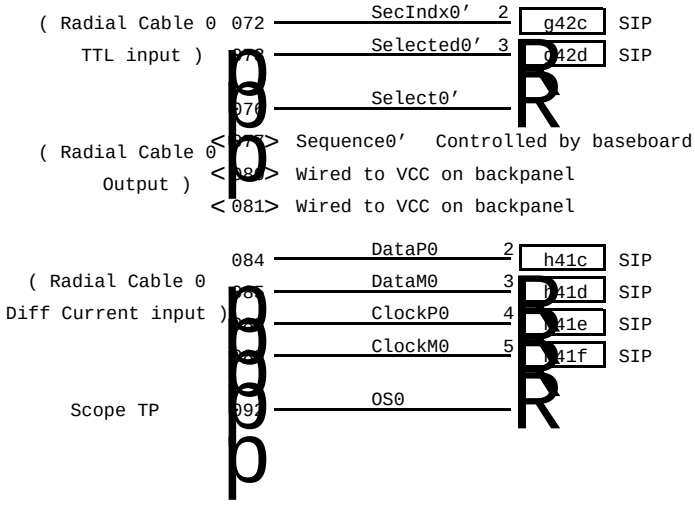

System Clocks

---

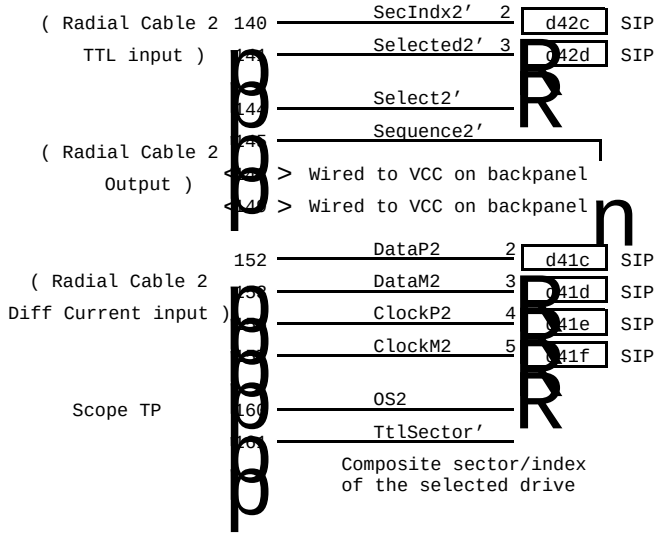
Disk Clocks



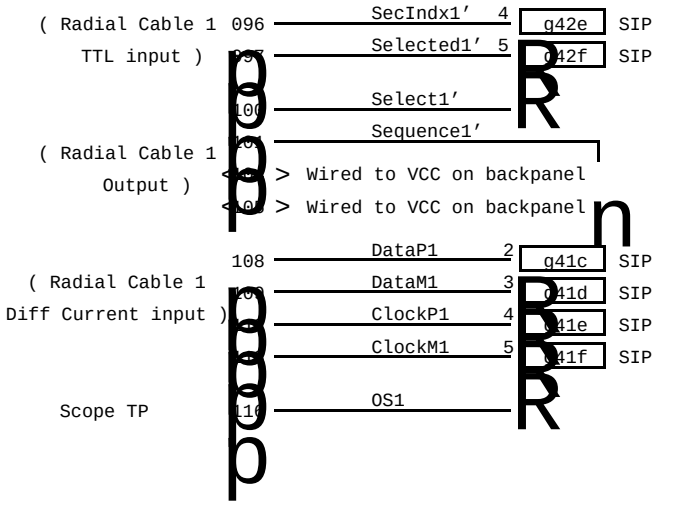
## Radial Cable for Drive 0



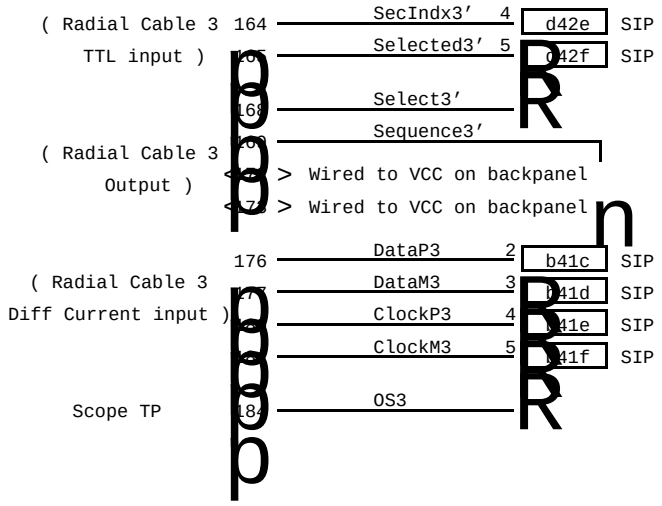

## Radial Cable for Drive 2



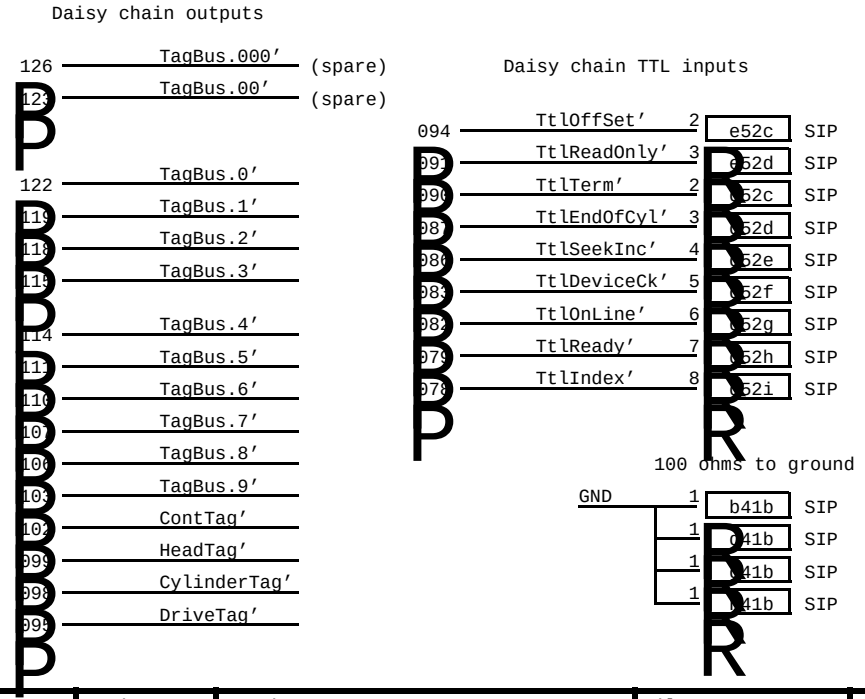

## Radial Cable for Drive 1



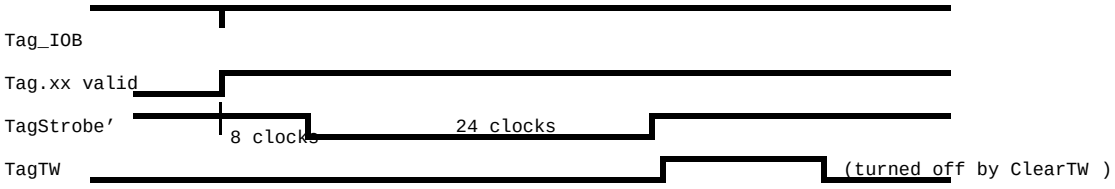

## Radial Cable for Drive 3



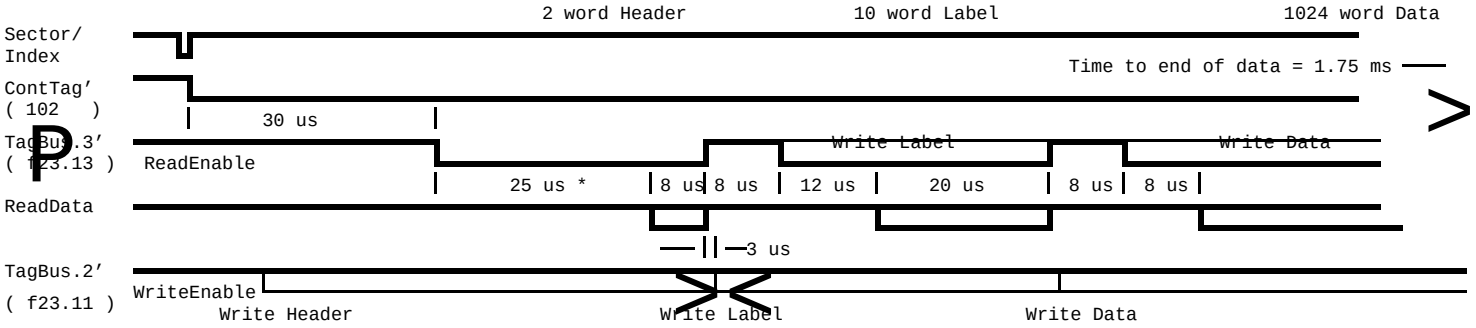

## Daisy Chain Cable



## Head or Cylinder Tag Instruction



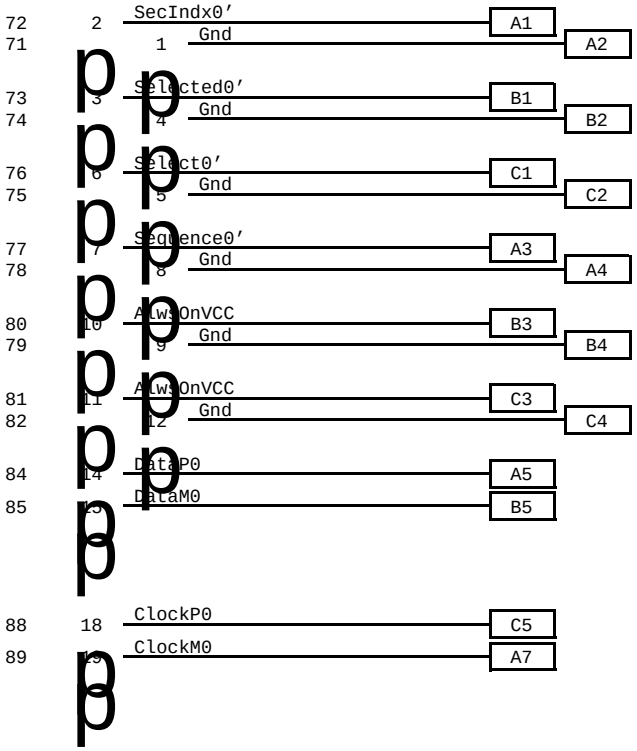

## Read or Write Instruction




* This value if for reading a pack on the same drive that Headers were written
It may vary by +/- 15 us on other drives

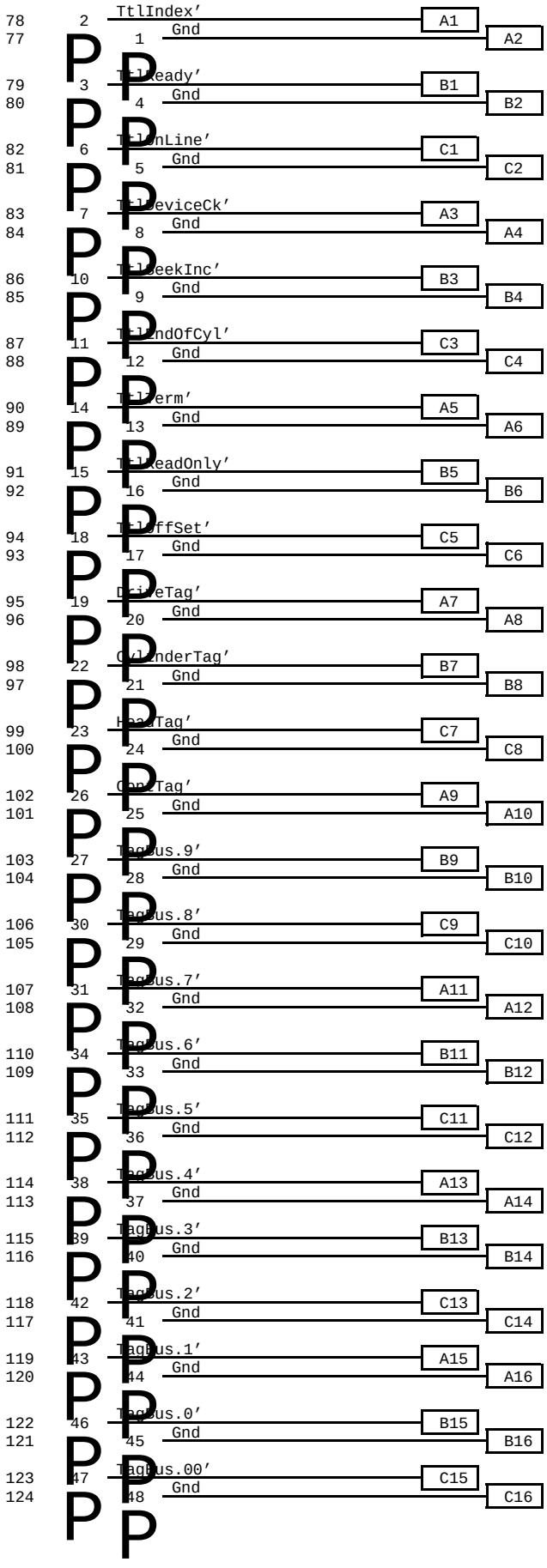
## Radial Cable for Drive 0

AMP 204729-1




## DAISEY CHAIN CABLE

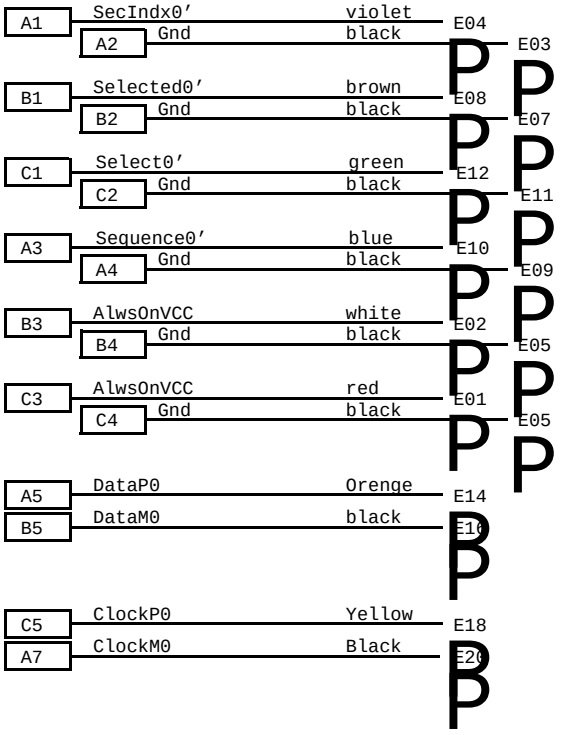
AMP 204733-1



## Radial Cable for Drive 0

AMP 204742-1

Cal-Comp
Assembly 12433



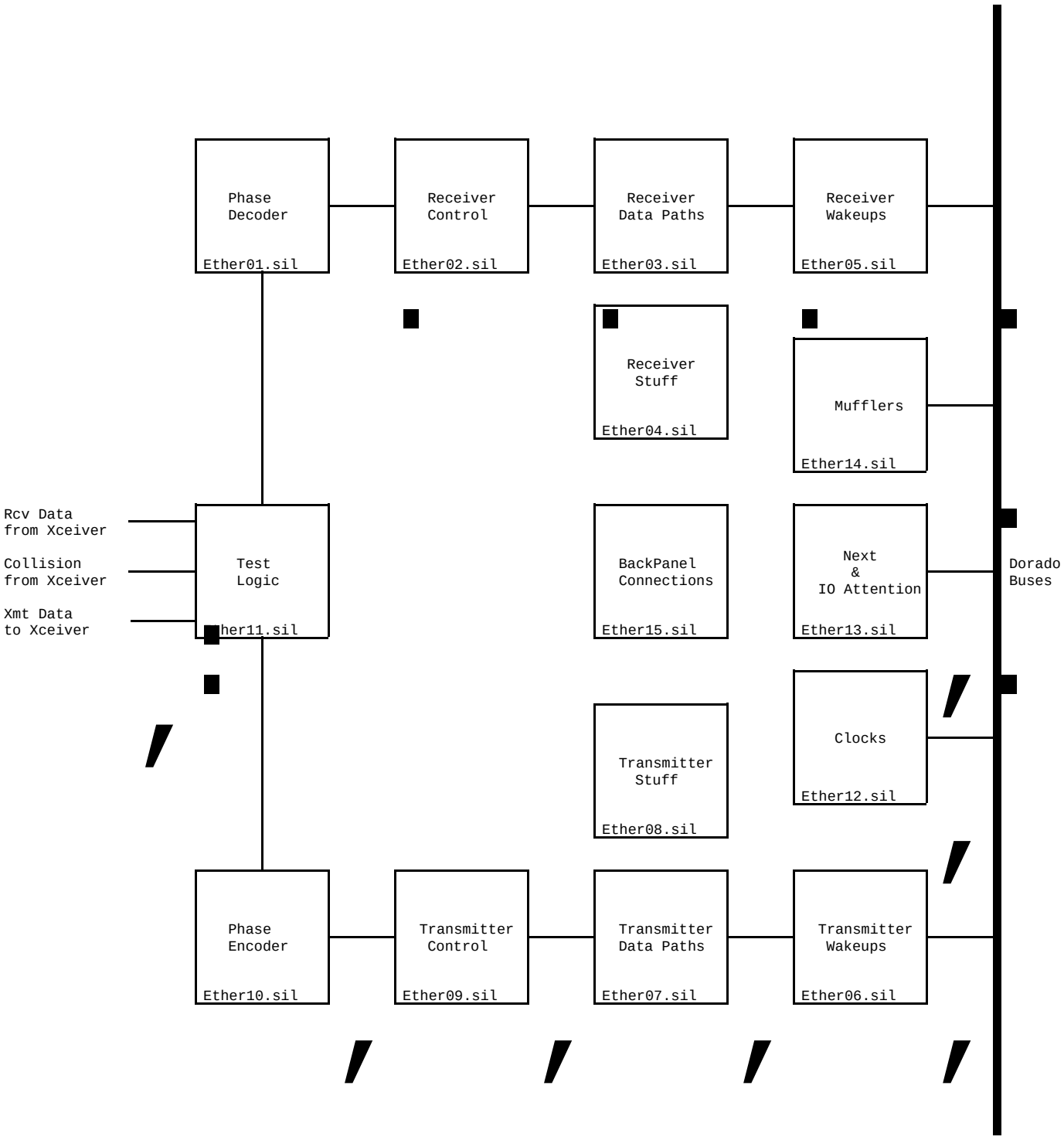

## DAISEY CHAIN CABLE

AMP 204746-1

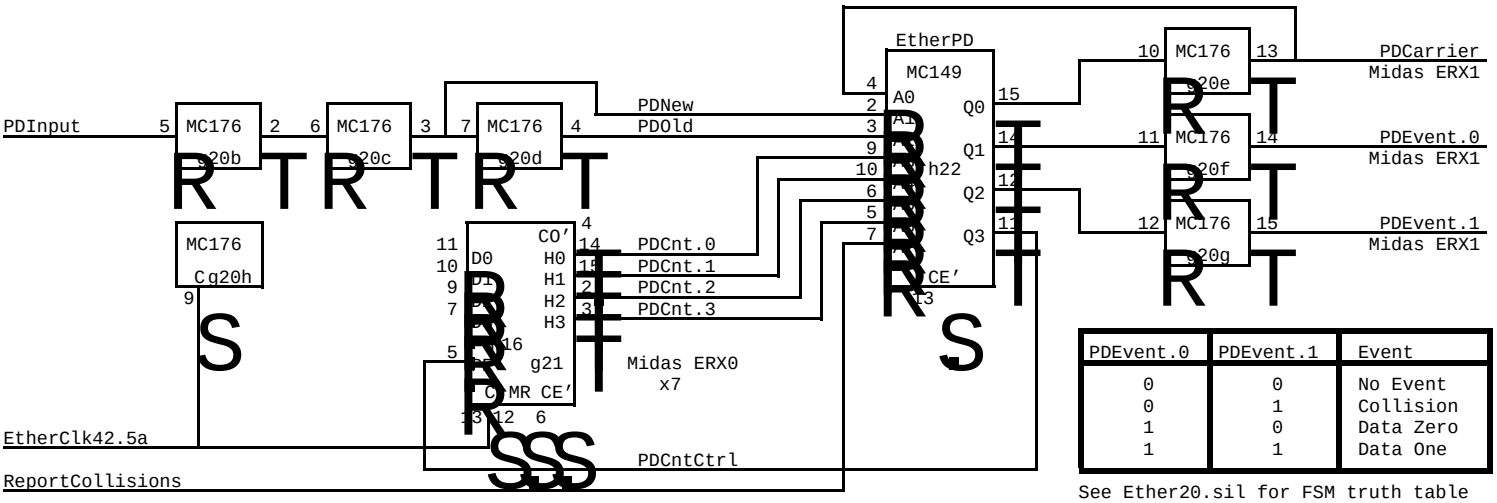
Cal-Comp
Assembly 12424

| | | | | |
|---|---|---|---|---|
| A1 | TtlIndex' | | E06 | |
| A2 | Gnd | | | E06G |
| B1 | TtlReady' | | E08 | |
| B2 | Gnd | | | E08G |
| C1 | TtlOnLine' | | E14 | |
| C2 | Gnd | | | E14G |
| A3 | TtlDeviceCk' | | E12 | |
| A4 | Gnd | | | E12G |
| B3 | TtlSeekInc' | | E16 | |
| B4 | Gnd | | | E16G |
| C3 | TtlEndOfCyl' | | E02 | |
| C4 | Gnd | | | E02G |
| A5 | TtlTerm' | | E35 | |
| A6 | Gnd | | | E35G |
| B5 | TtlReadOnly' | | E10 | |
| B6 | Gnd | | | E10G |
| C5 | TtlOffSet' | | E04 | |
| C6 | Gnd | | | E04G |
| A7 | Not used | | | |
| A8 | Gnd | | | |
| B7 | CylinderTag' | | E39 | |
| B8 | Gnd | | | E39G |
| C7 | HeadTag' | | E40 | |
| C8 | Gnd | | | E40G |
| A9 | ContTag' | | E37 | |
| A10 | Gnd | | | E37G |
| B9 | TagBus.9' | | E38 | |
| B10 | Gnd | | | E38G |
| C9 | TagBus.8' | | E36 | |
| C10 | Gnd | | | E36G |
| A11 | TagBus.7' | | E34 | |
| A12 | Gnd | | | E34G |
| B11 | TagBus.6' | | E32 | |
| B12 | Gnd | | | E32G |
| C11 | TagBus.5' | | E30 | |
| C12 | Gnd | | | E30G |
| A13 | TagBus.4' | | E28 | |
| A14 | Gnd | | | E28G |
| B13 | TagBus.3' | | E26 | |
| B14 | Gnd | | | E26G |
| C13 | TagBus.2' | | E24 | |
| C14 | Gnd | | | E24G |
| A15 | TagBus.1' | | E22 | |
| A16 | Gnd | | | E22G |
| B15 | TagBus.0' | | E20 | |
| B16 | Gnd | | | E20G |
| C15 | Not used | | | |
| C16 | Gnd | | | |

| XEROX PARC | Project | Reference | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Dorado to Trident Cables | TriconD17.sil | Roger Bates | Ce | 7/08/79 | 22b |



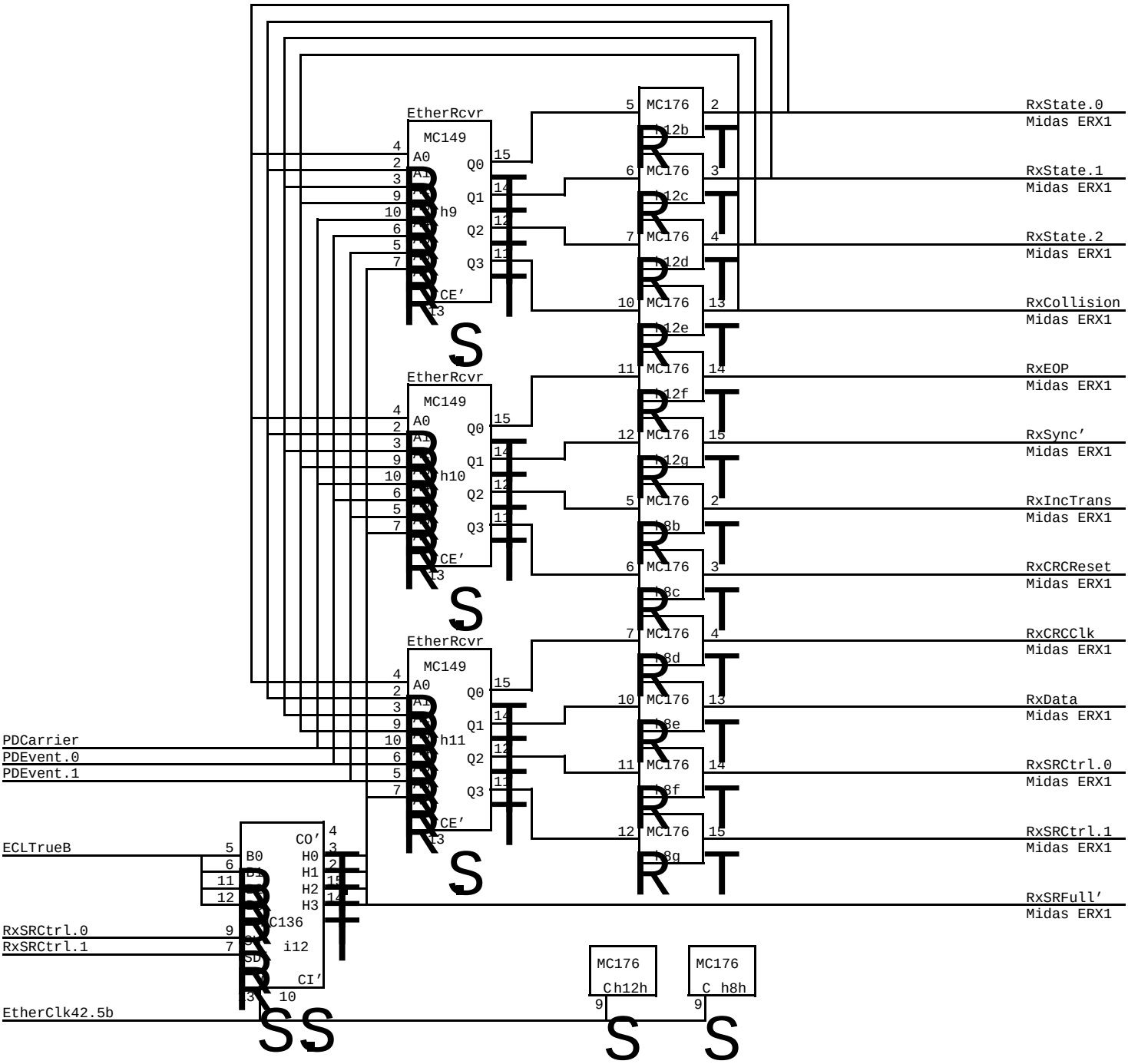

See DskEth*.sil for IOA, IOB, Muffler Control and Board Clocks




| PDEvent.0 | PDEvent.1 | Event |
|---|---|---|
| 0 | 0 | No Event |
| 0 | 1 | Collision |
| 1 | 0 | Data Zero |
| 1 | 1 | Data One |

See Ether20.sil for FSM truth table

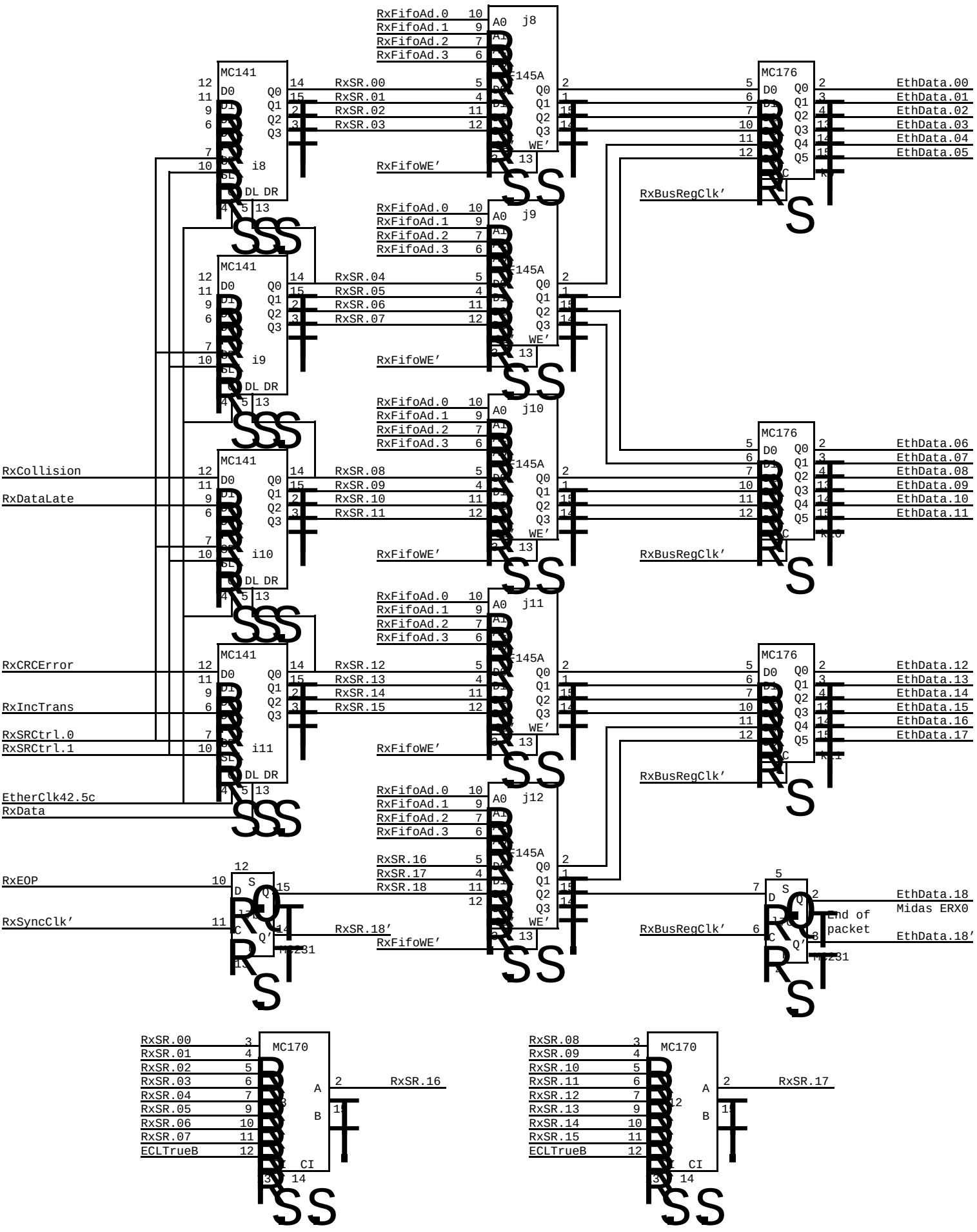
| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Phase Decoder | Ether01.sil | David Boggs | Ce | 7/08/79 | 24 |



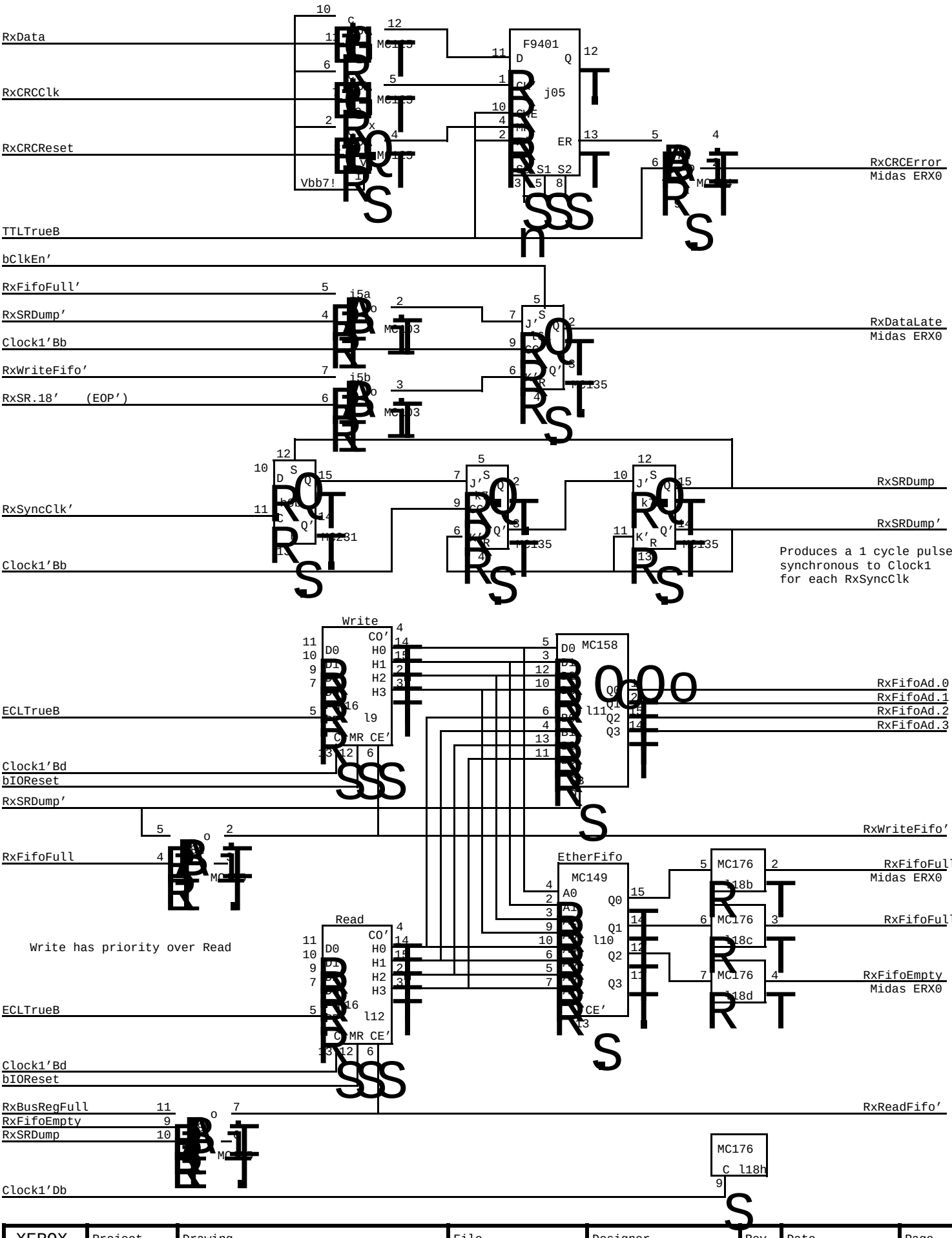

See Ether18.sil for timing diagrams

The slowest Dorado clock speed at which the receiver works is 85 ns (T0 to T1)

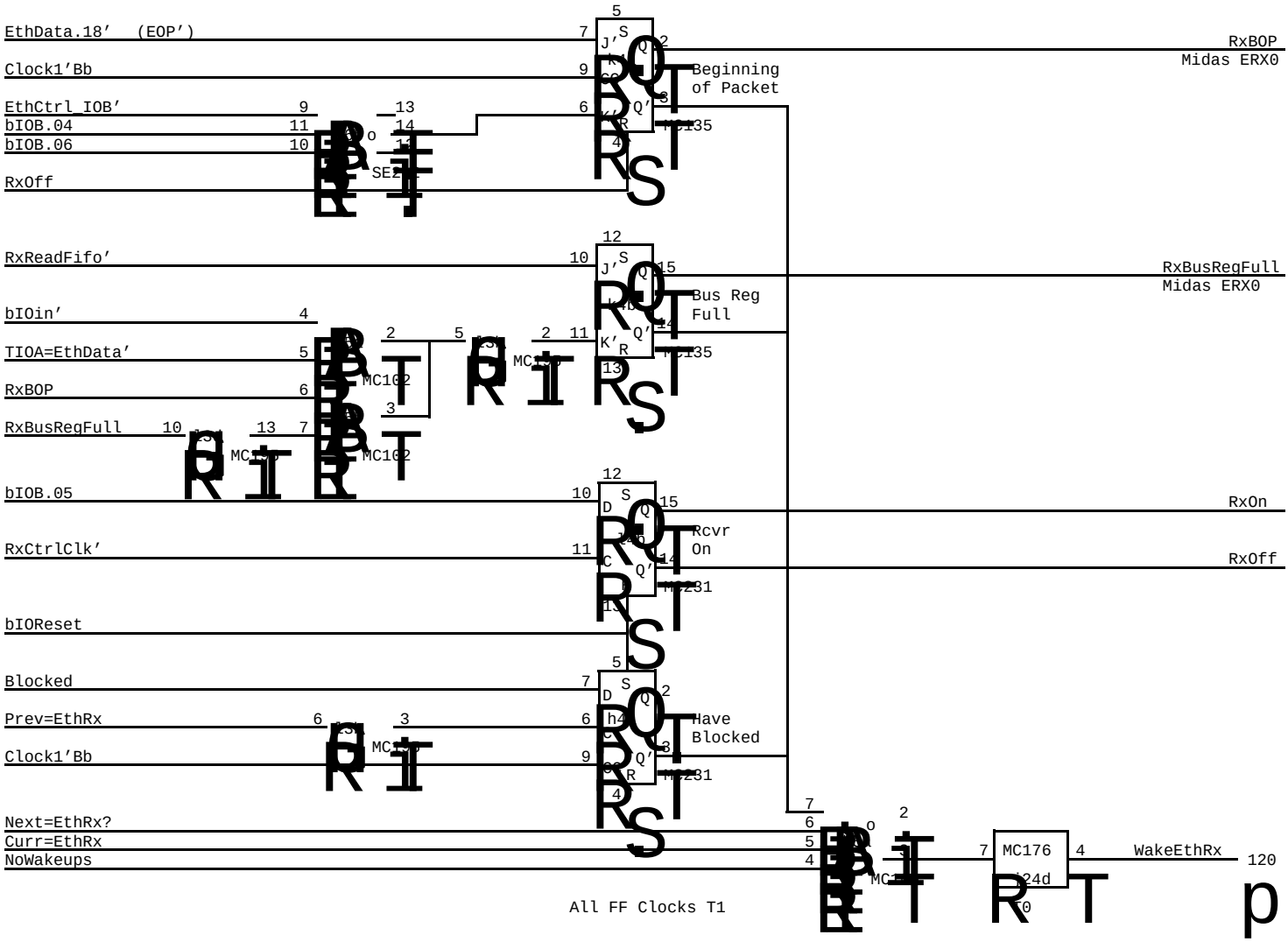
| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Receiver Control | Ether02.sil | David Boggs | Ce | 9/24/79 | 25 |




| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Receiver Data Paths | Ether03.sil | David Boggs | Ce | 7/08/79 | 26 |

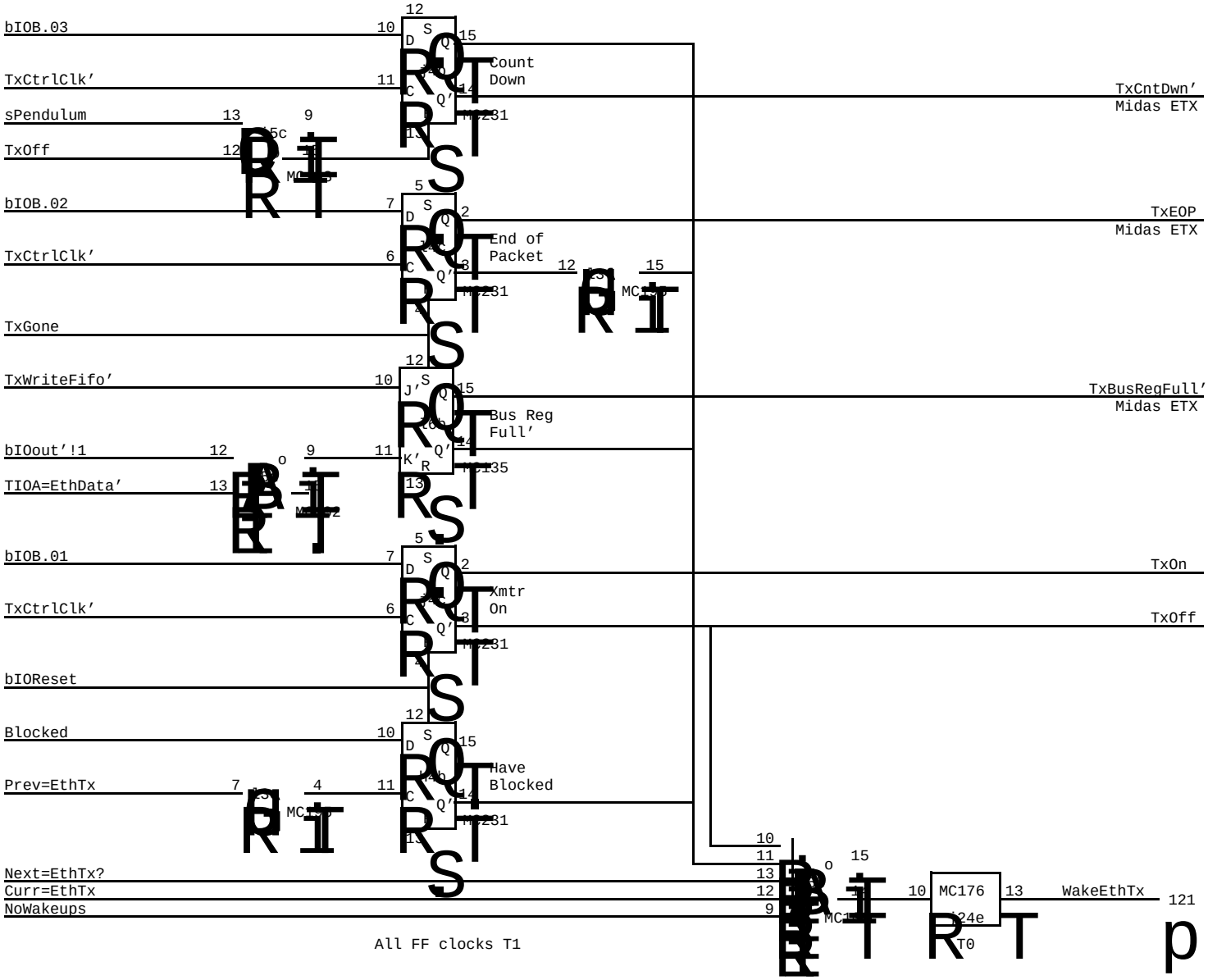



| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Receiver Stuff | Ether04.sil | David Boggs | Ce | 7/08/79 | 27 |



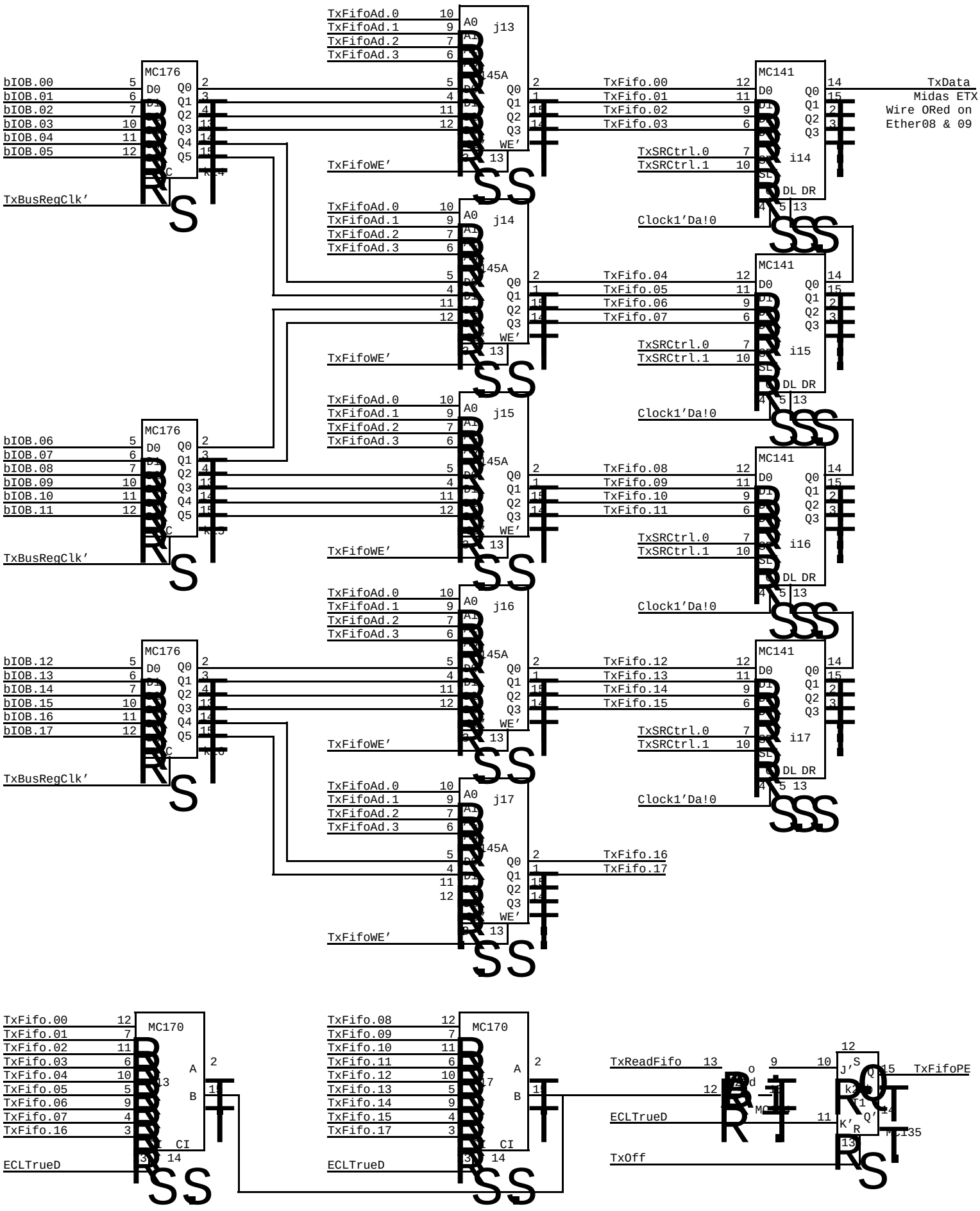

See Ether21 & 22.sil for wakeup timing diagrams

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Receiver Wakeups | Ether05.sil | David Boggs | Ce | 7/08/79 | 28 |

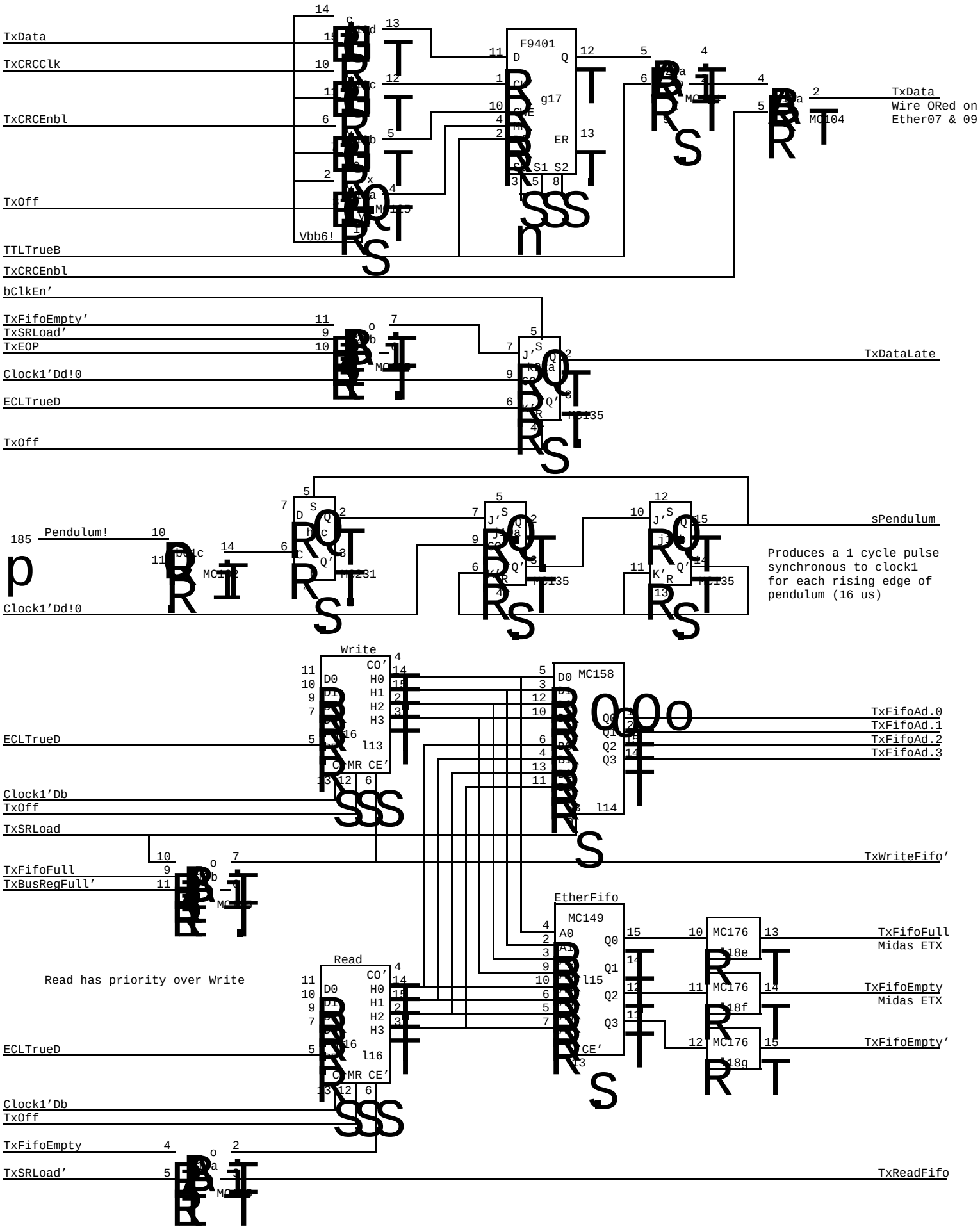



See Ether21 & 22.sil for wakeup timing diagrams

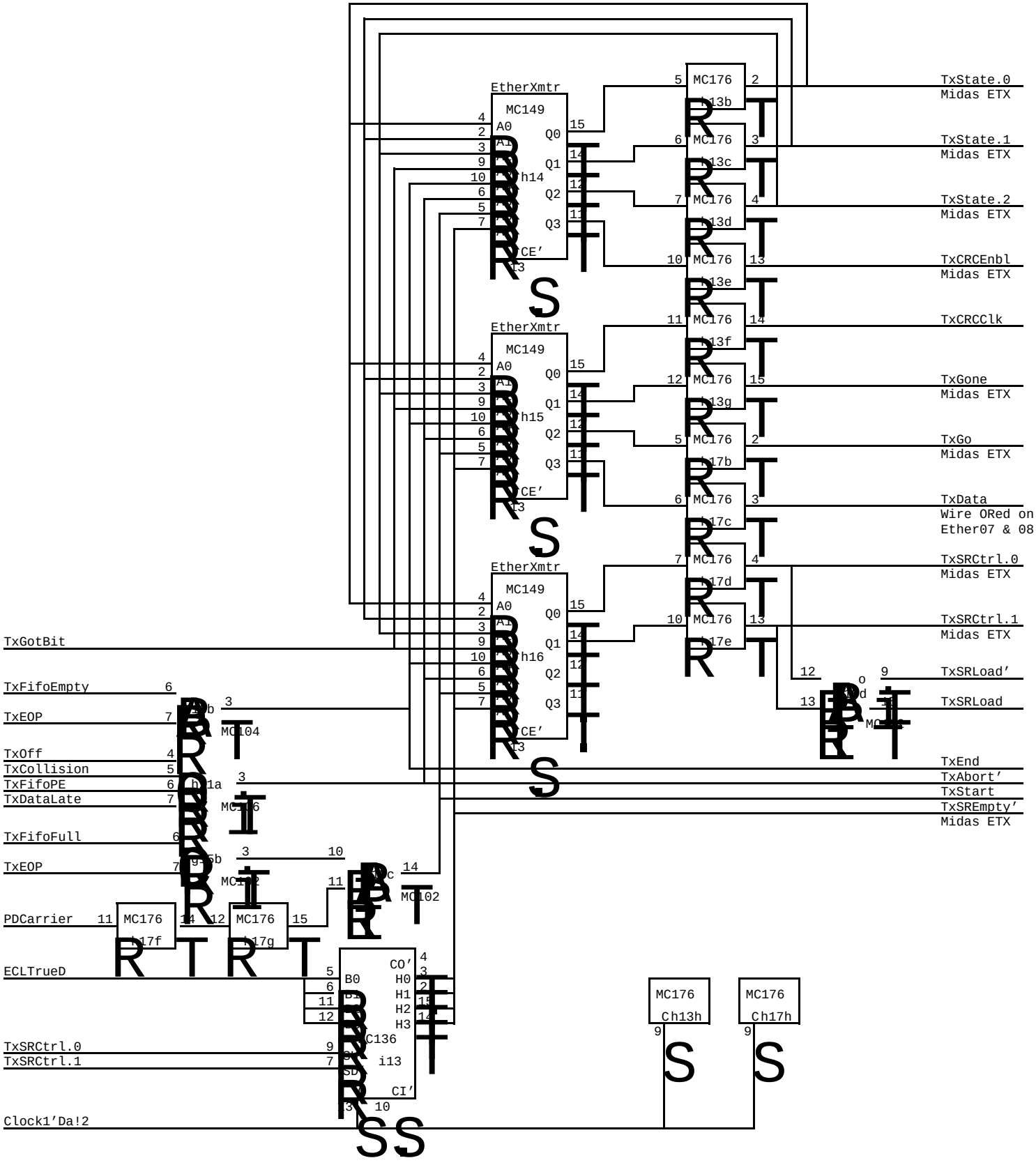
| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Transmitter Wakeups | Ether06.sil | David Boggs | Ce | 7/08/79 | 29 |




| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Transmitter Data Paths | Ether07.sil | David Boggs | Ce | 7/08/79 | 30 |

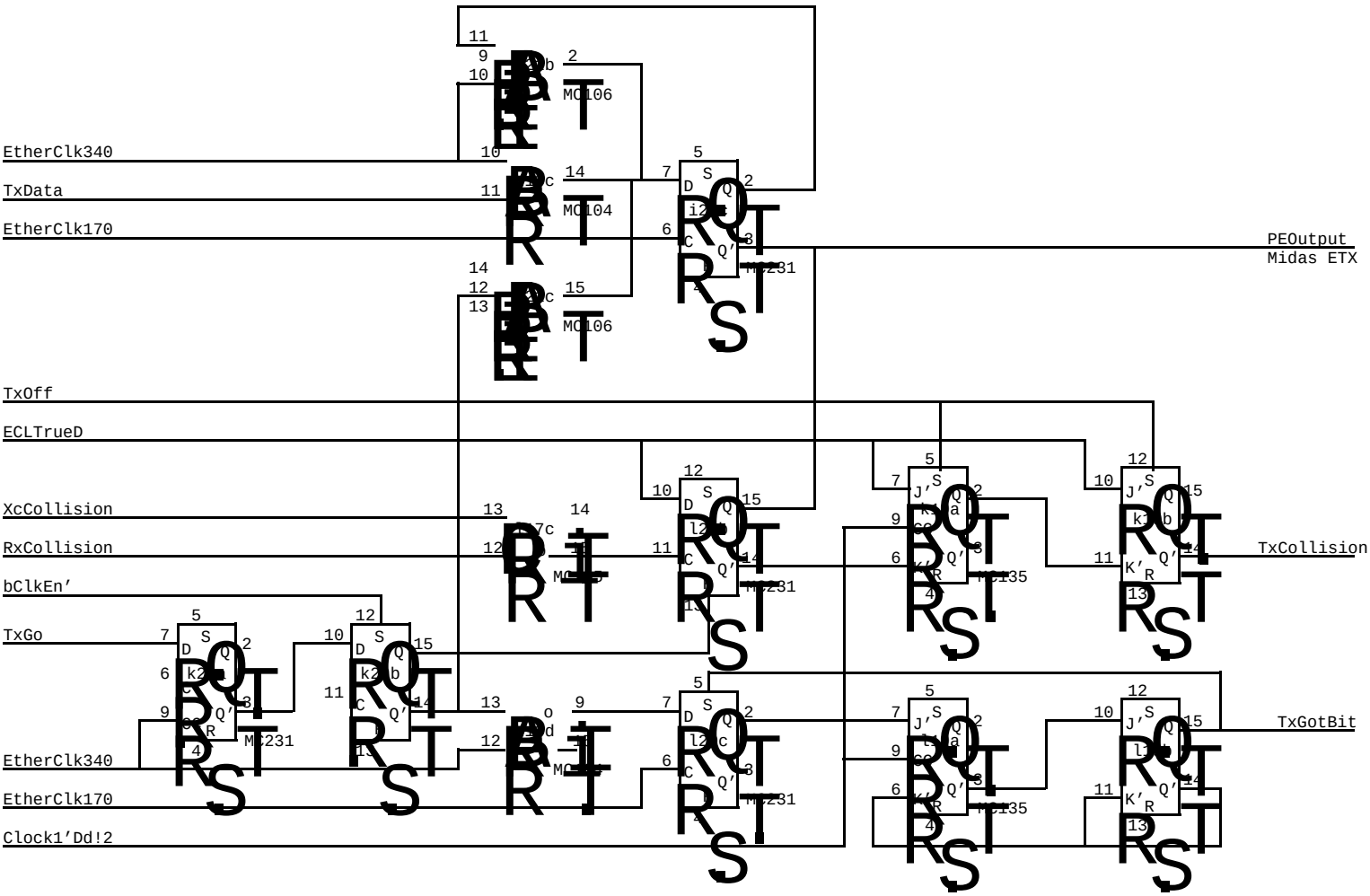



| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Transmitter Stuff | Ether08.sil | David Boggs | Ce | 7/08/79 | 31 |




See Ether17.sil for timing diagrams

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Transmitter Control | Ether09.sil | David Boggs | Ce | 9/24/79 | 32 |

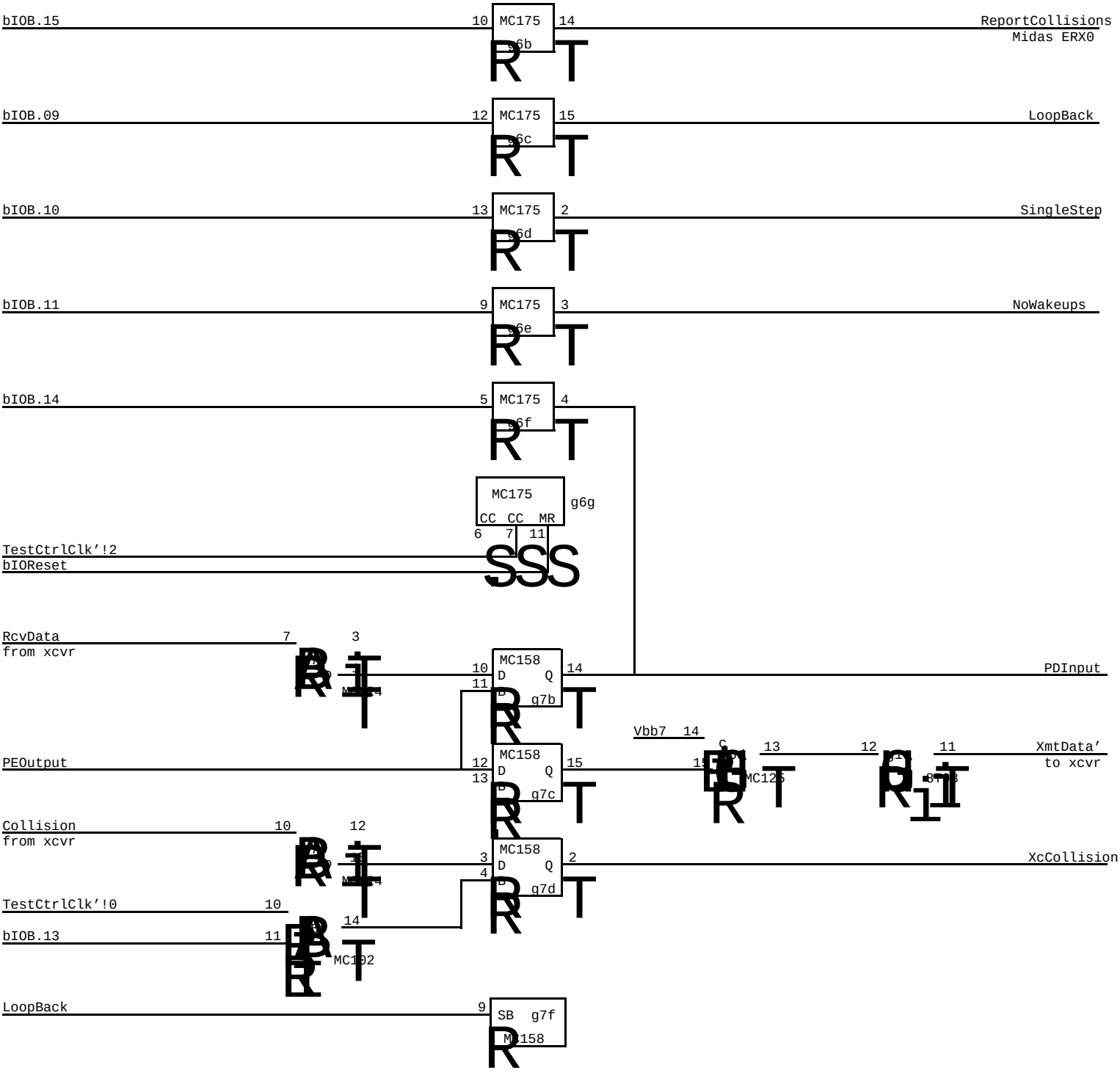



See Ether19.sil for timing diagrams

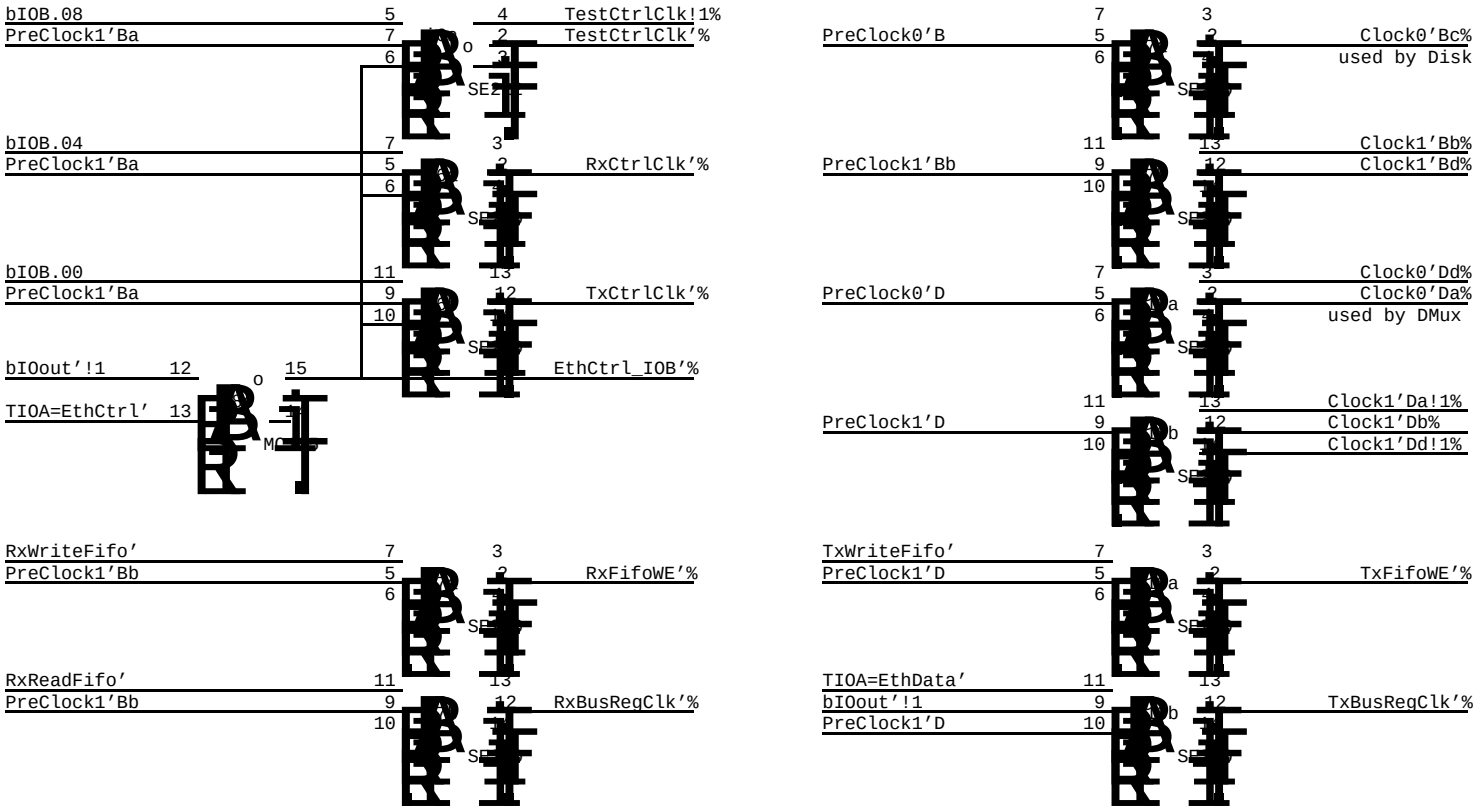
The slowest Dorado clock speed at which the transmitter works is 42.5 ns (T0 to T1)

525 ns < length of jam < 915 ns

| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Phase Encoder | Ether10.sil | David Boggs | Ce | 9/24/79 | 33 |

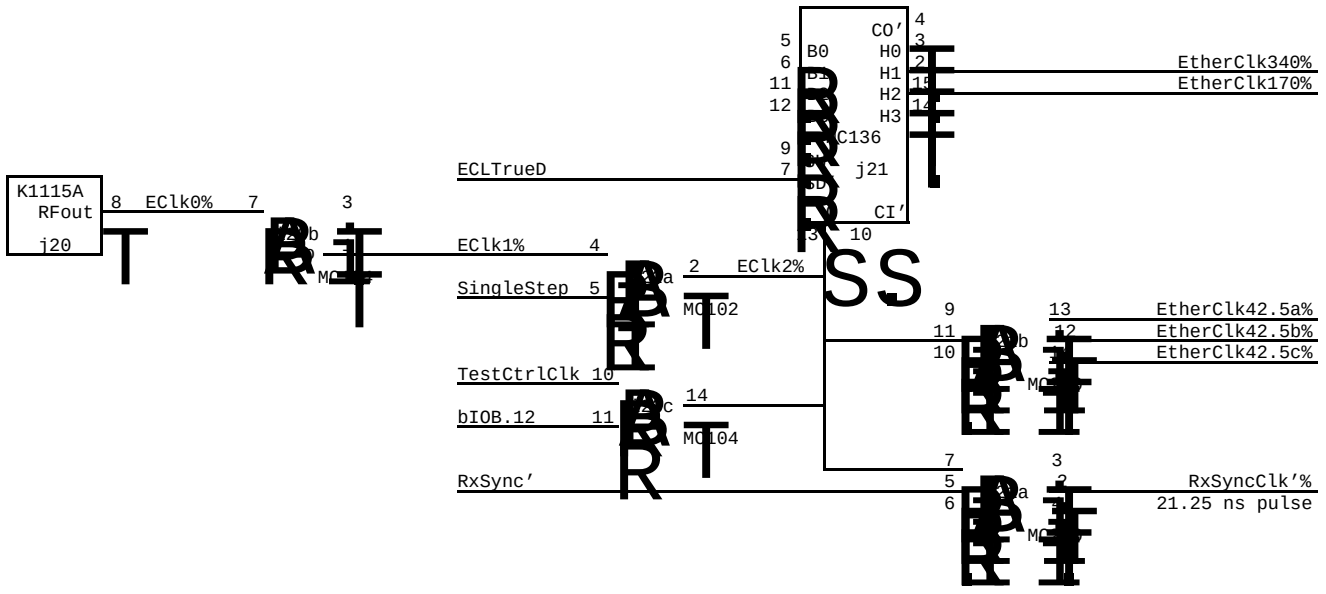



| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Test Logic | Ether11.sil | David Boggs | Ce | 7/08/79 | 34 |

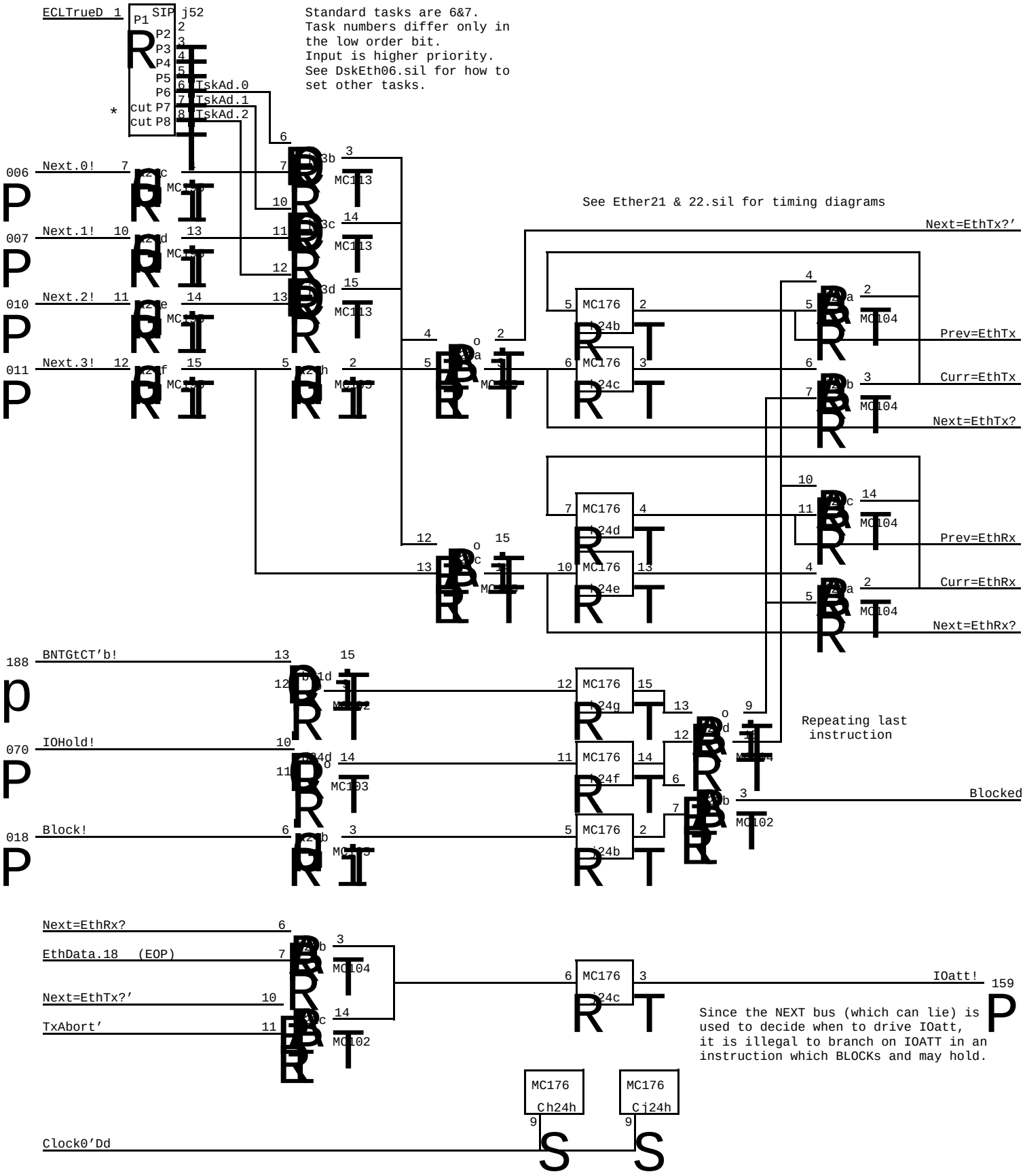



## Dorado Synchronous Clocks

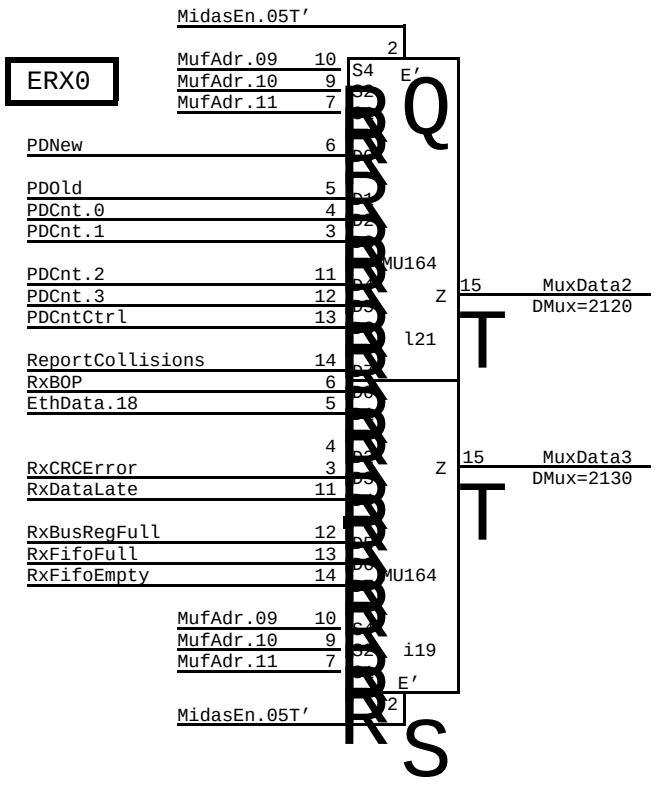
### Free-running Ether Clocks

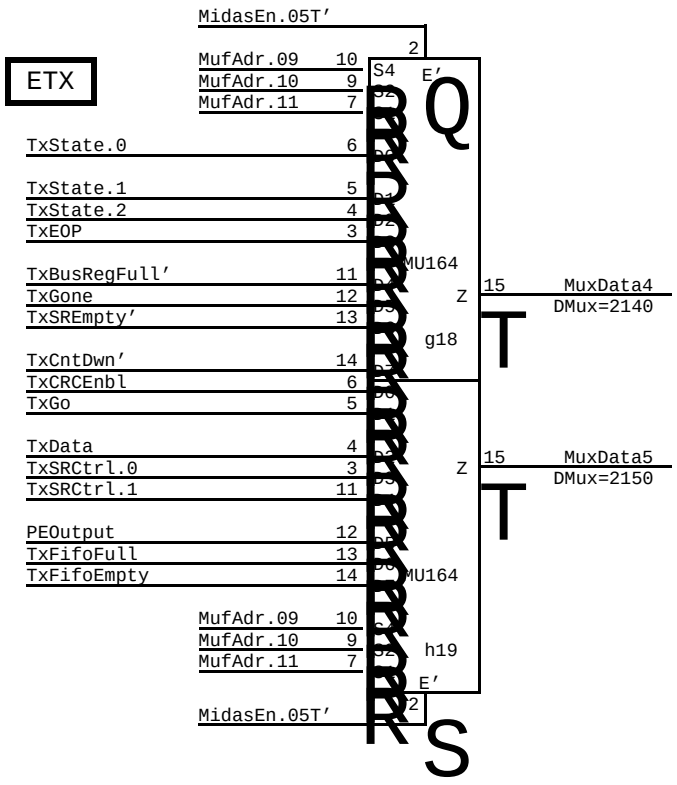



| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Clocks | Ether12.sil | David Boggs | Ce | 9/24/79 | 35 |

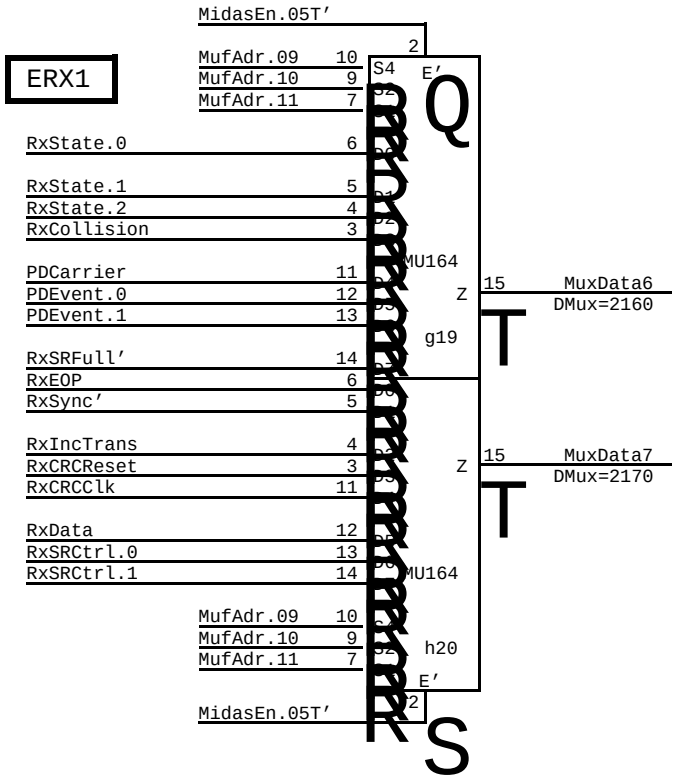



| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Next & IOAttention | Ether13.sil | David Boggs | Ce | 7/08/79 | 36 |

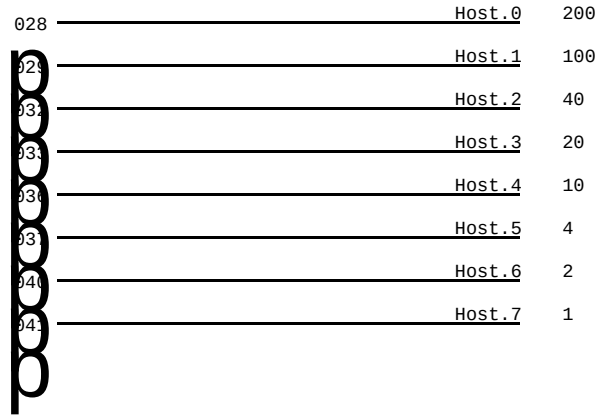


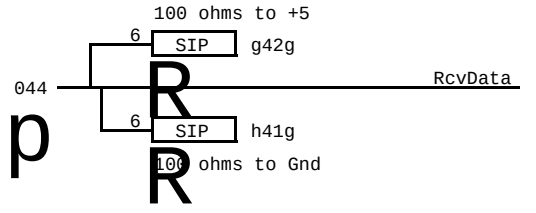



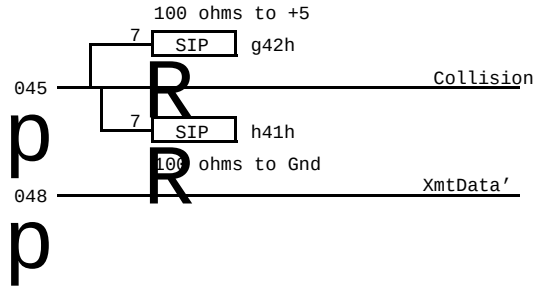

See DskEth01.sil for muffler control logic.
DMux addresses 2000-2117 are used by the disk.

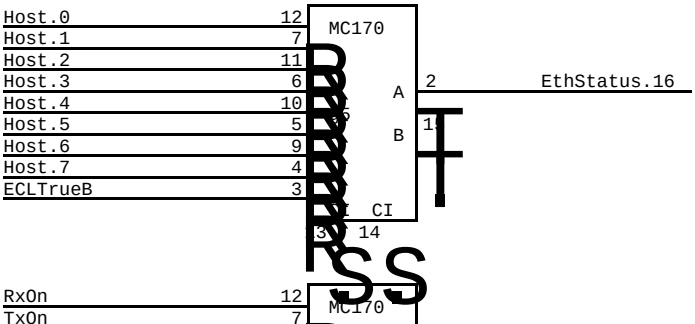


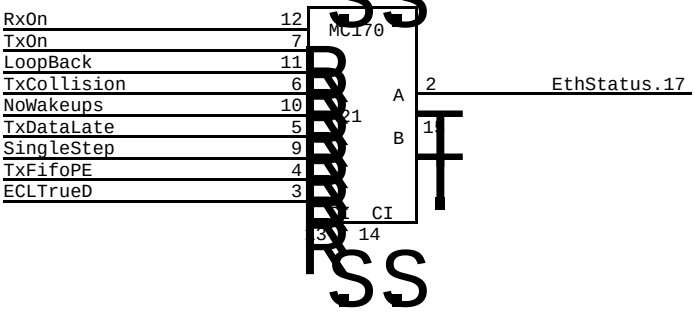
To set a host address bit to 1
pull it up to gnd through 91 ohms.

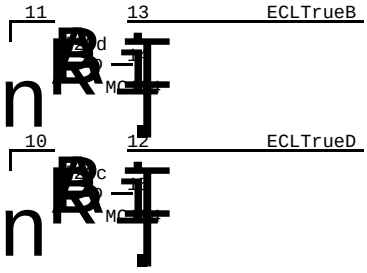


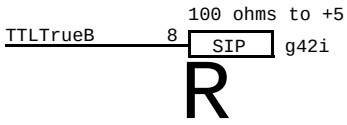



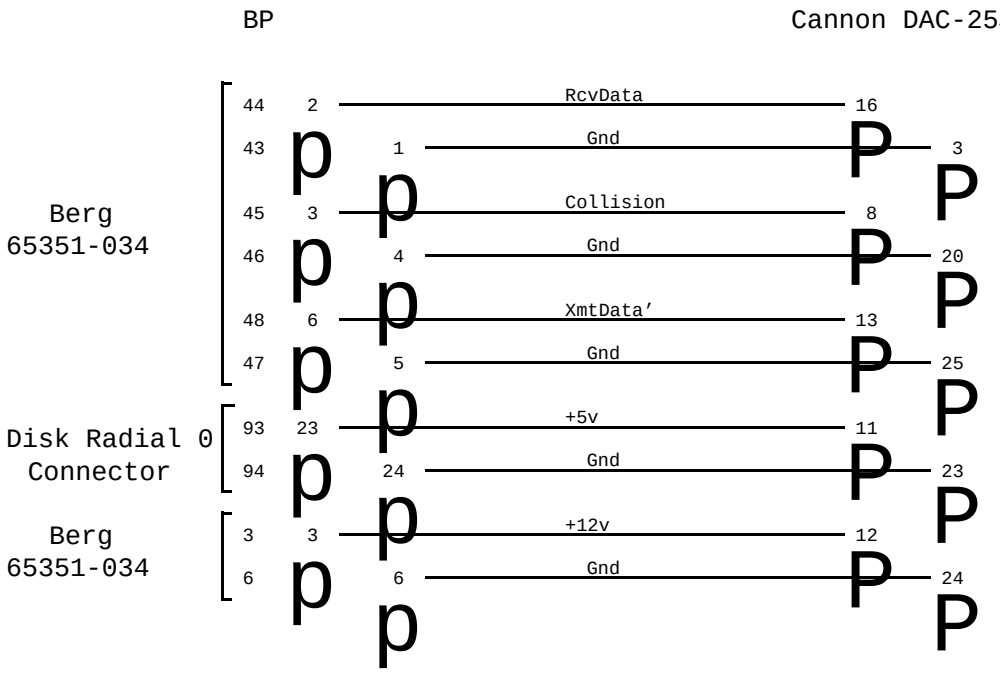



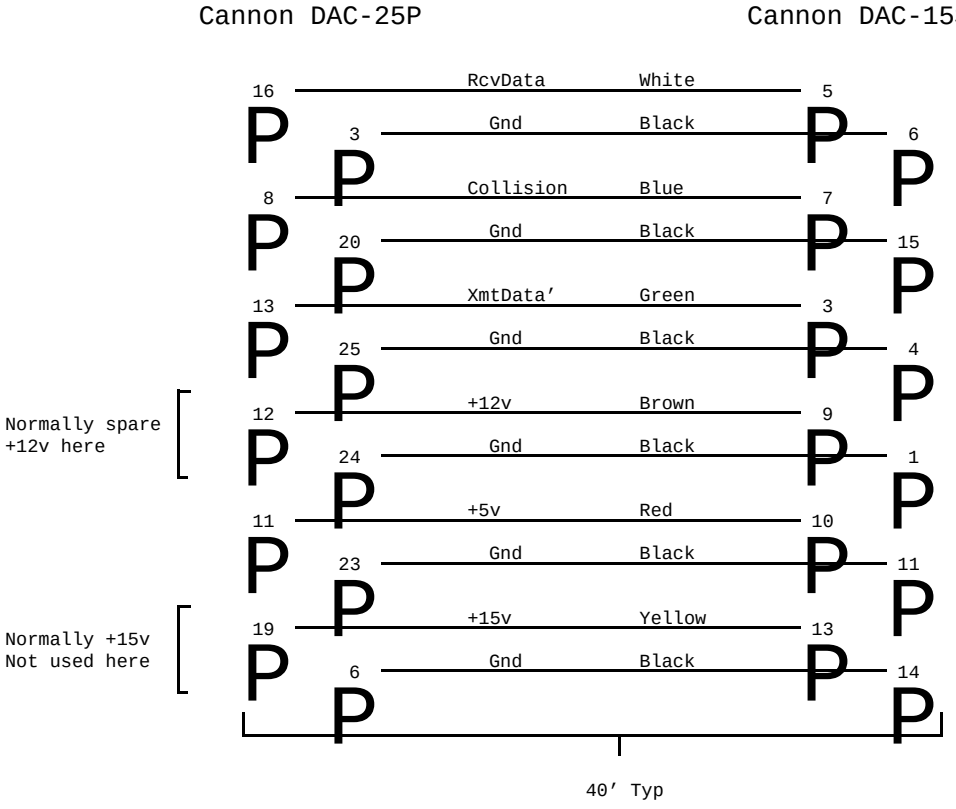




| XEROX PARC | Project | Drawing | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | BackPanel Connections | Ether15.sil | David Boggs | Ce | 9/24/79 | 38 |



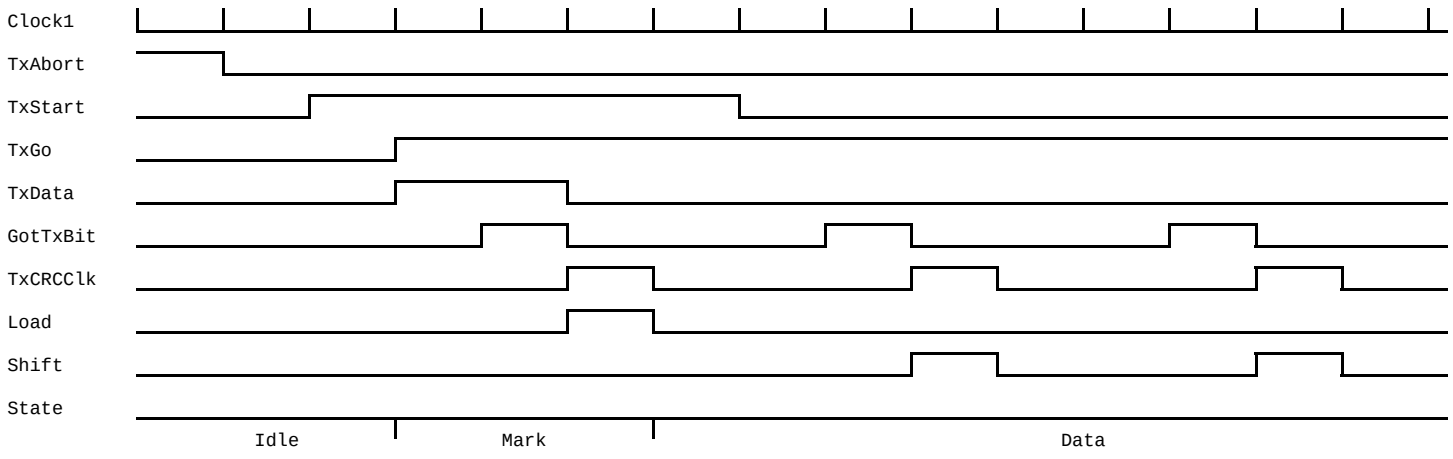

Internal Cable

External Cable

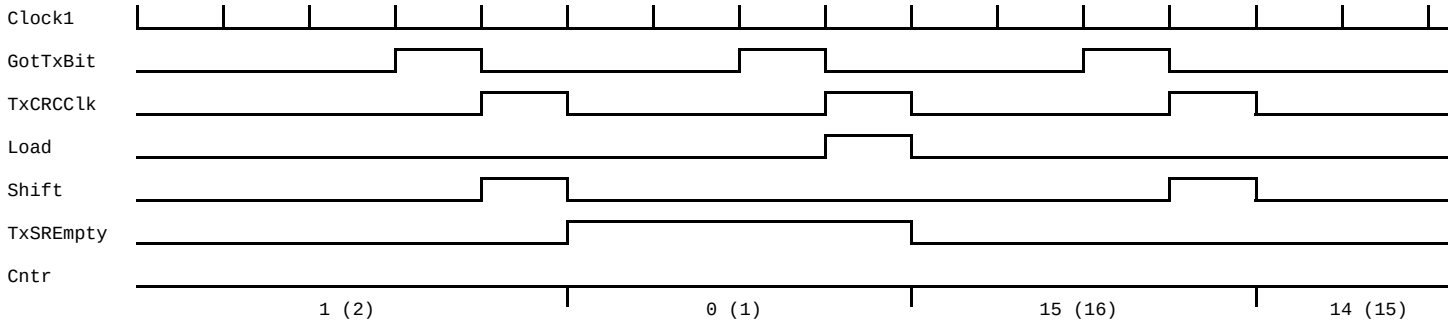



This is a standard Alto II
Ethernet external cable
part # 216411

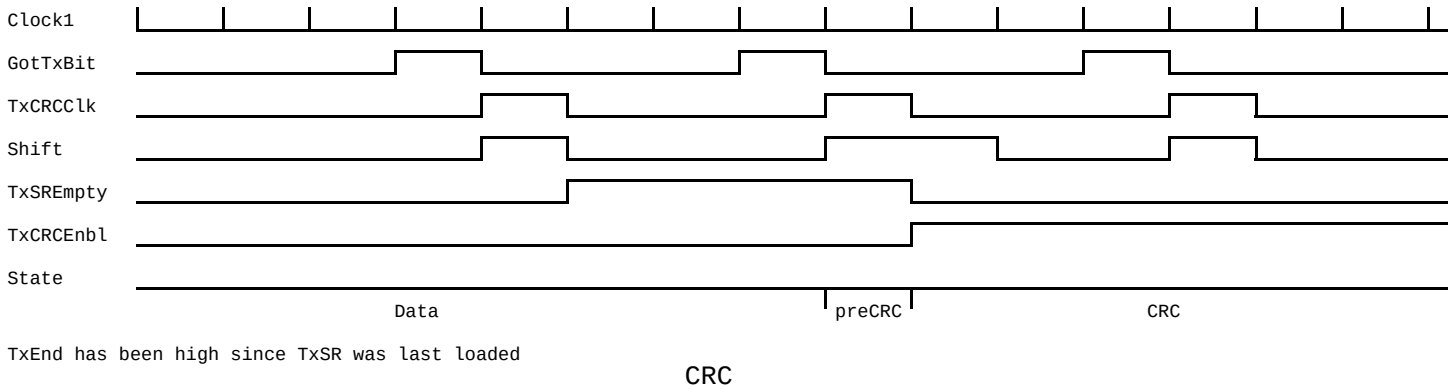
| XEROX PARC | Project | Reference | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Ethernet Cables | Ether16.sil | David Boggs | Ce | 7/08/79 | 39 |




Startup

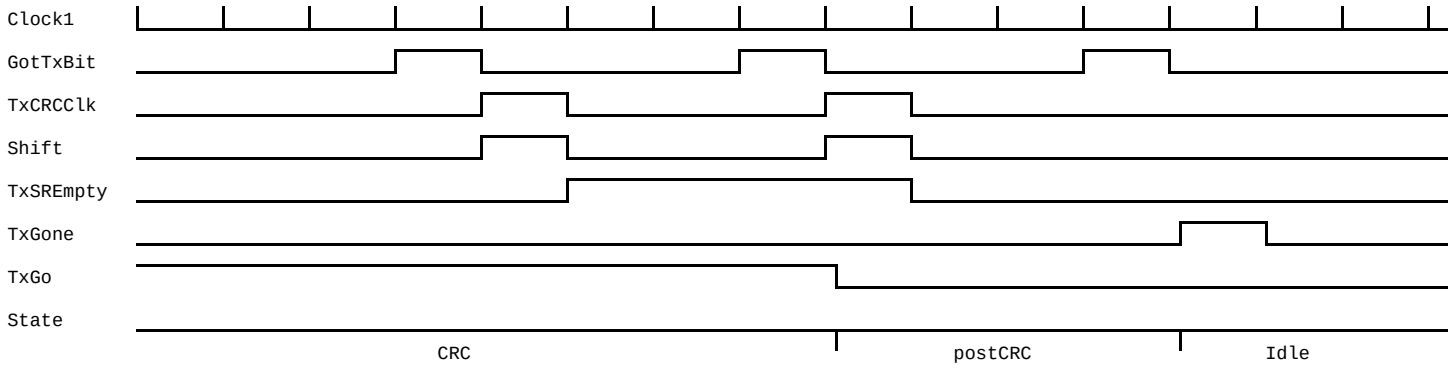



Loading Tx Shift Register



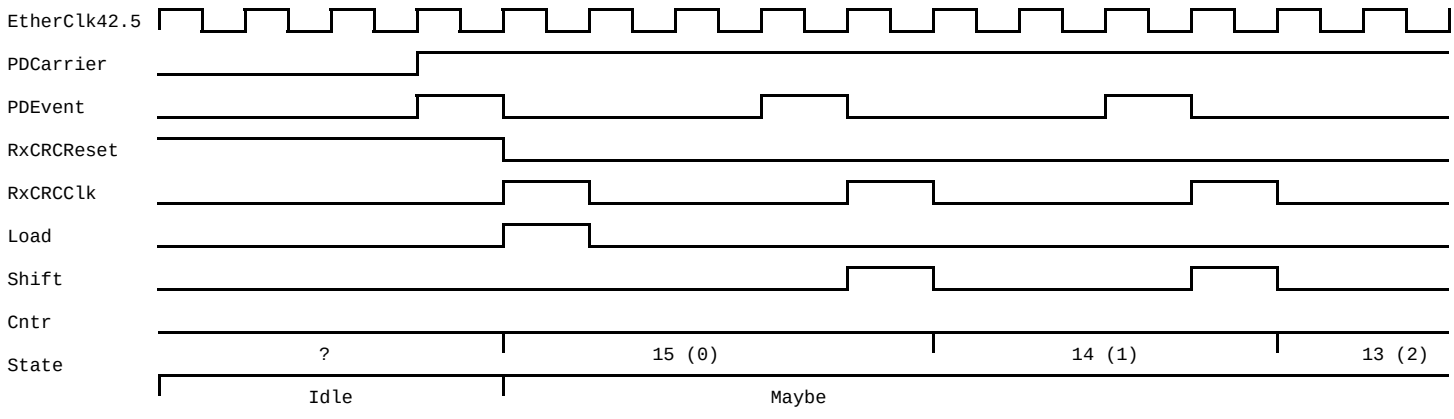

TxEnd has been high since TxSR was last loaded

CRC

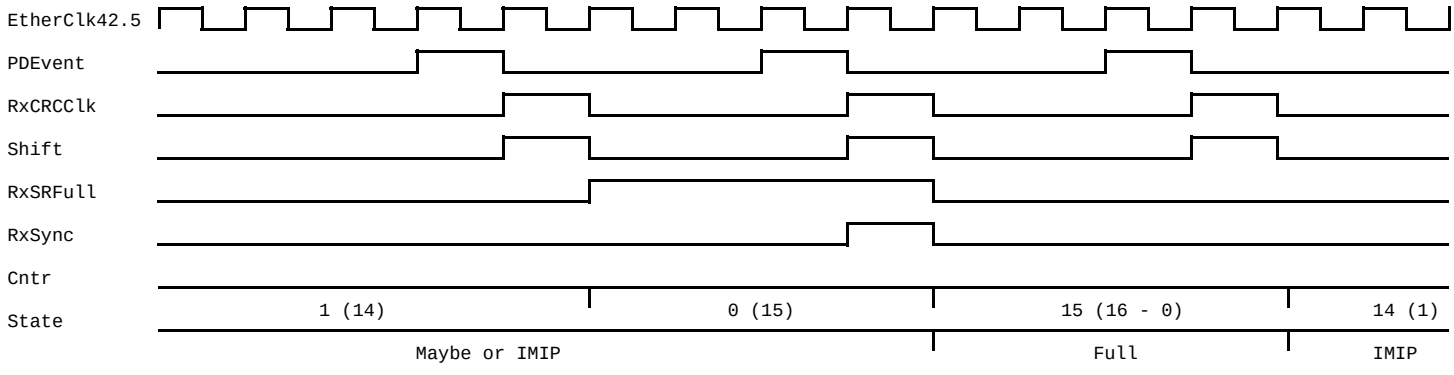



ShutDown

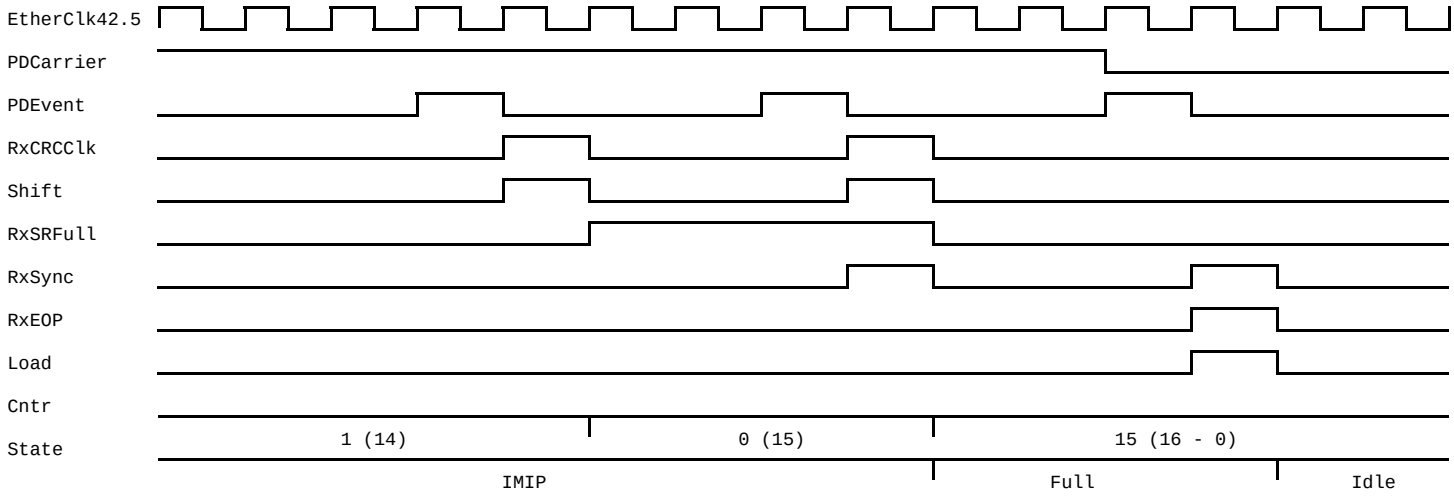
| XEROX PARC | Project | Reference | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Transmitter Timing | Ether17.sil | David Boggs | Ce | 7/08/79 | 40 |




Startup




Dumping Rx Shift Register




ShutDown

Cntr notation is <cntr value>(<# occupied postions>)
Phase decoder events are encoded in PDEvent.x
Shift and Load are encoded in RxSRCtrl.x
state is encoded in RxState.x
shift also decrements Cntr

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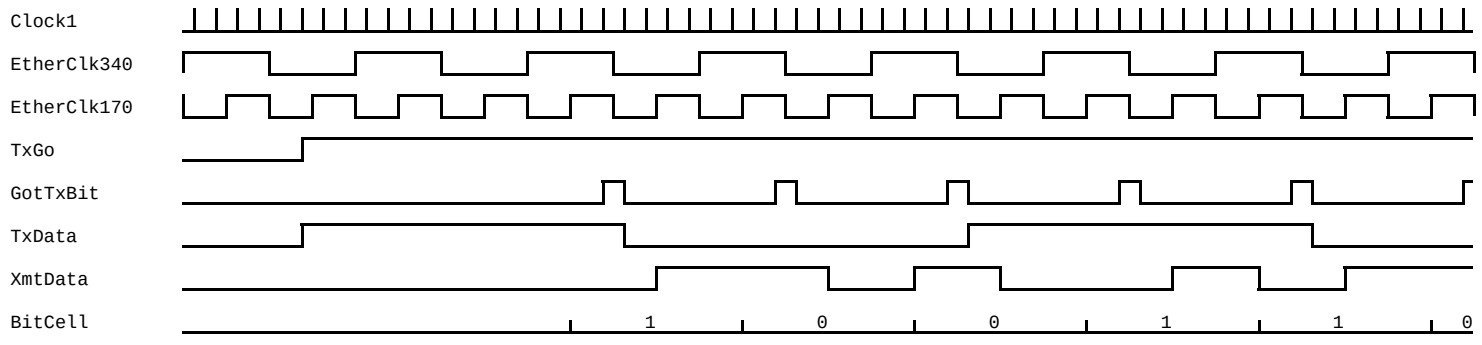
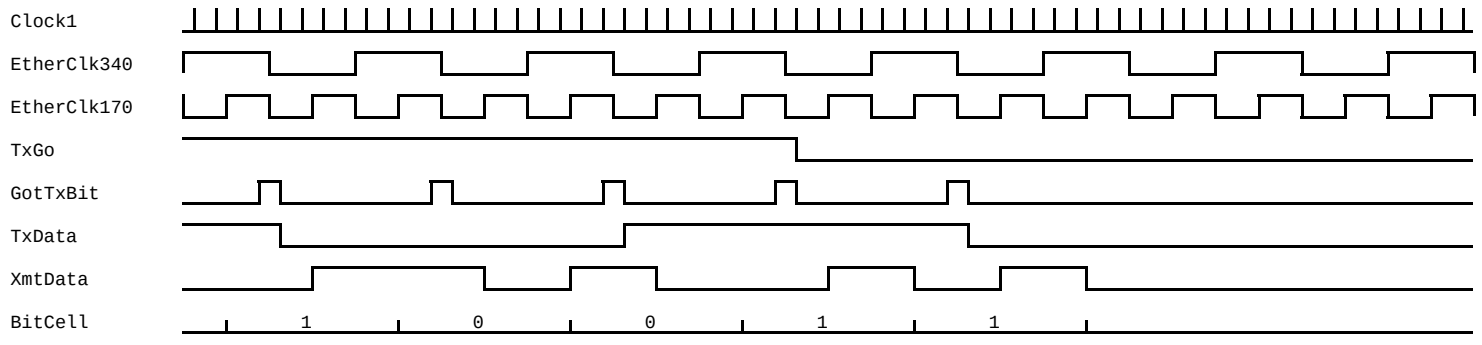
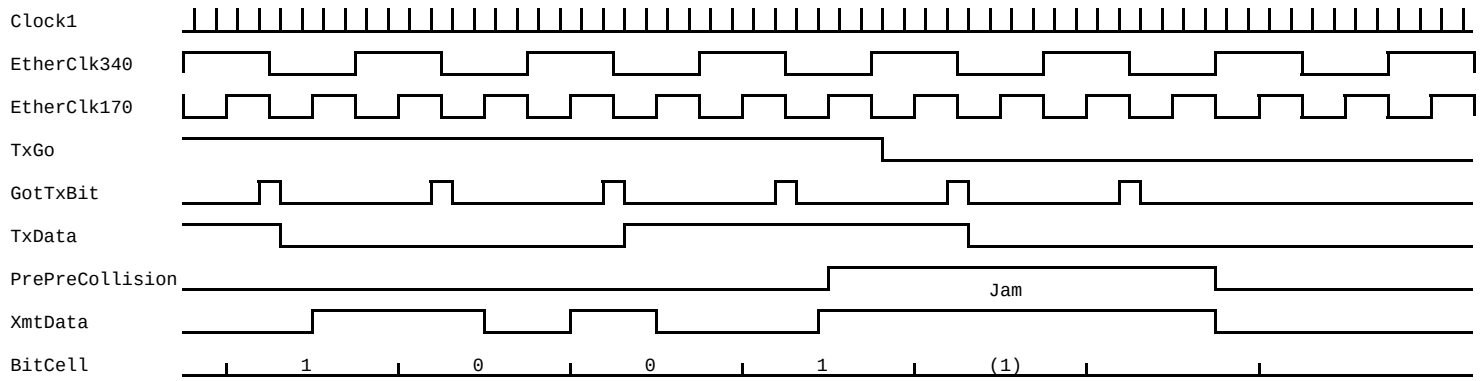
|---|---|---|---|---|---|---|---|
| | Dorado | Receiver Timing | Ether18.sil | David Boggs | Ce | 7/08/79 | 41 |




Startup



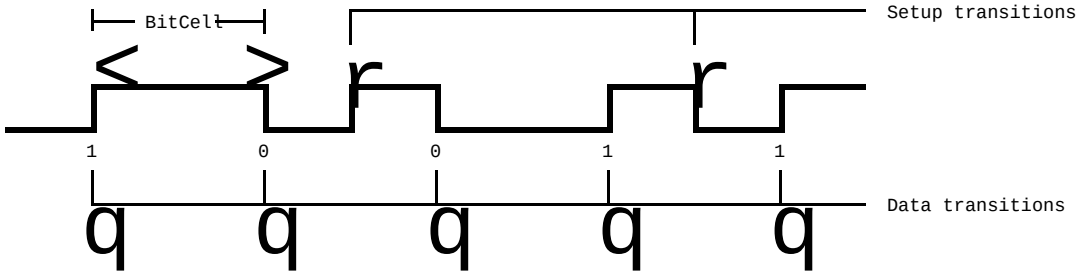

Shutdown




PrePreCollision is the output of the first stage of the Collision synchronizer

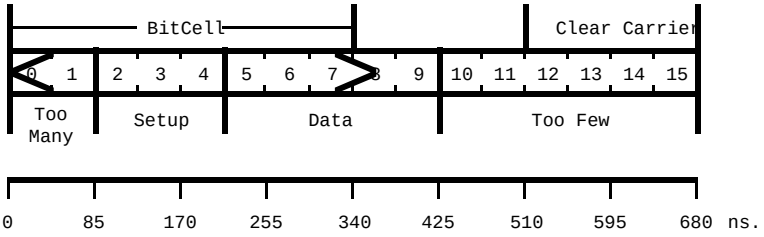
Collision

| XEROX PARC | Project | Reference | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Phase Encoder Timing | Ether19.sil | David Boggs | Ce | 7/08/79 | 42 |




A bitcell is nominally 340 ns.

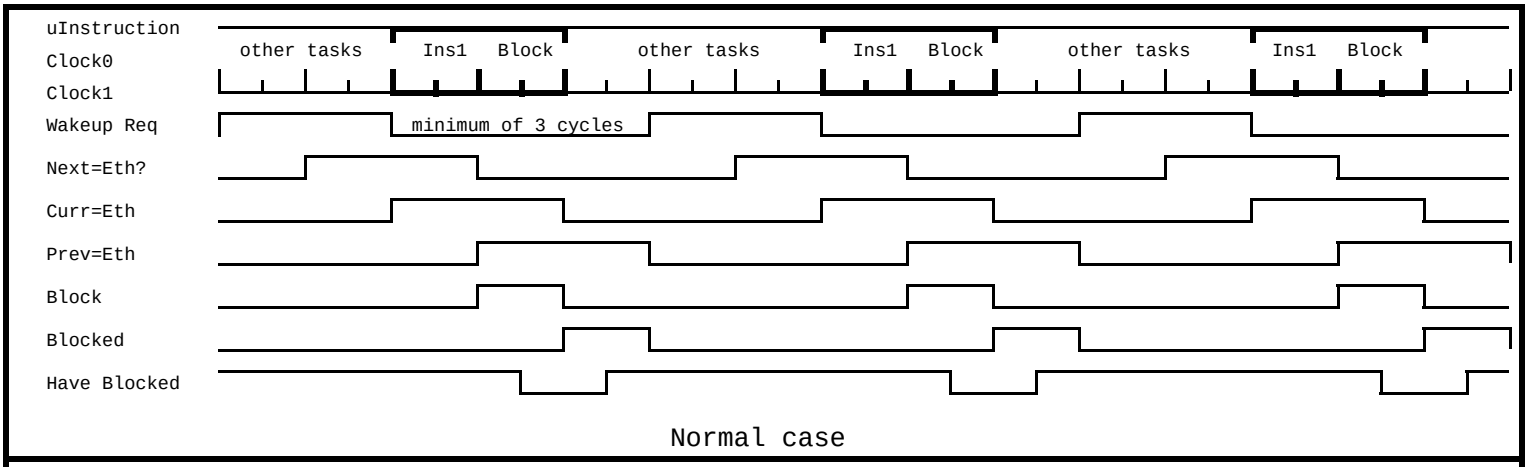
A sample is nominally 42.5 ns.



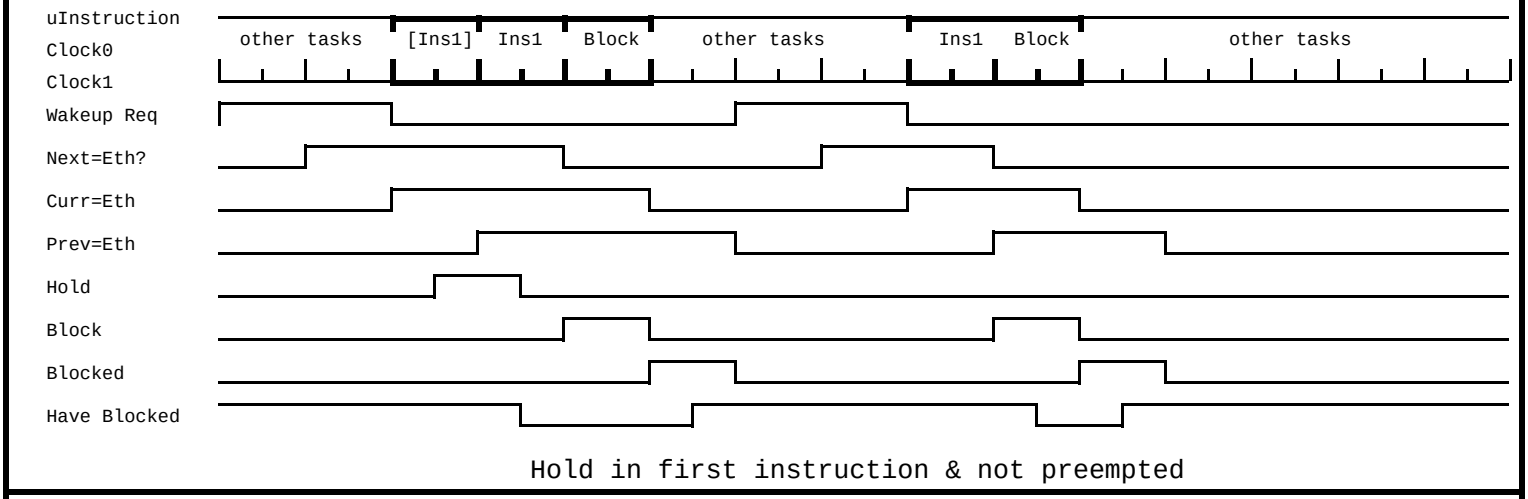

| Inputs | | | | Outputs | | | Comment |
|---|---|---|---|---|---|---|---|
| Carrier | Old | New | Cnt | Carrier | Event | CntCtrl | |
| Low | Low | Low | d/c | Low | NoEvent | Count | Idle |
| Low | Low | High | d/c | High | One | Reset | Start of packet (start bit) |
| Low | High | Low | d/c | High | Collision | Reset | Impossible |
| Low | High | High | d/c | Low | NoEvent | Count | Impossible |
| High | Low | High | 0-1 | High | Collision | Count | Too many transitions |
| High | High | Low | 0-1 | High | Collision | Count | Too many transitions |
| High | Low | High | 2-4 | High | NoEvent | Count | Setup transition (zero next) |
| High | High | Low | 2-4 | High | NoEvent | Count | Setup transition (one next) |
| High | Low | High | 5-9 | High | One | Reset | Data transition |
| High | High | Low | 5-9 | High | Zero | Reset | Data transition |
| High | Low | High | 10-15 | High | Collision | Reset | Too few transitions |
| High | High | Low | 10-15 | High | Collision | Reset | Too few transitions |
| High | Low | Low | 0-11 | High | NoEvent | Count | Active |
| High | High | High | 0-11 | High | NoEvent | Count | Active |
| High | Low | Low | 12-15 | Low | Collision | Reset | End of packet |
| High | High | High | 12-15 | High | Collision | Reset | Jam |

"Impossible" conditions can happen right after power up.

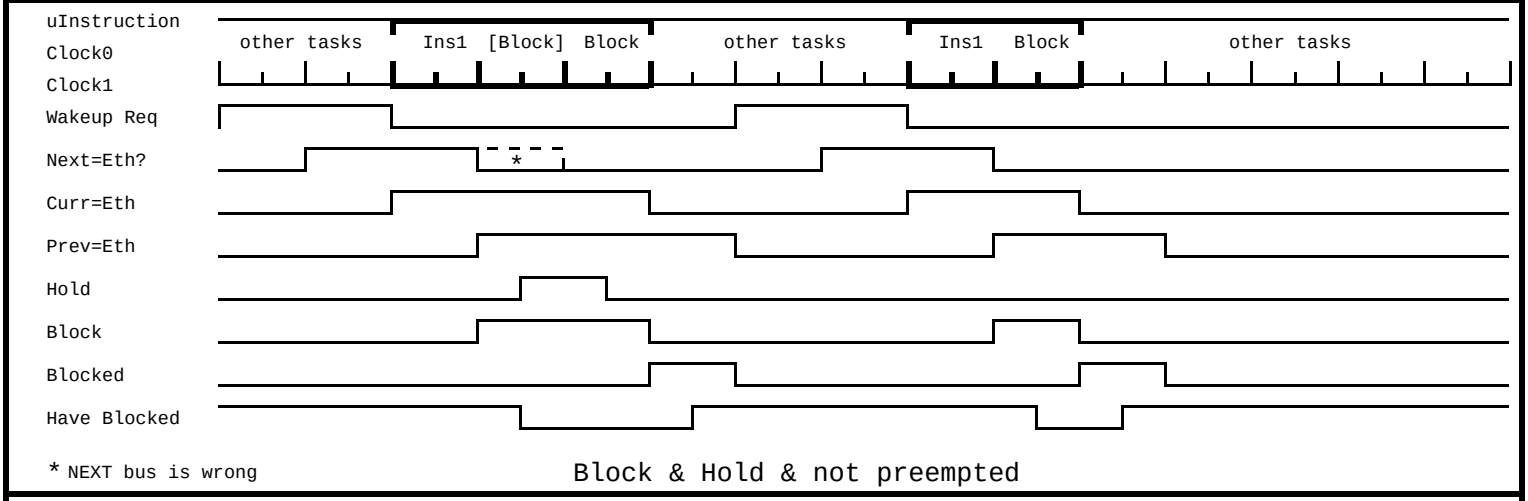
d/c means "don't care".




Normal case

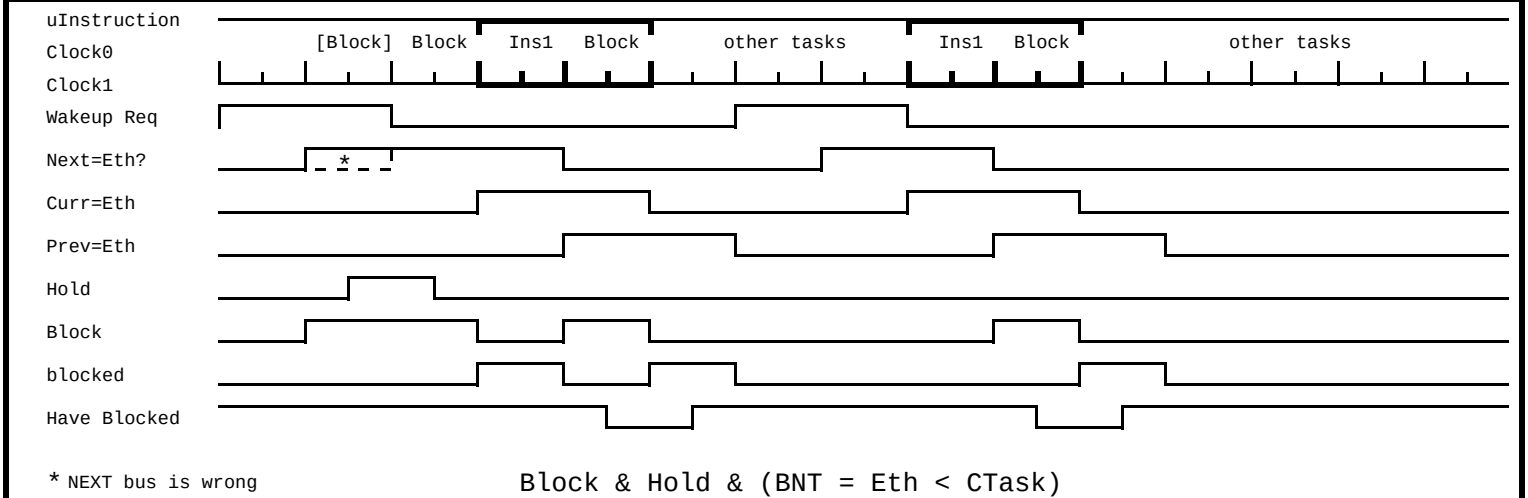



Hold in first instruction & not preempted




* NEXT bus is wrong

Block & Hold & not preempted




* NEXT bus is wrong

Block & Hold & (BNT = Eth < CTask)

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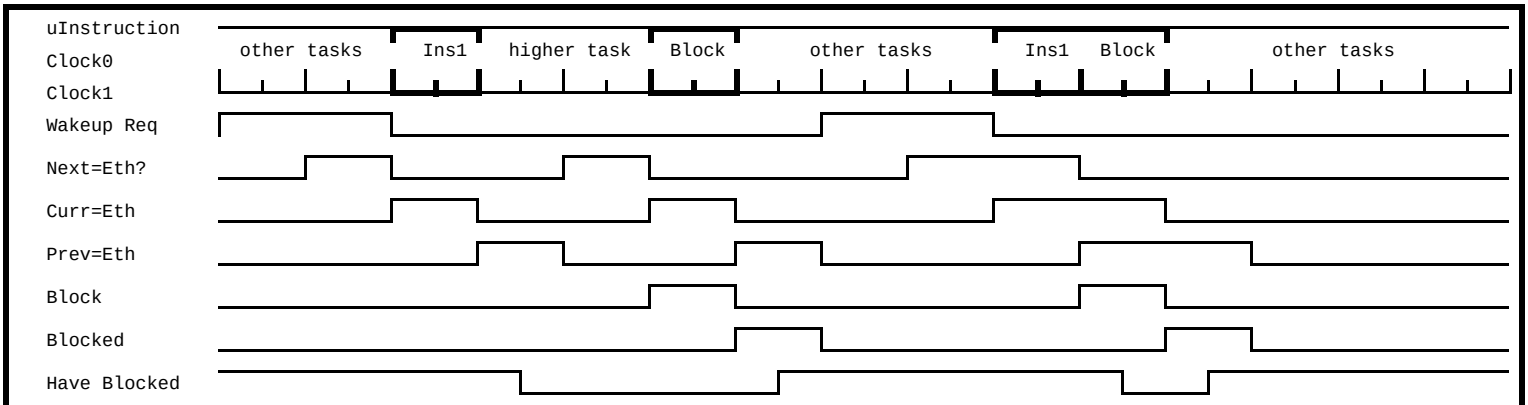
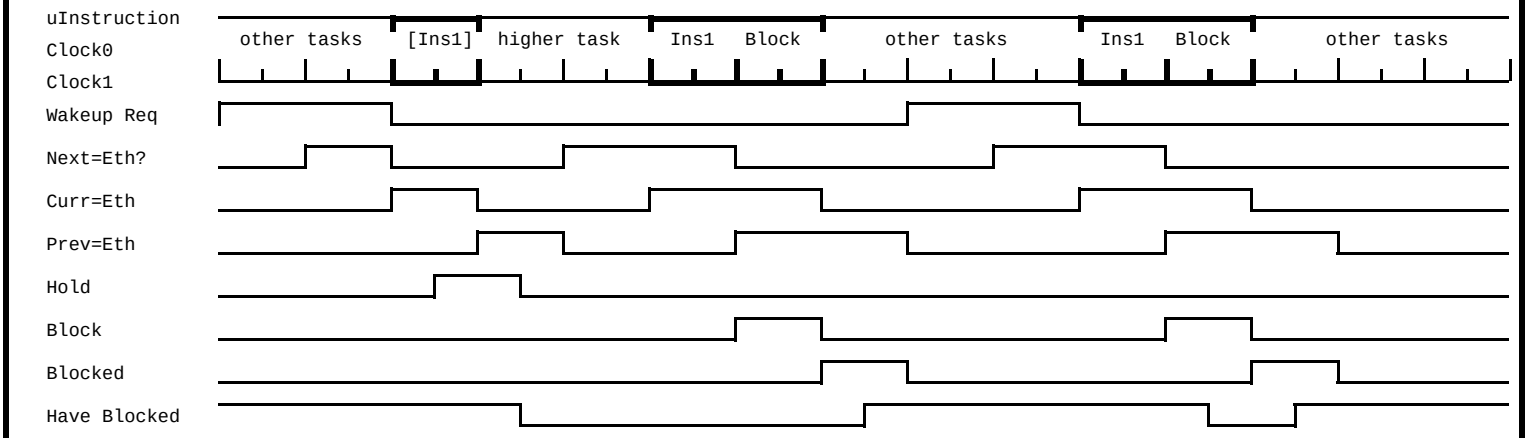
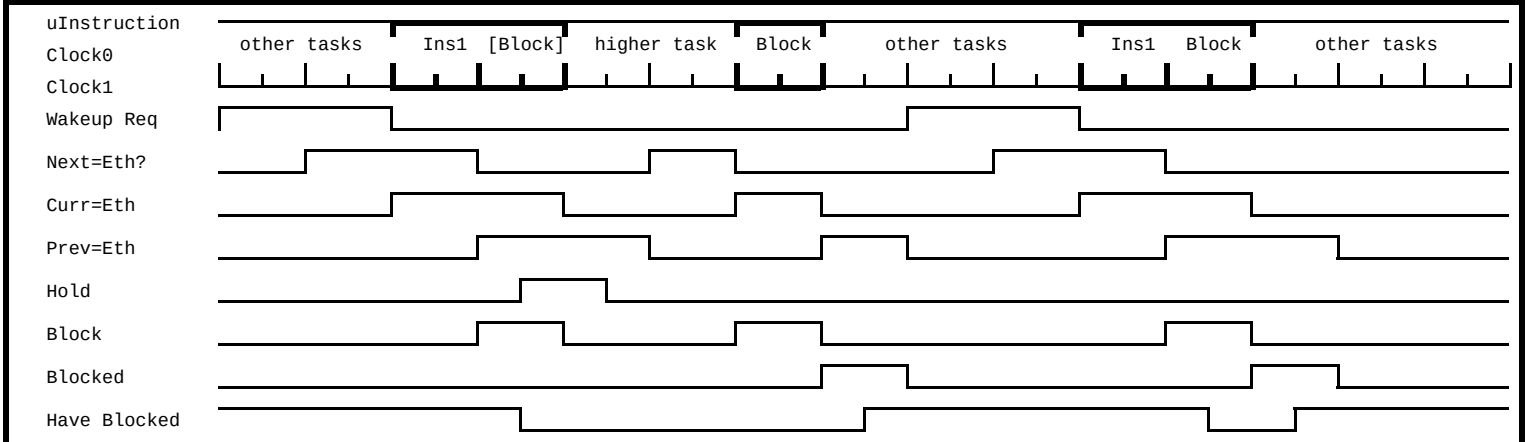
|---|---|---|---|---|---|---|---|
| | Dorado | Wakeup Timing | Ether21.sil | David Boggs | Ce | 7/08/79 | 44 |



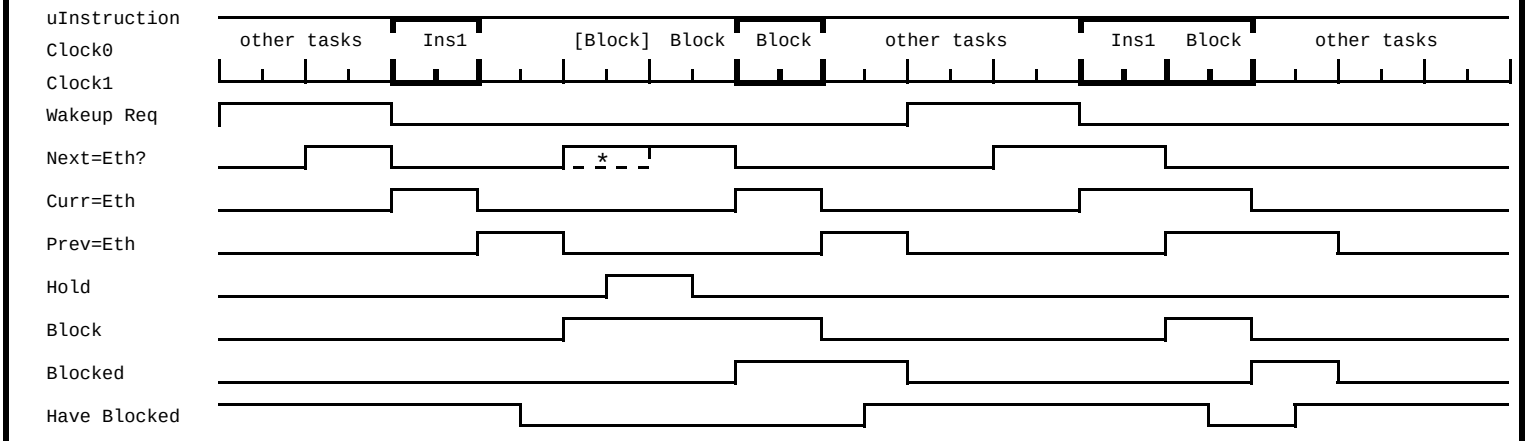

Preemption after first instruction




Hold in first instruction & then preempted



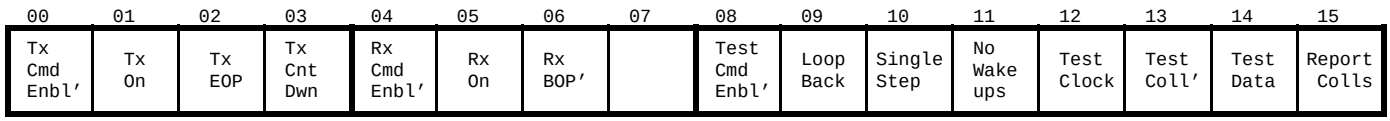

Block & Hold & then preempted



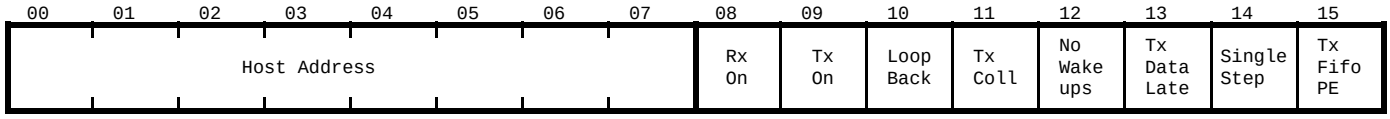

* NEXT bus is wrong

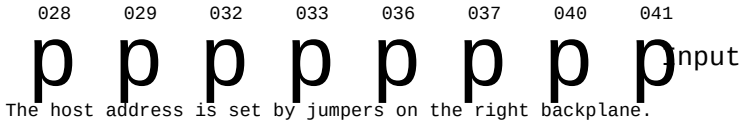
Block & Hold & (BNT = Eth < CTask) while Eth is preempted

| XEROX PARC | Project | Reference | File | Designer | Rev | Date | Page |
|---|---|---|---|---|---|---|---|
| | Dorado | Wakeup Timing | Ether22.sil | David Boggs | Ce | 7/08/79 | 45 |




Output




Input

The host address is set by jumpers on the right backplane.

To set a bit to one, pull it up to ground through 91 ohms.