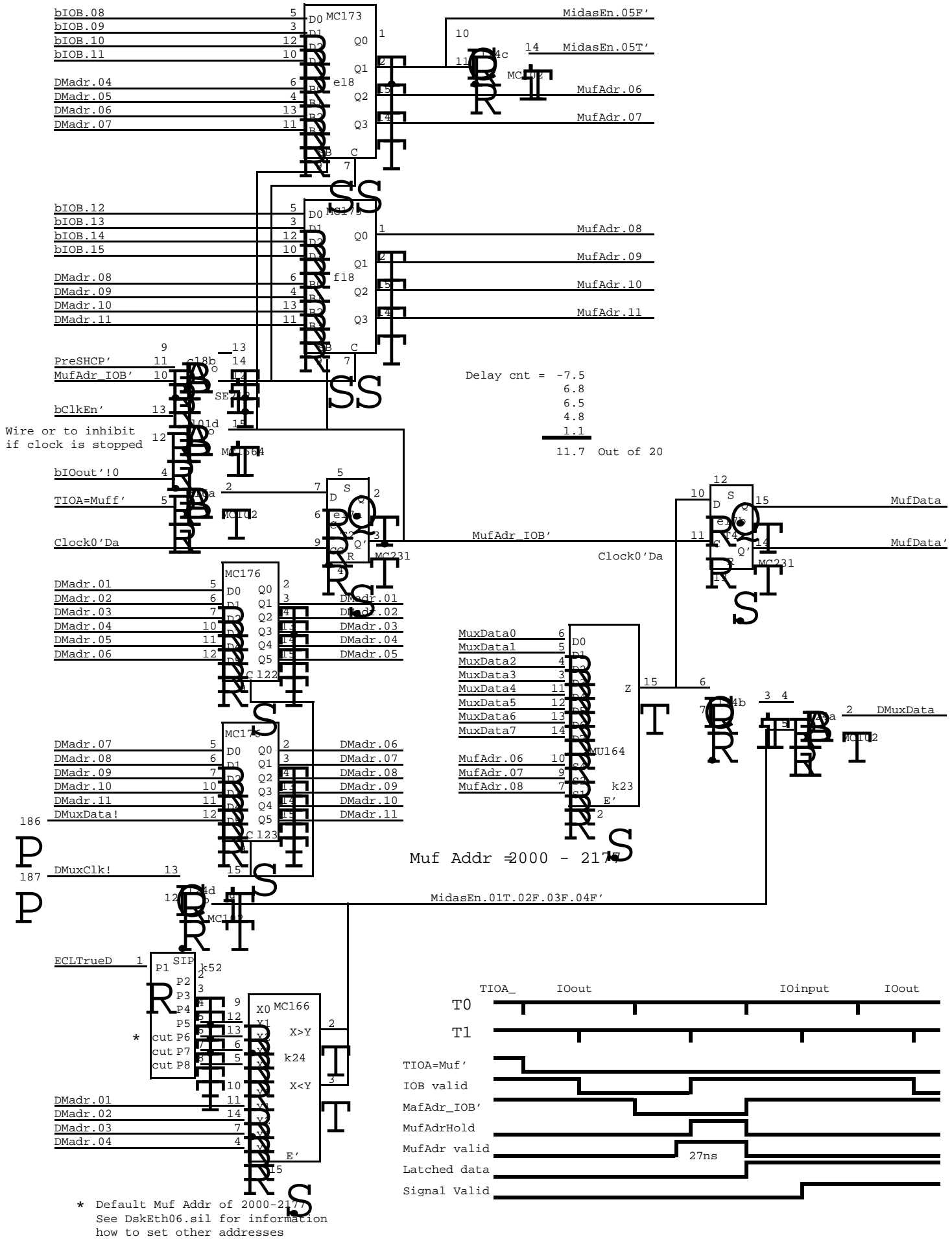
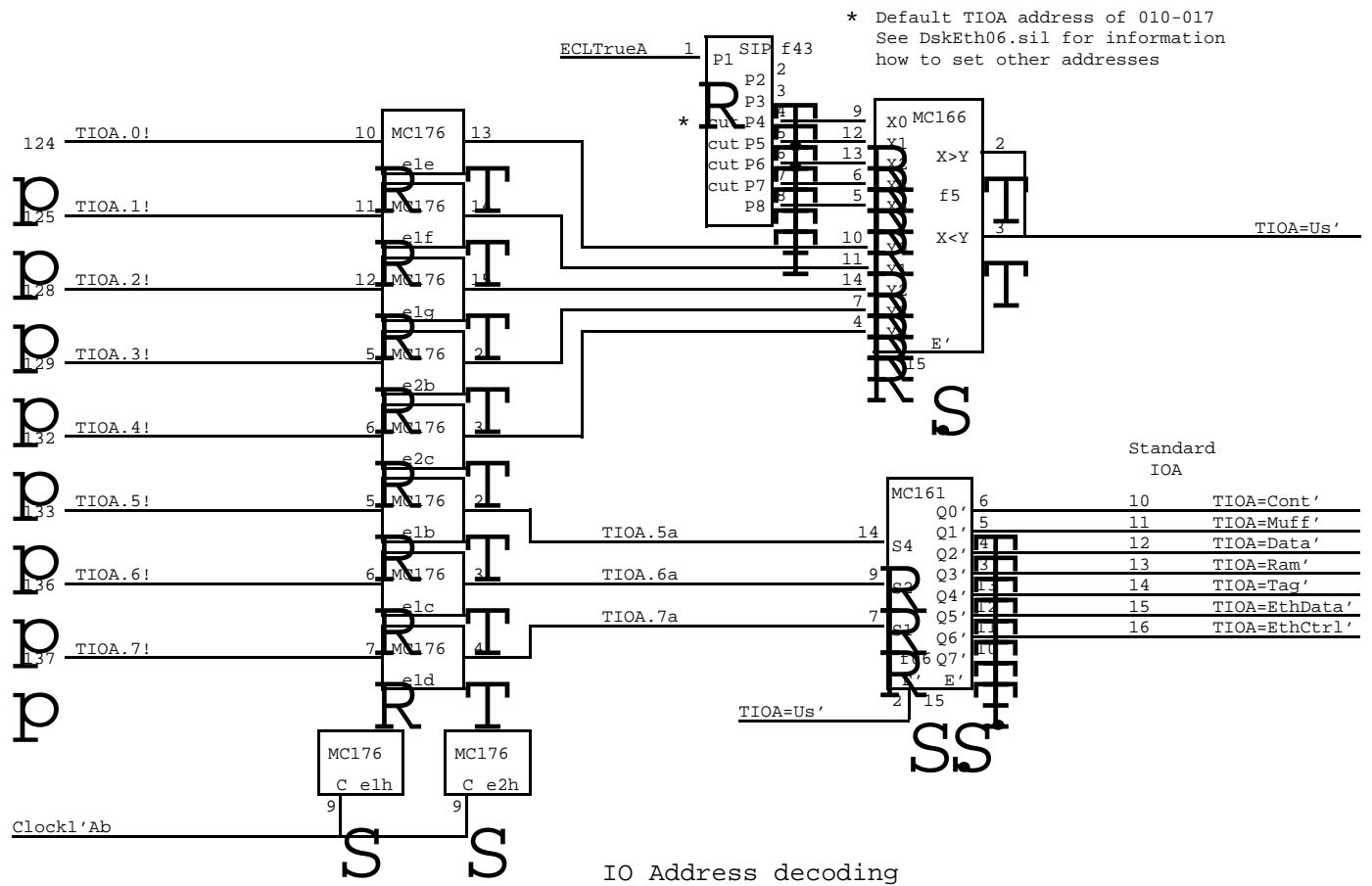


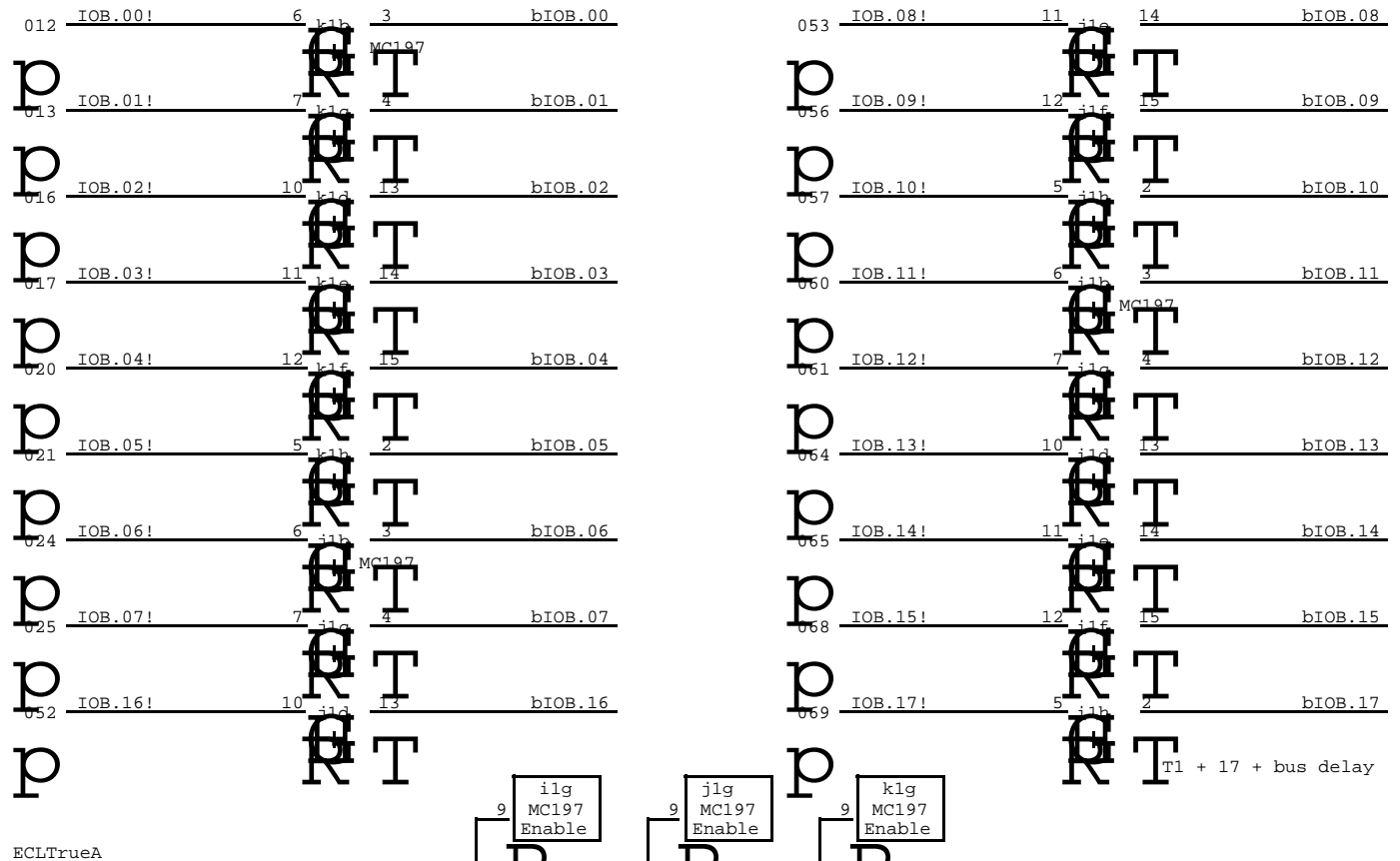
1) Drawings of common logic	01
Midas Muffler Control	01
TIOA and IOB receivers/drivers	02
Common Clock and Temperature Sense	04
Layout	05
2) Drawings for TriconD disk Controller	07
State Control Register	08
Format Ram, Counter and Proms	09
Tag Register	10
Disk Drive Control	11
FIFO	13
Error Correction Shift Register	15
Task Wake-Up and IOB parity check	16
Disk Mufflers	18
Dorado and Disk Clock Distribution	19
I/O pins and Termination	20
Timing Diagram	21
Cable Assembly Drawings	22
3) Drawings for Ethernet Controller	23
Phase Decoder	24
Receiver	25
Transmitter	29
Phase Encoder	33
Test Logic	34
Dorado and Ether Clock Distribution	35
Next Bus and IOattention	36
Ether Mufflers	37
Cable I/O and termination	38
Timing Diagrams	40





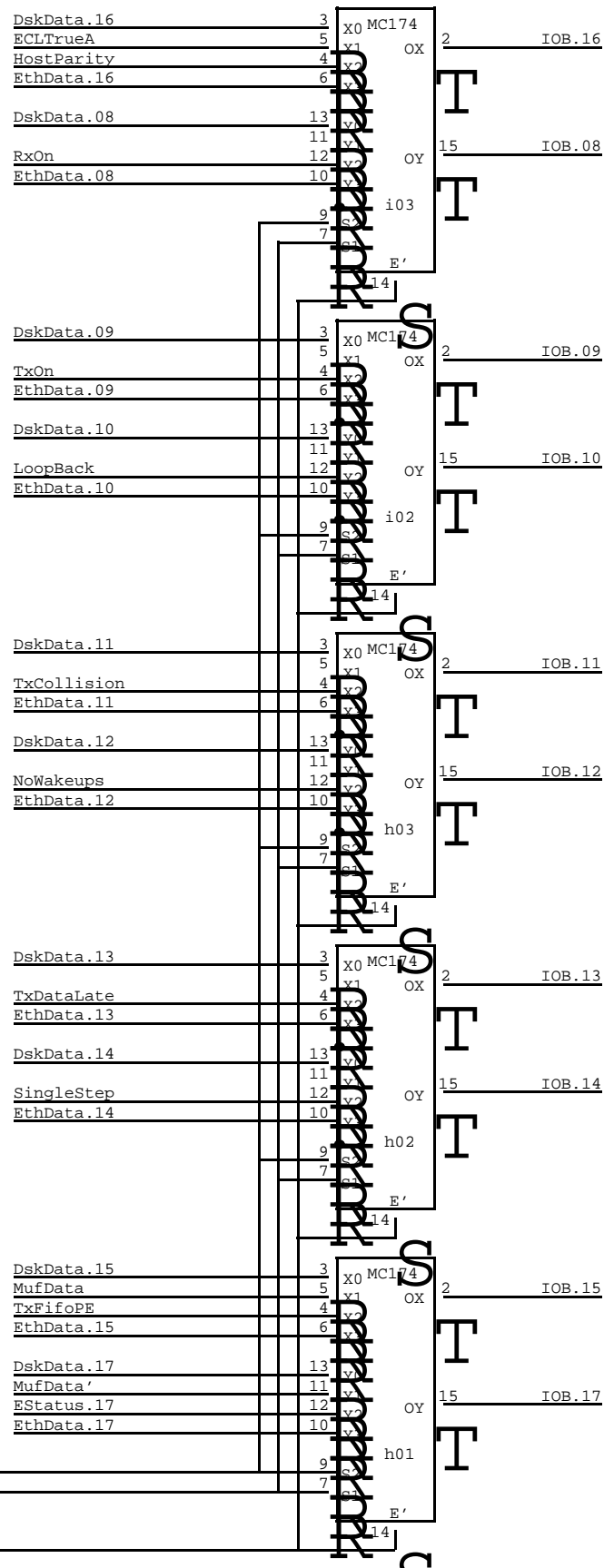
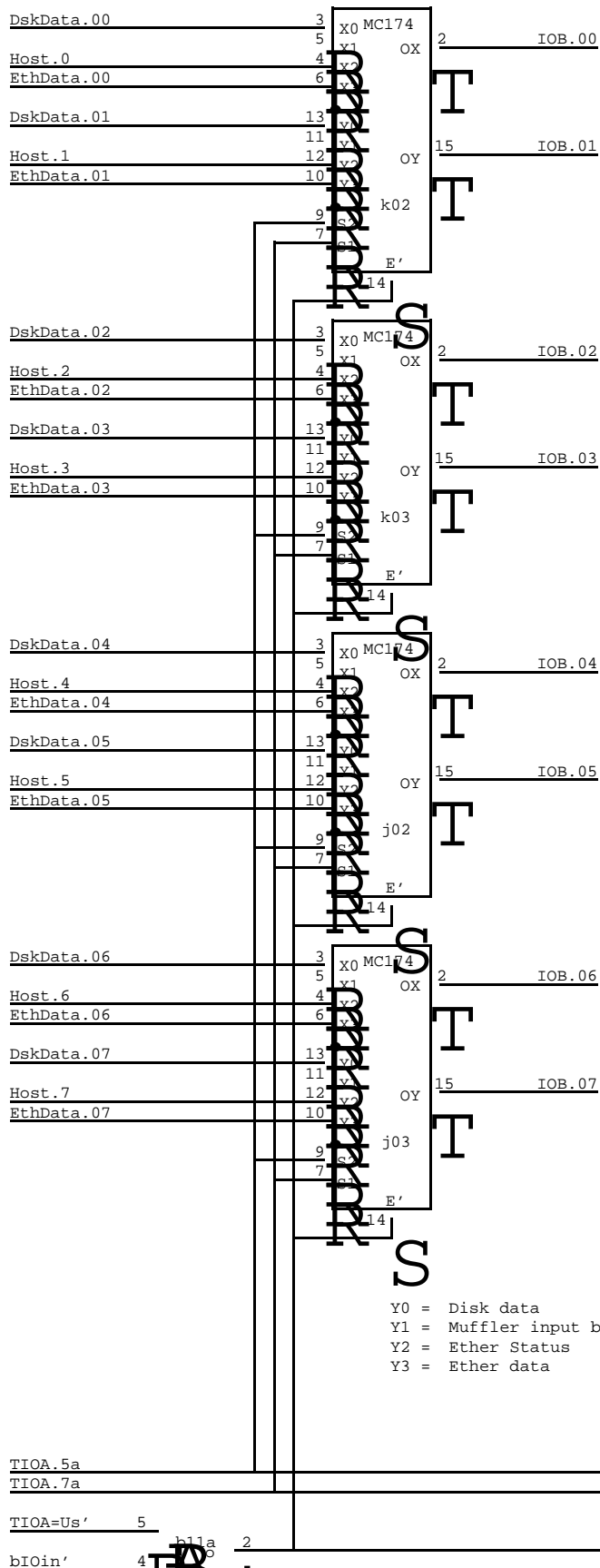
IO Address decoding

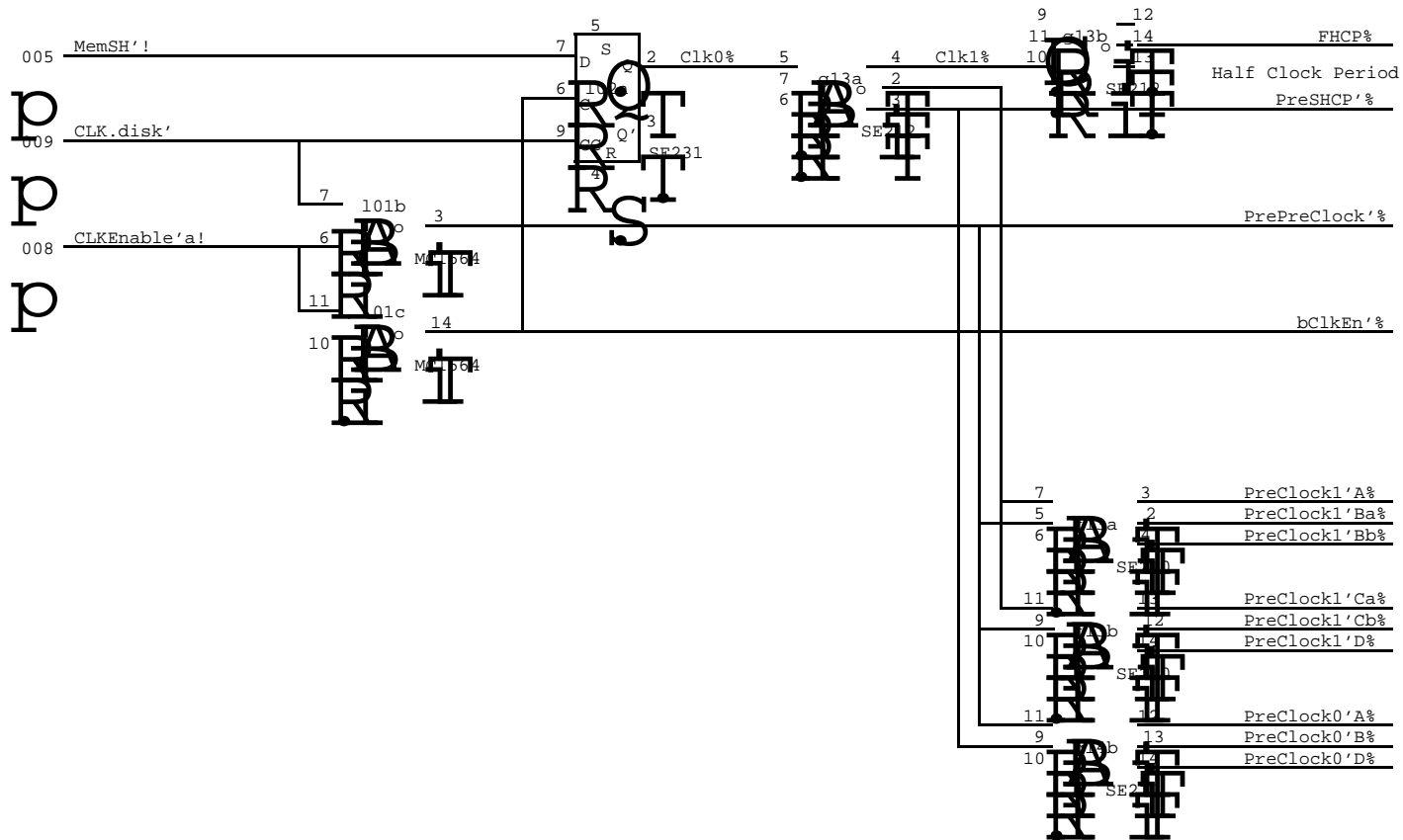
IOB receivers



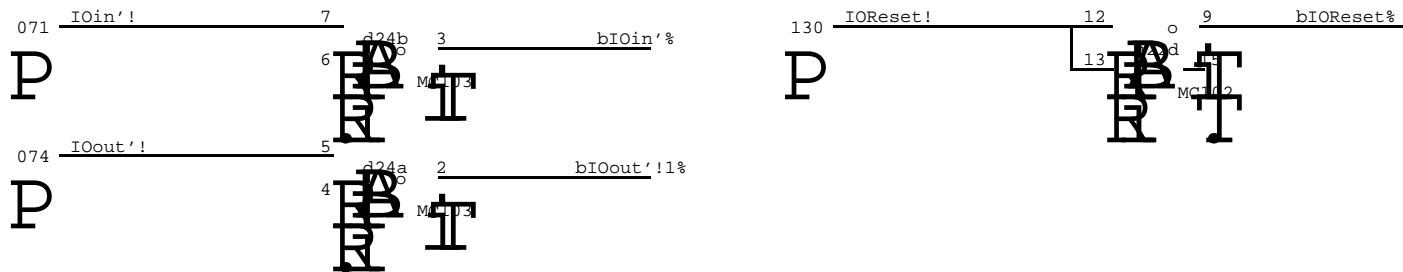
NOTE: IOB data received by this board is tested as part of the disk controller (Pg 18)
Both the disk and the Ethernet check the data parity after it has gone
through the respective FIFO's.

XEROX PARC	Project Dorado	Drawing IOA & IOB	File DskEth02.sil	Designer Bates/Boggs	Rev Bd	Date 1/15/79	Page 02
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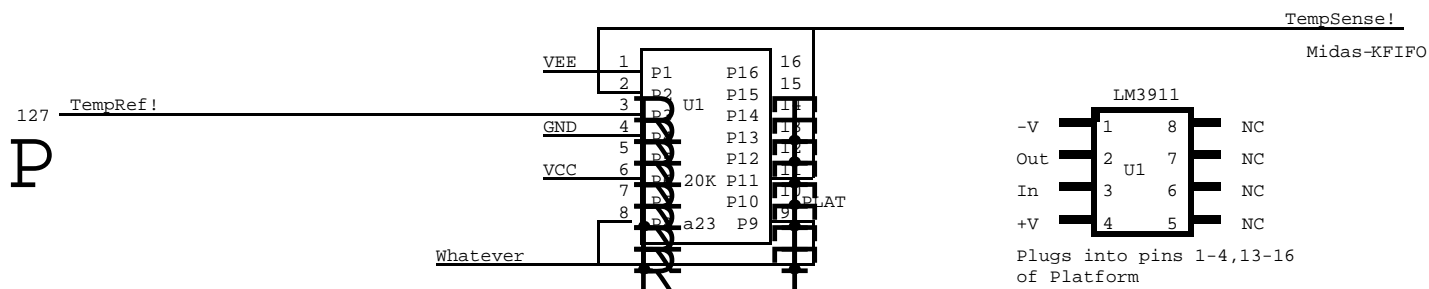




Common Clock circuitry



Temperature Sensor

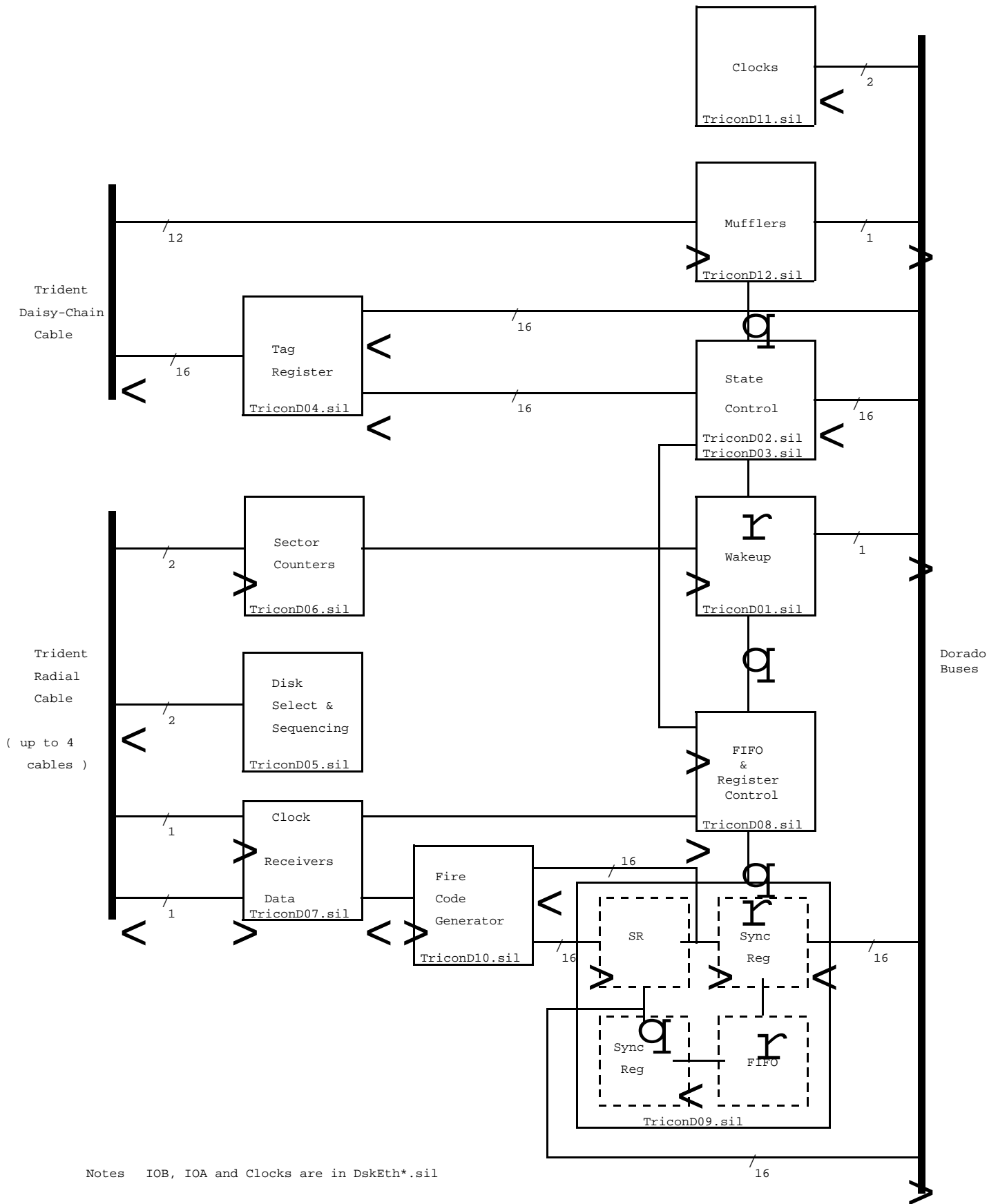


Cut SIP legs at k52 to set the
Muffler addresses for the board

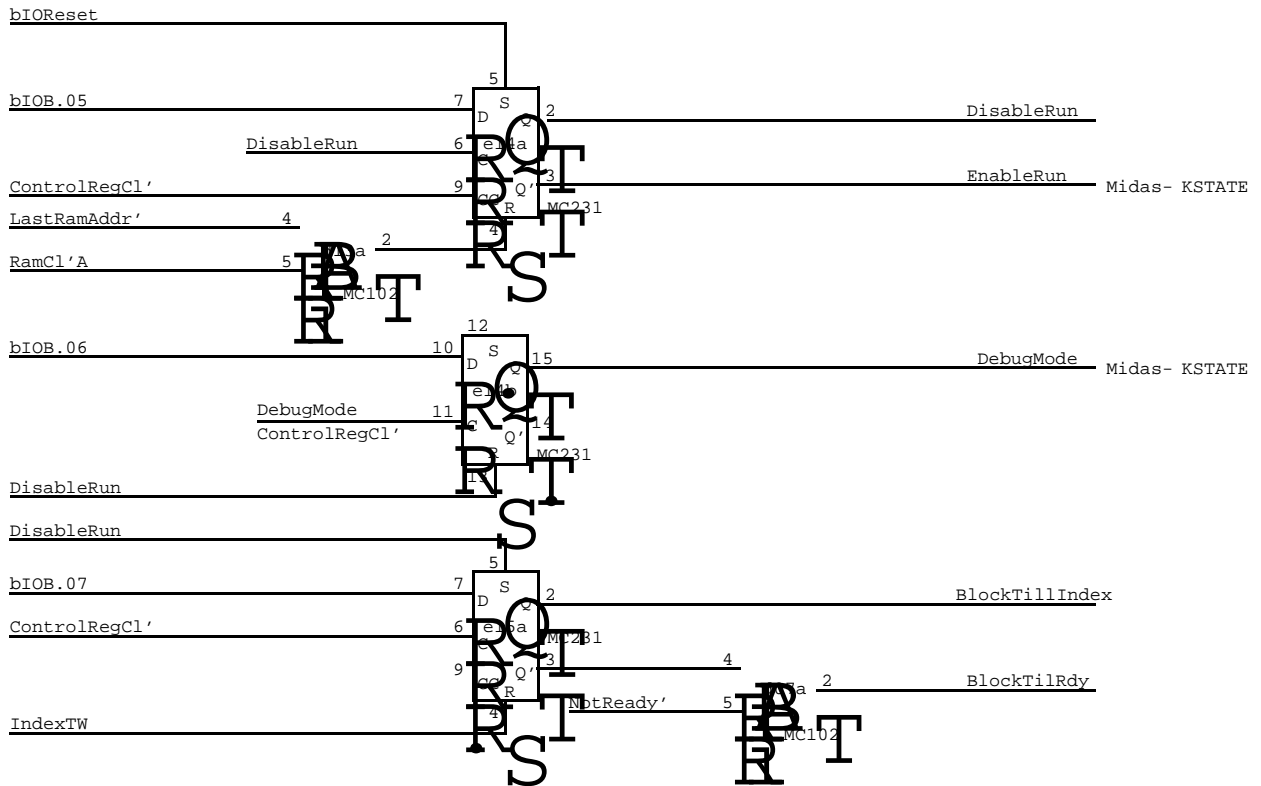
Muff Addr	P5	P6	P7	P8
0000-0177	cut	cut	cut	cut
0200-0377	cut	cut	cut	
0400-0577	cut	cut		cut
0600-0777	cut	cut		
1000-1177	cut		cut	cut
1200-1377	cut		cut	
1400-1577	cut			cut
1600-1777	cut			
2000-2177		cut	cut	cut
2200-2377		cut	cut	
2400-2577		cut		cut
2600-2777		cut		
3000-3177			cut	cut
3200-3377			cut	
3400-3577				cut
3600-3777				

Cut SIP legs at f43 to set the
IOA bus addresses for the board

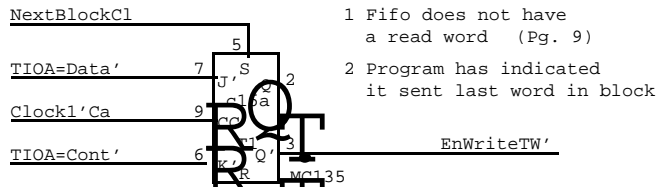
IOA	P4	P5	P6	P7	P8
000-007	cut	cut	cut	cut	cut
010-017	cut	cut	cut	cut	
020-027	cut	cut	cut		cut
030-037	cut	cut	cut		
040-047	cut	cut		cut	cut
050-057	cut	cut		cut	
060-067	cut	cut			cut
070-077	cut	cut			
100-107	cut		cut	cut	cut
110-117	cut		cut	cut	
120-127	cut		cut		cut
130-137	cut		cut		
140-147	cut			cut	cut
150-157	cut			cut	
160-167	cut				cut
170-177	cut				
200-207		cut	cut	cut	cut
210-217		cut	cut	cut	
220-227		cut	cut	cut	cut
230-237		cut	cut	cut	
240-247		cut		cut	cut
250-257		cut			
260-267		cut			cut
270-277		cut			
300-307			cut	cut	cut
310-317			cut	cut	
320-327			cut		cut
330-337			cut		
340-347				cut	cut
350-357				cut	
360-367					cut
370-377					



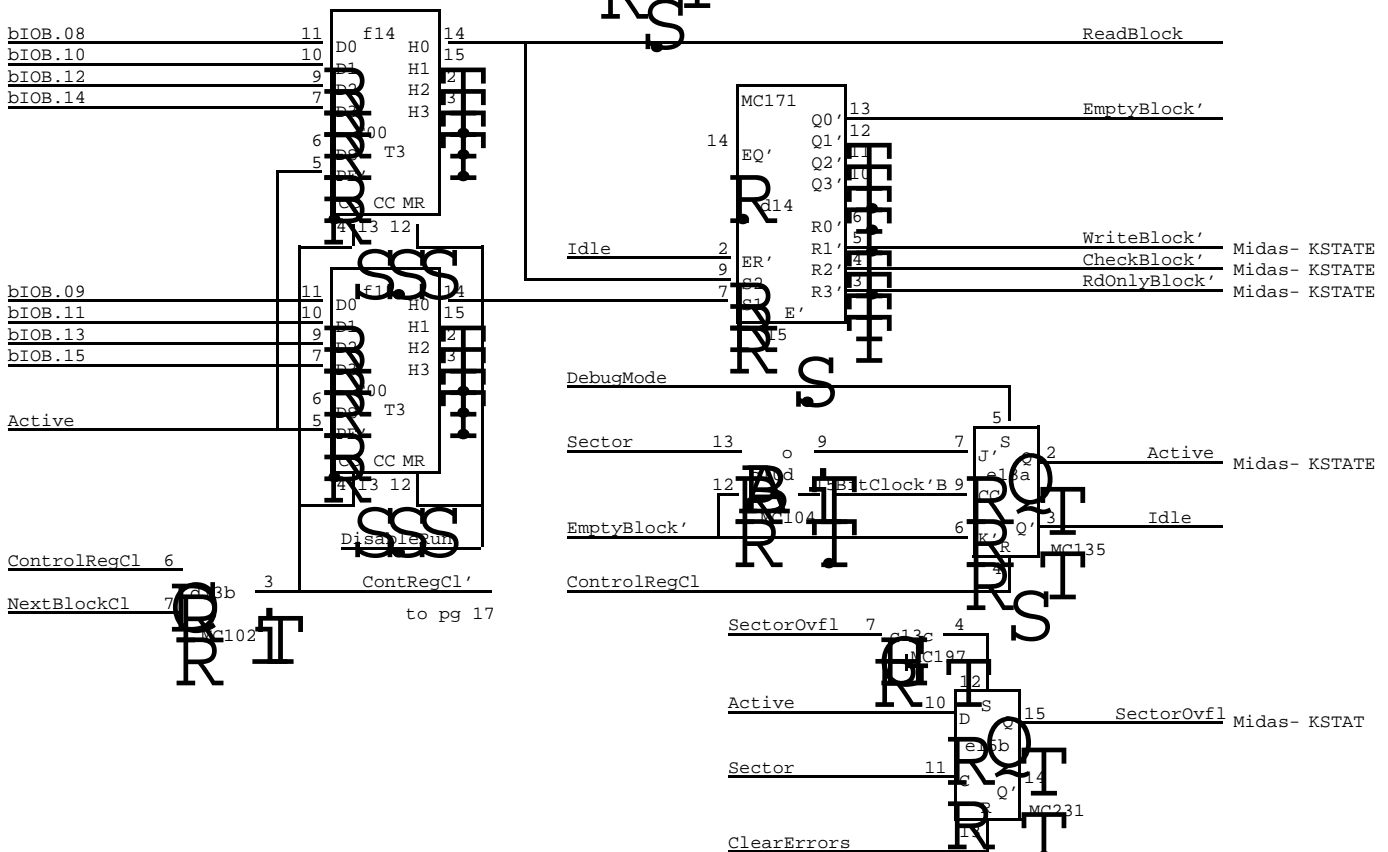
Notes IOB, IOA and Clocks are in DskEth*.sil

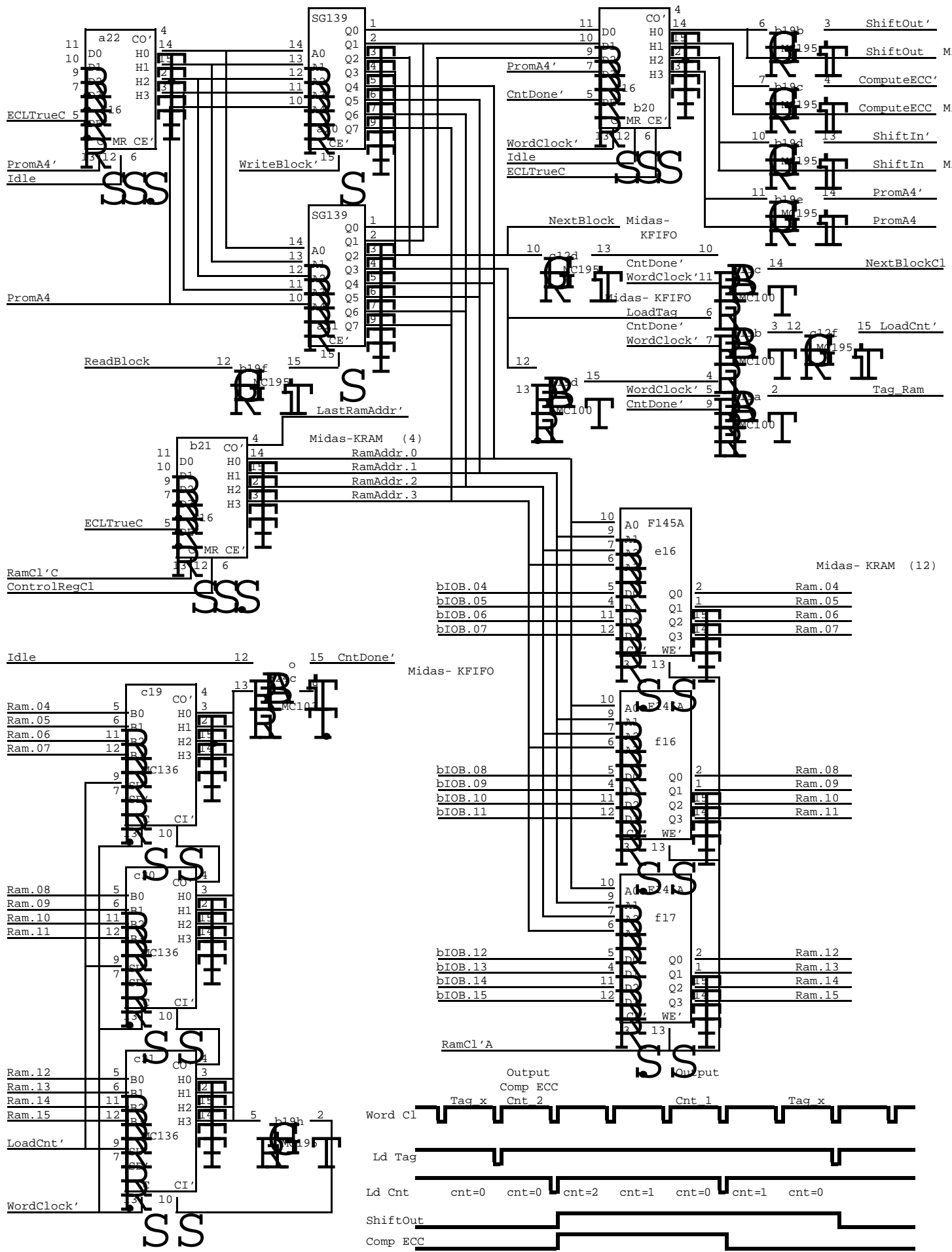


EnWriteTW' is low when:



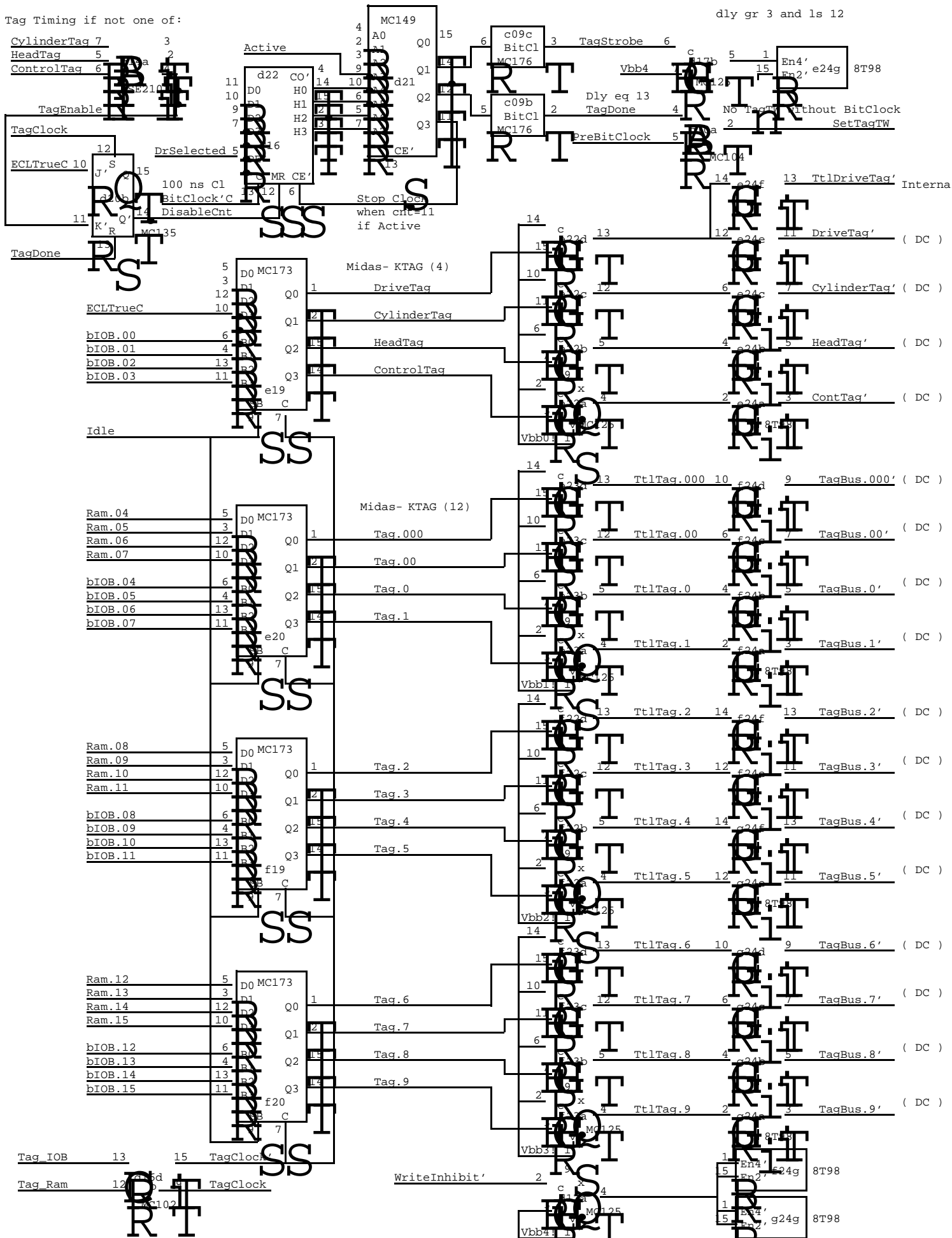
- 1 Fifo does not have a read word (Pg. 9)
- 2 Program has indicated it sent last word in block

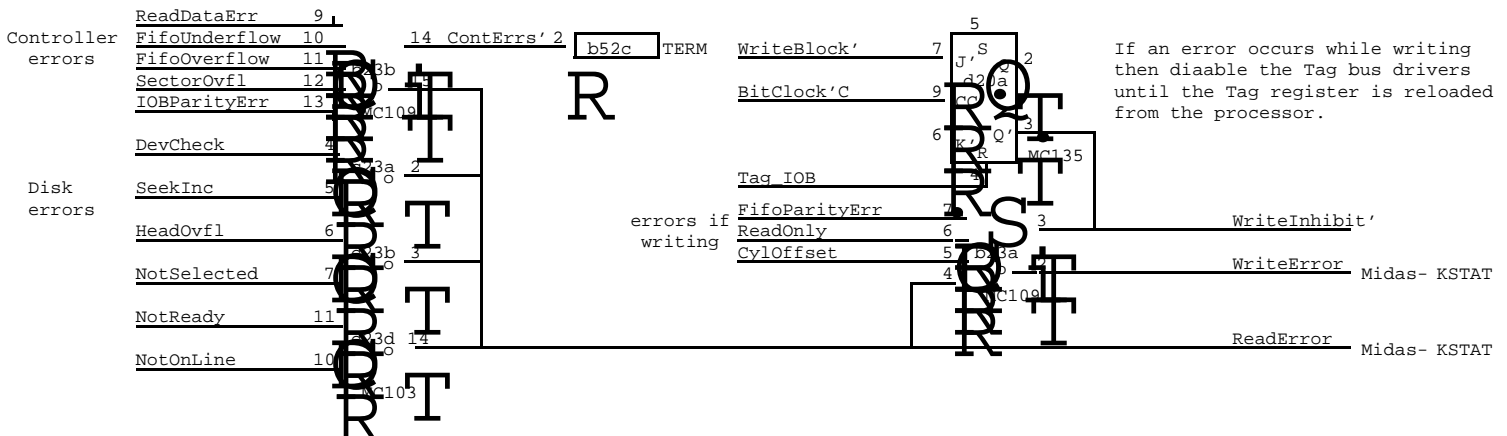
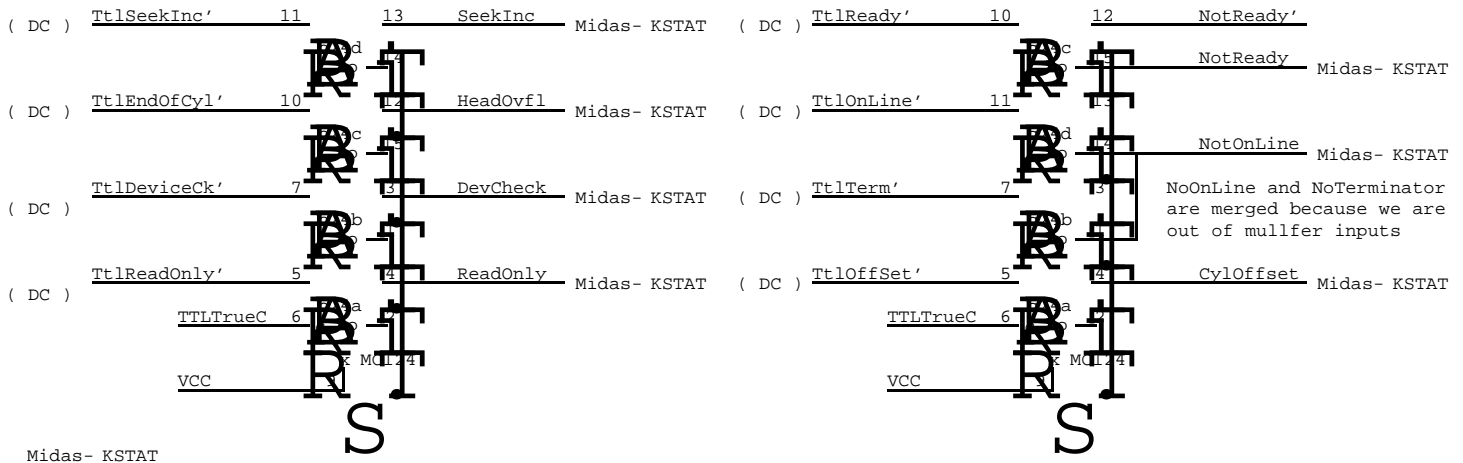
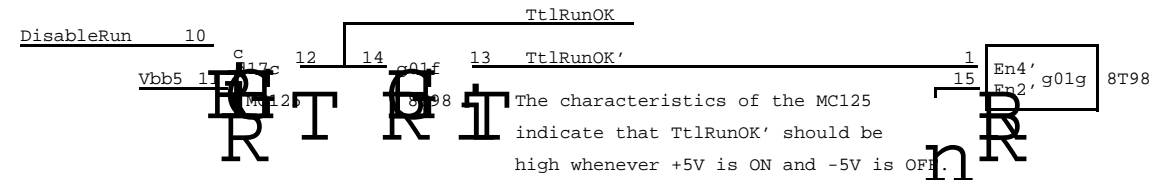
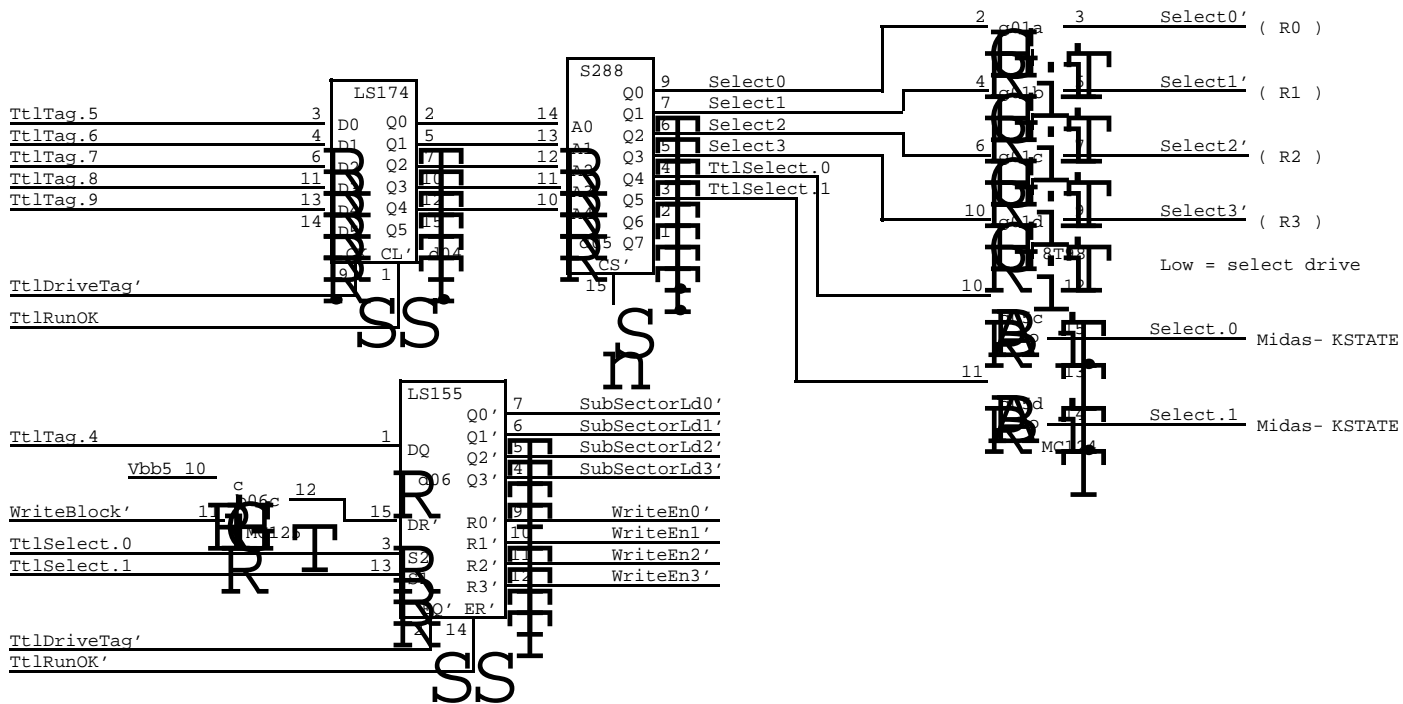


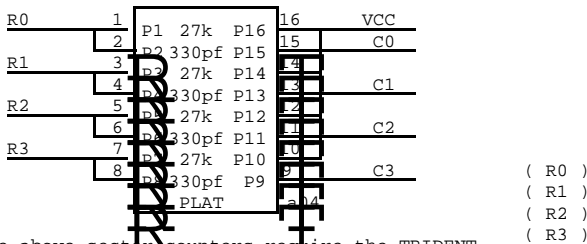
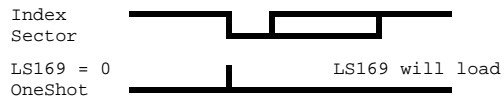
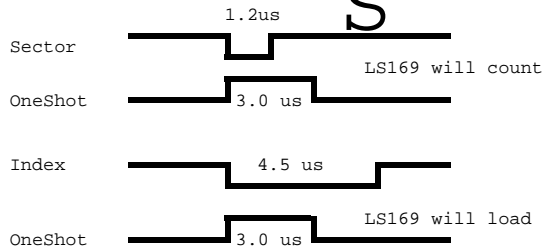
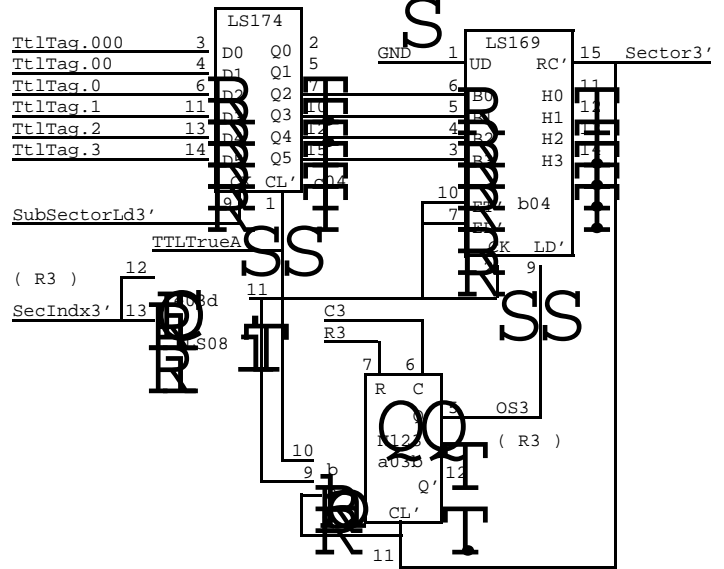
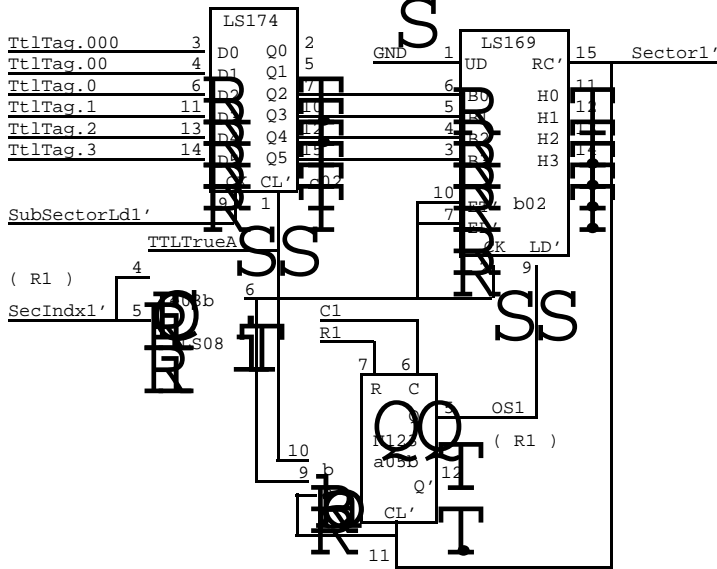
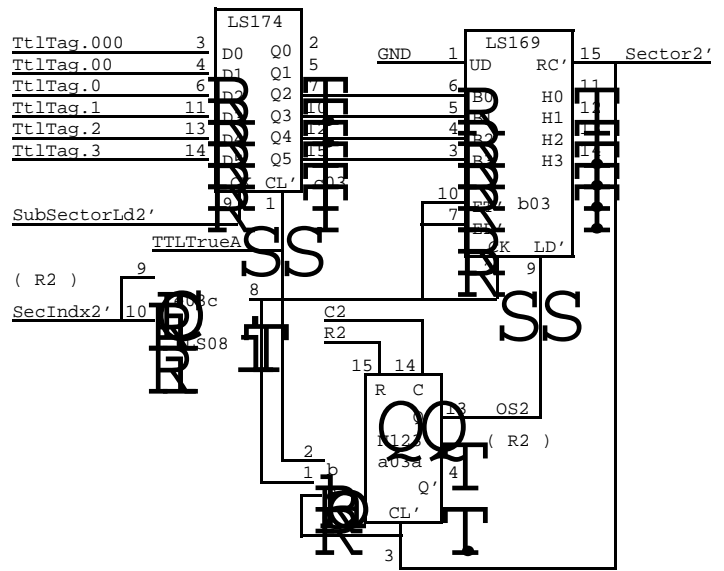
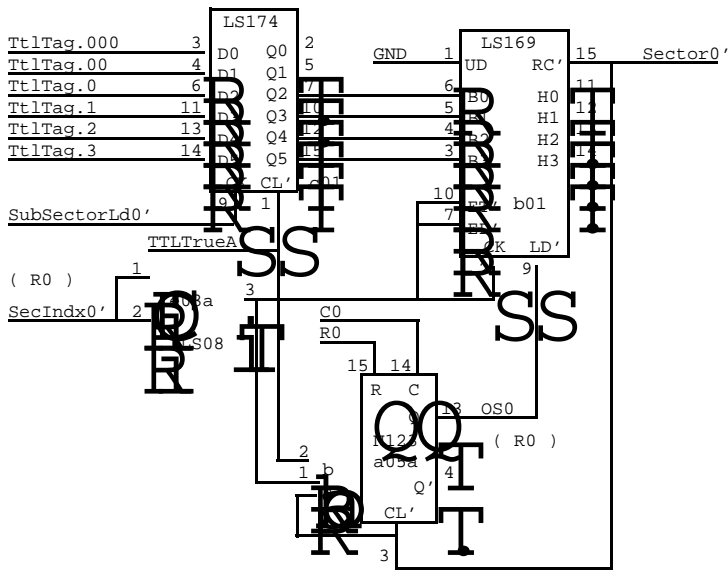


No Tag Timing if not one of:

dly gr 3 and ls 12

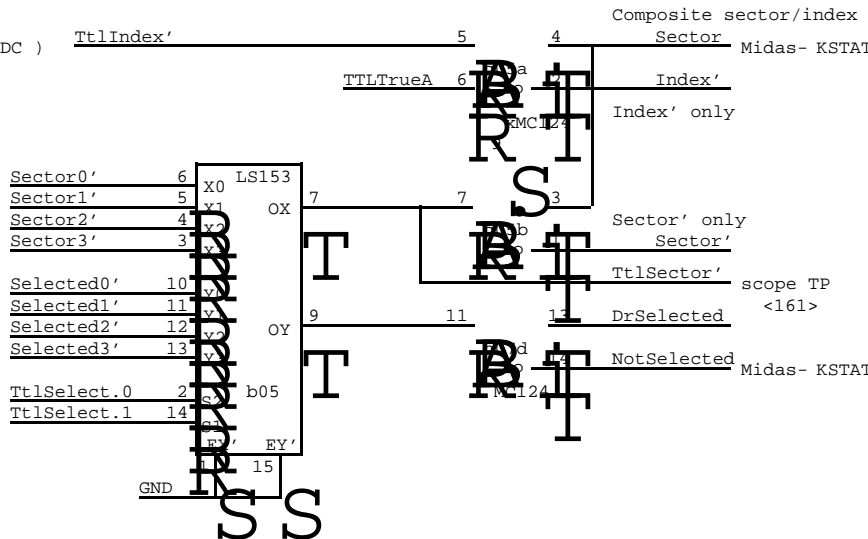


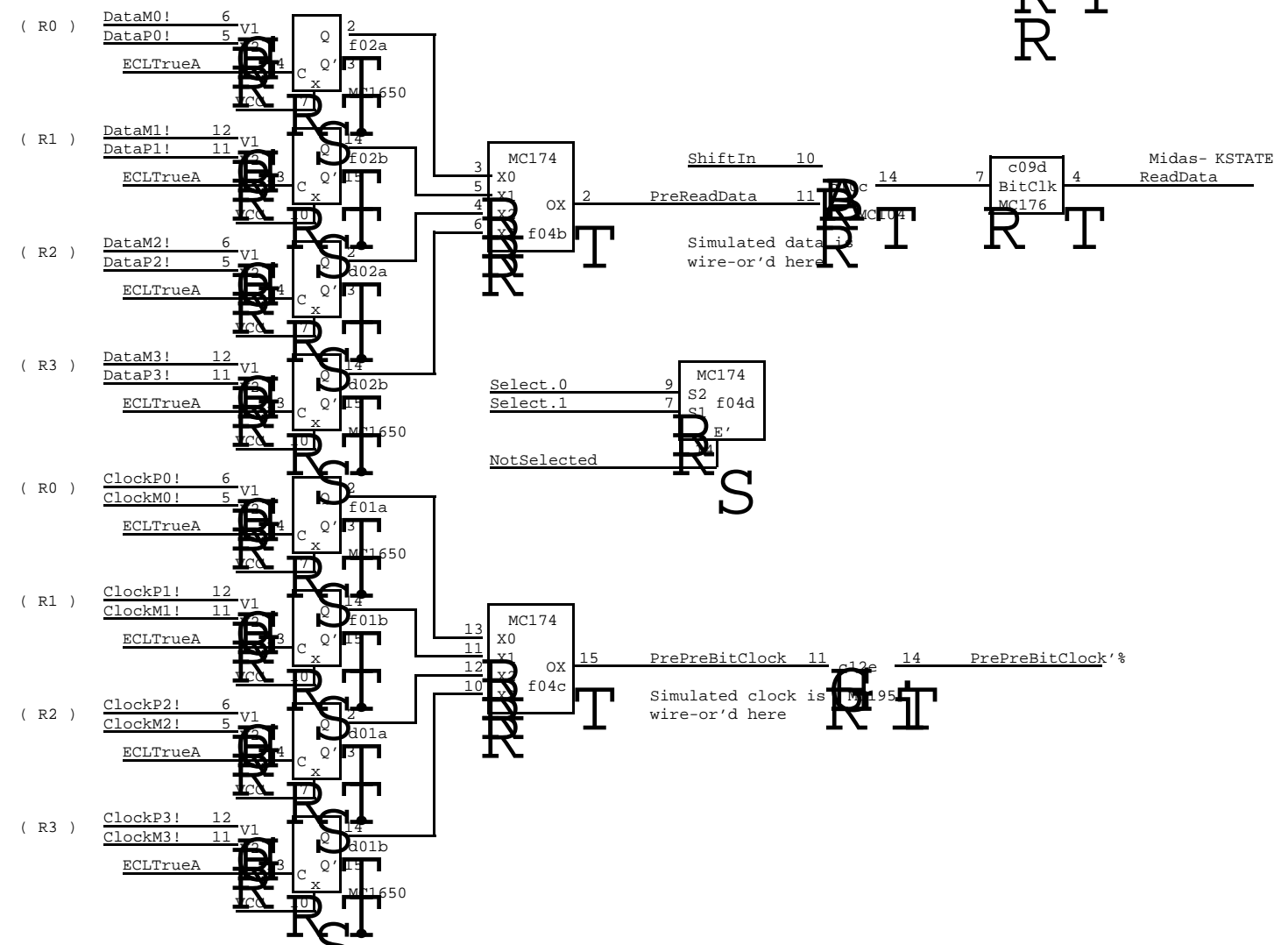
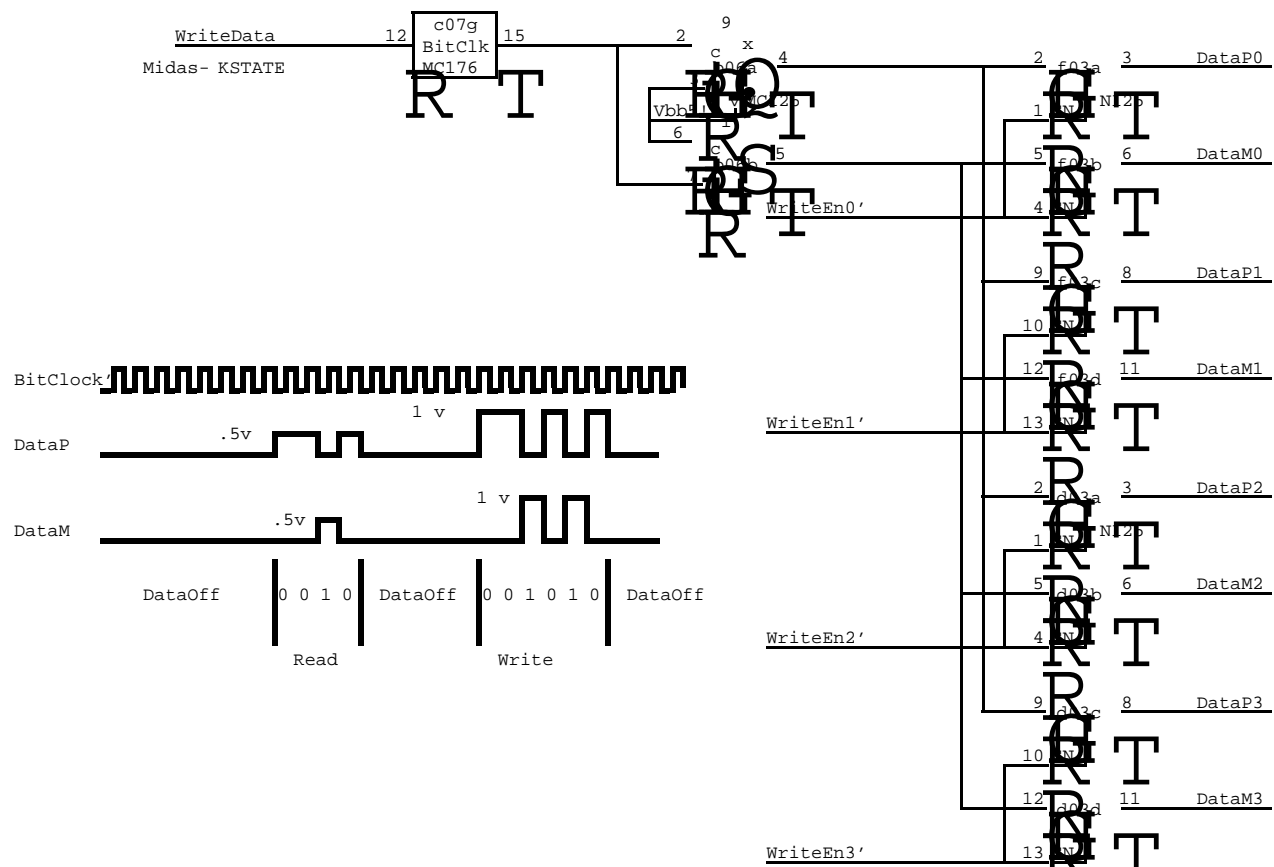


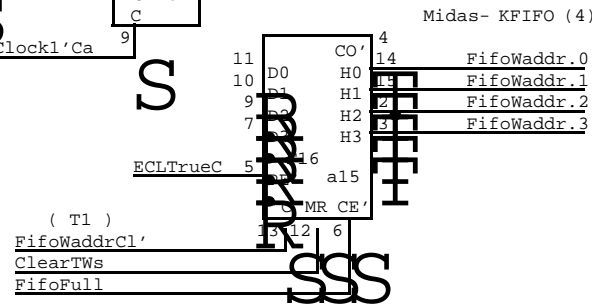
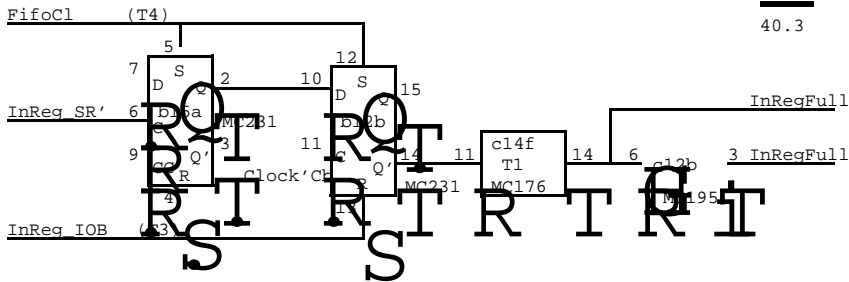
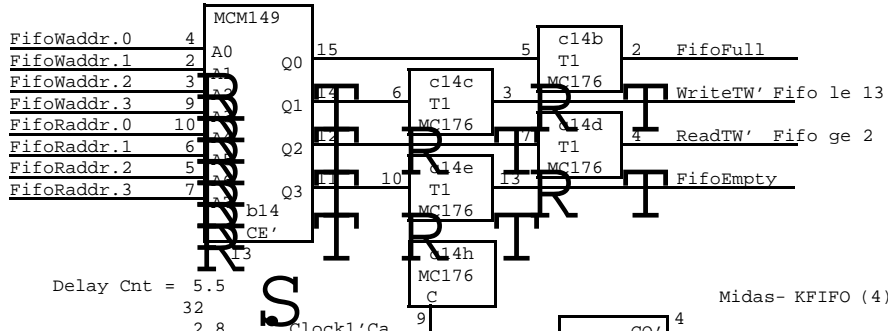
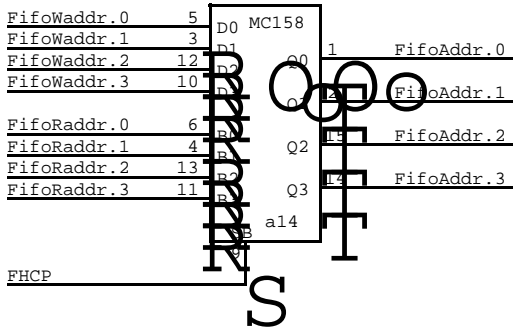


The above sector counters require the TRIDENT disk to have its sector counters set to provide 117 "sub-sector" pulses per revolution. This is done by setting the disk jumpers as follows:

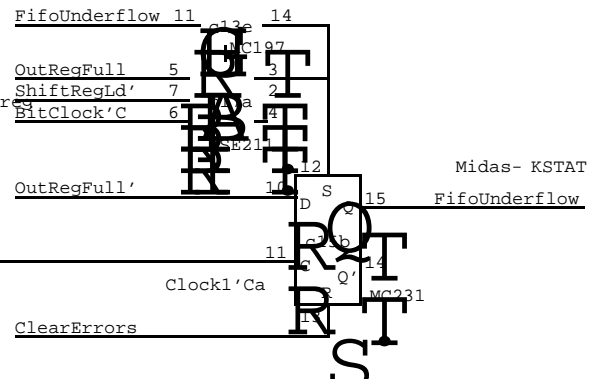
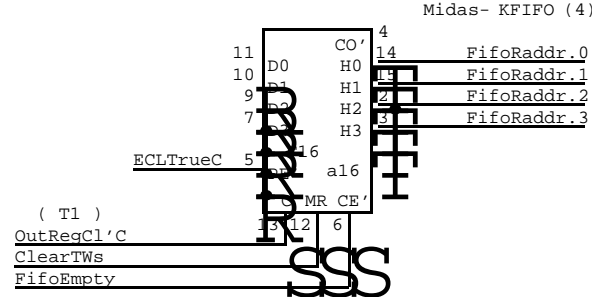
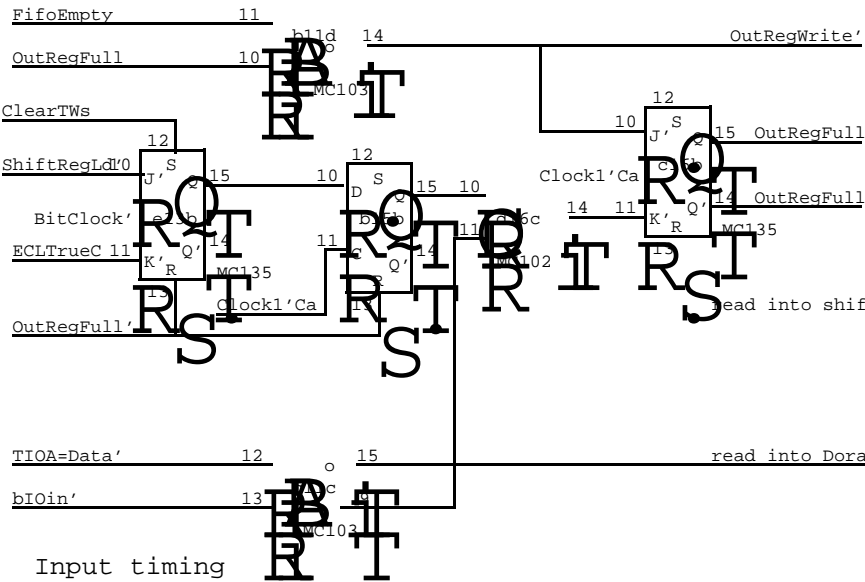
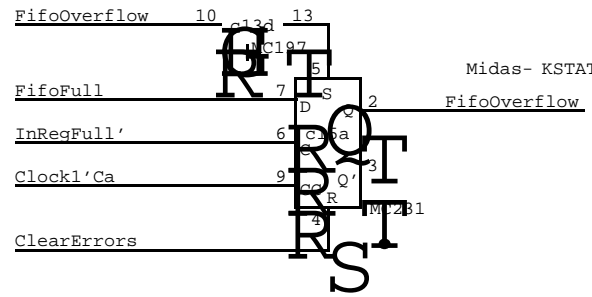
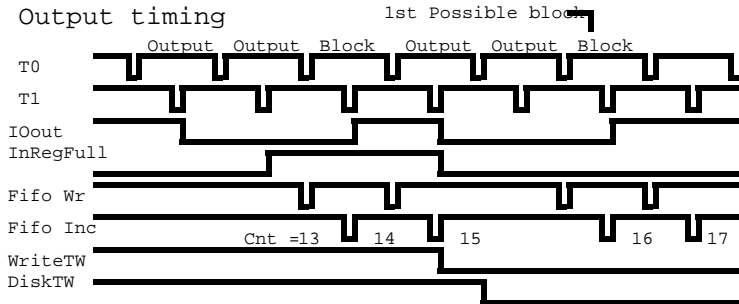
X6A	X6B
4 - 11	2 - 13
5 - 10	3 - 12
	4 - 11
	5 - 10
	6 - 09



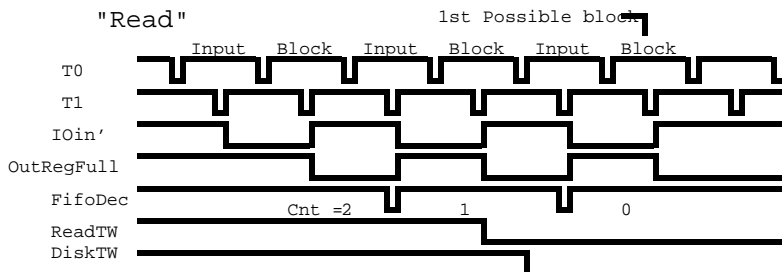




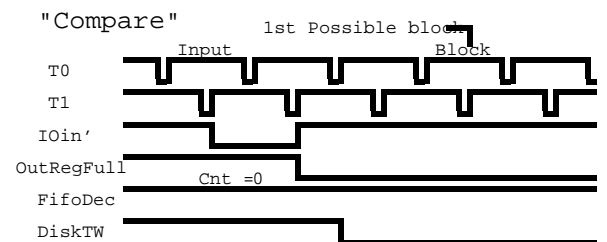
Output timing

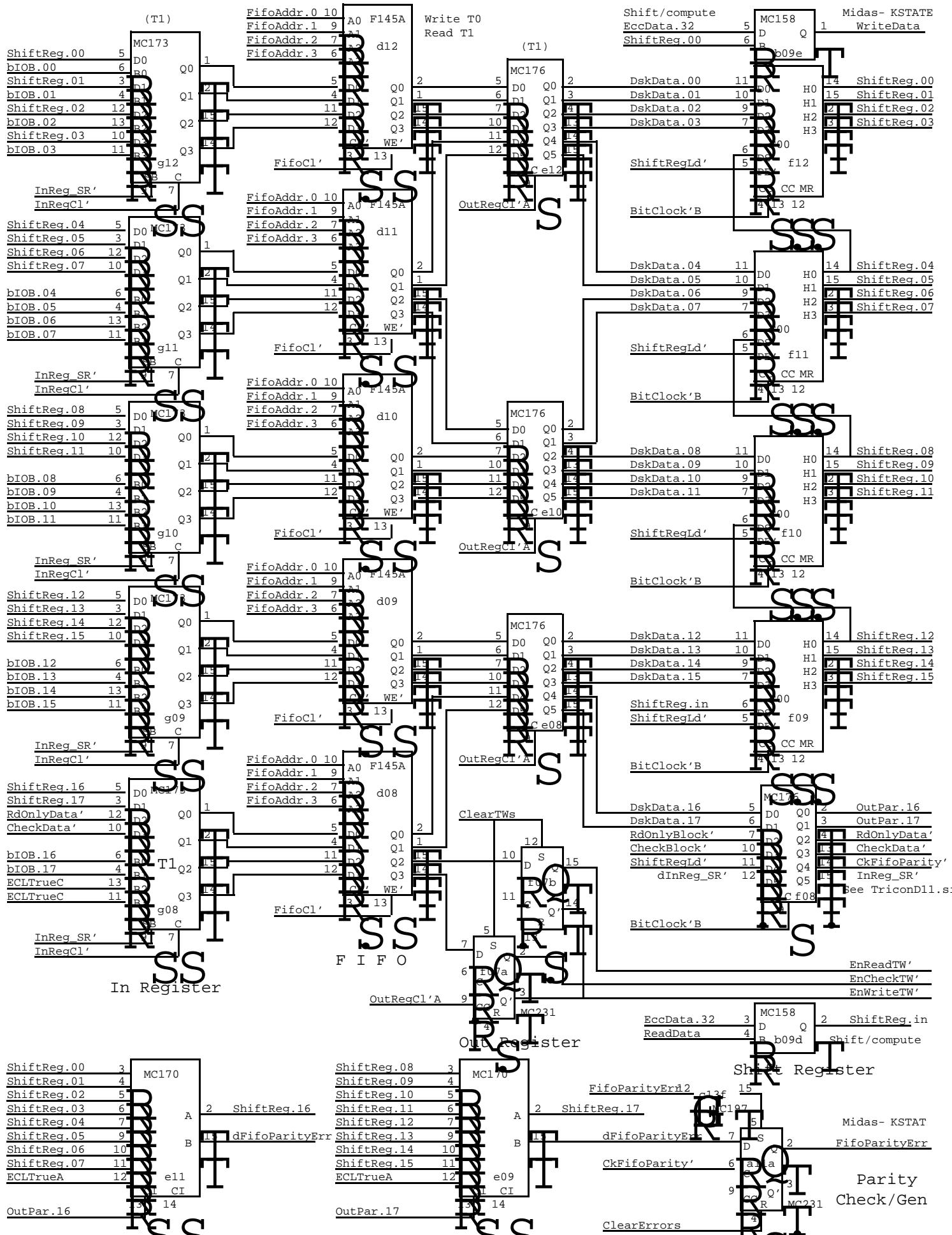


Input timing



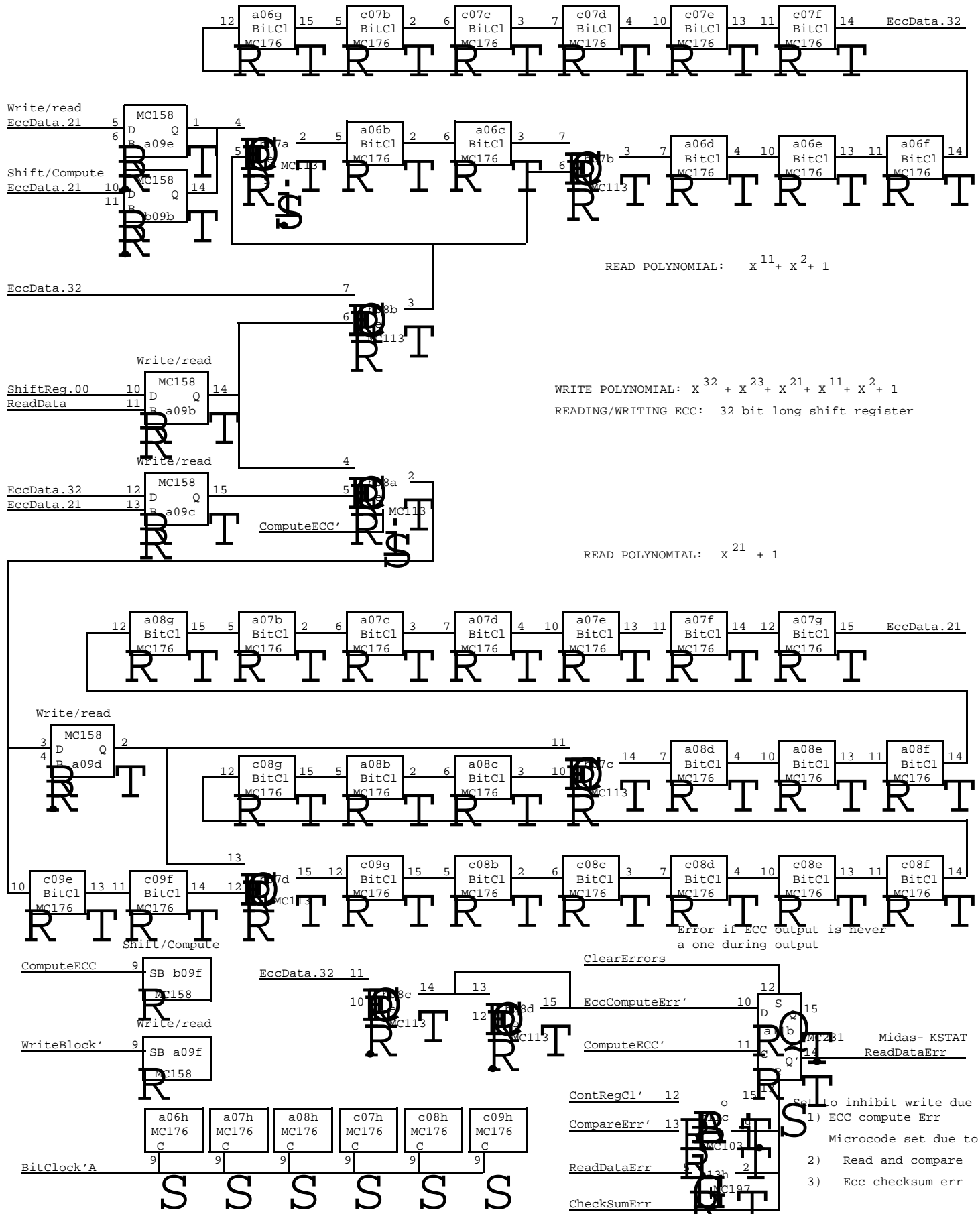
"Compare"

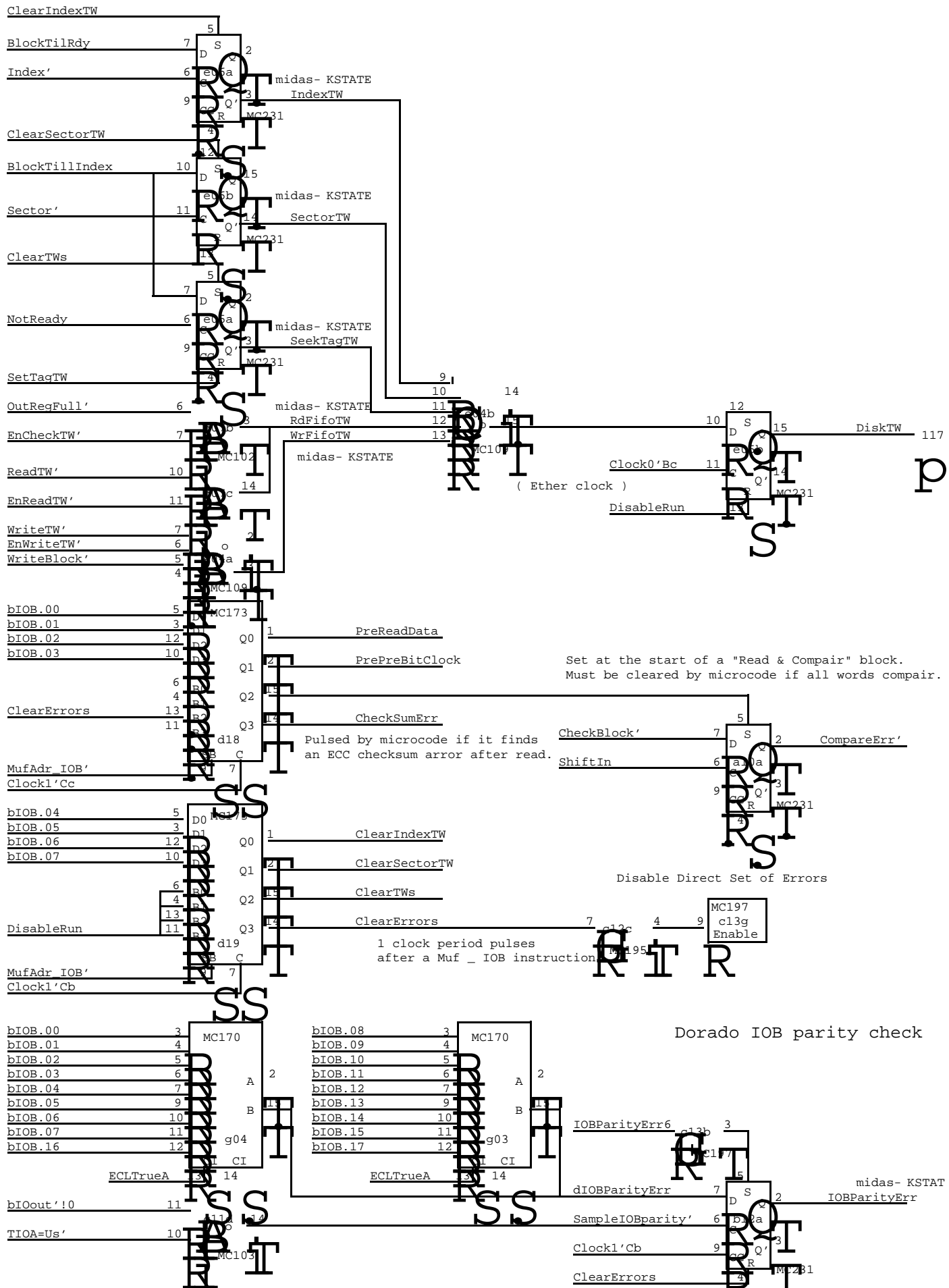


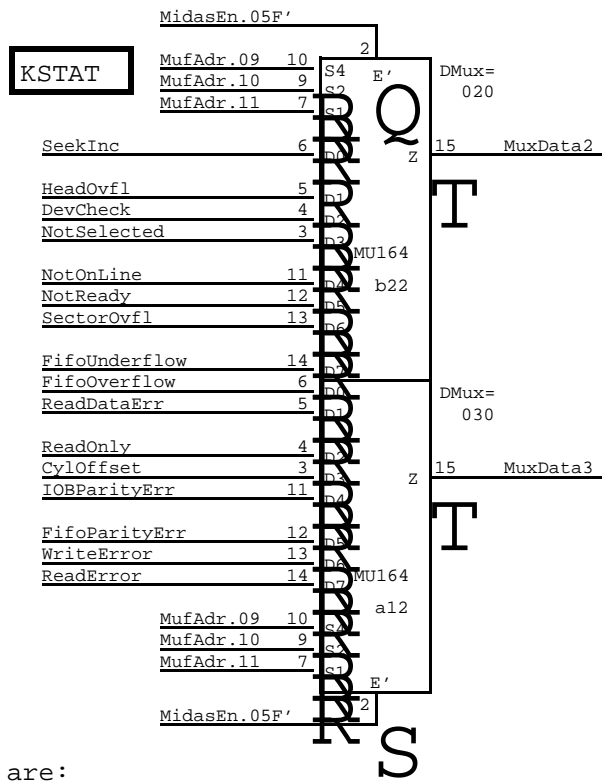
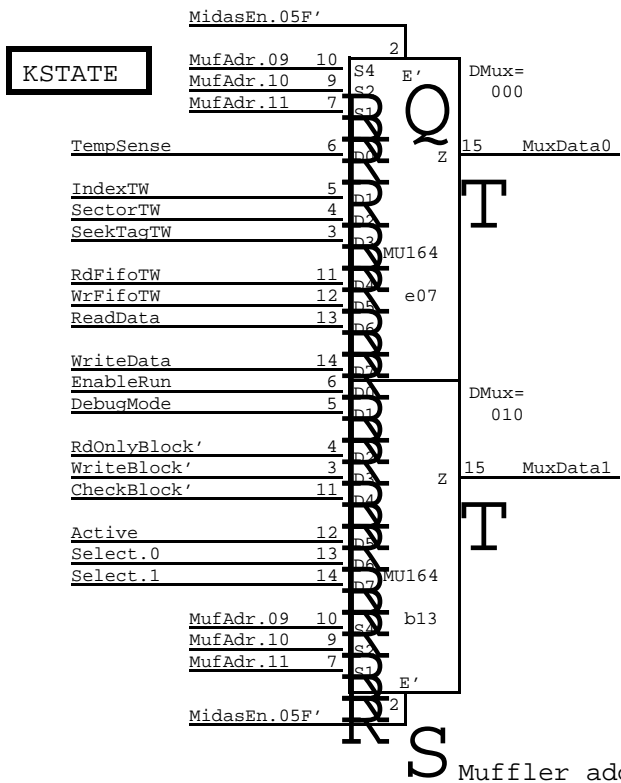


XEROX	Project	Drawing	File	Designer	Rev	Date	Page
PARC	Dorado	F I F O and Shift Register	TriconD09.sil	Roger Bates	Bd	1/8/79	15

POLYNOMIAL DIVIDER FOR FIRE CODE GENERATION



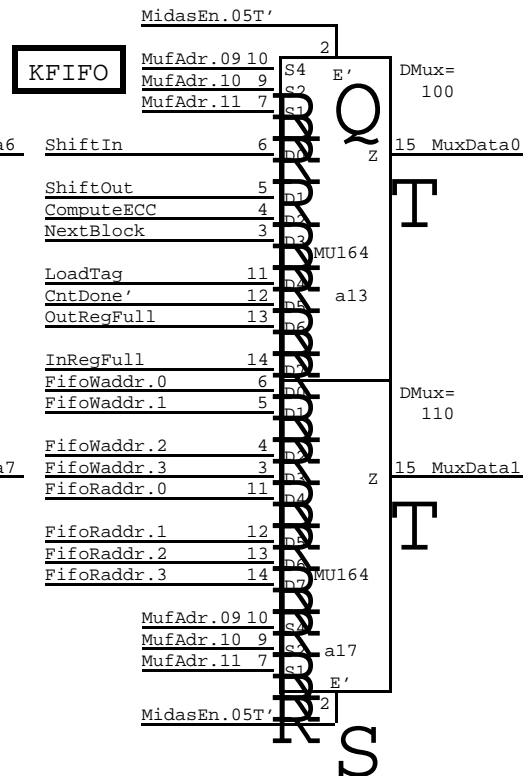
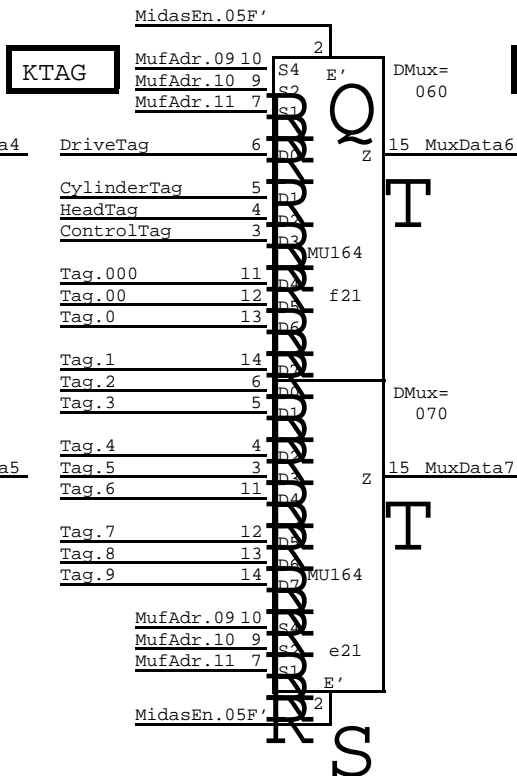
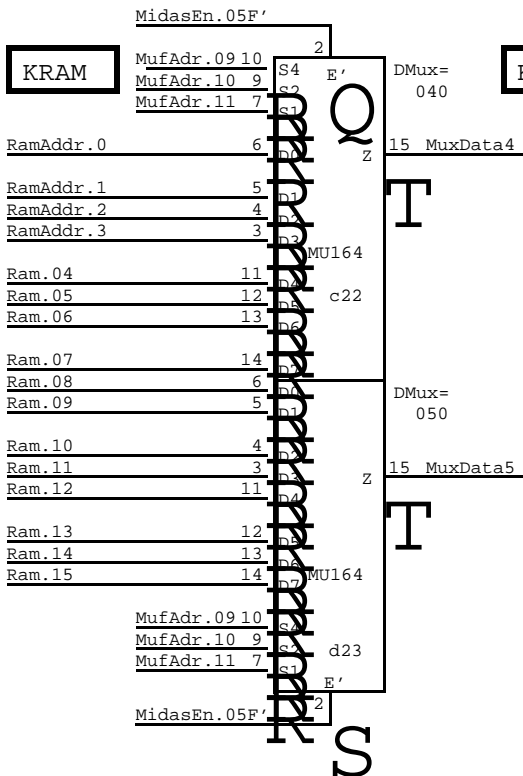


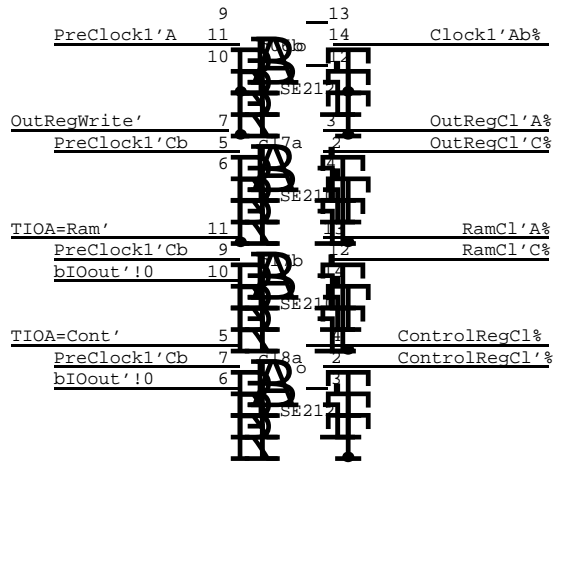
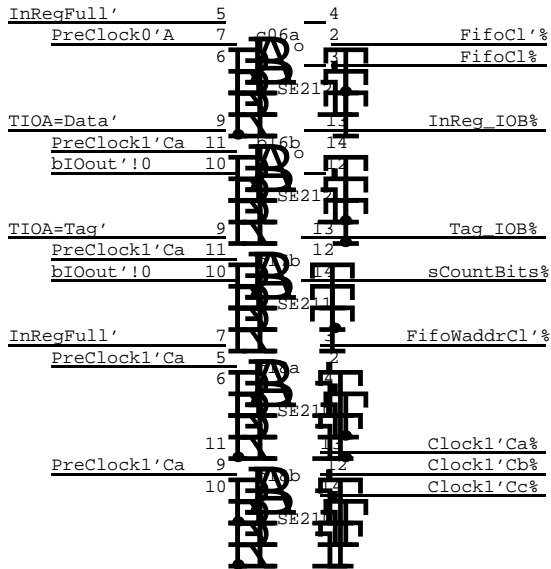
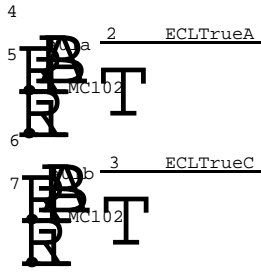


Muffler addresses are:

Value listed for Program input
Value plus 2000 for Midas input

Values from 120 to 177 are
used by the Ethernet

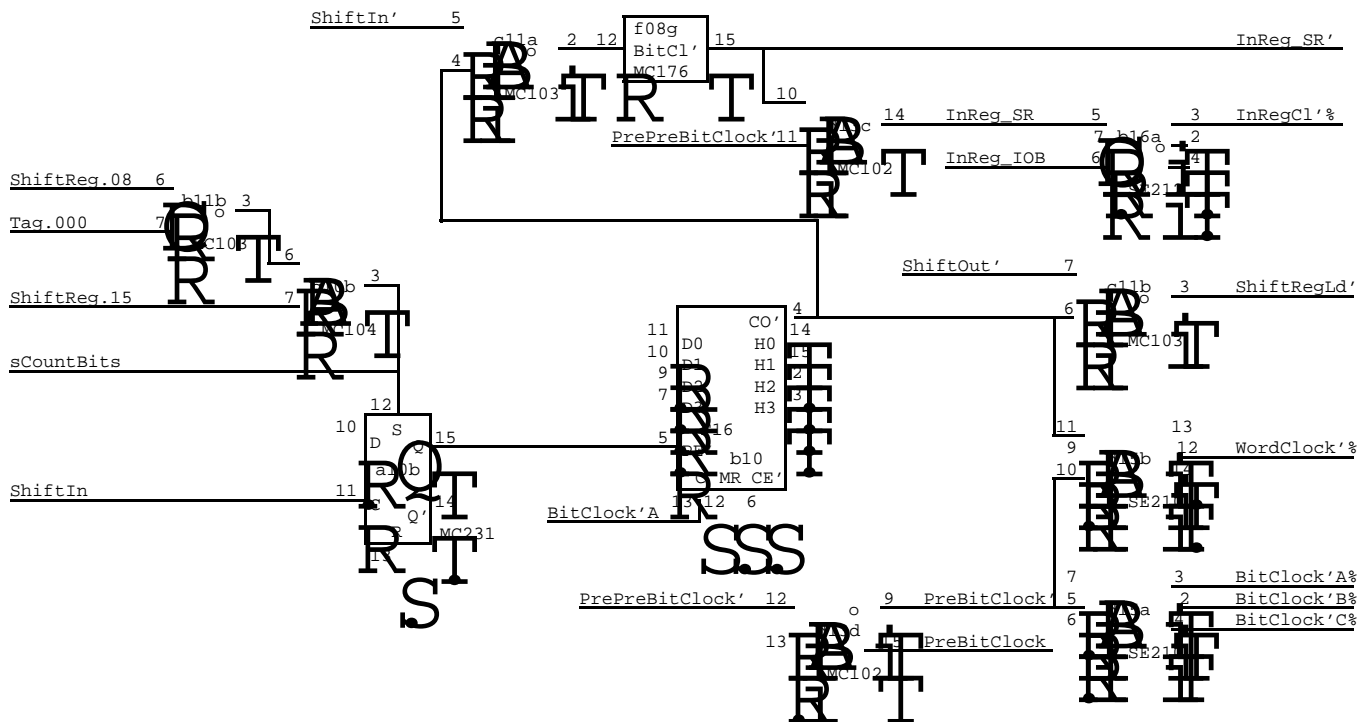




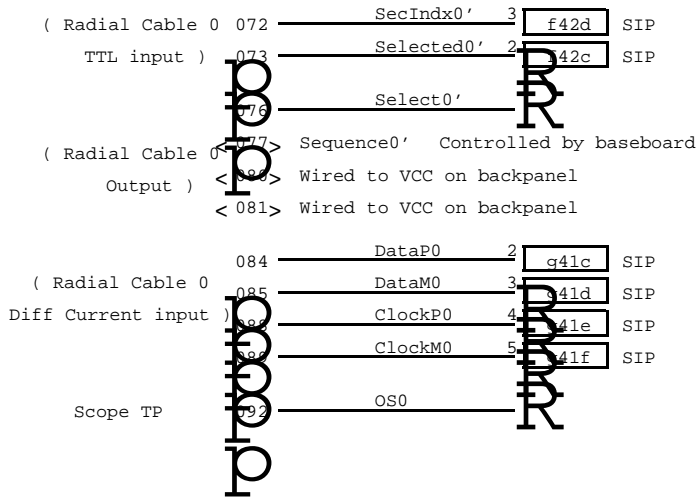
System Clocks

Disk Clocks

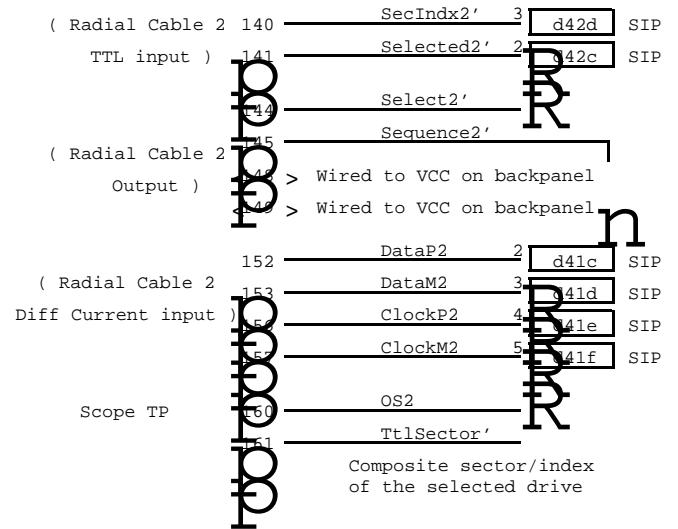
Delay reading of shift register
by 1 bit for correct bit alignment



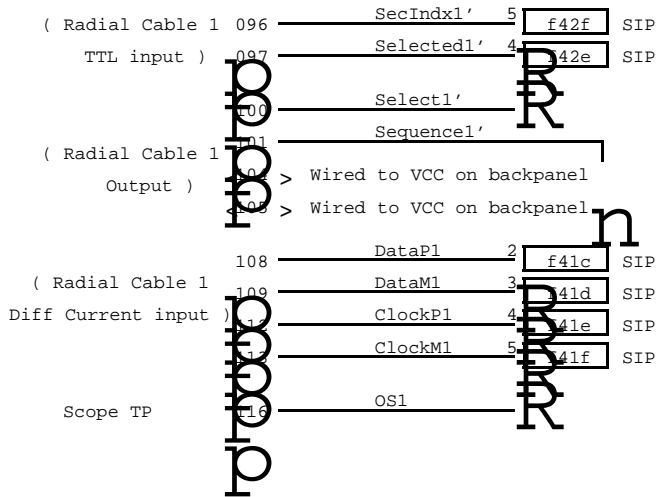
Radial Cable for Drive 0



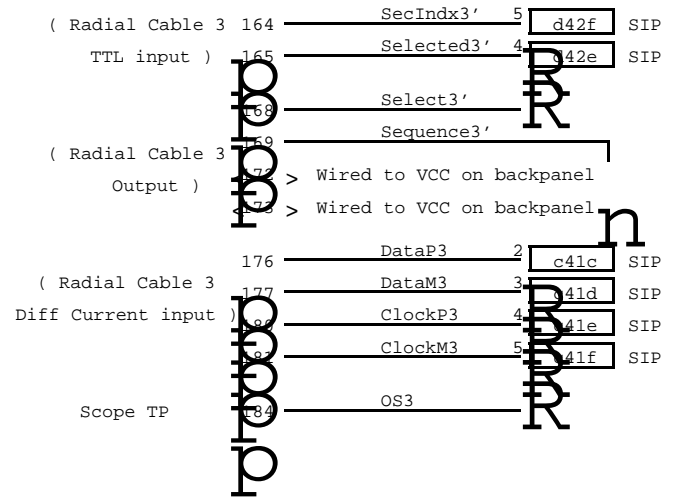
Radial Cable for Drive 2



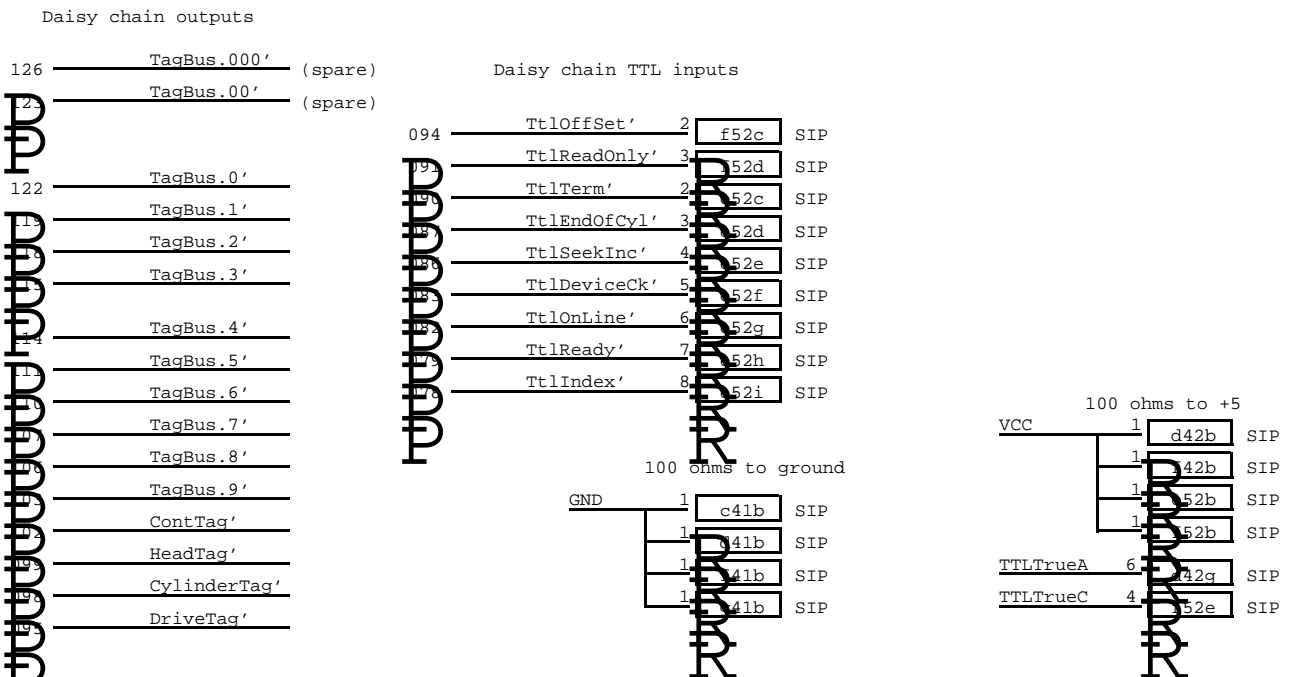
Radial Cable for Drive 1



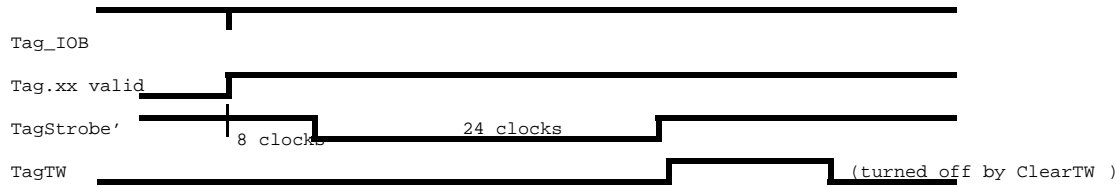
Radial Cable for Drive 3



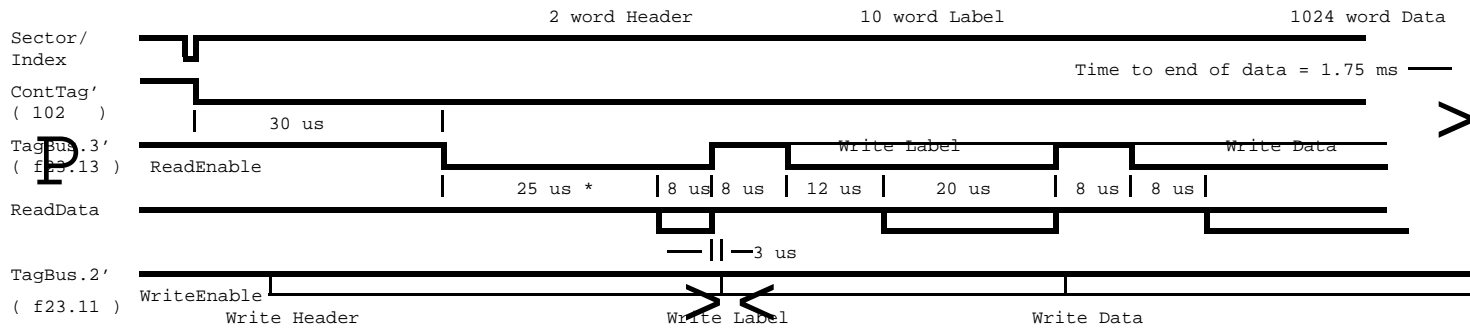
Daisy Chain Cable



Head or Cylinder Tag Instruction



Read or Write Instruction



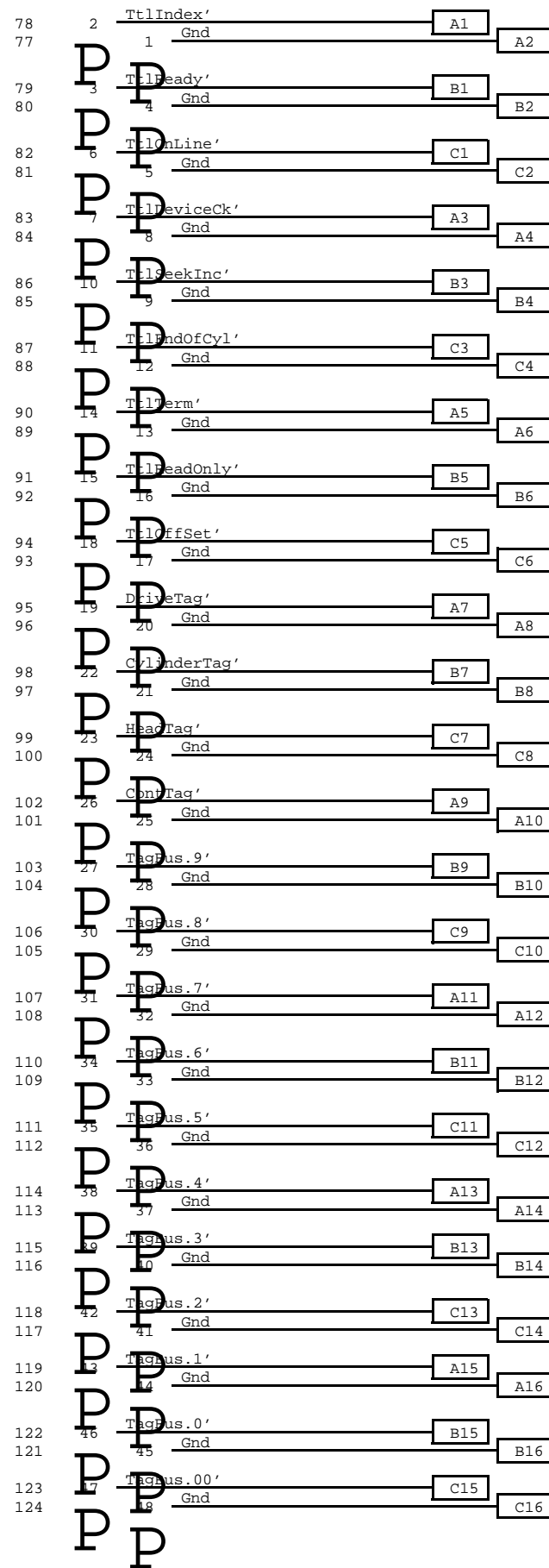
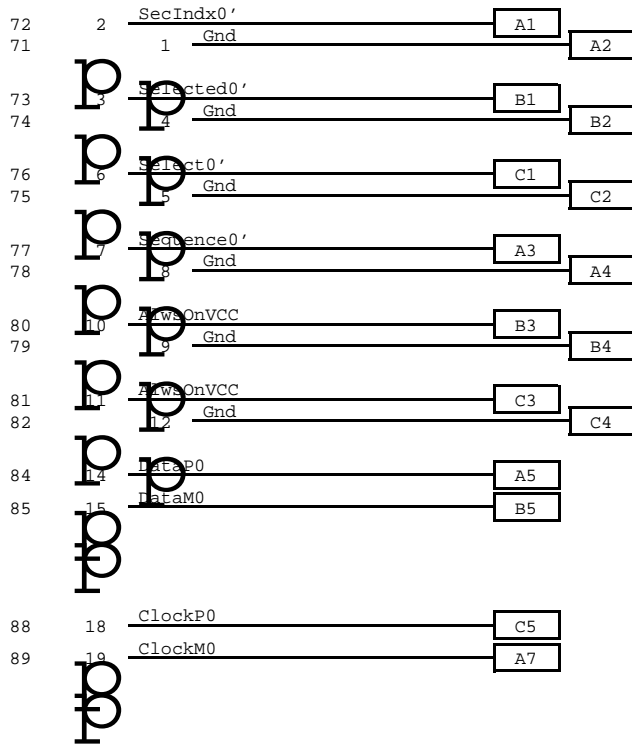
* This value is for reading a pack on the same drive that Headers were written
It may vary by +/- 15 us on other drives

Radial Cable for Drive 0

DAISEY CHAIN CABLE

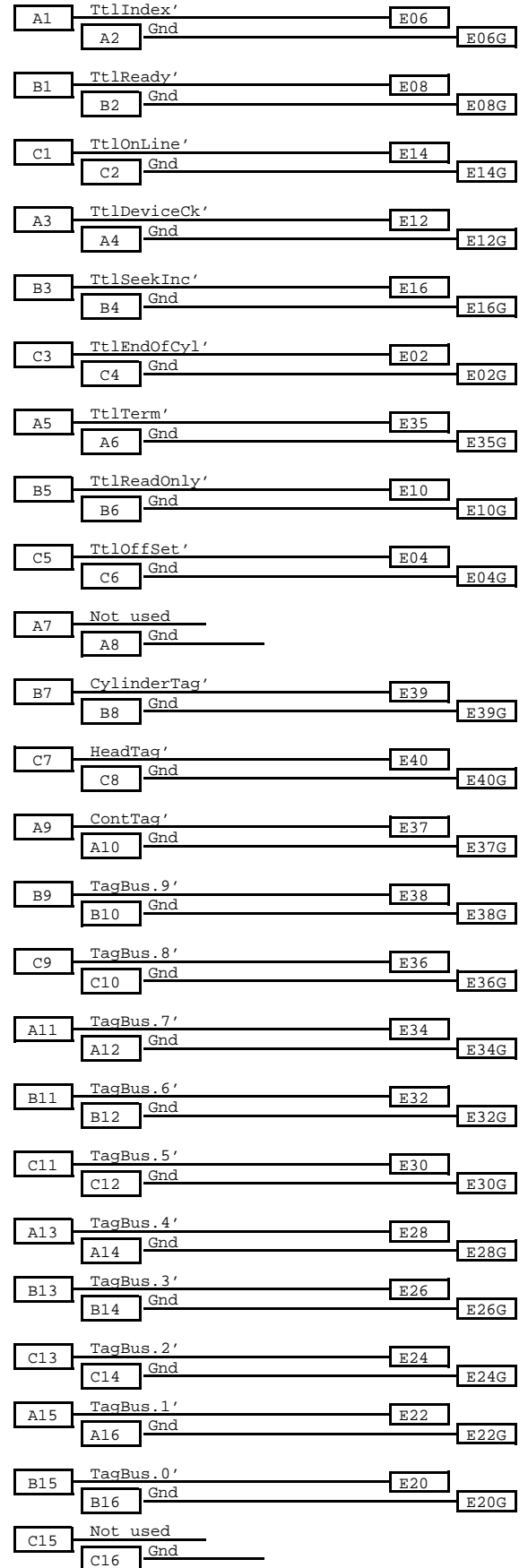
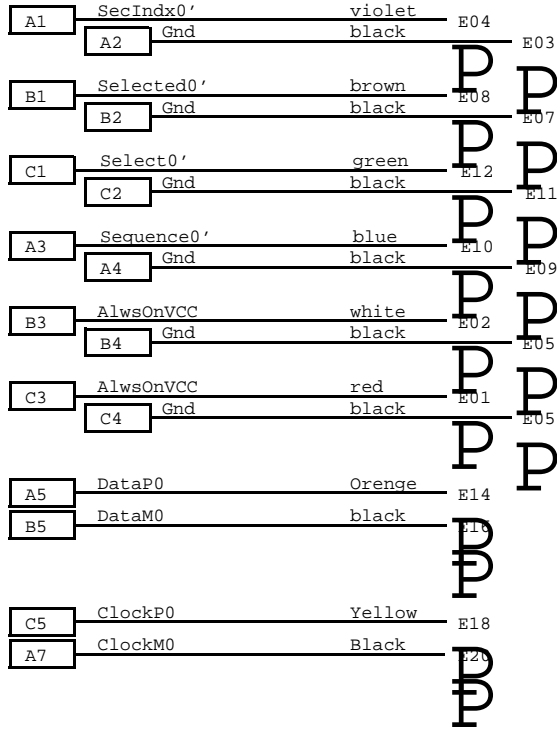
AMP 204733-1

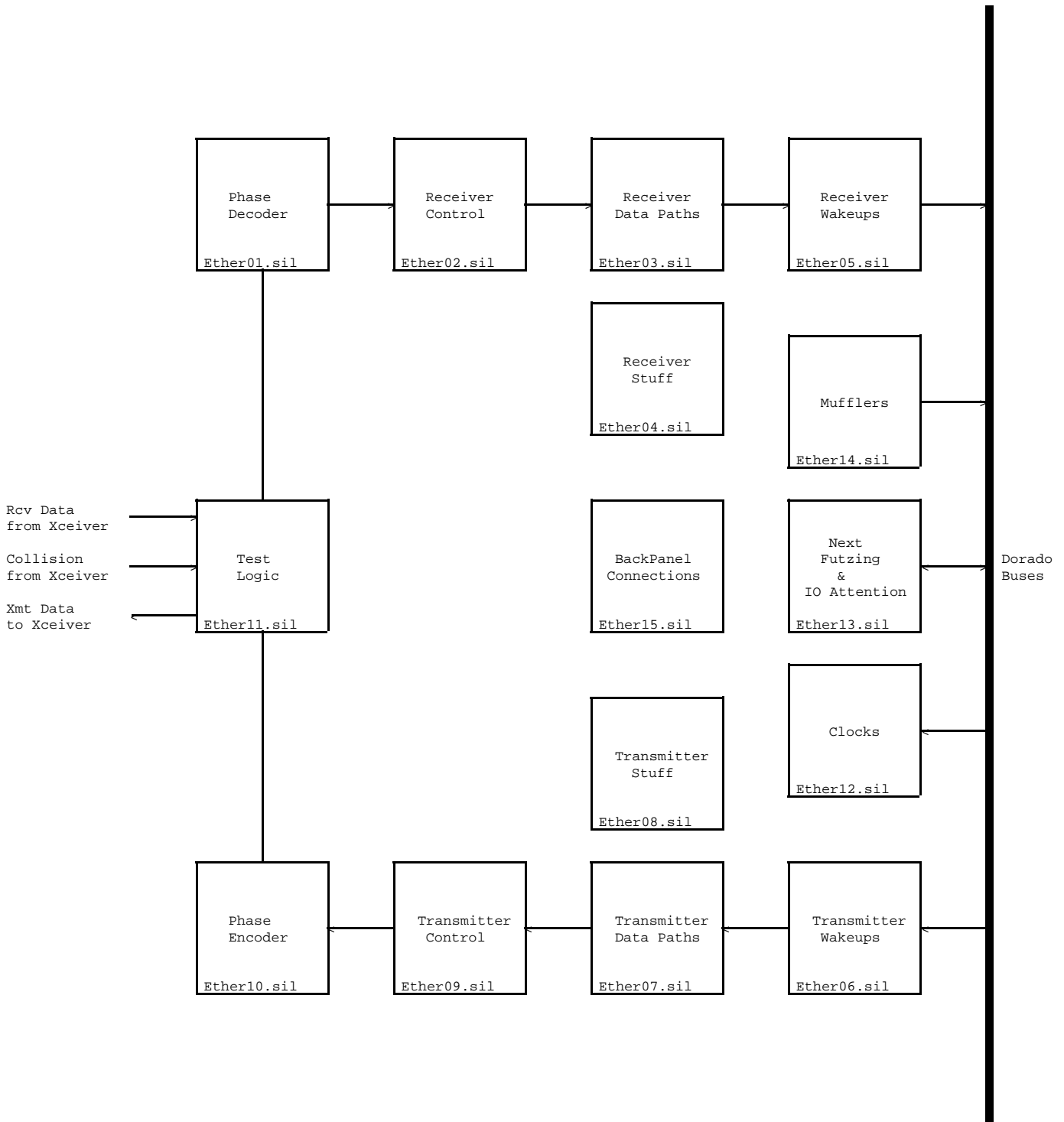
AMP 204729-1



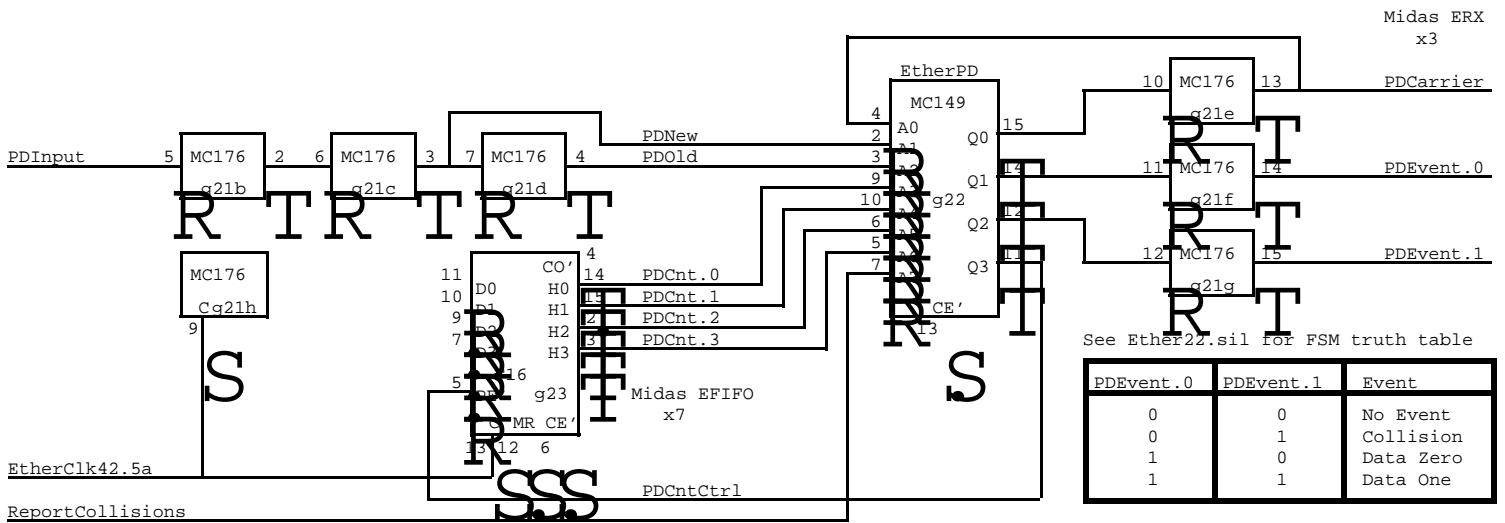
AMP 204742-1

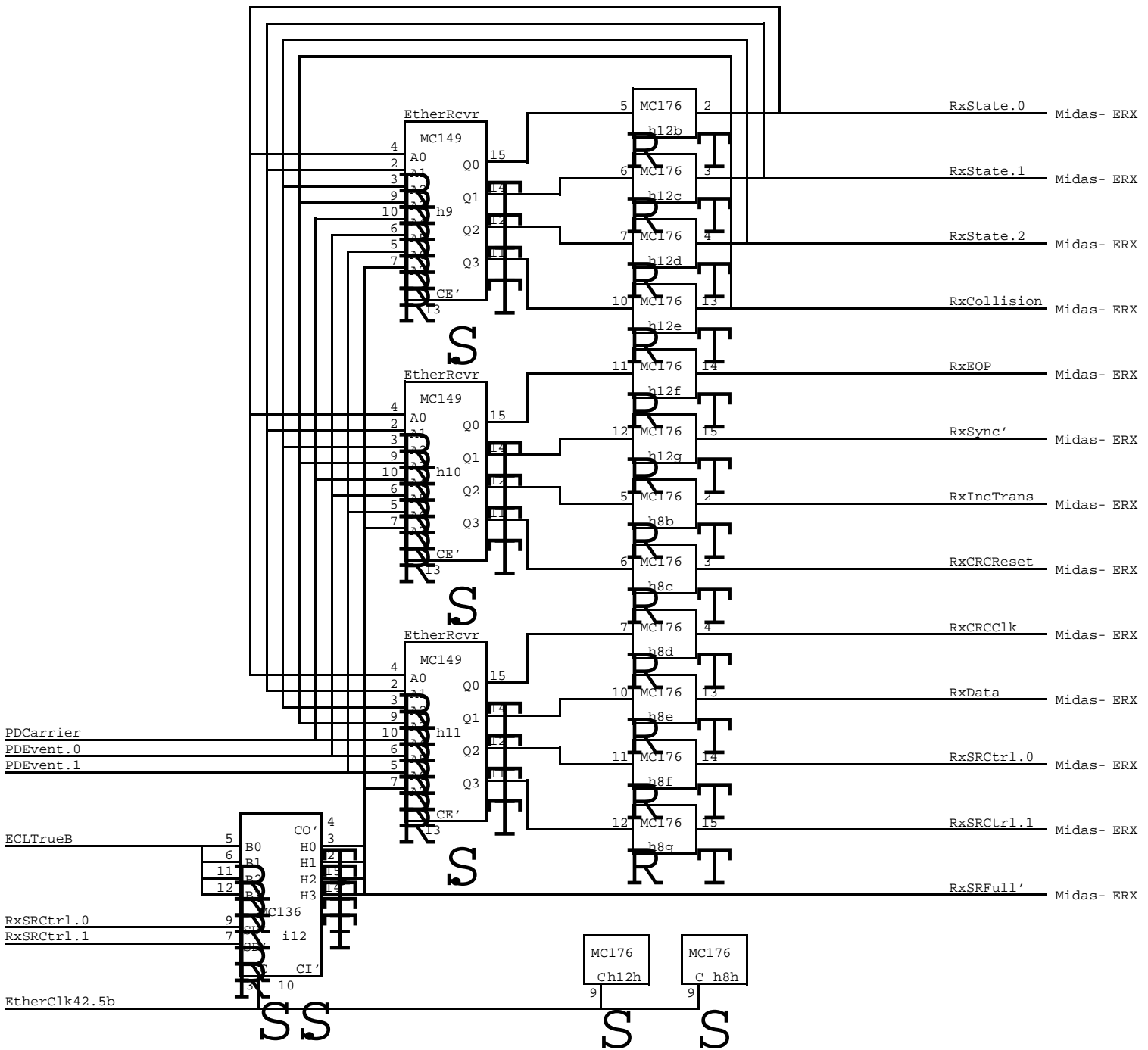
Cal-Comp
Assembly 12433



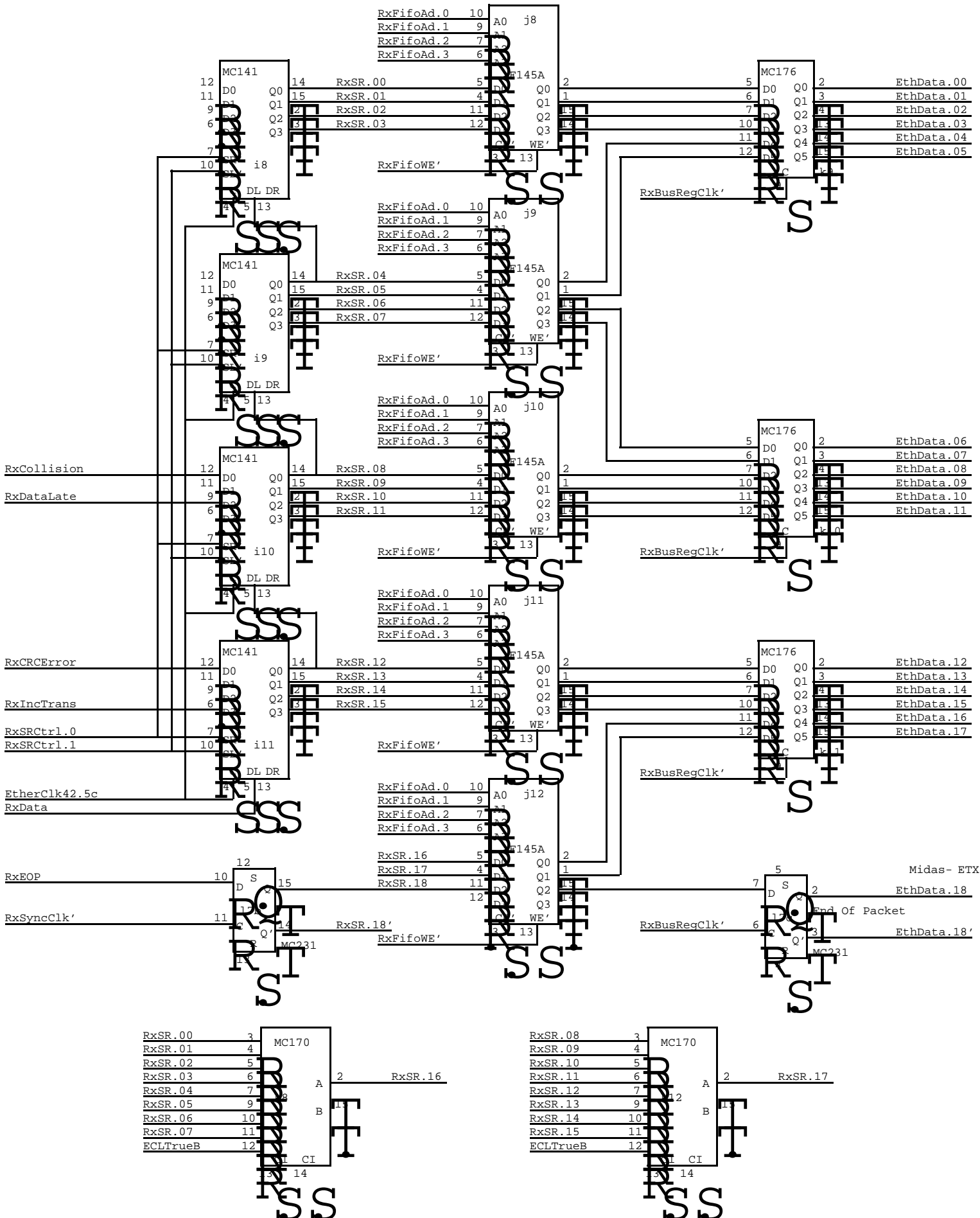


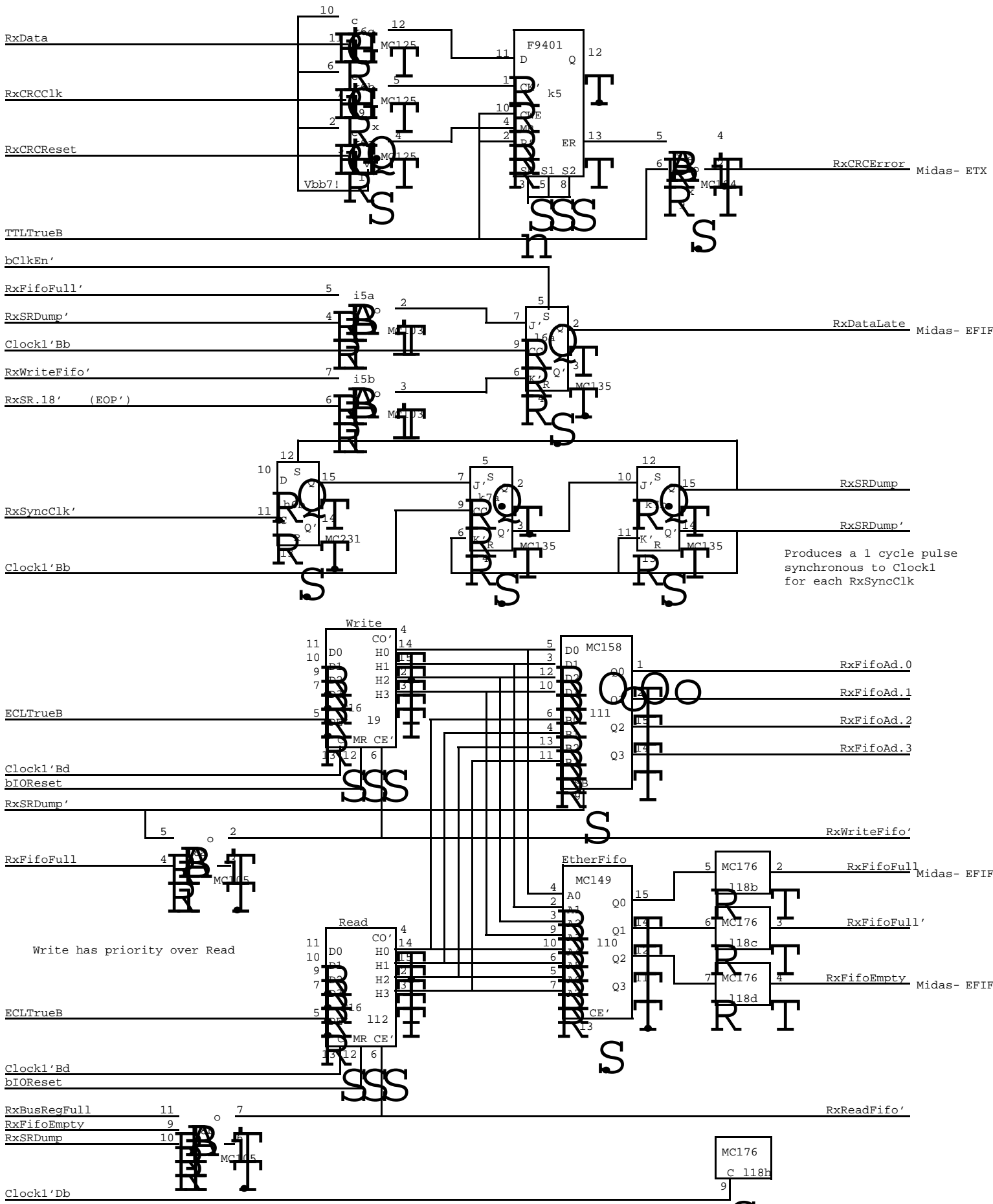
See DskEth*.sil for IOA, IOB, Muffler Control and Board Clocks

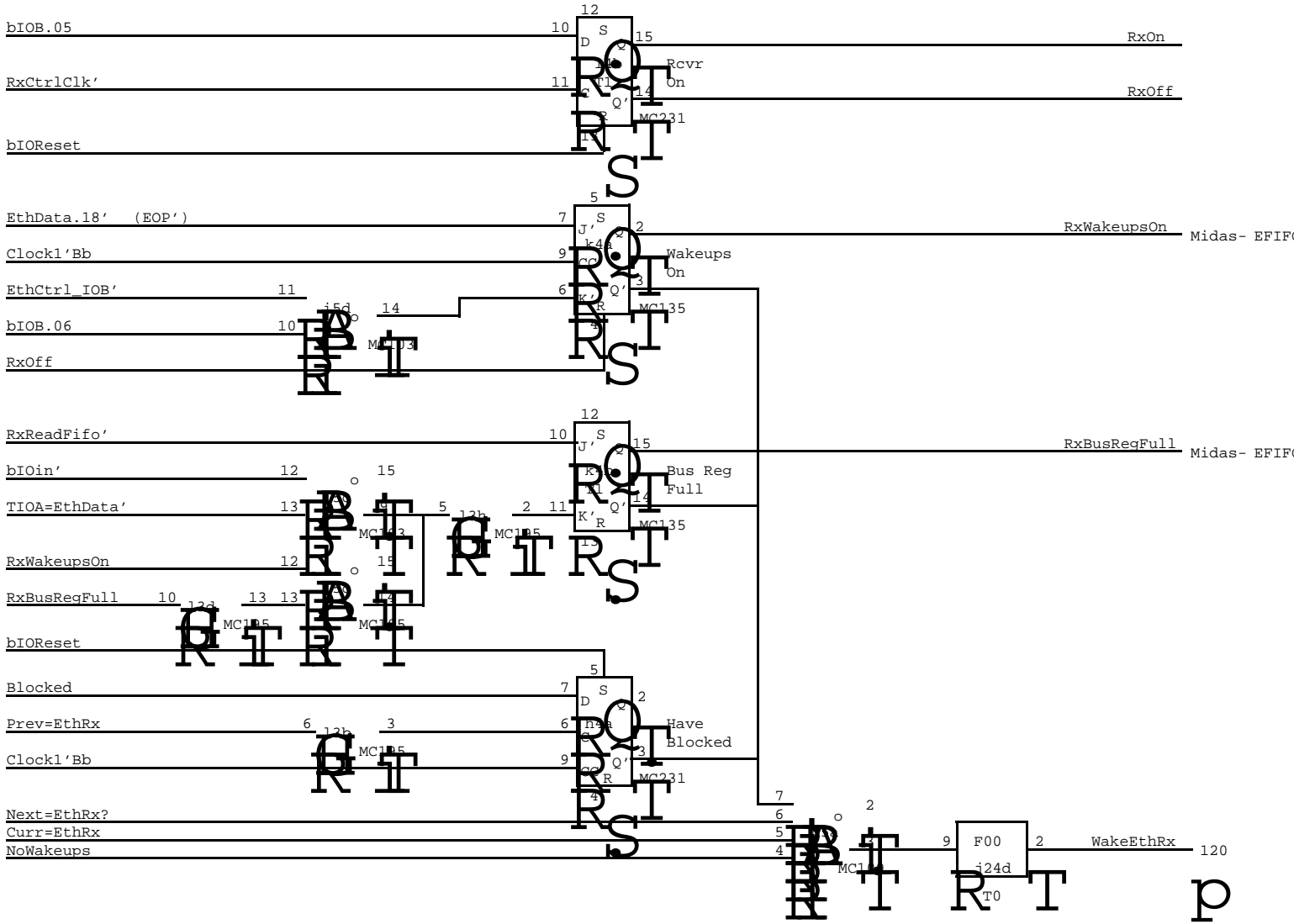




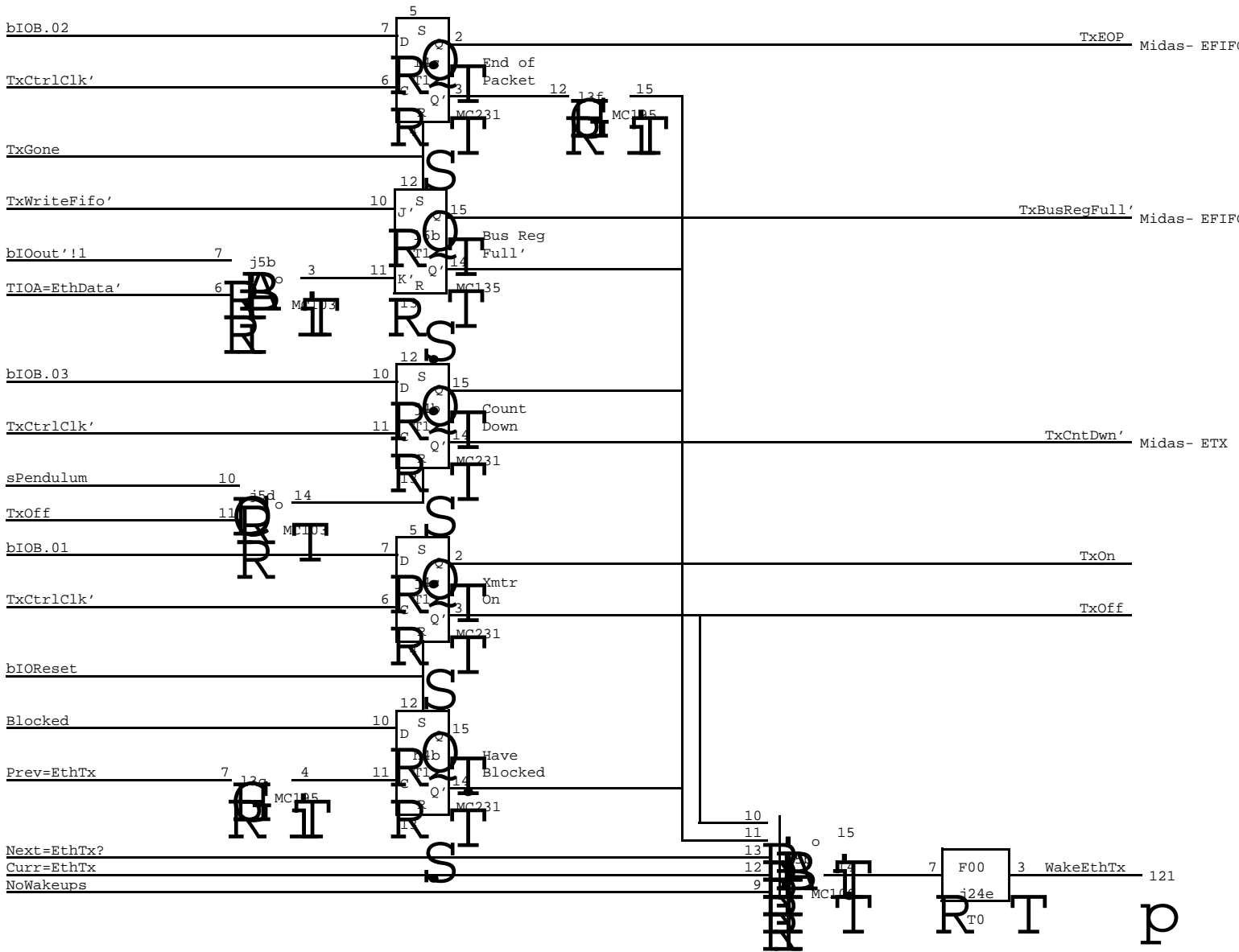
See Ether18.sil for timing diagrams



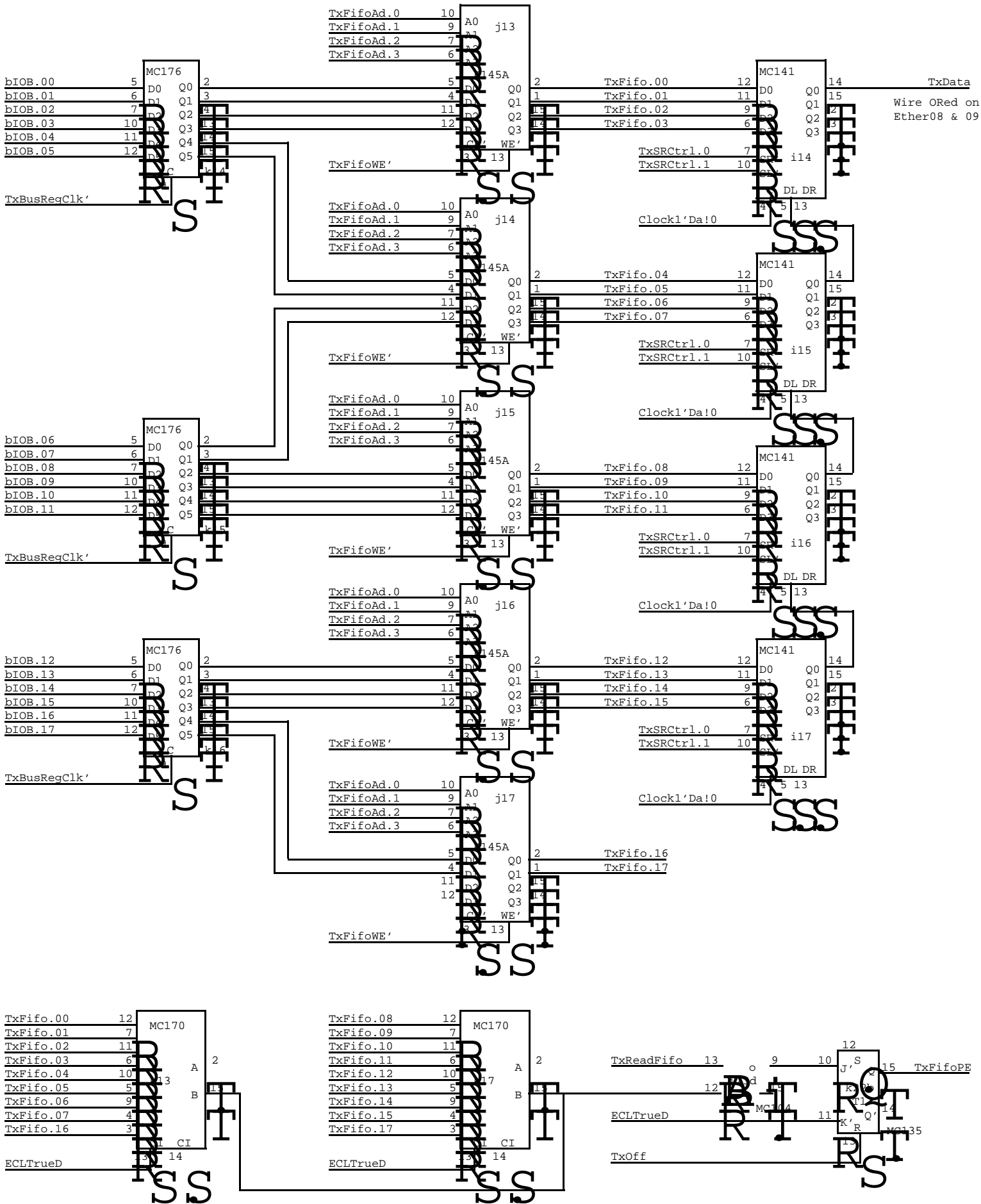


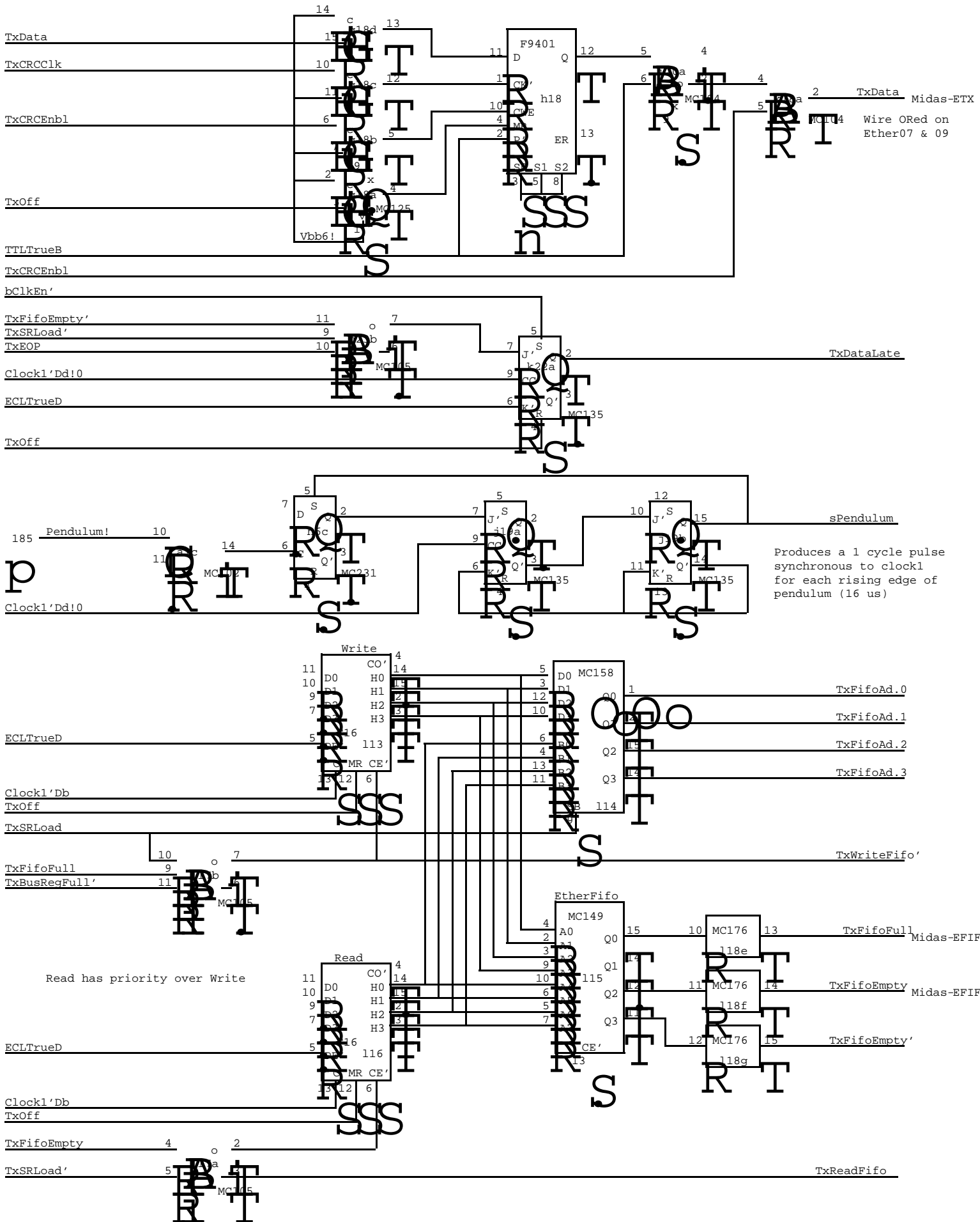


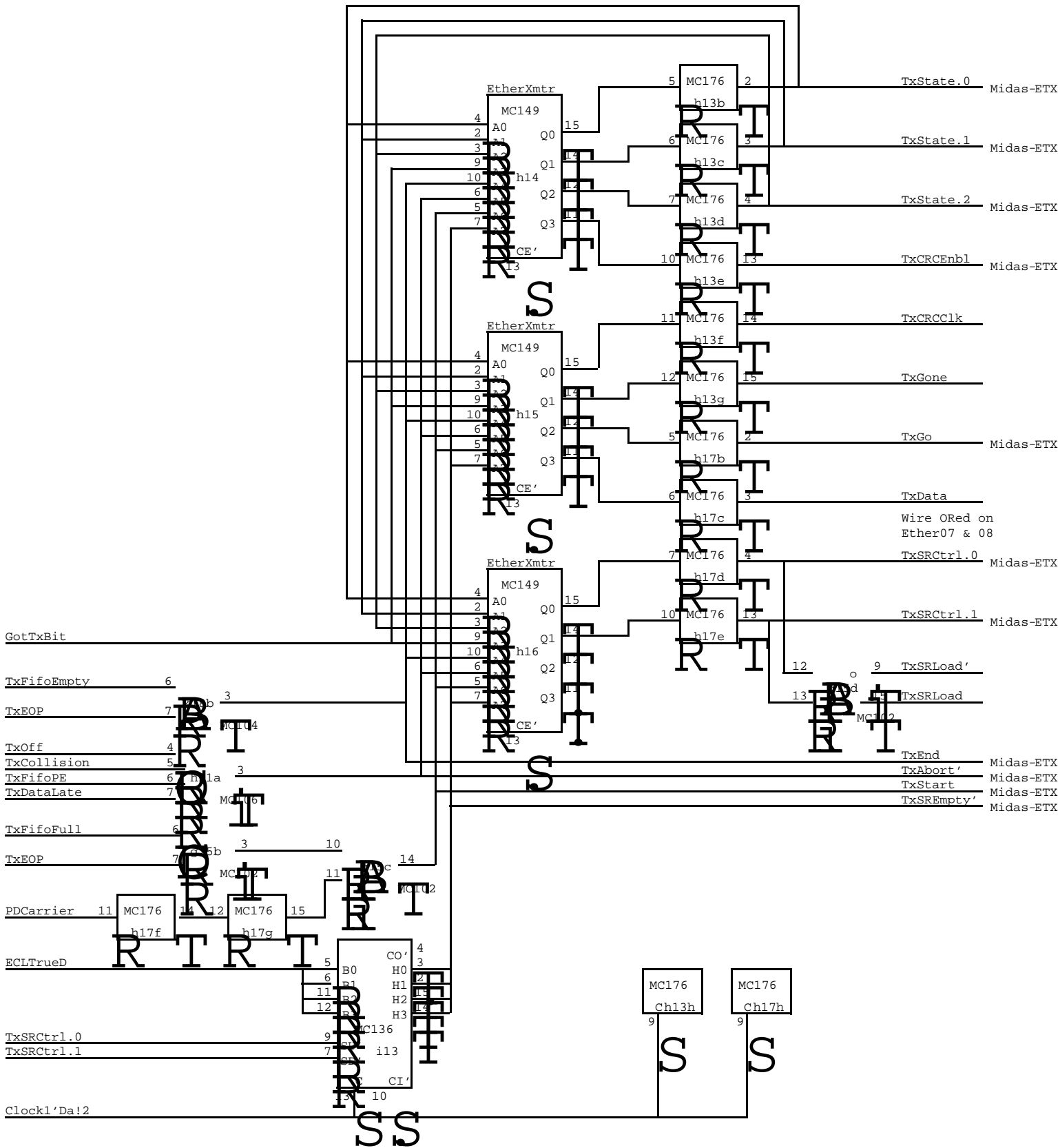
See Ether20.sil for wakeup timing diagram



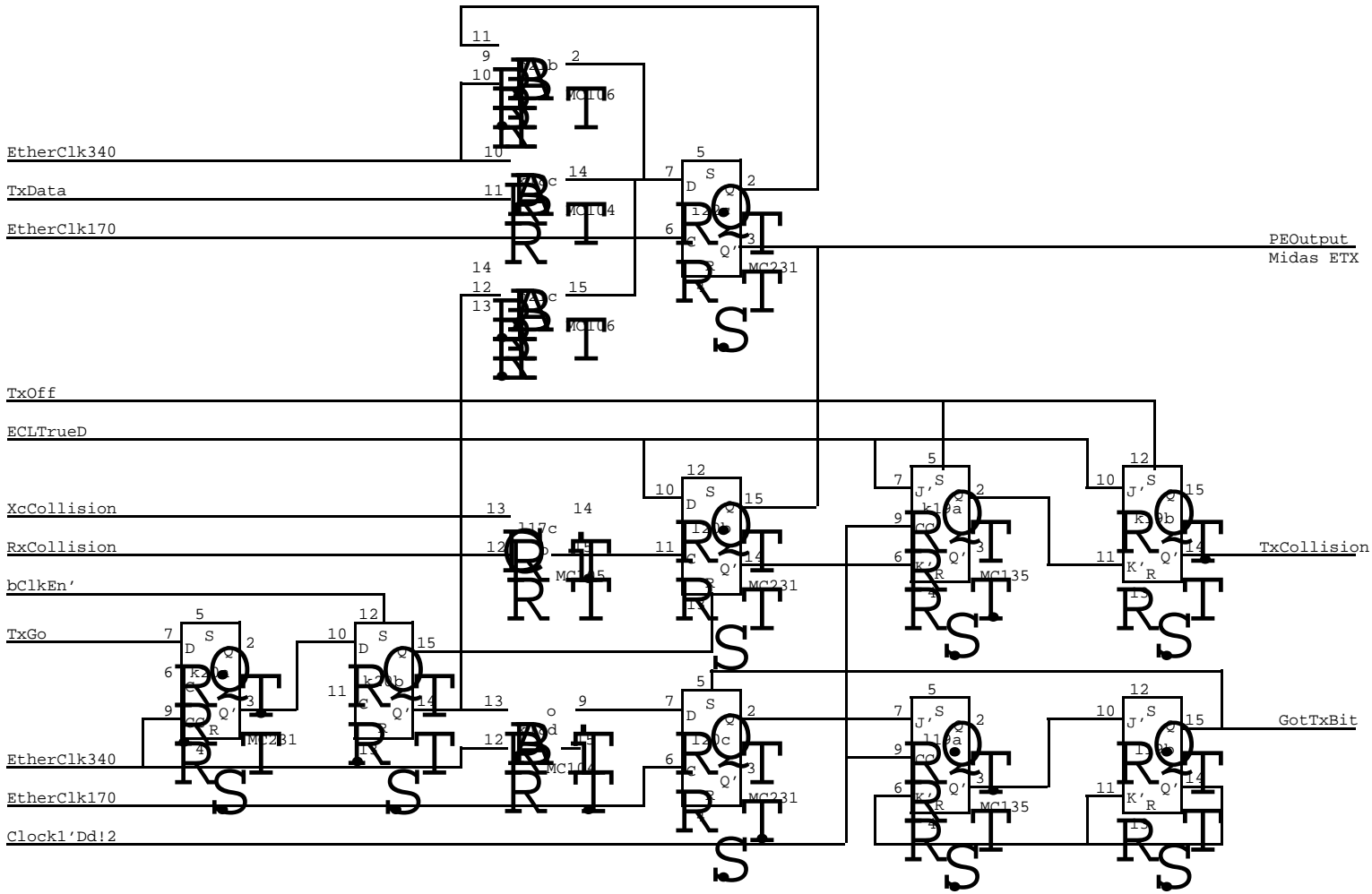
See Ether20.sil for wakeup timing diagram



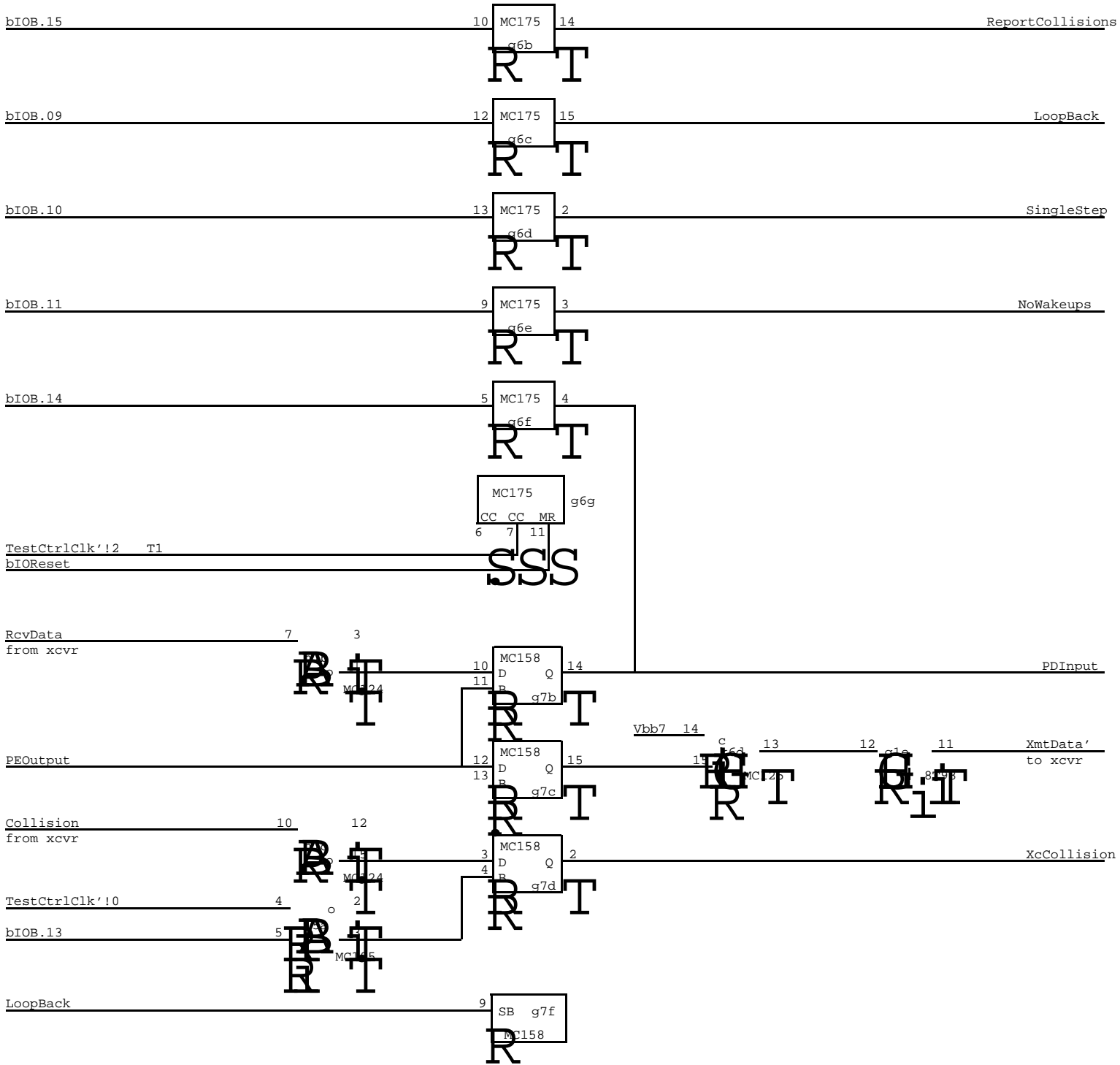


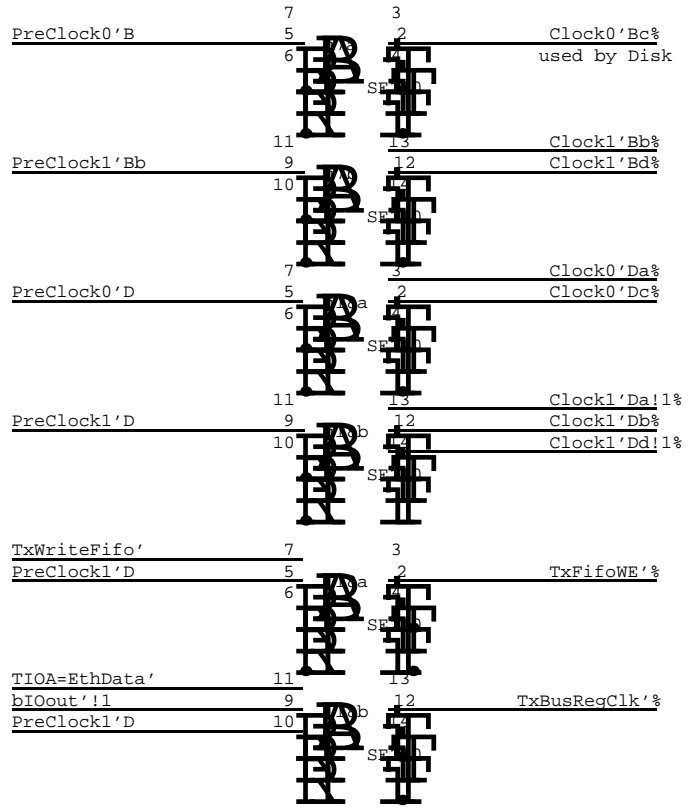
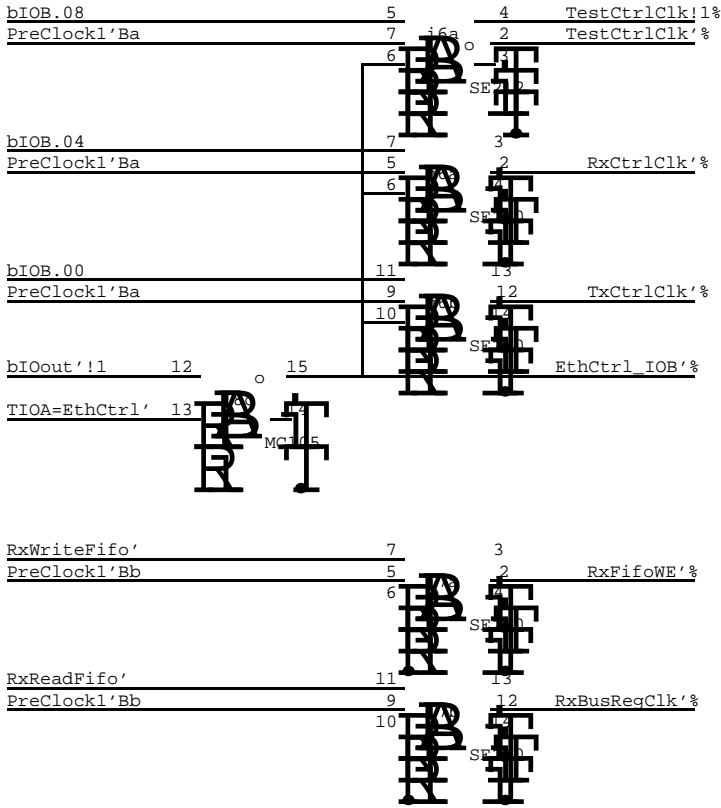


See Ether17.sil for timing diagrams

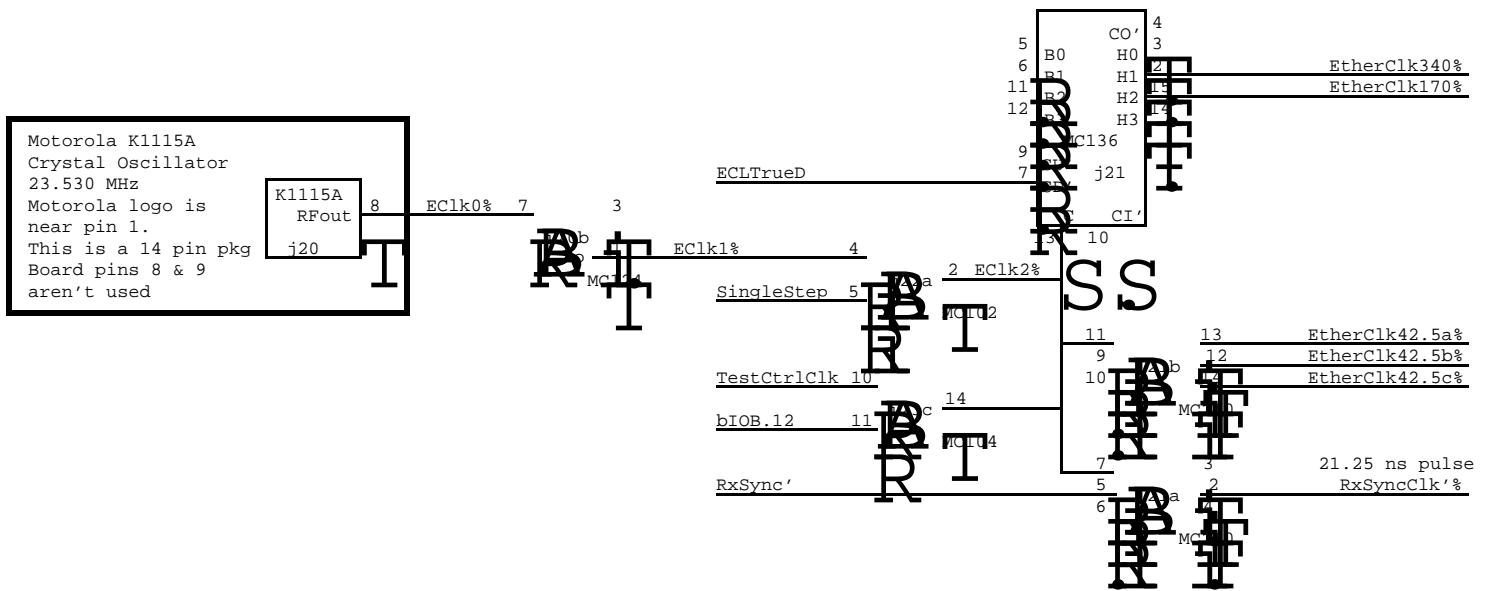


See Ether19.sil for timing diagrams



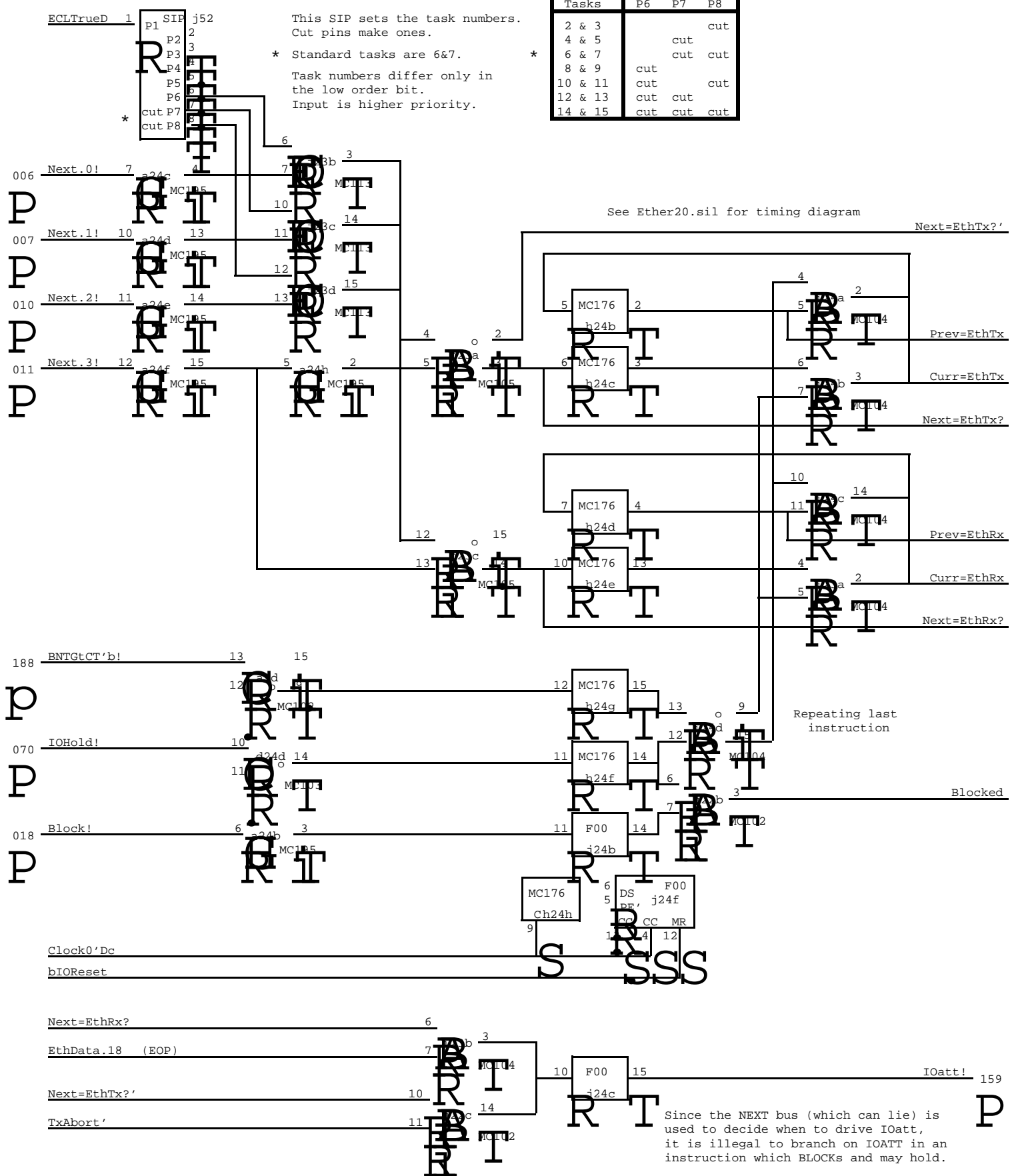


Dorado Synchronous Clocks
Free-running Ether Clocks



Tasks	P6	P7	P8
2 & 3			cut
4 & 5			cut
6 & 7		cut	cut
8 & 9	cut		
10 & 11	cut		cut
12 & 13	cut	cut	
14 & 15	cut	cut	cut

This SIP sets the task numbers.
Cut pins make ones.
* Standard tasks are 6&7.
* Task numbers differ only in the low order bit.
Input is higher priority.

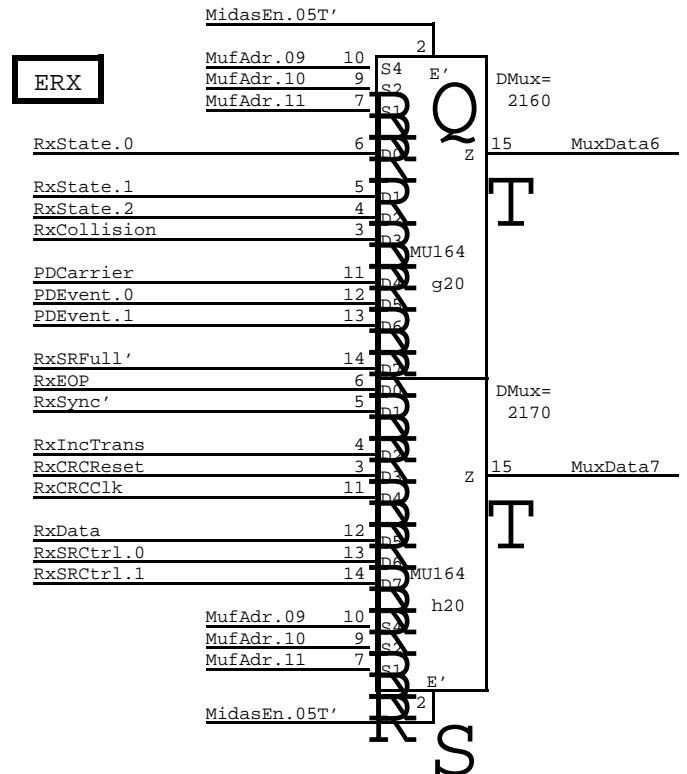
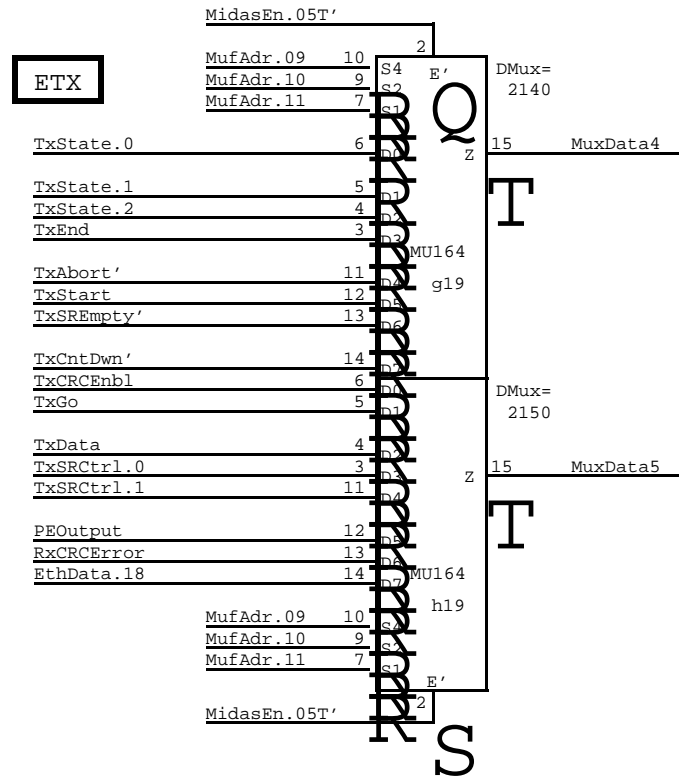
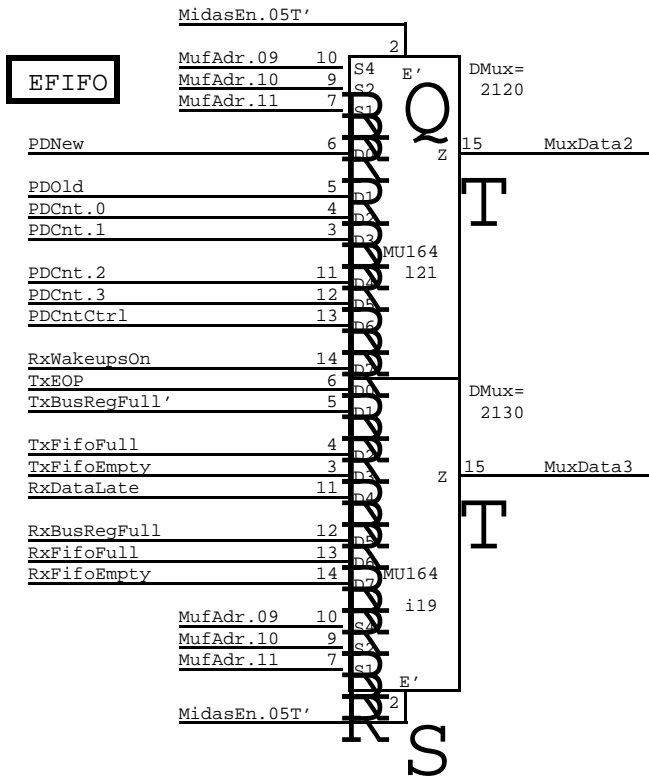


See Ether20.sil for timing diagram

Repeating last instruction

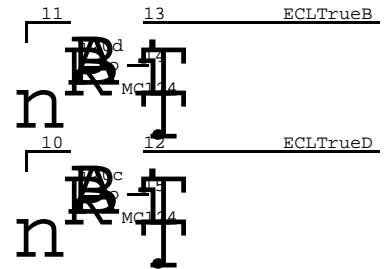
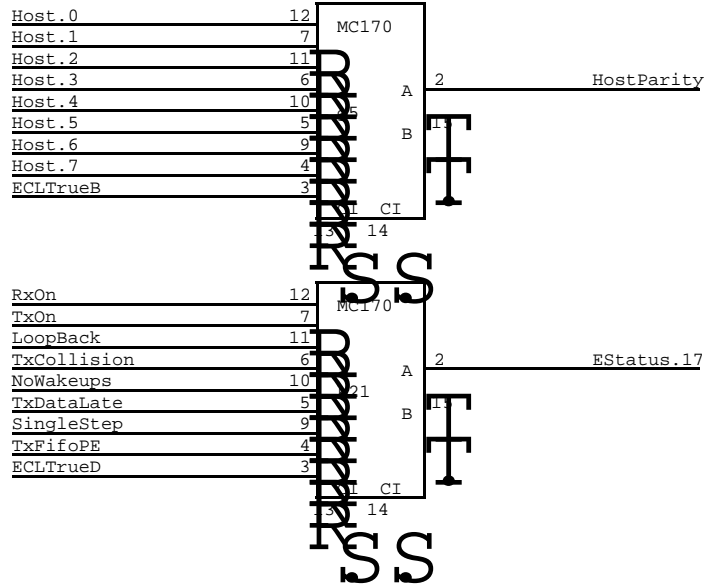
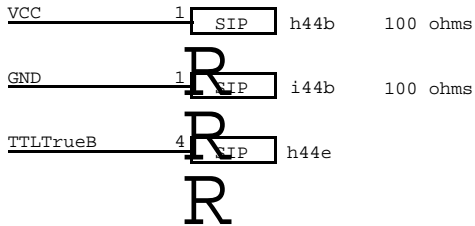
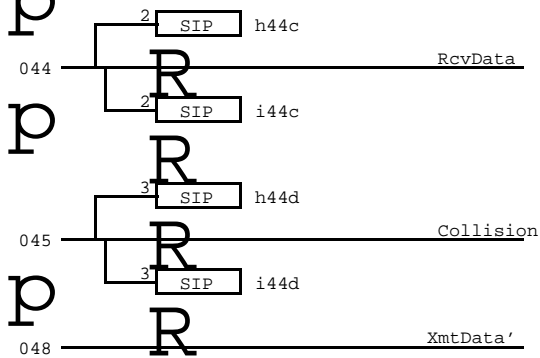
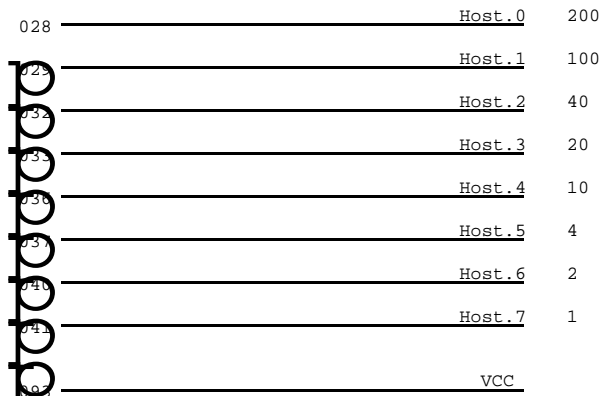
Blocked

Since the NEXT bus (which can lie) is used to decide when to drive IOAtt, it is illegal to branch on IOATT in an instruction which BLOCKs and may hold.



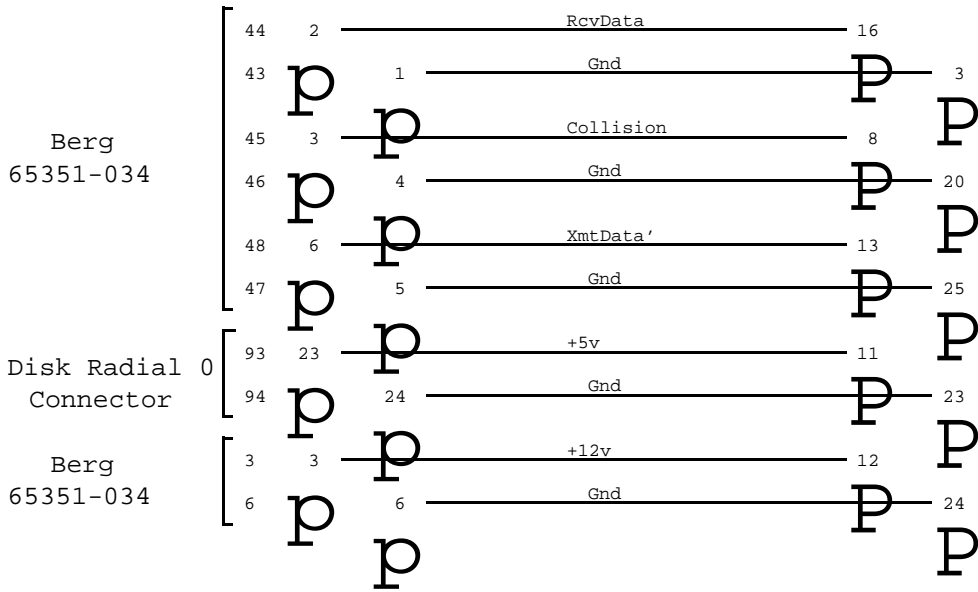
See DskEth01.sil for muffler control logic

To set a host address bit to 1
pull it up to gnd through 91 ohms.



BP

Cannon DAC-25S

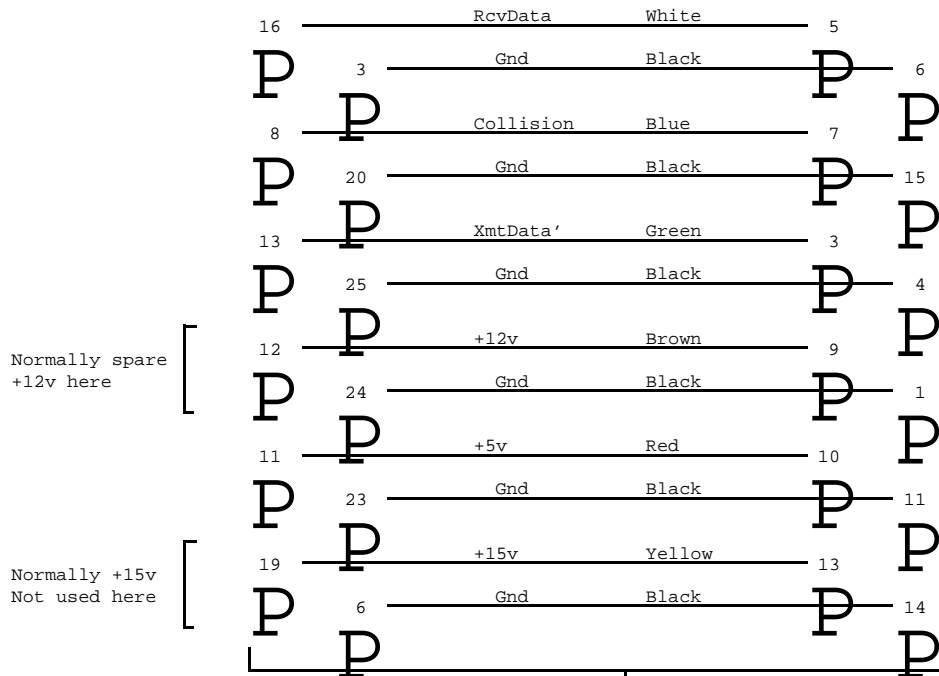


Internal Cable

External Cable

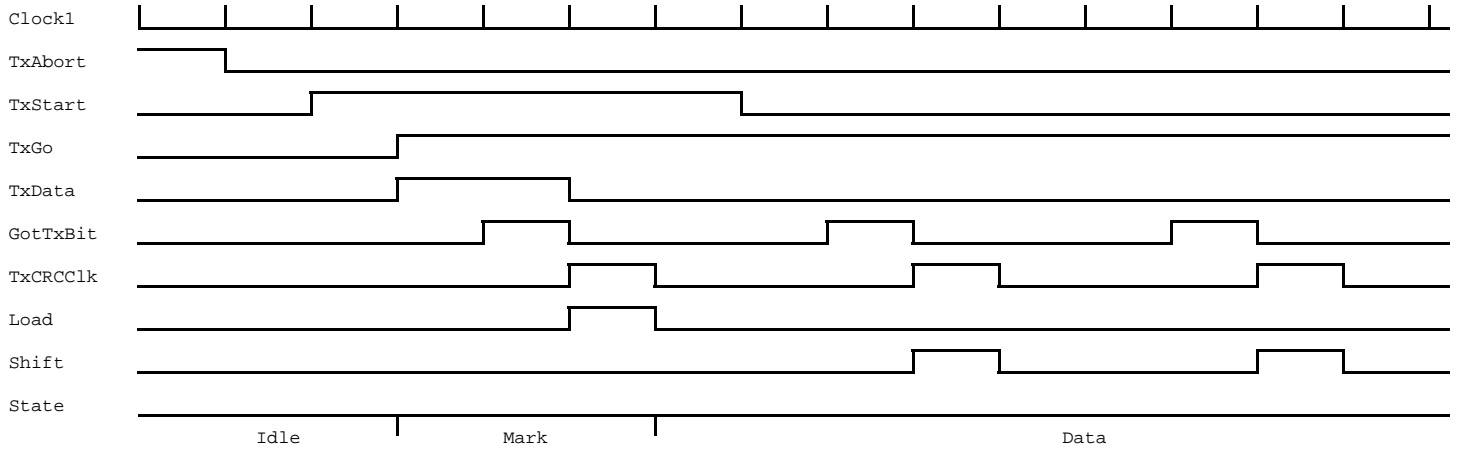
Cannon DAC-25P

Cannon DAC-15S

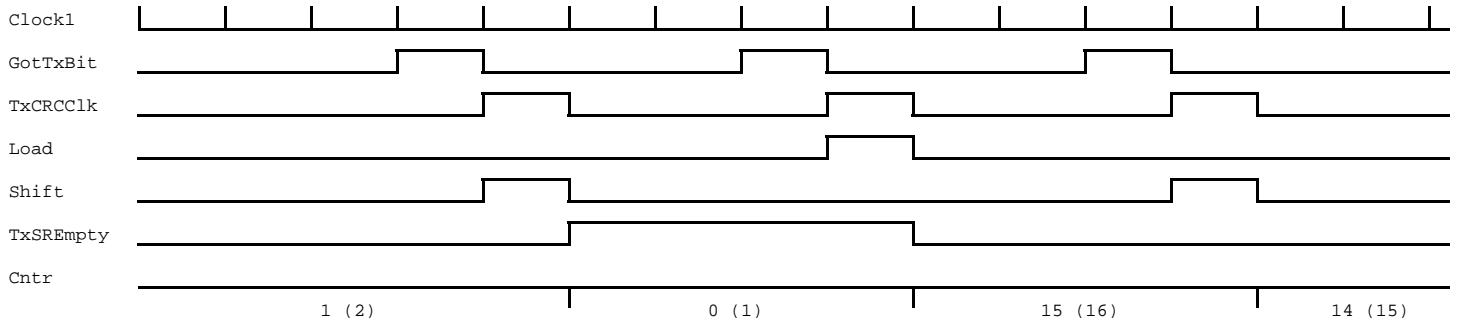


40' Typ

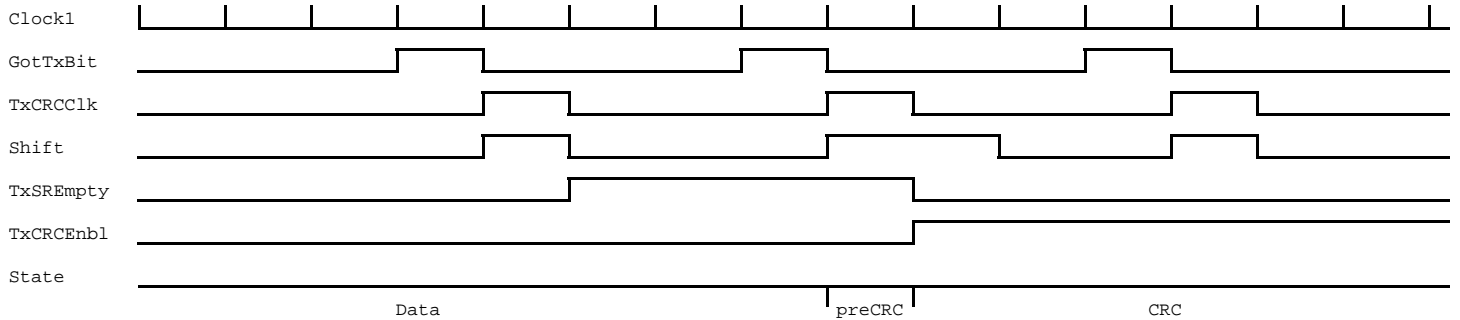
This is a standard Alto II Ethernet external cable part # 216411



Startup

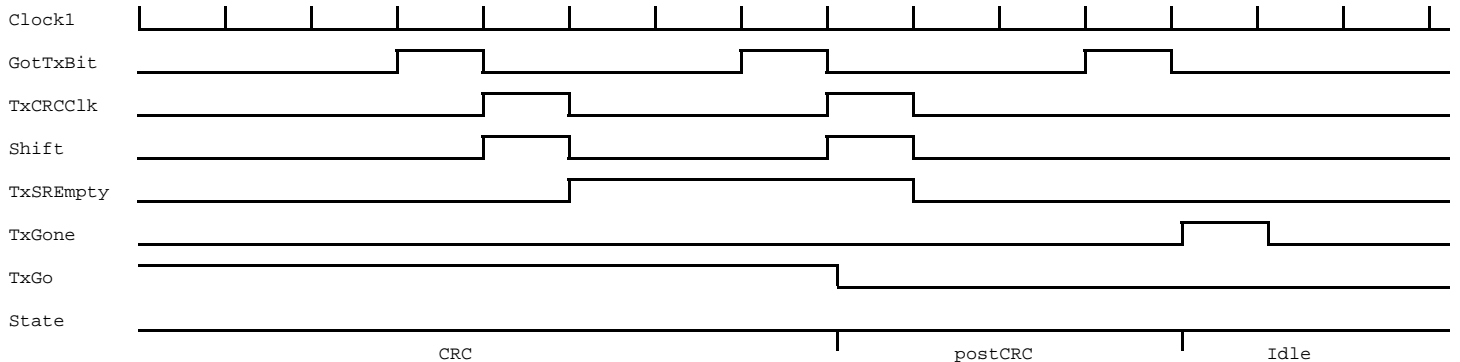


Loading Tx Shift Register

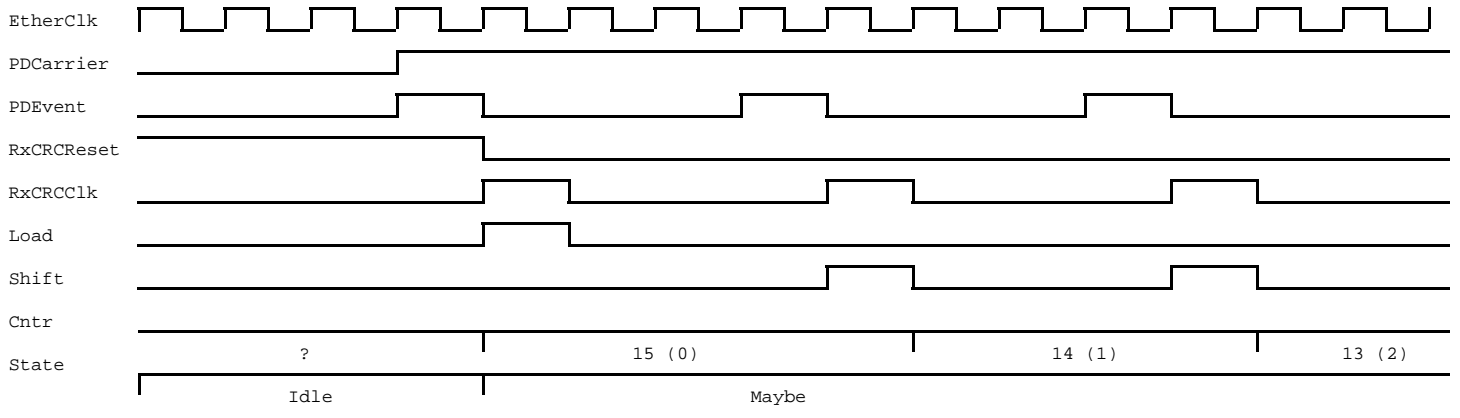


TxEnd has been high since TxSR was last loaded

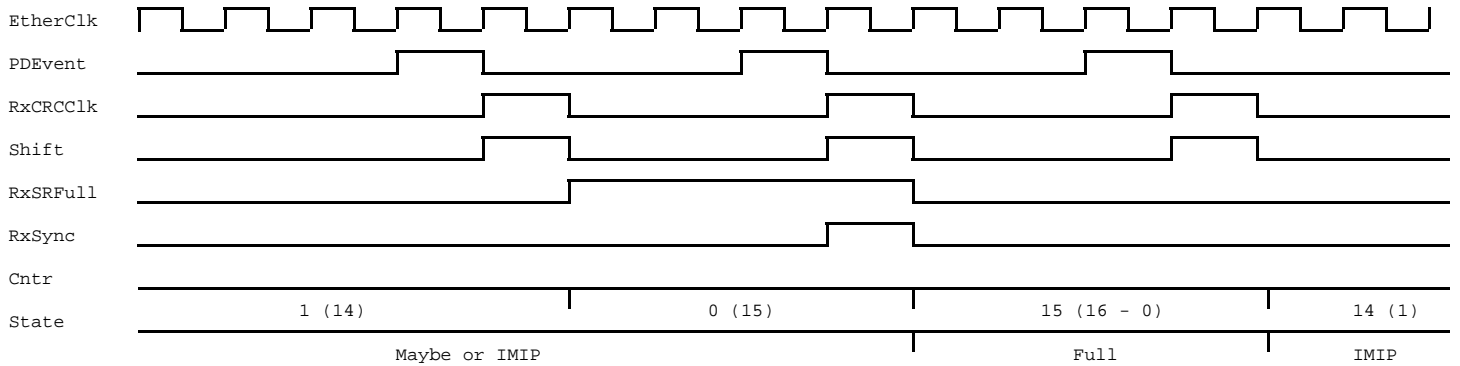
CRC



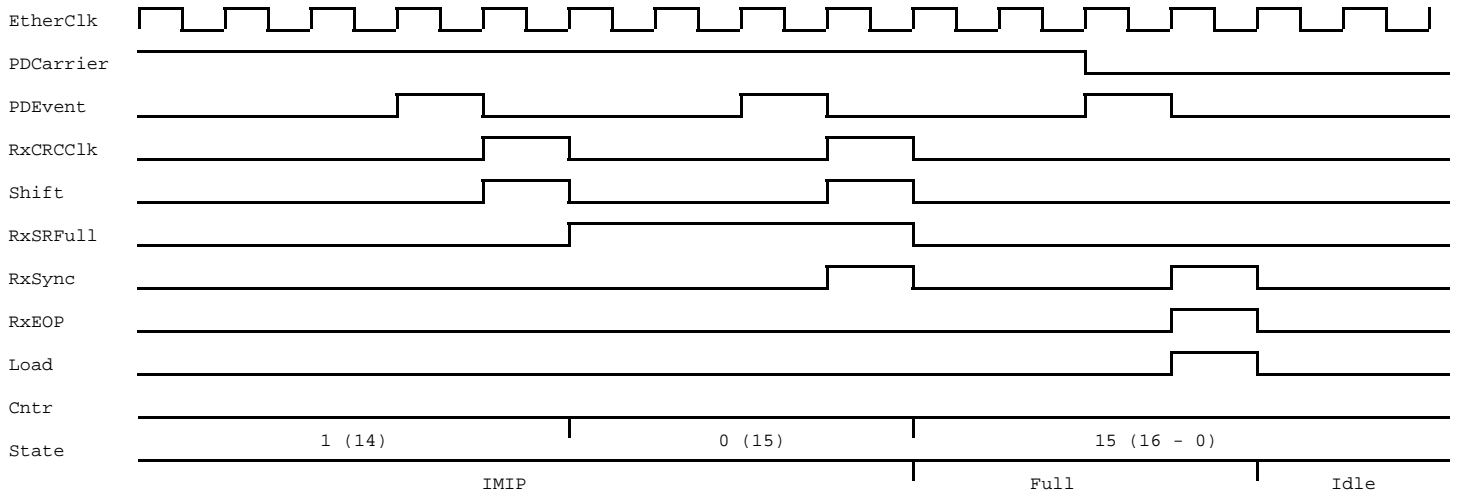
ShutDown



Startup

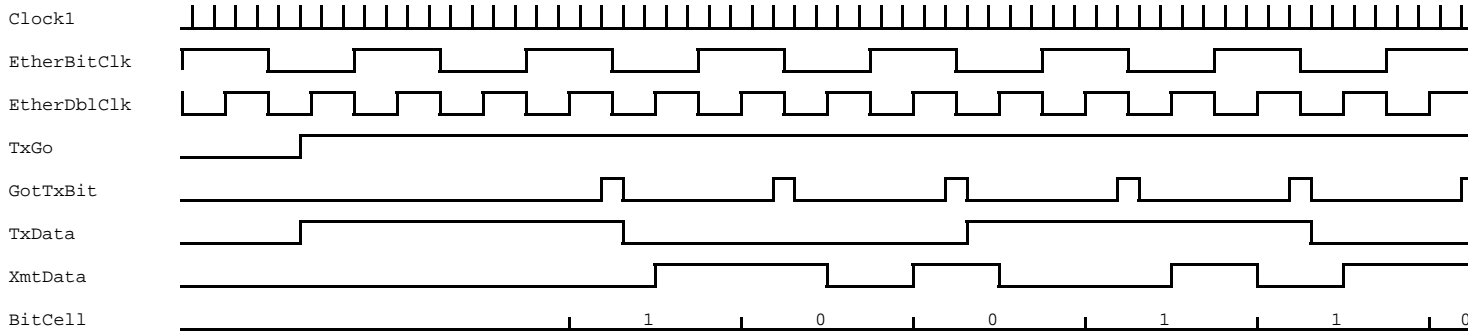


Dumping Rx Shift Register

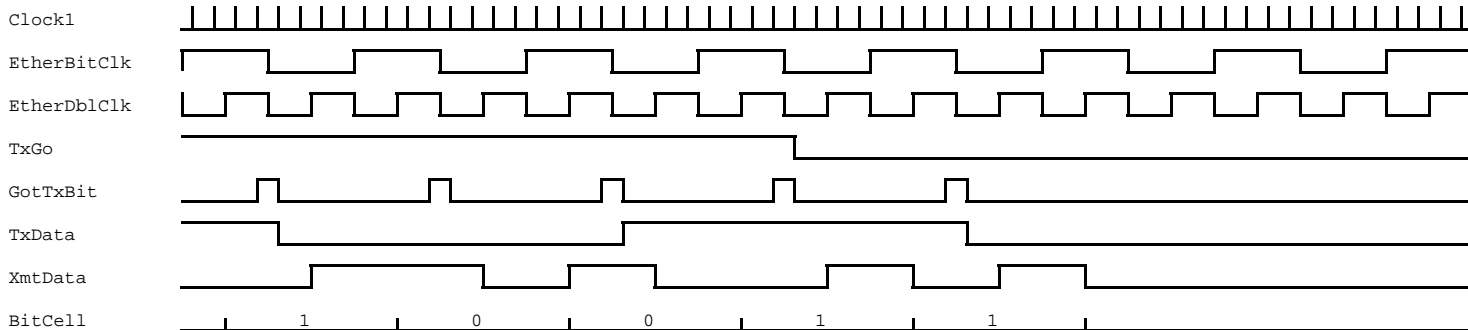


ShutDown

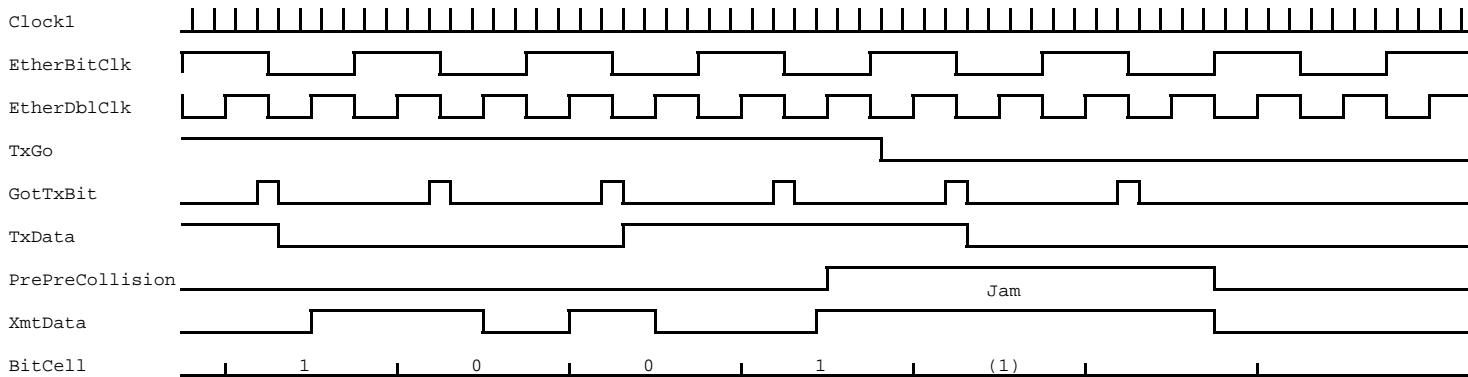
Cntr notation is <cntr value>(<# occupied postions>)
 Phase decoder events are encoded in PDEvent.x
 Shift and Load are encoded in RxSRCtrl.x
 state is encoded in RxState.x
 shift also decrements Cntr



Startup

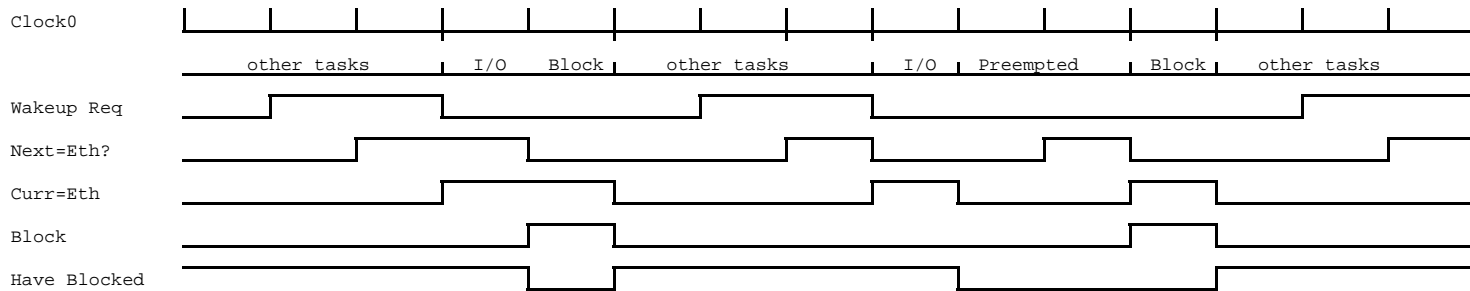


Shutdown



PrePreCollision is the output of the first stage of the Collision synchronizer

Collision



I/O means TIOA=EthData and FF=Input or Output

Wakeup Timing

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Tx Cmd Enbl'	Tx On	Tx EOP	Tx Cnt Dwn	Rx Cmd Enbl'	Rx On	Rx BOP'		Test Cmd Enbl'	Loop Back	Single Step	No Wake ups	Test Clock	Test Coll'	Test Data	Report Colls

Output

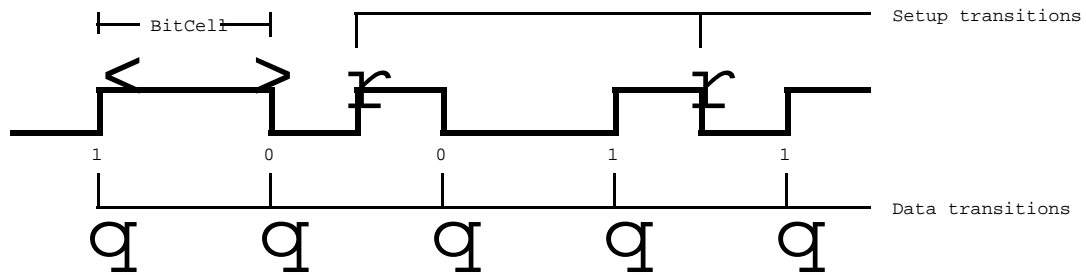
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Host Address								Rx On	Tx On	Loop Back	Tx Coll	No Wake ups	Tx Data Late	Single Step	Tx Fifo PE

028 029 032 033 036 037 040 041

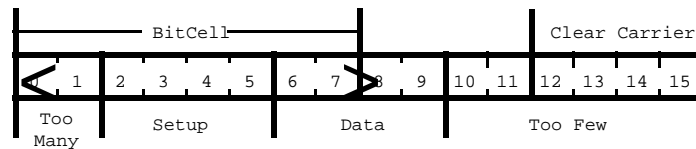
p p p p p p p p Input

The host address is set by jumpers on the right backplane.

To set a bit to one, pull it up to ground through 91 ohms.



A bitcell is nominally 340 ns.
A sample is nominally 42.5 ns.



Inputs				Outputs			Comment
Carrier	Old	New	Cnt	Carrier	Event	CntCtrl	
Low	Low	Low	d/c	Low	Nothing	Count	Idle
Low	Low	High	d/c	High	One	Reset	Start of packet (start bit)
Low	High	Low	d/c	High	Collisior	Reset	Impossible
Low	High	High	d/c	Low	Nothing	Count	Impossible
High	low	High	0-1	High	Collisior	Count	Too many transitions
High	High	low	0-1	High	Collisior	Count	Too many transitions
High	low	High	2-5	High	Nothing	Count	Setup transition (zero next)
High	High	low	2-5	High	Nothing	Count	Setup transition (one next)
High	low	High	6-9	High	One	Reset	Data transition
High	High	low	6-9	High	Zero	Reset	Data transition
High	low	High	10-15	High	Collisior	Reset	Too few transitions
High	High	low	10-15	High	Collisior	Reset	Too few transitions
High	Low	Low	0-11	High	Nothing	Count	Active
High	High	High	0-11	High	Nothing	Count	Active
High	Low	Low	12-15	Low	Collisior	Reset	End of packet
High	High	High	12-15	High	Collisior	Reset	Jam

"Impossible" conditions can happen right after power up.
d/c means "don't care".