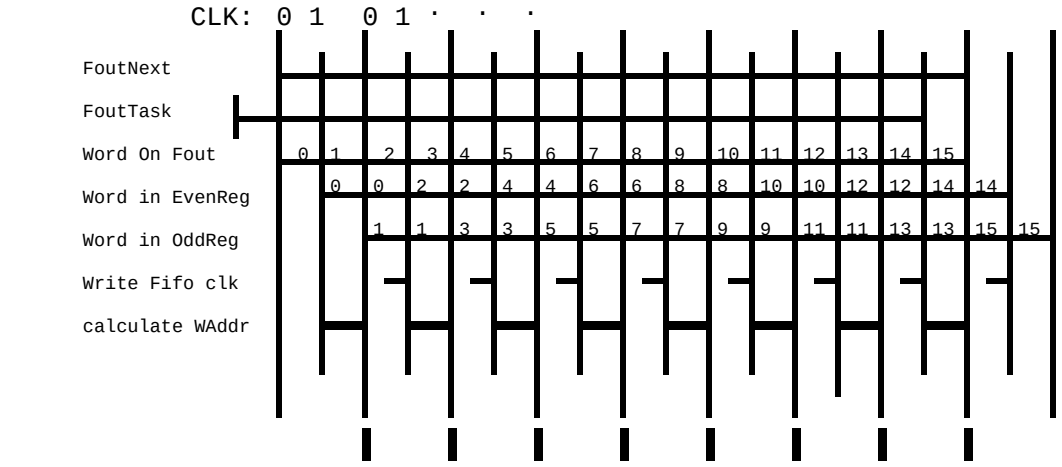
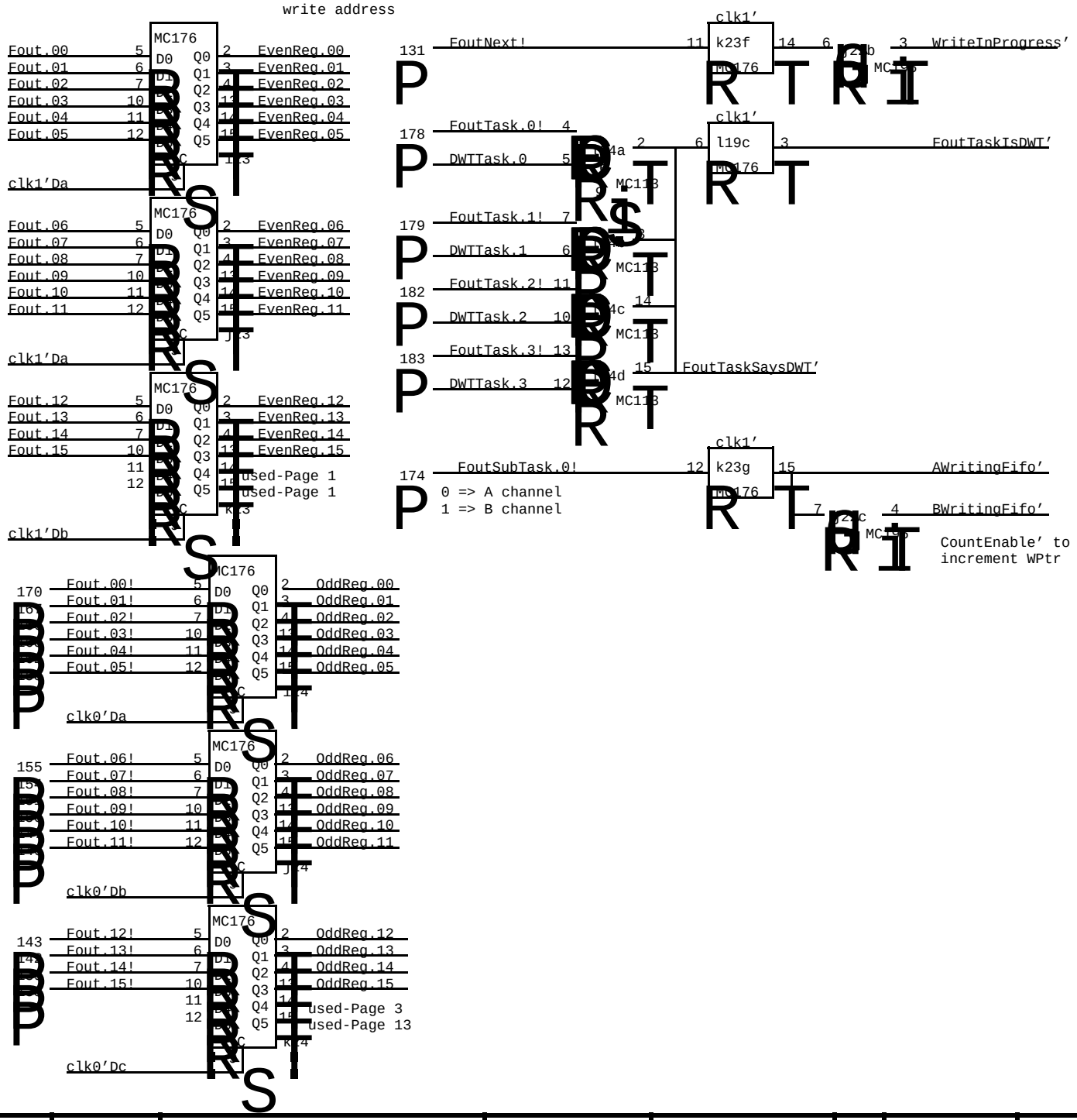
D O R A D O S C H E M A T I C S

D i s p l a y Y

Table of contents





XEROX PARC	Project		File	Designer	Rev	Date	Page
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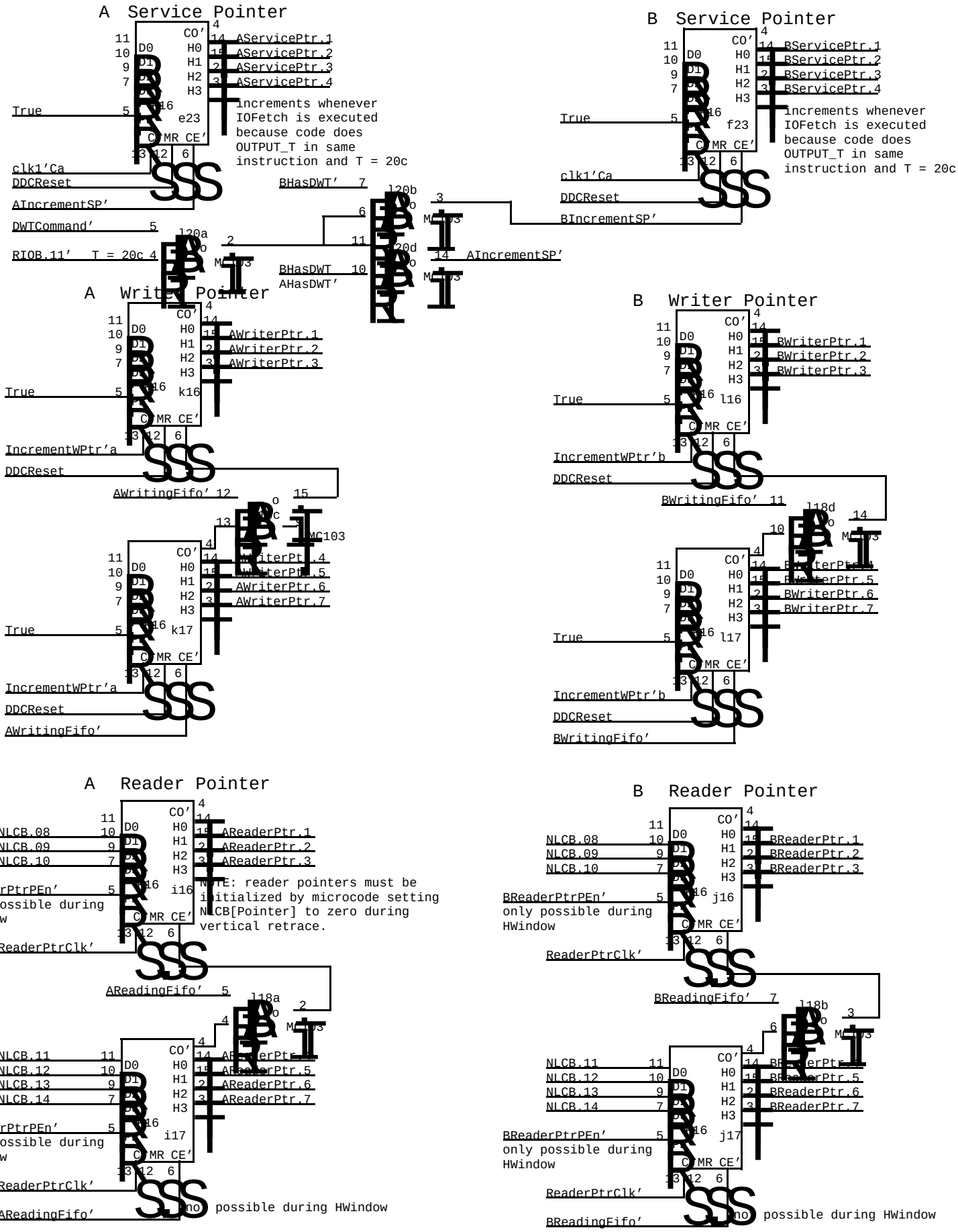

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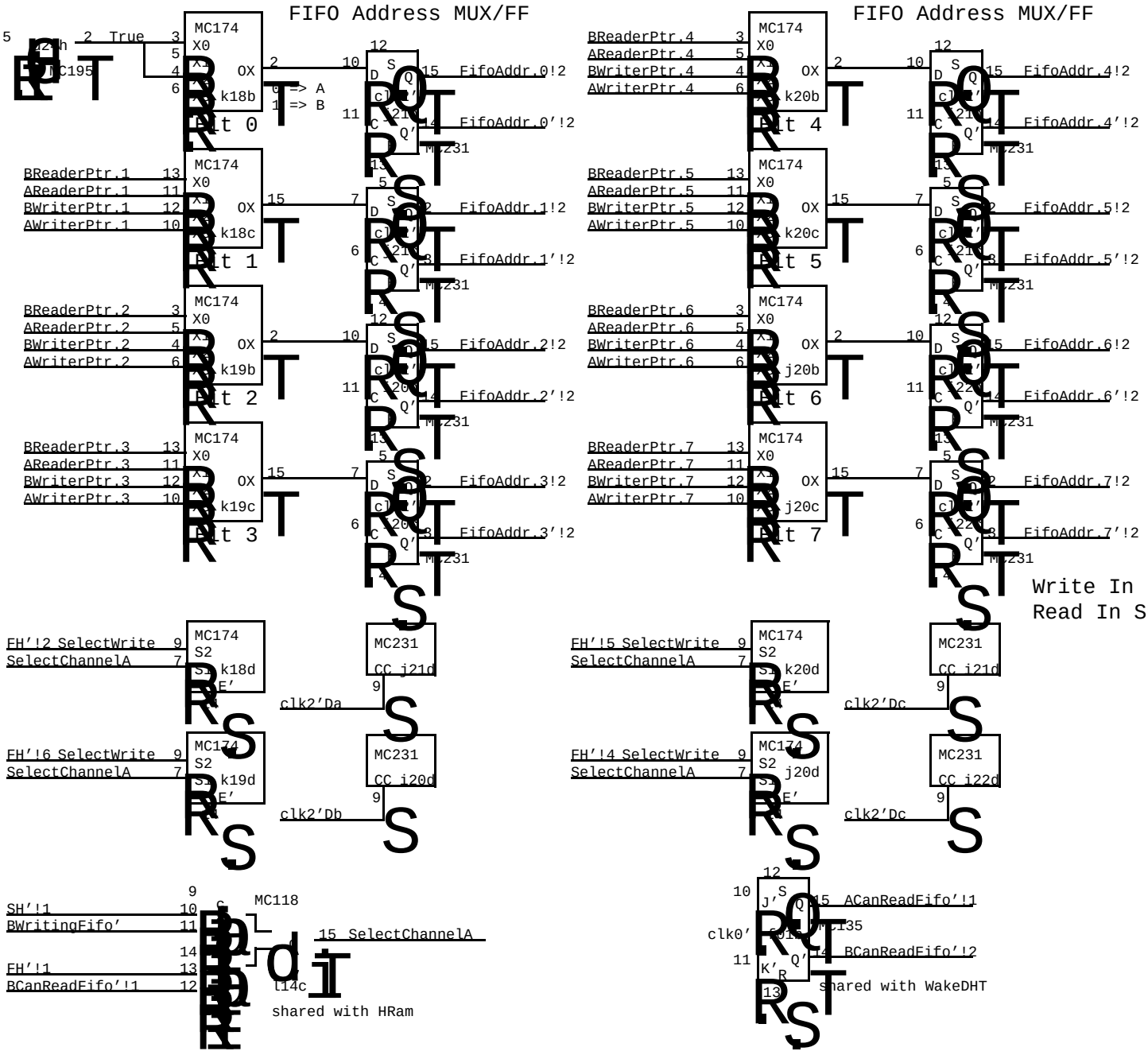

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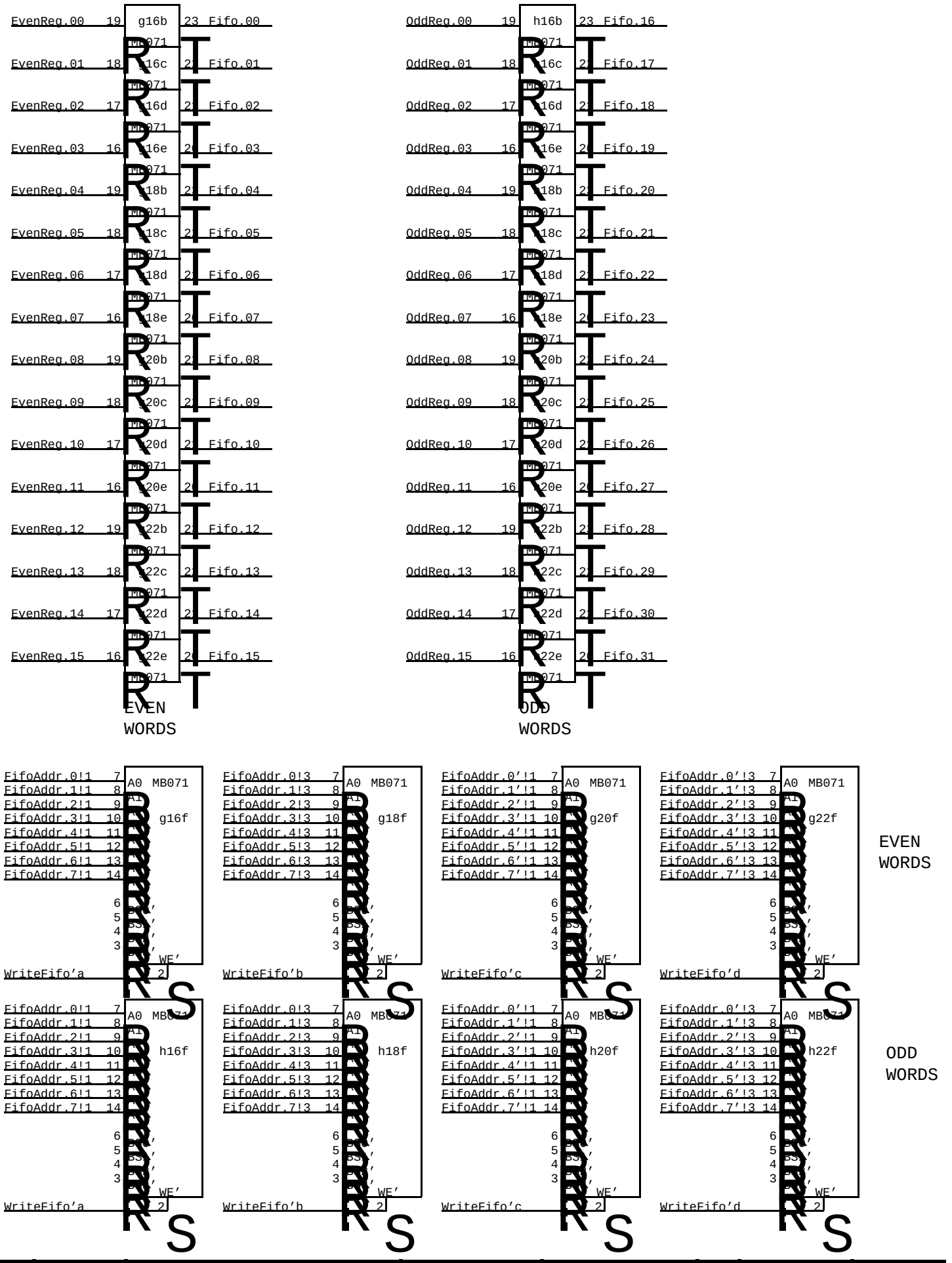
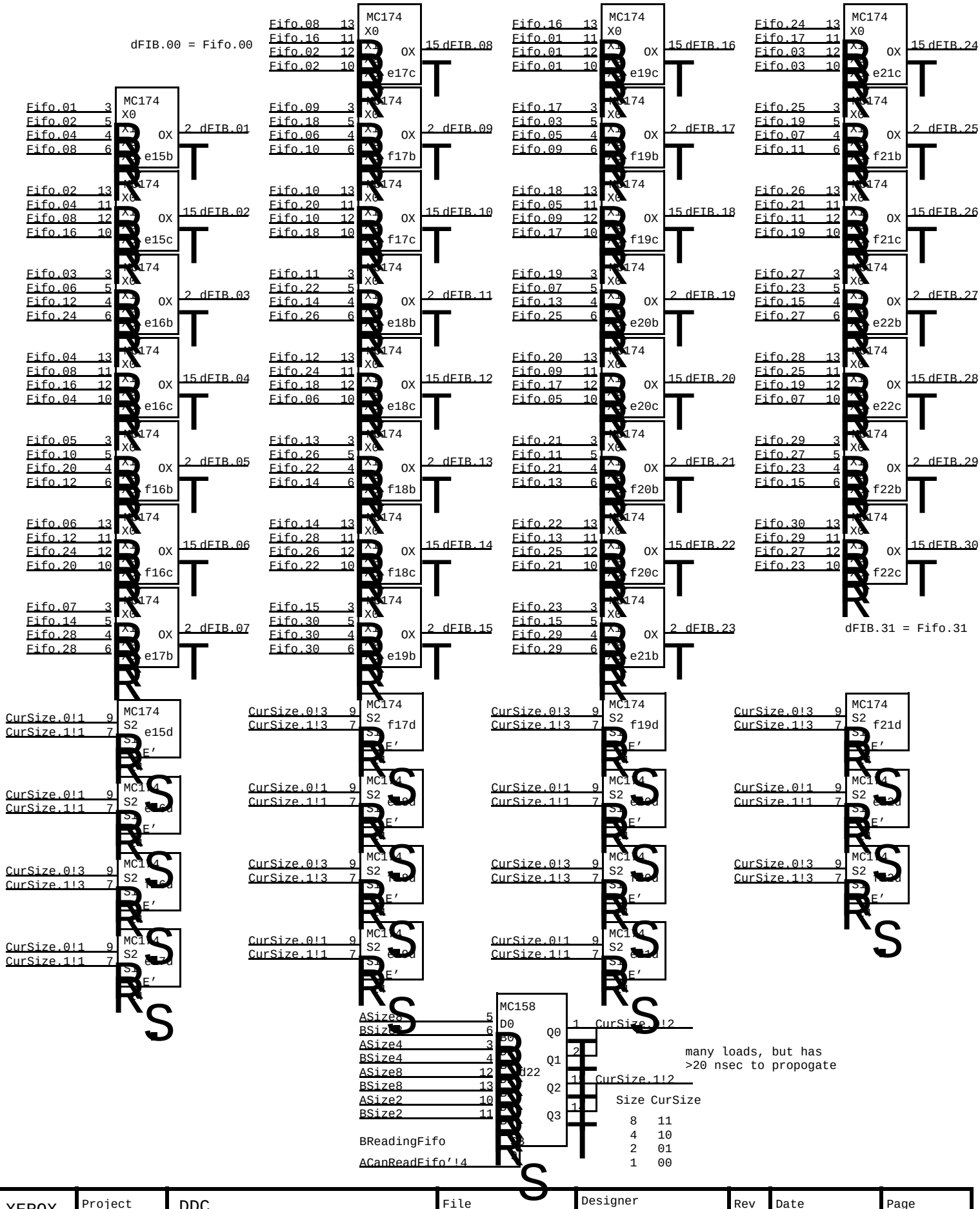
	Dorado	DispY03.sil	K. Pier	Da	11/02/79	03

DDC
Fifo Address Logic

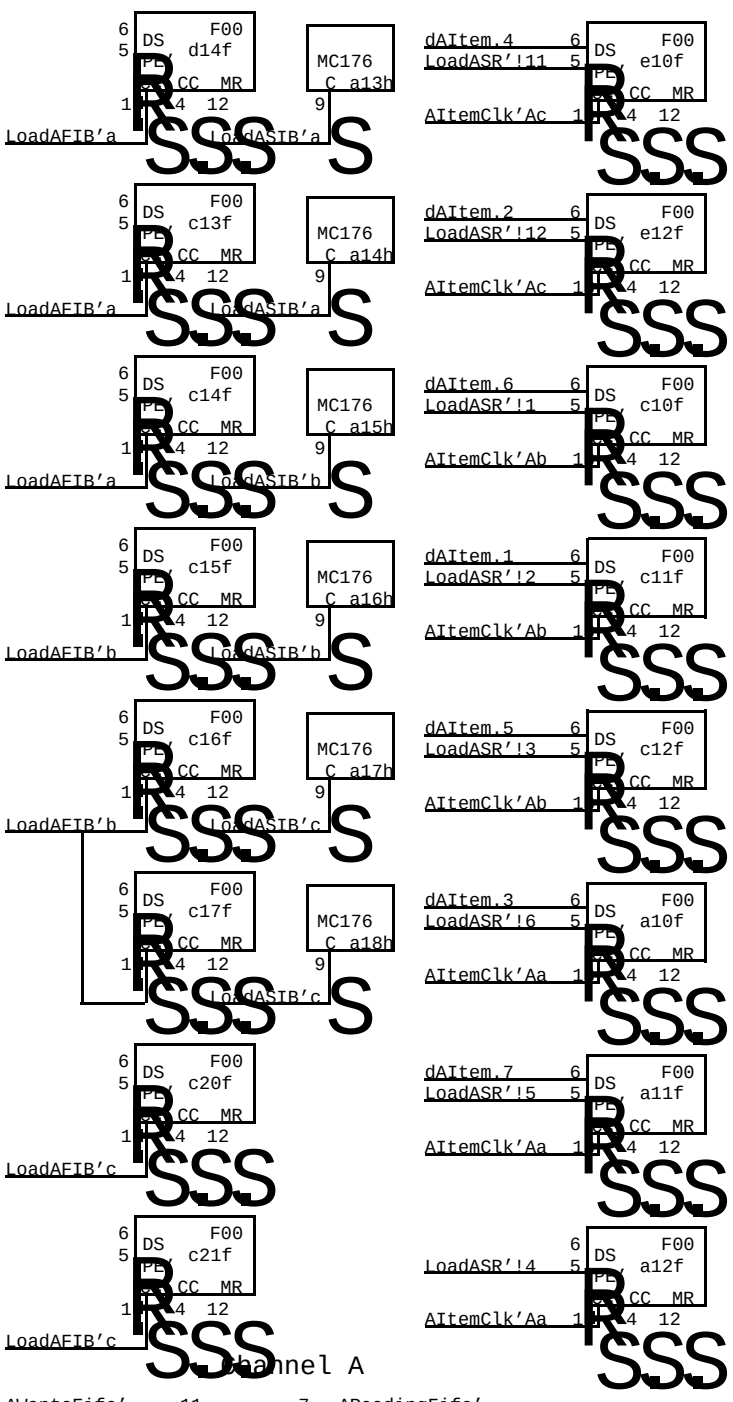


XEROX PARC	Project		File	Designer	Rev	Date	Page
	Dorado	DDC Fifo RAM chips	DispY04.sil	K. Pier	Da	7/19/79	04

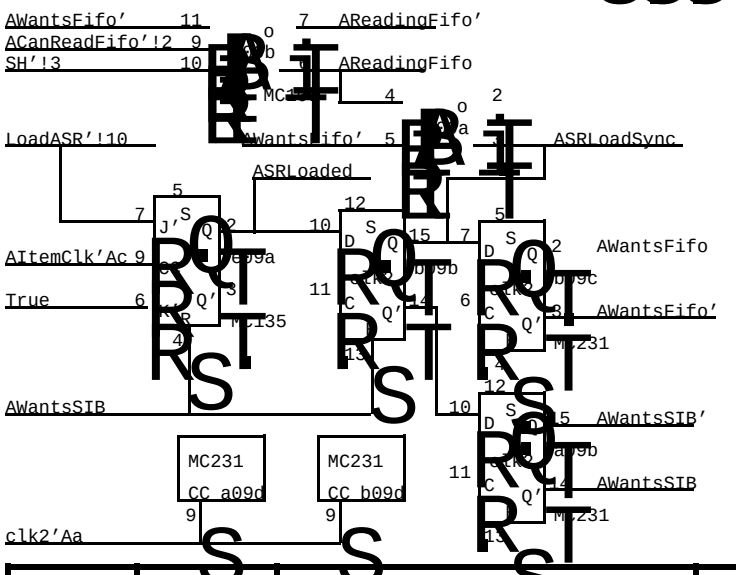
Item Generator Permuter
See ItemGenerator table for input specs

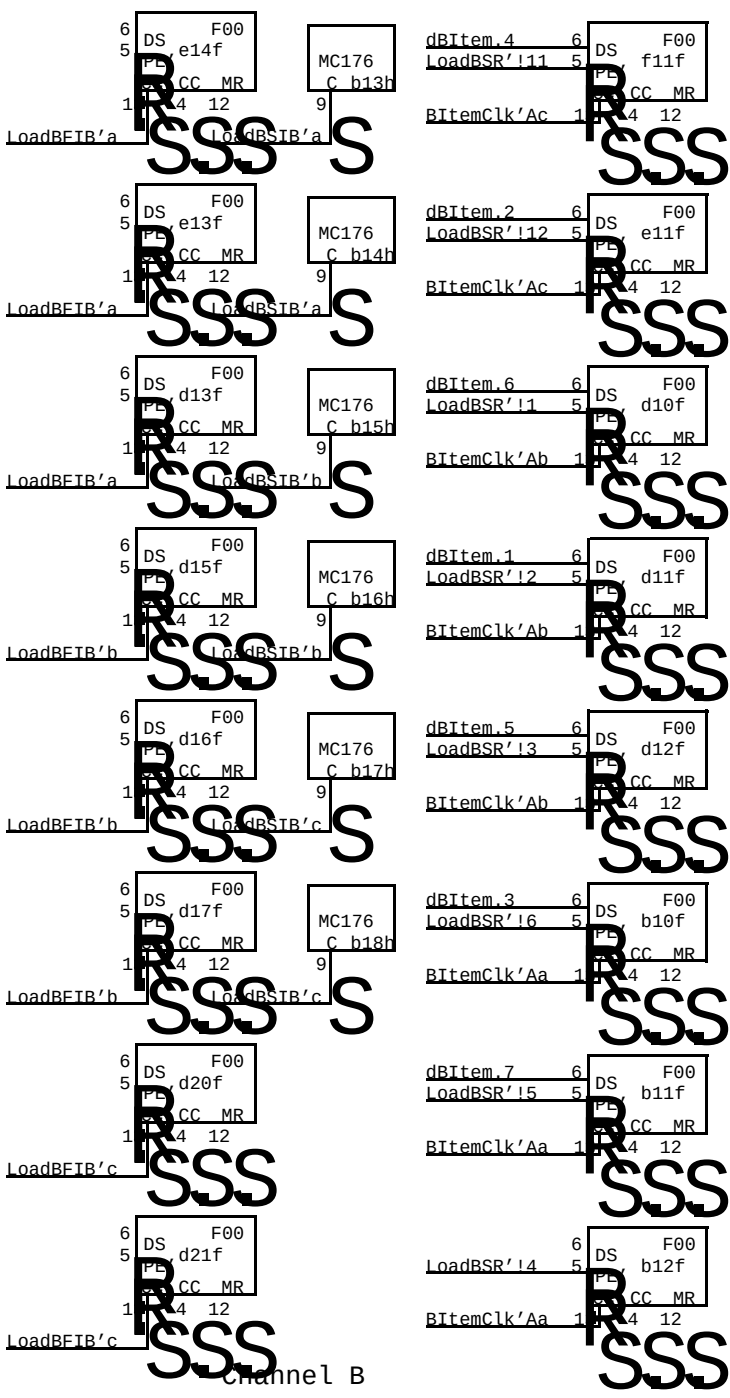


XEROX PARC	Project Dorado	DDC Item Permutation Logic	File DispY05.sil	Designer K. Pier	Rev Da	Date 11/02/79	Page 05

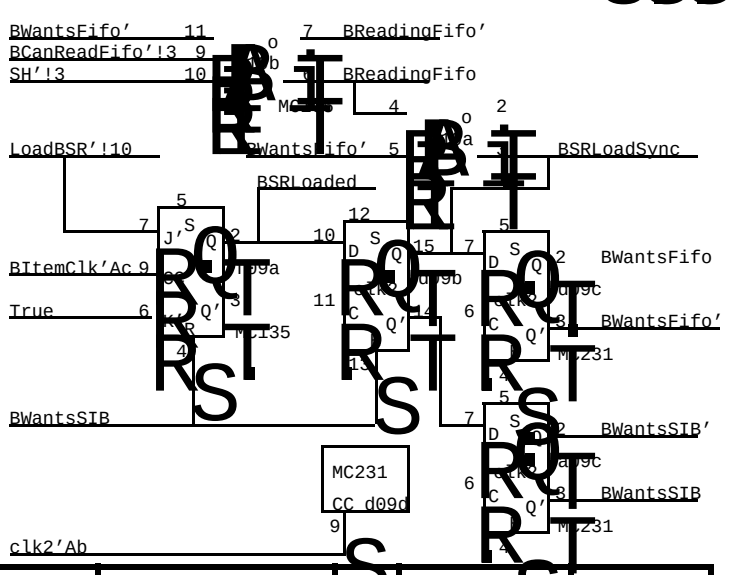


Channel A

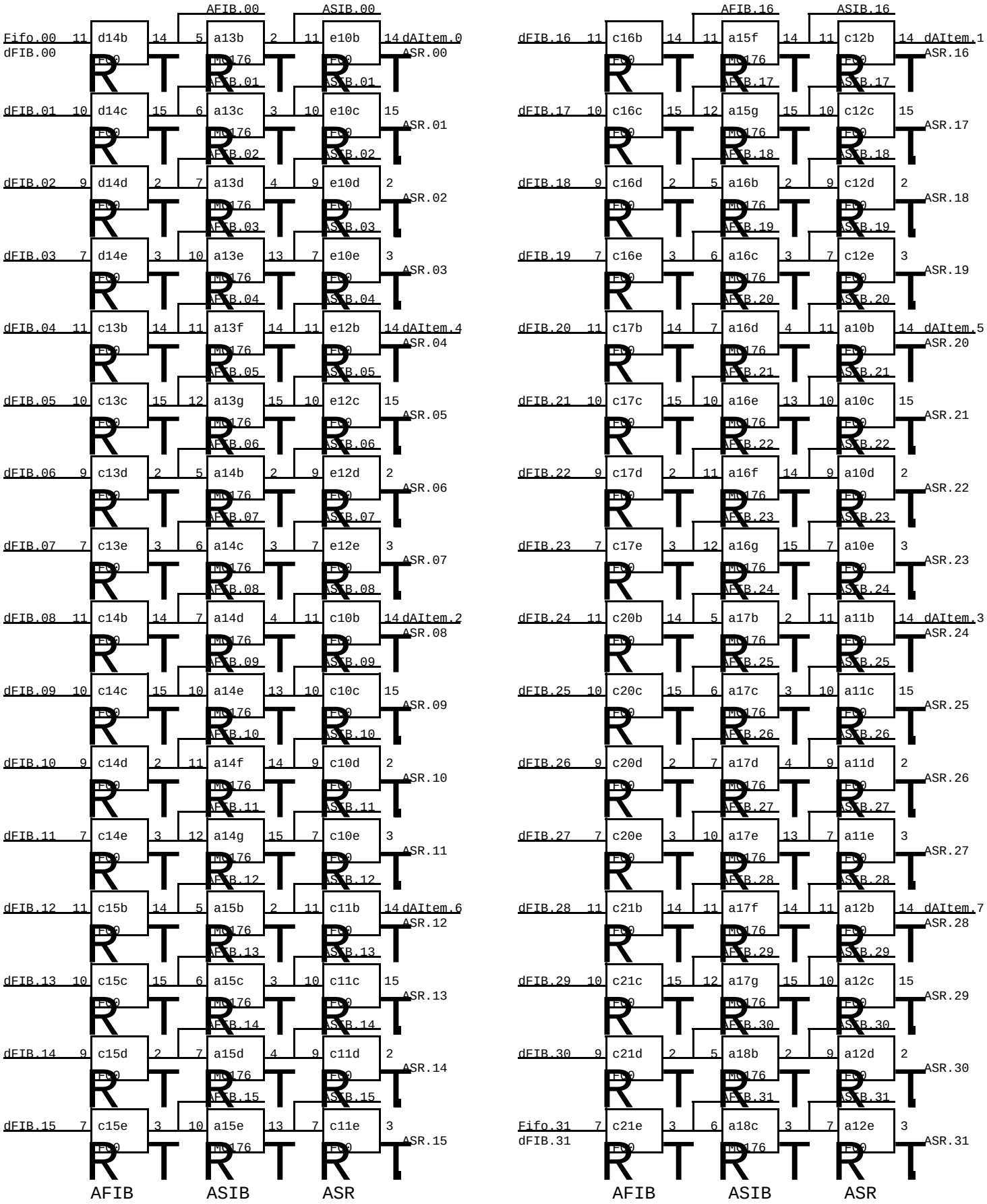




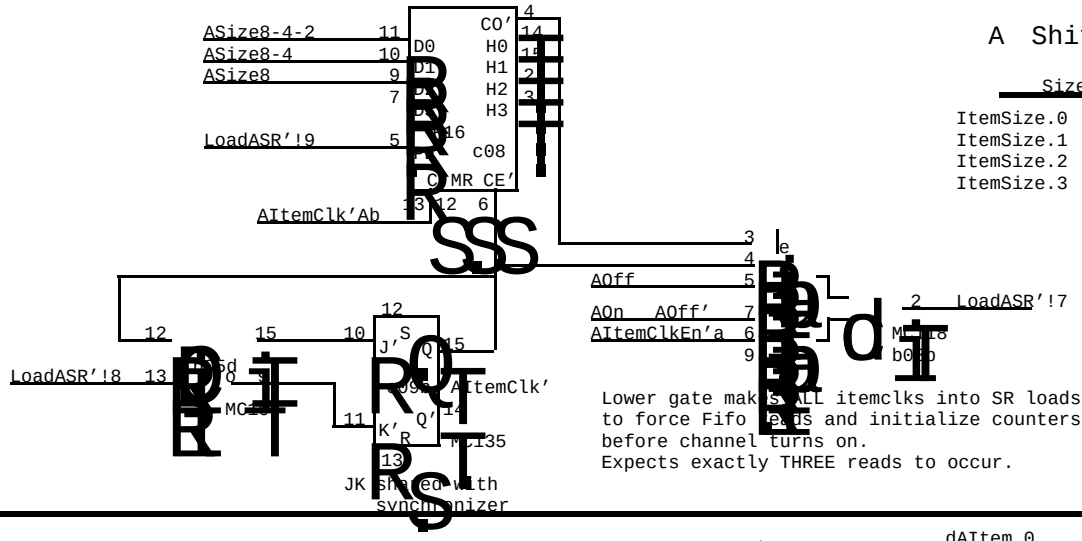
Channel B



XEROX PARC	Project Dorado	DDC Intermediate Buffer Control	File DispY06.sil	Designer K. Pier	Rev Da	Date 11/02/79	Page 06



XEROX PARC	Project		File	Designer	Rev	Date	Page
	Dorado	DDC Channel A Data Path	DispY07.sil	K. Pier	Da	7/19/79	07

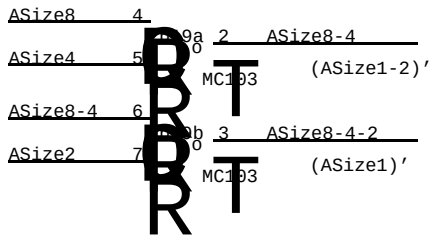


Lower gate makes ALL itemclks into SR loads to force Fifo reads and initialize counters before channel turns on.
Expects exactly THREE reads to occur.

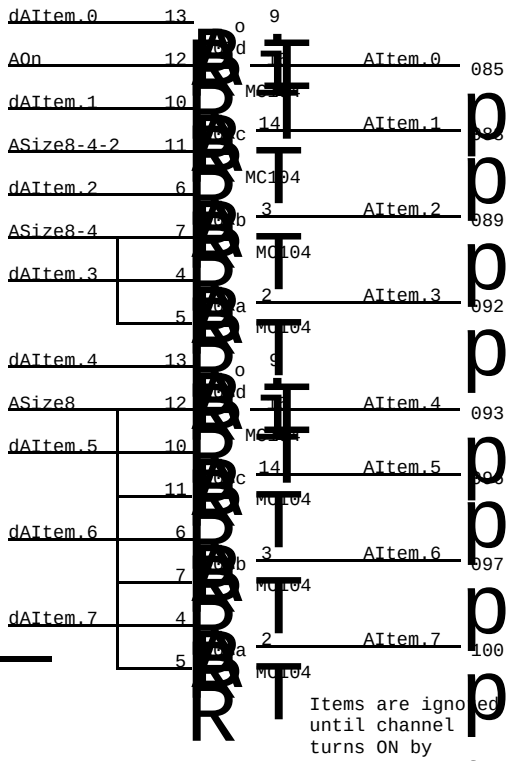
A Shift Register Control

Size	8	4	2	1
ItemSize.0	1	1	1	0
ItemSize.1	1	1	0	0
ItemSize.2	1	0	0	0
ItemSize.3	0	0	0	0

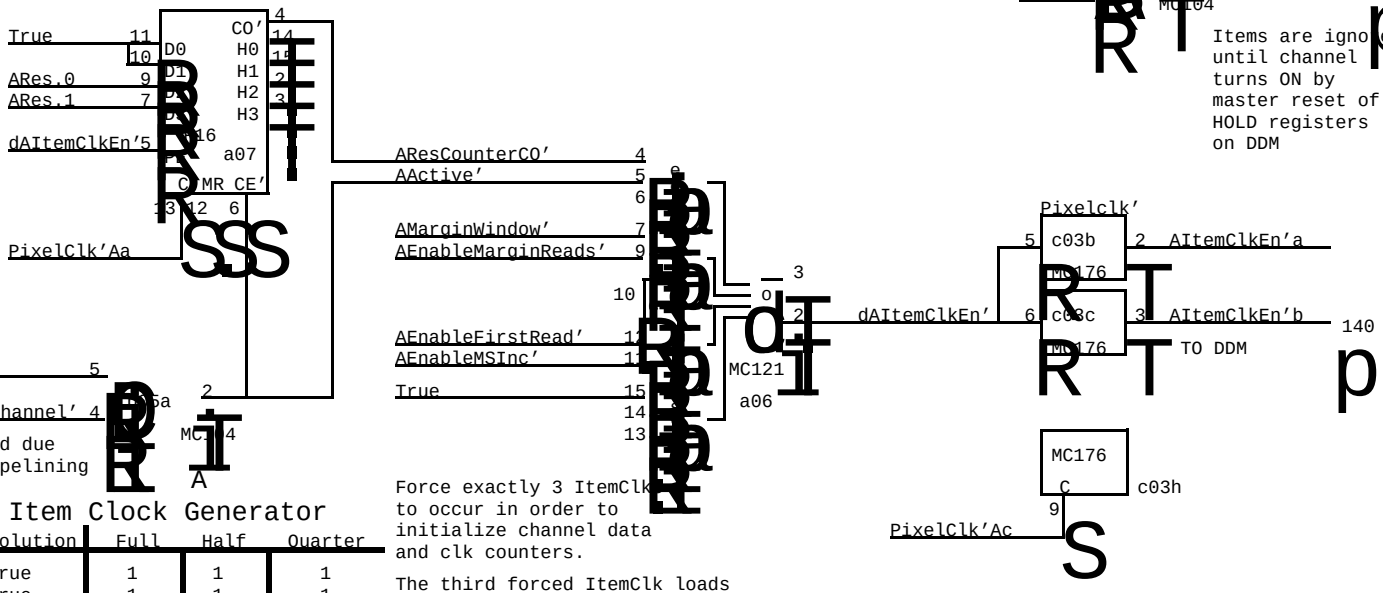
A Item buffer logic



dItems are garbage until channel becomes active



Items are ignored until channel turns ON by master reset of HOLD registers on DDM



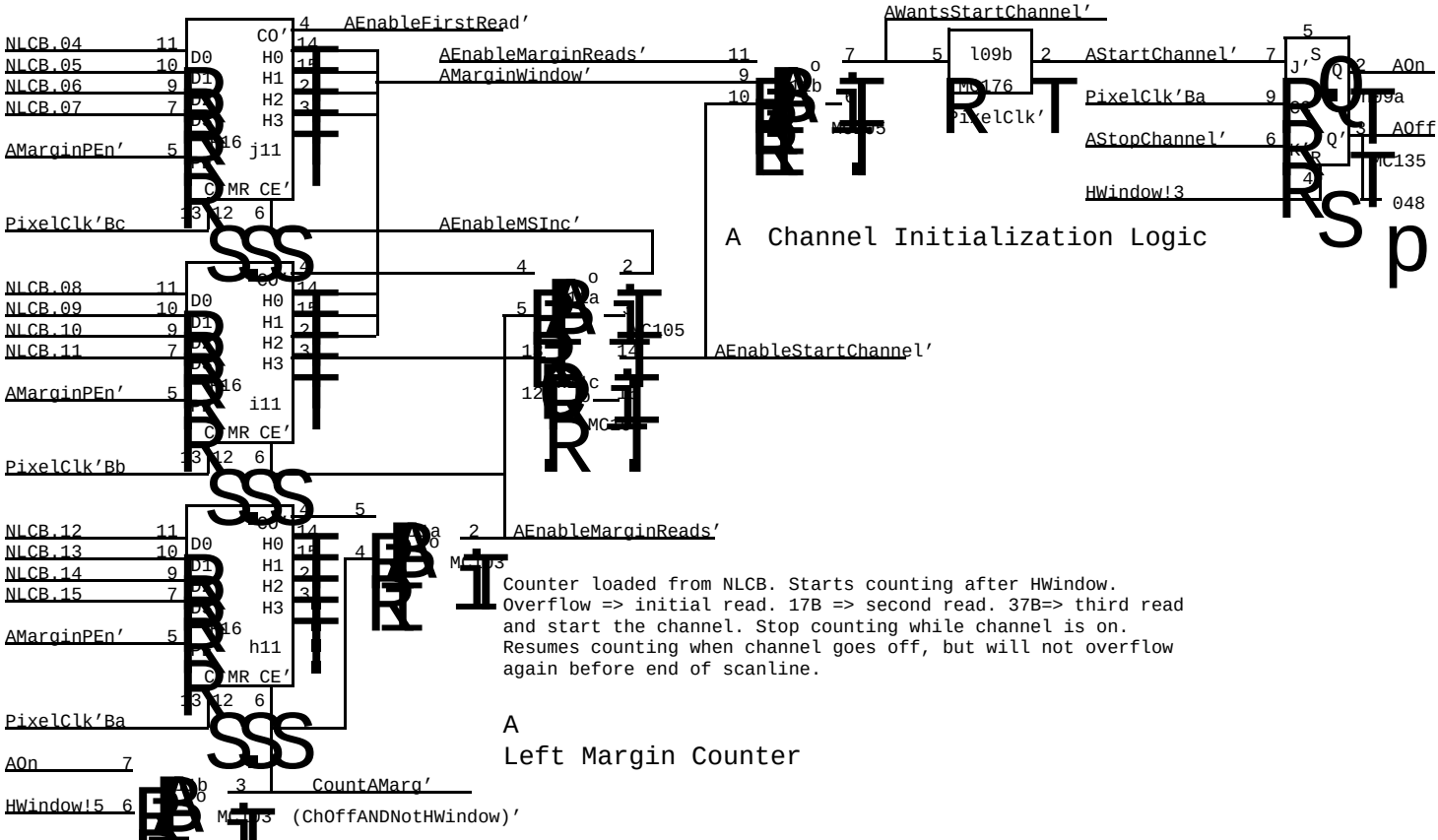
Item Clock Generator

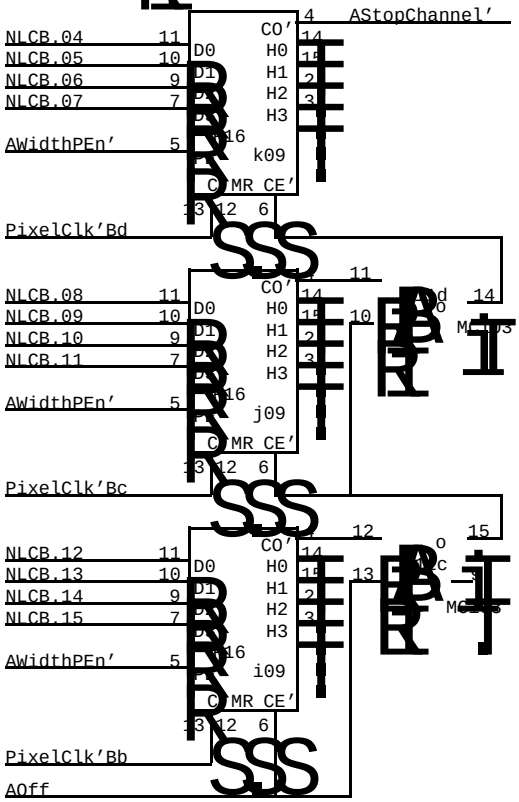
Resolution	Full	Half	Quarter
True	1	1	1
True	1	1	1
Res.0	1	1	0
Res.1	1	0	0

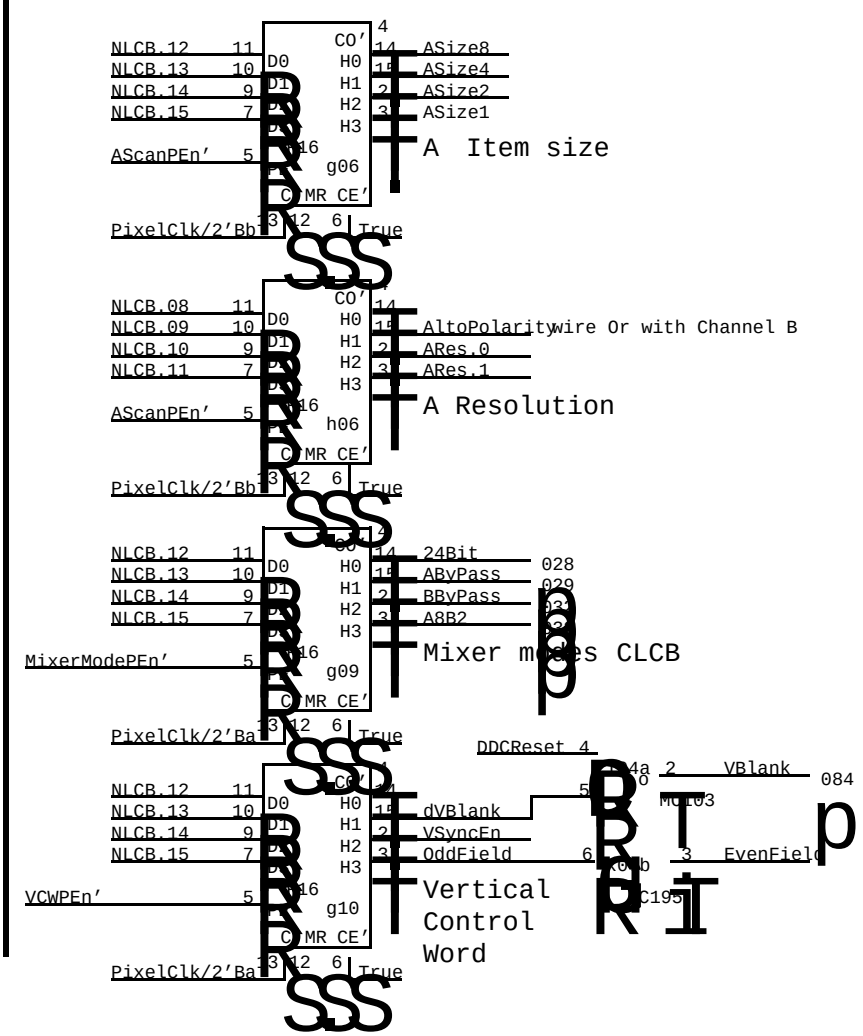
Force exactly 3 ItemClk to occur in order to initialize channel data and clk counters.

The third forced ItemClk loads SR with good data and turns the channel ON.

XEROX PARC	Project Dorado	DDC Channel A Items plus SR and ItemClk Control	File DispY08.sil	Designer K. Pier	Rev Da	Date 7/19/79	Page 08

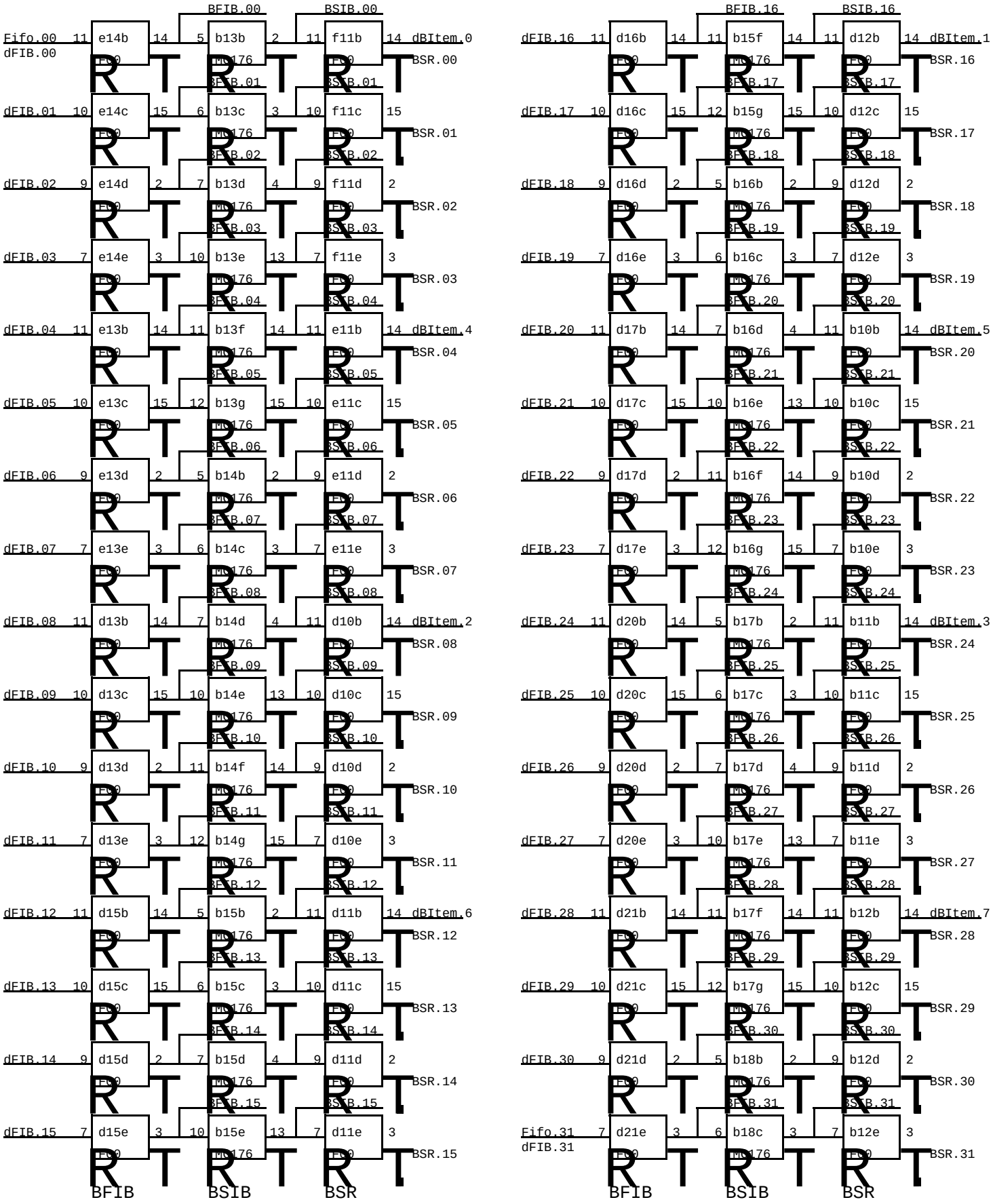




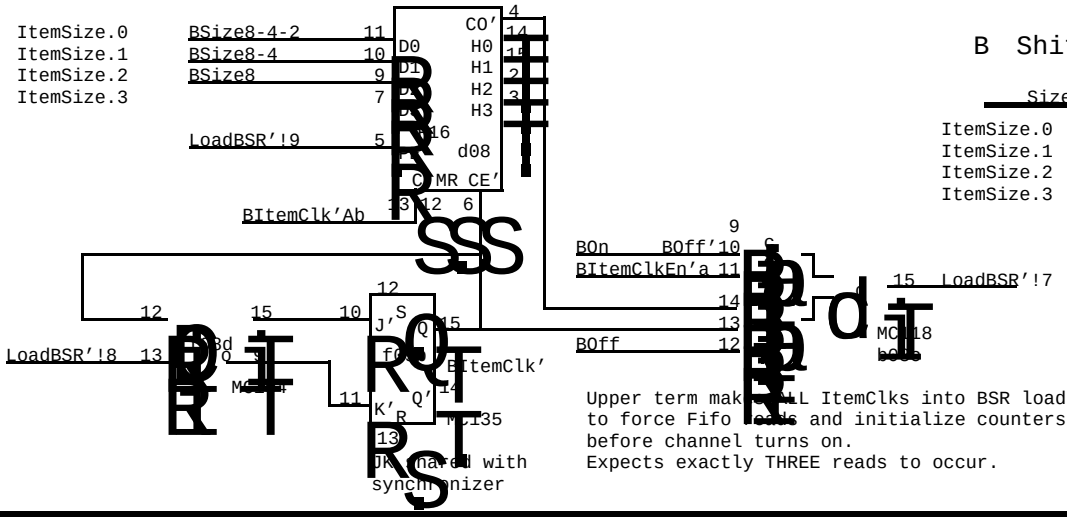


XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	DispY09.sil	K. Pier	Da	7/19/79	09

DDC Channel A
Current Line Ctrl Block



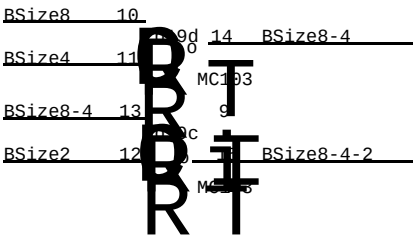
XEROX PARC	Project		File	Designer	Rev	Date	Page
	Dorado	DDC Channel B Data Path	DispY10.sil	K. Pier	Da	7/19/79	10



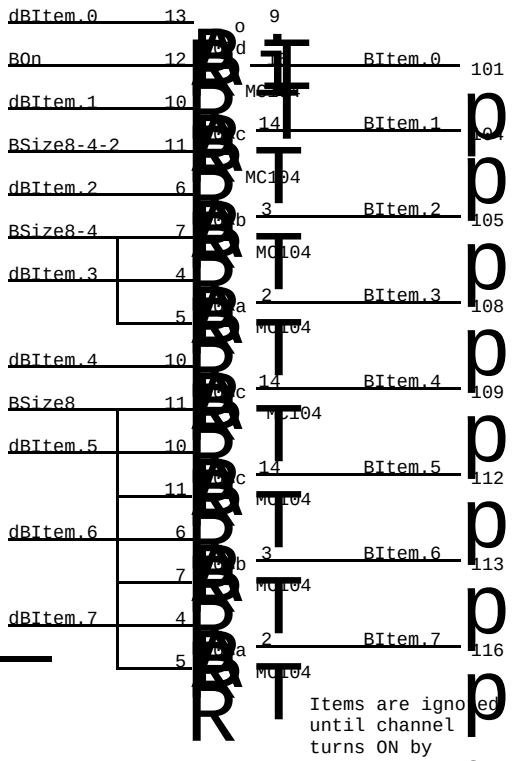
B Shift Register Control

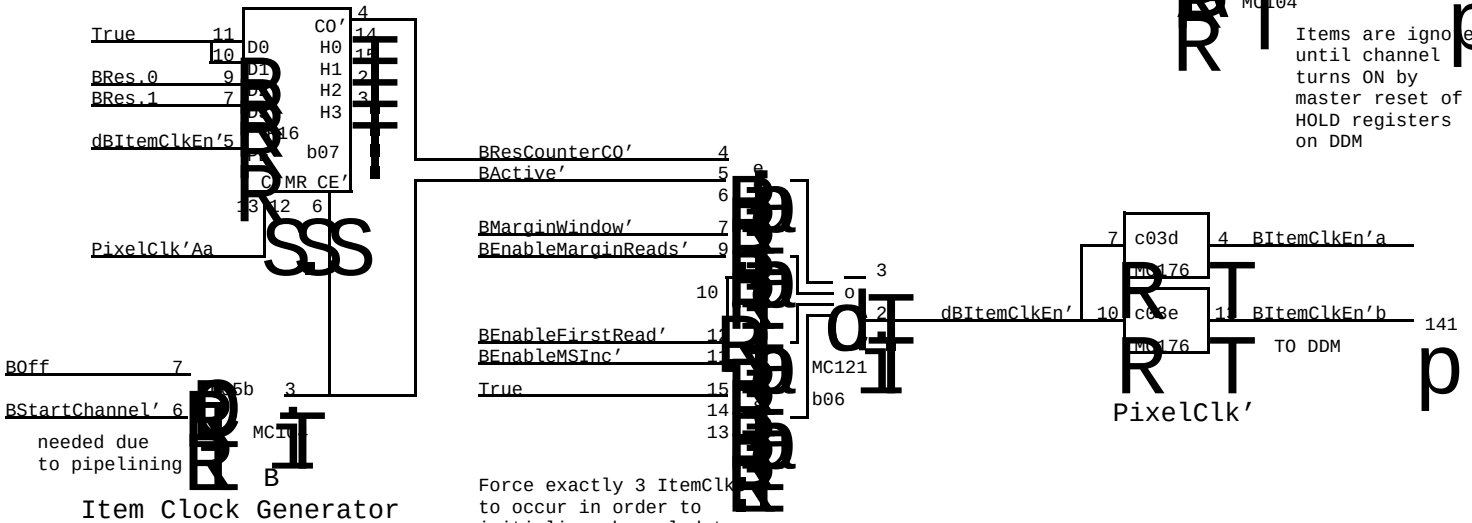
Size	8	4	2	1
ItemSize.0	1	1	1	0
ItemSize.1	1	1	0	0
ItemSize.2	1	0	0	0
ItemSize.3	0	0	0	0

B Item buffer logic



dItems are
garbage until
channel
becomes active

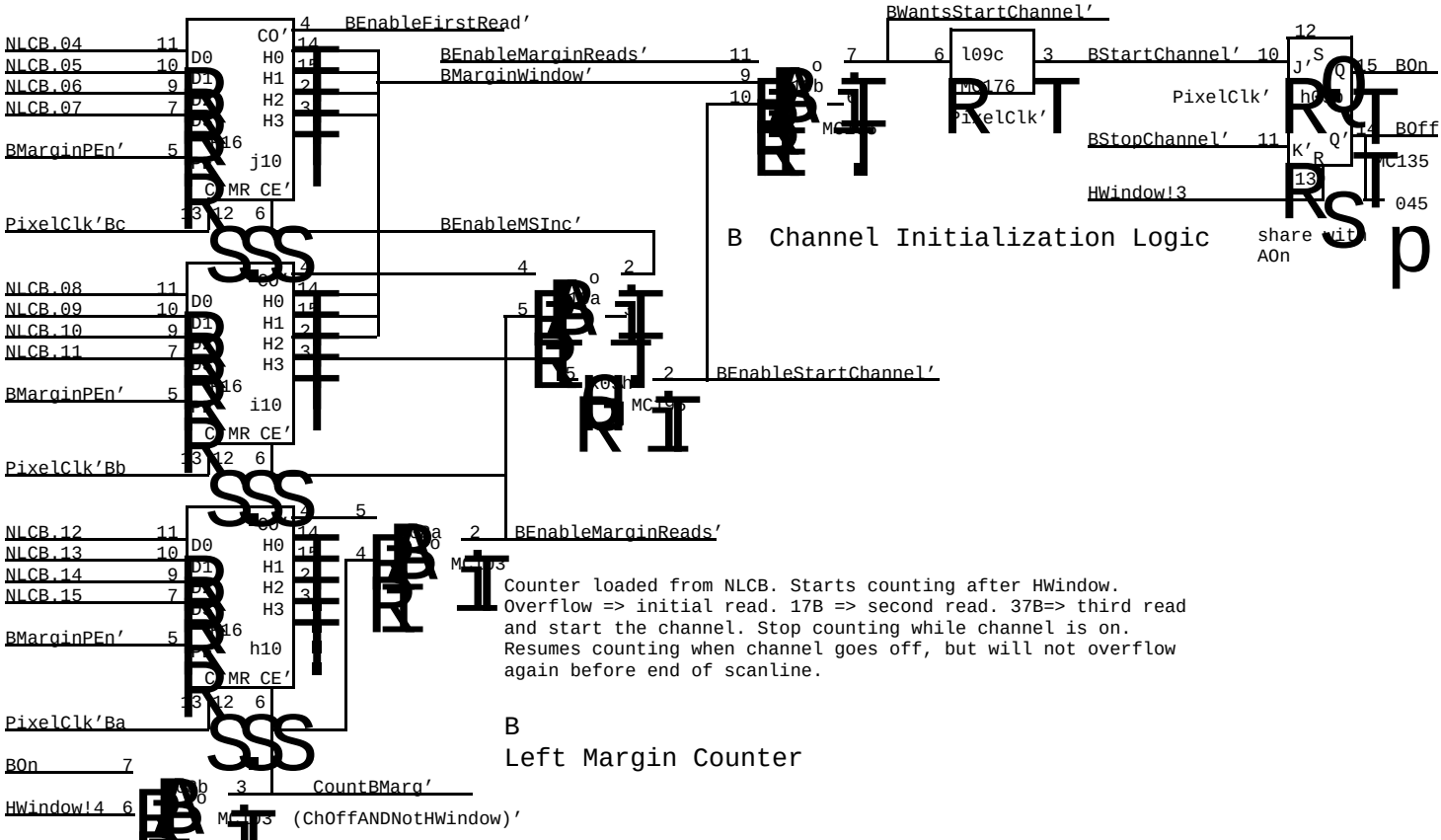


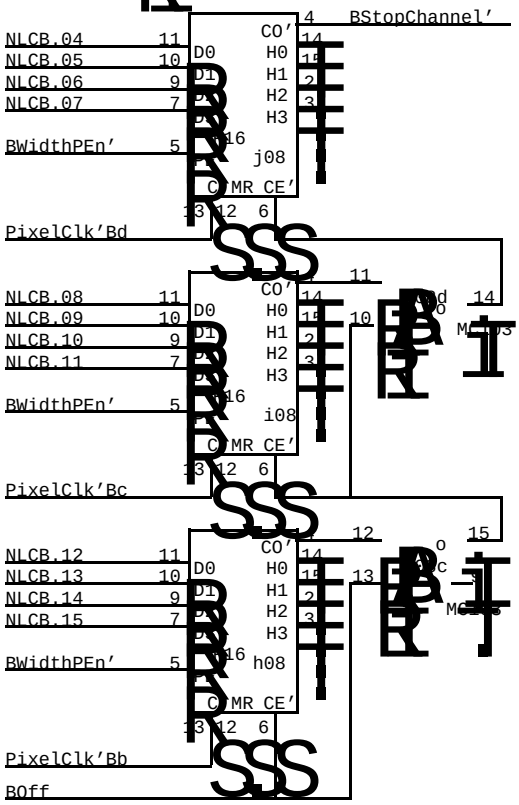


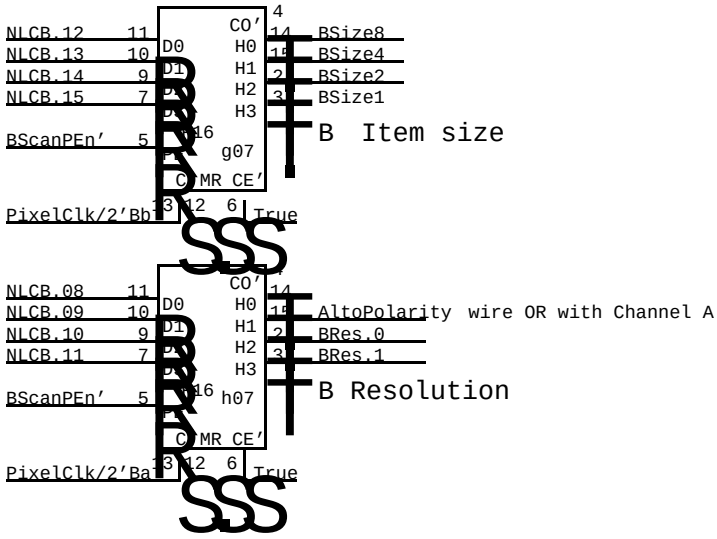
Item Clock Generator

Resolution	Full	Half	Quarter
True	1	1	1
True	1	1	1
Res.0	1	1	0
Res.1	1	0	0

XEROX PARC	Project Dorado	DDC Channel B Items, SR and ItemClk Control	File DispY11.sil	Designer K. Pier	Rev Da	Date 7/19/79	Page 11

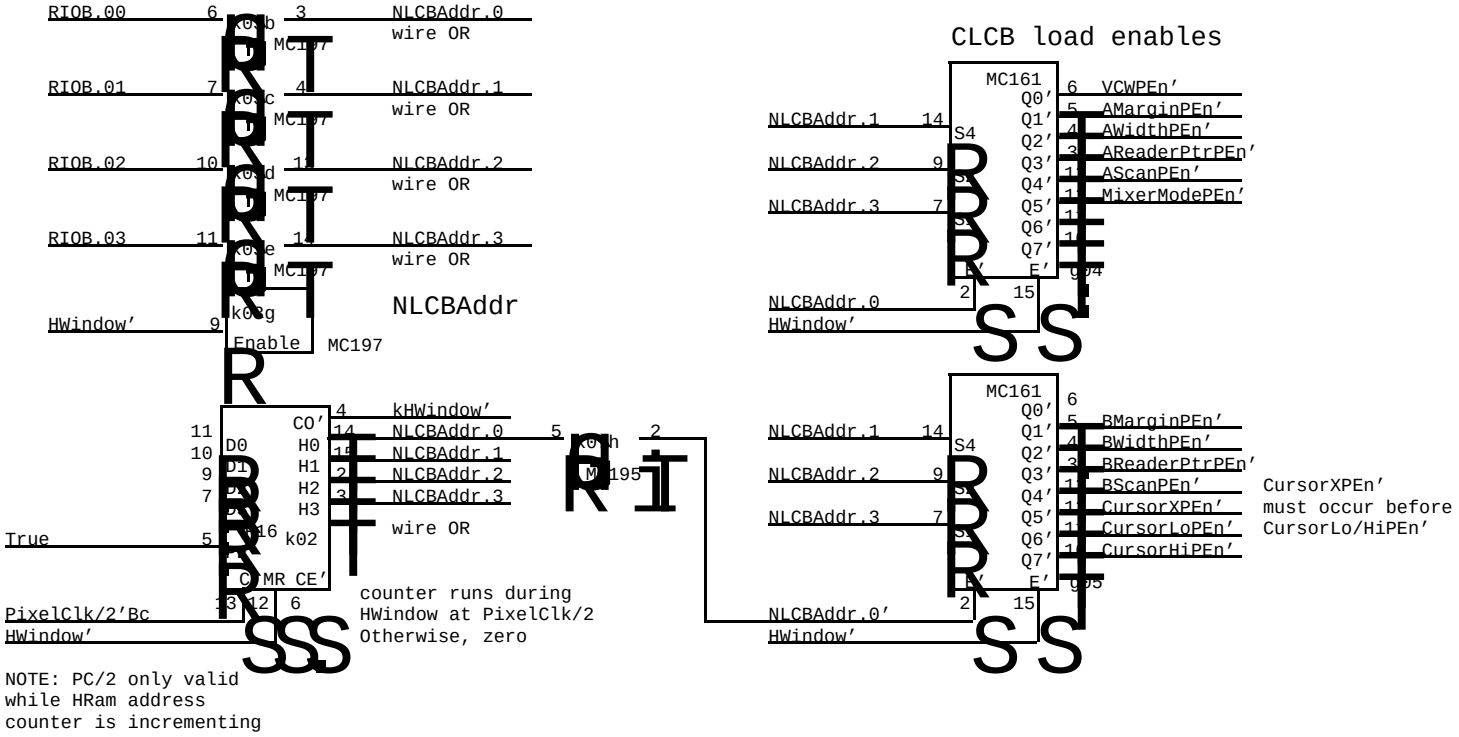


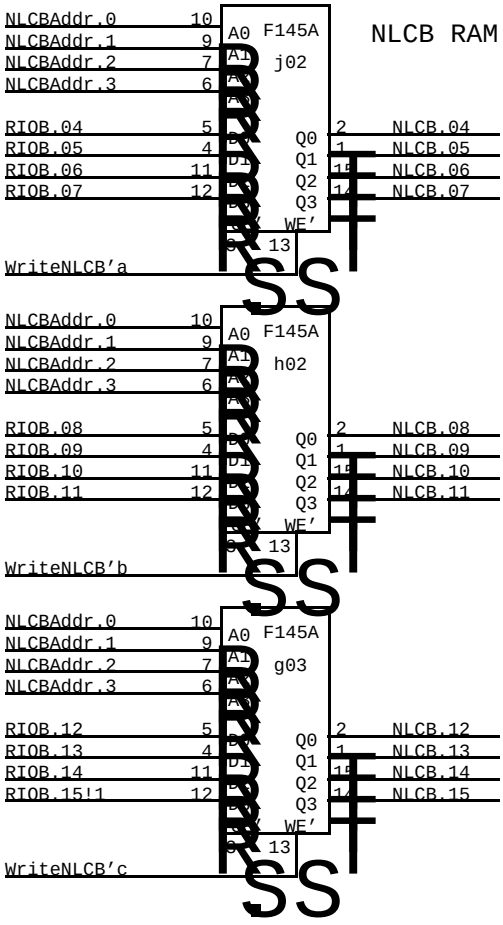


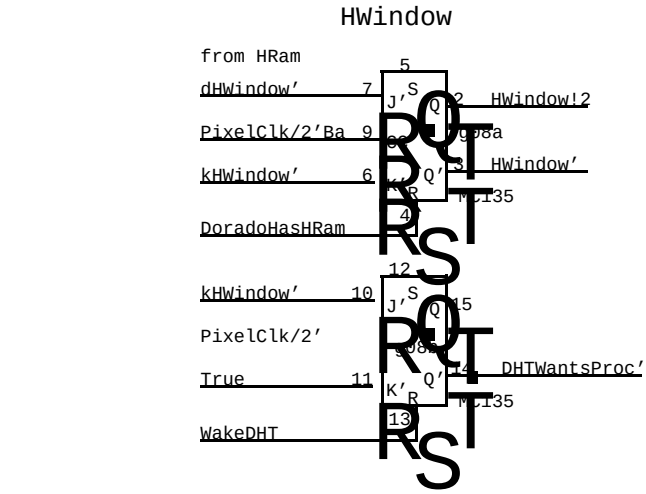


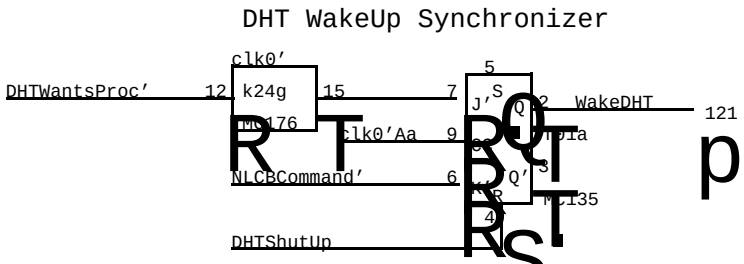
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	DispY12.sil	K. Pier	Da	7/19/79	12

DDC Channel B
Current Line Ctrl Block



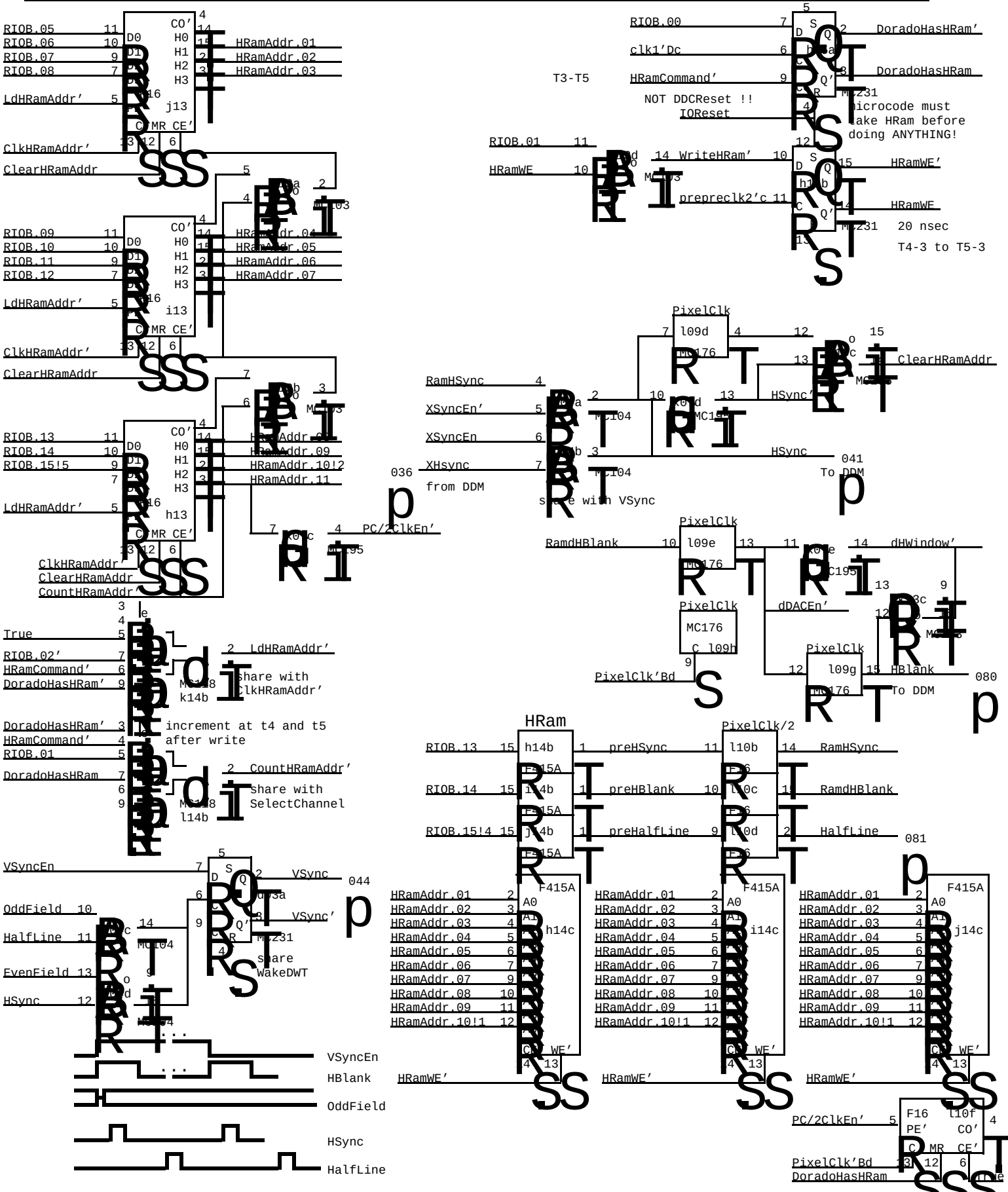






XEROX PARC	Project		File	Designer	Rev	Date	Page
	Dorado	DDC Next Line Control Block	DispY13.sil	K. Pier	Da	7/19/79	13

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Keep HRam'	Write HRam'	Load HRam Addr	X	12 bits of HRam data											



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado DDC Horizontal RAM	DispY14.sil	K. Pier	Da	7/19/79	14

THE DDC MAINTAINS, FOR EACH CHANNEL, TWO FLAGS:

NEXT Word Control Block Flag (NextWCBFlag)
Current Word Control Block Flag (CurrentWCBFlag)

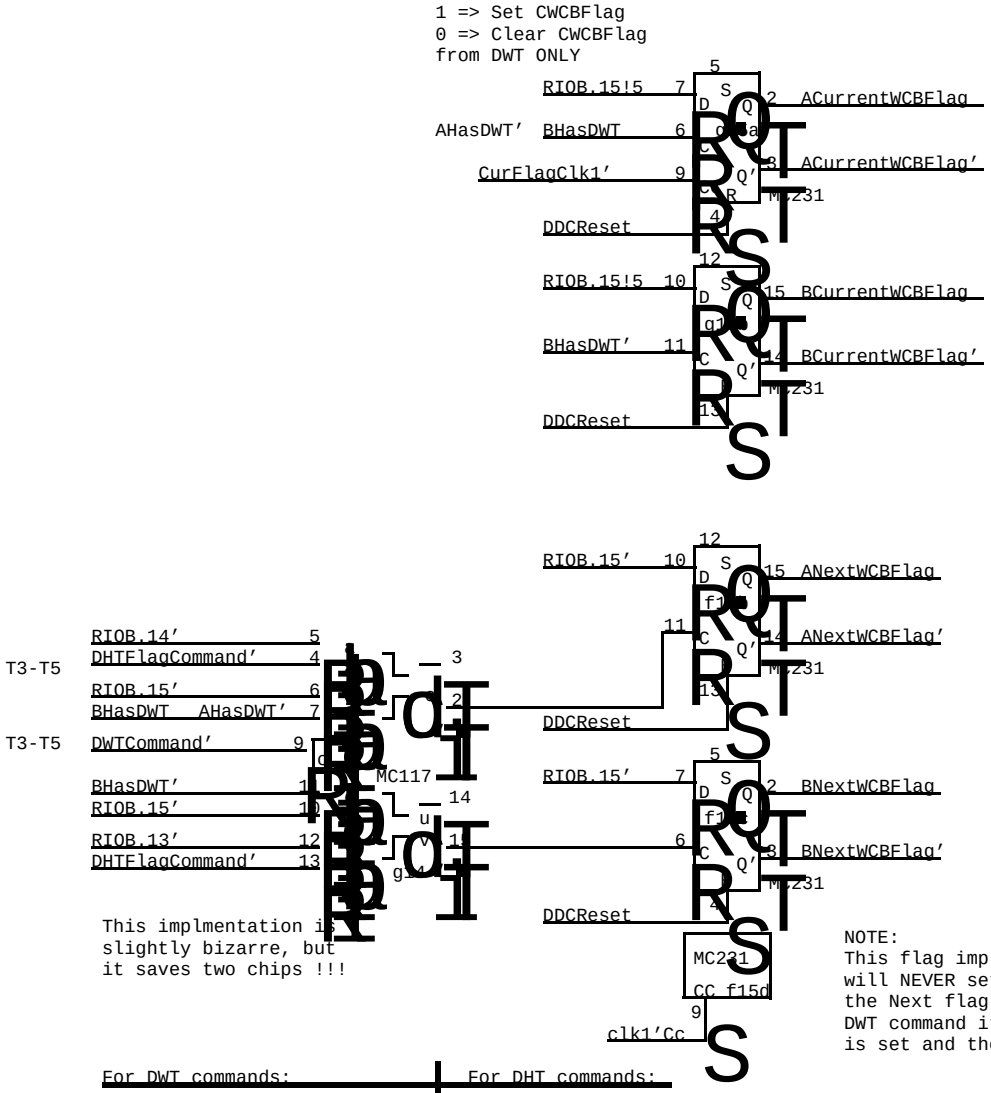
A Word Control Block is a pair of values called Address and MunchCount, for either the CURRENT or the NEXT scanline.

Flag management	SET	CLEARED
NextWCBFlag	by DHT when it has filled the NextWCB	by DWT when it has copied NextWCB into CurrentWCB
CurrentWCBFlag	by DWT when it has copied NextWCB into CurrentWCB	by DWT after it has sent out all the data from the CurrentWCB

WakeUp conditions:

WakeDHT: whenever CLCB _ NLCB i.e.: end of every HWindow

WakeDWT: (CurrentWCBFlag AND BufferAvailable)OR (NextWCBFlag AND NOT(CurrentWCBFlag))



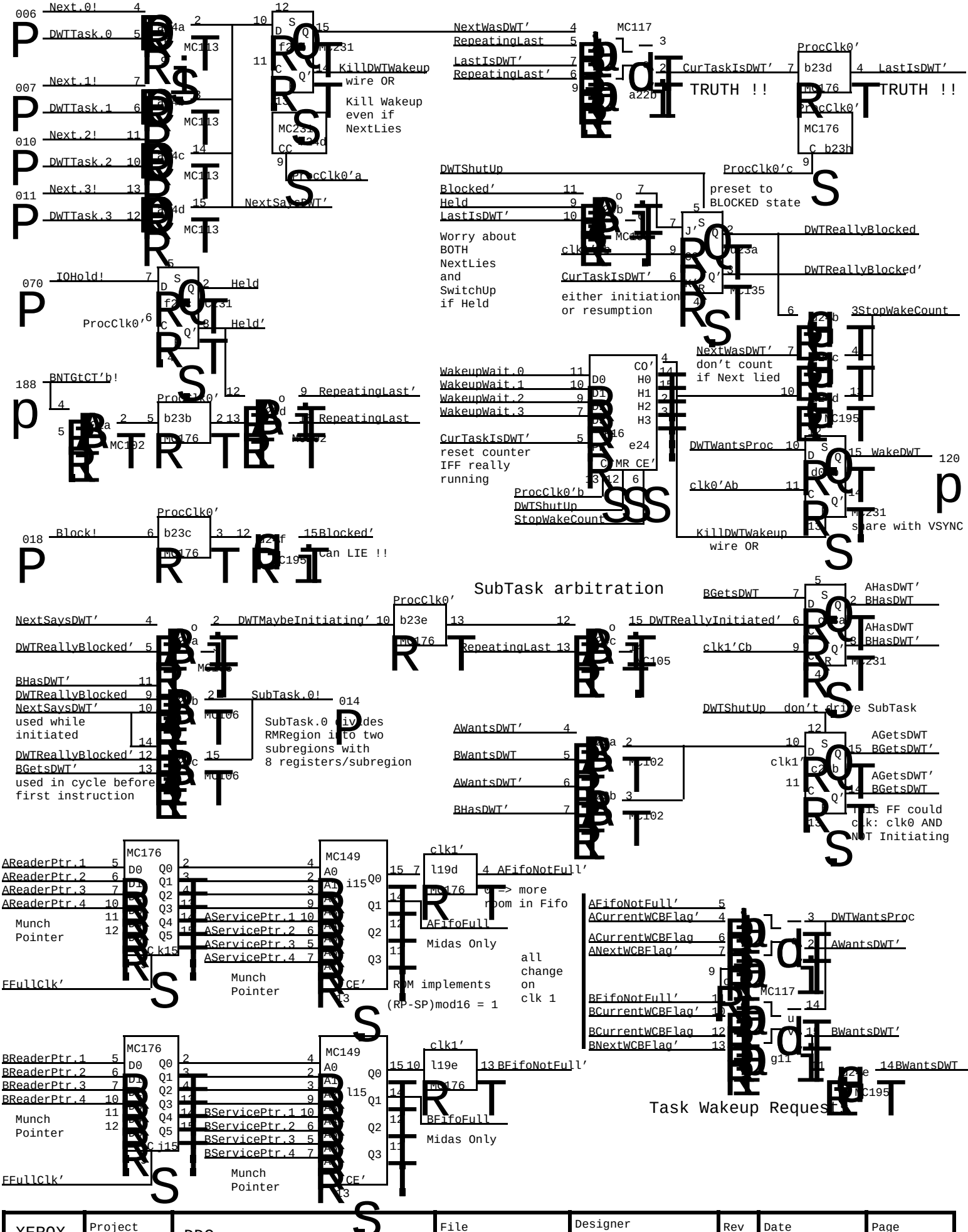
This circuit ASSUMES:
1. a DWT command with RIOB.11 set is to be ignored.See clock page.
2. Any DWT command with RIOB.11 low is a CWCBFlag command, either set or clear. See clock page.

This implmentation is slightly bizarre, but it saves two chips !!!

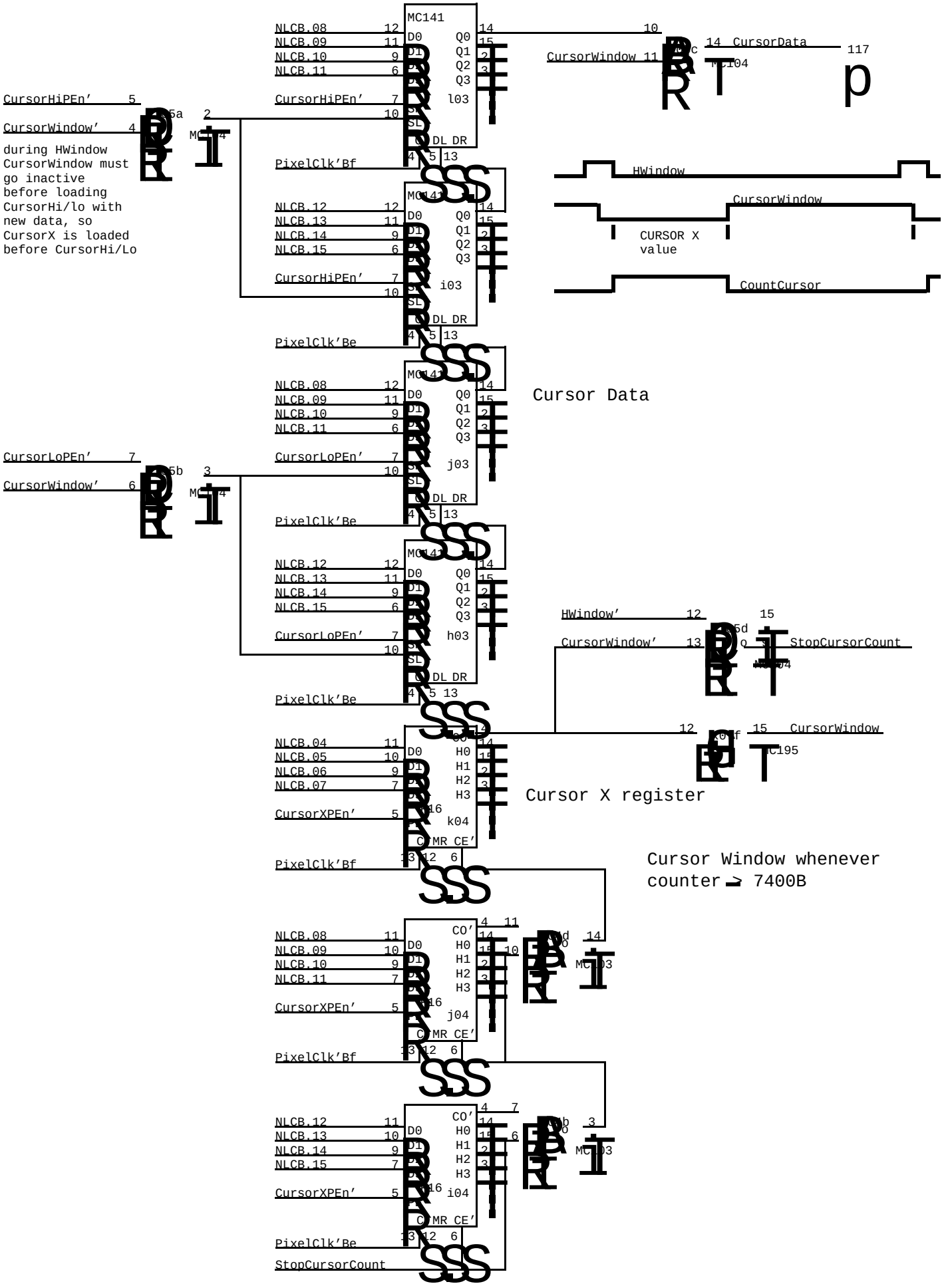
NOTE:
This flag implementation assumes that DHT flag commands will NEVER set bit 15 and will ALWAYS set either 13 or 14, the Next flag to set.Also, it assumes the ONLY kind of DWT command it should respond to is one in which bit 15 is set and therefore NextWCBFlag is to be cleared.

For DWT commands:		For DHT commands:	
RIOB	Means	RIOB	Means
=20c	IOFetch signal don't touch Flags	=2c	Set ANextWCBFlag
=1c	Set CWCBFlag and Clear NWCBFlag	=4c	Set BNextWCBFlag
=0c	Clear CWCBFlag		

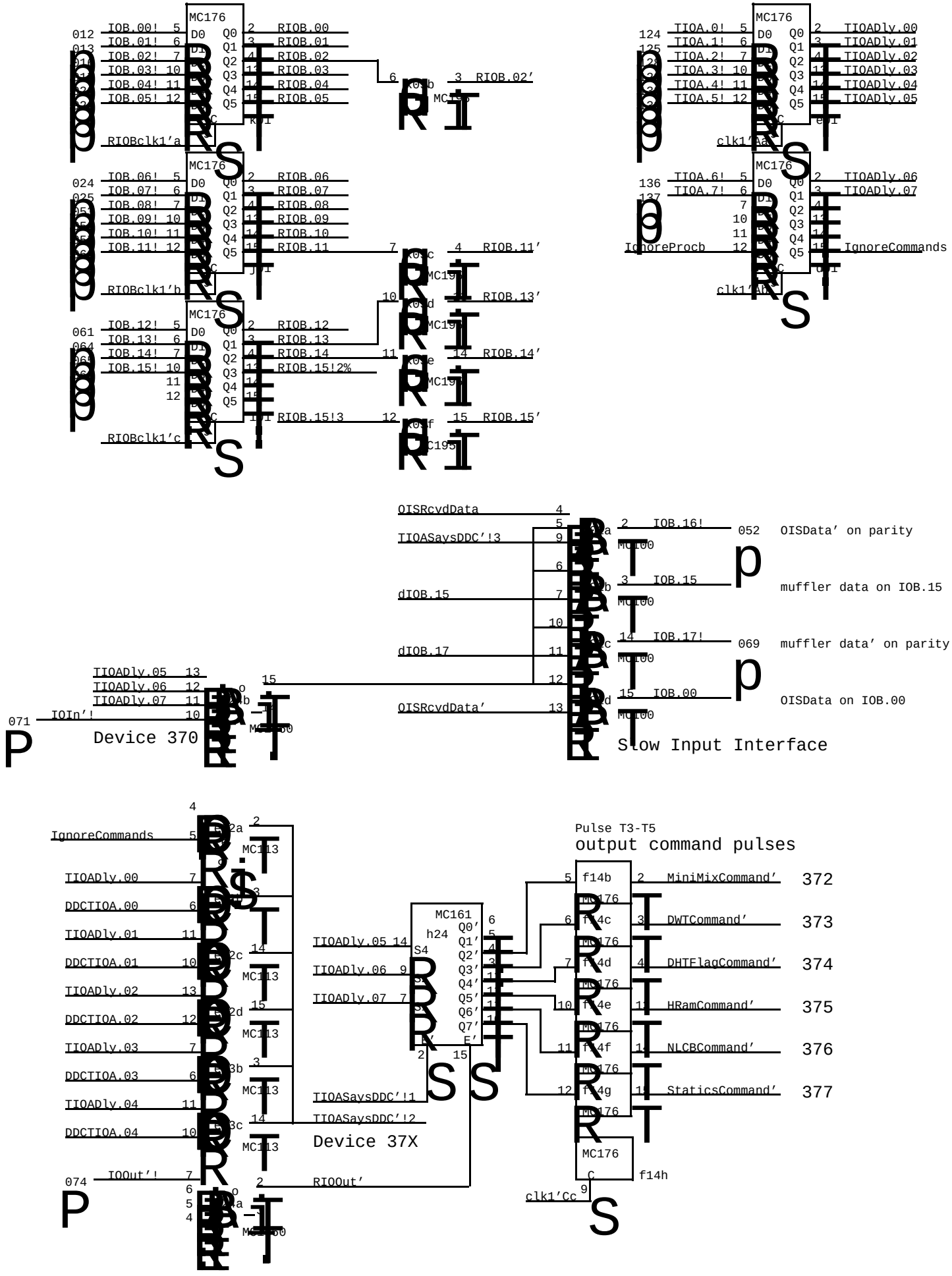
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado DDC Flag control logic	DispY15.sil	K. Pier	Da	7/19/79	15



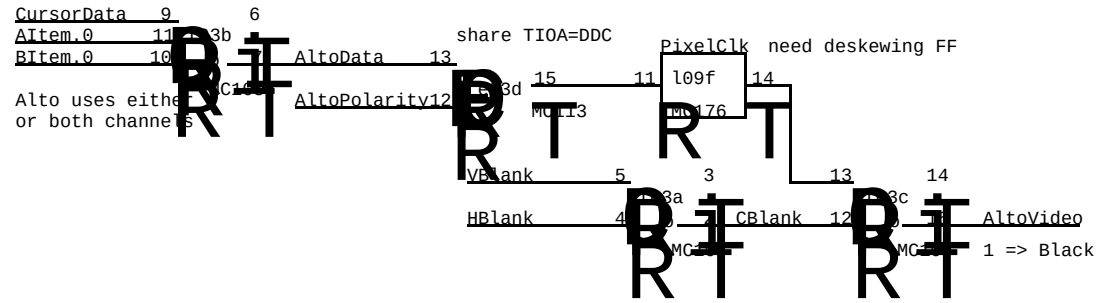
XEROX PARC	Project	DDC DWT Task Wakeup Logic	File	Designer	Rev	Date	Page
	Dorado		DispY16.sil	K. Pier	Da	4/07/81	16

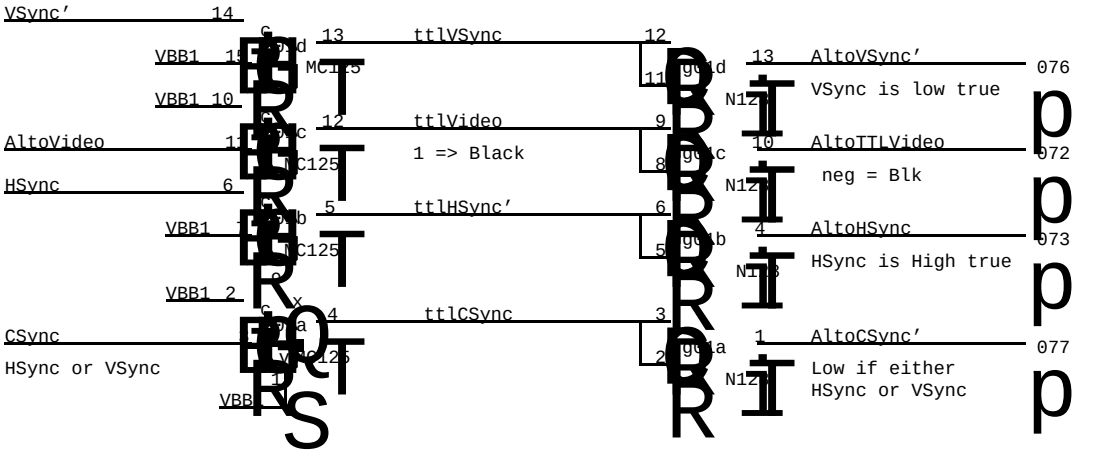


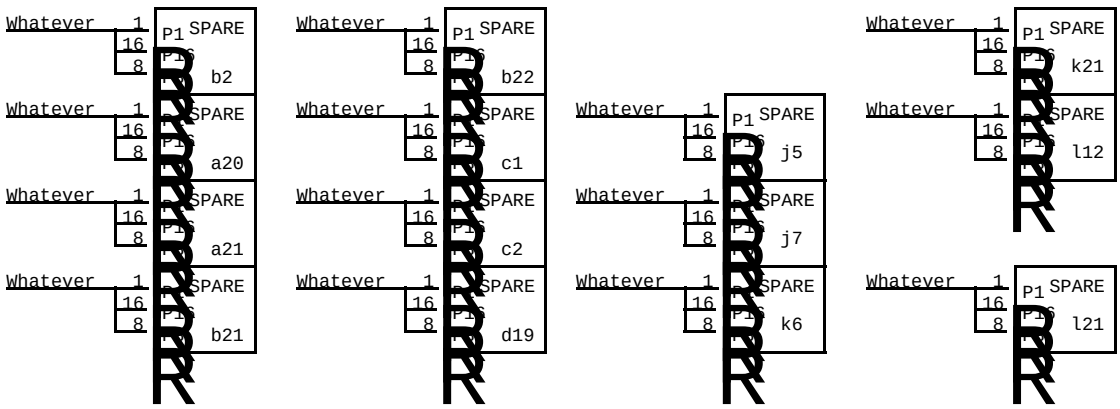
XEROX PARC	Project		File	Designer	Rev	Date	Page
	Dorado	DDC Cursor Hardware	DispY17.sil	K. Pier	Da	7/19/79	17

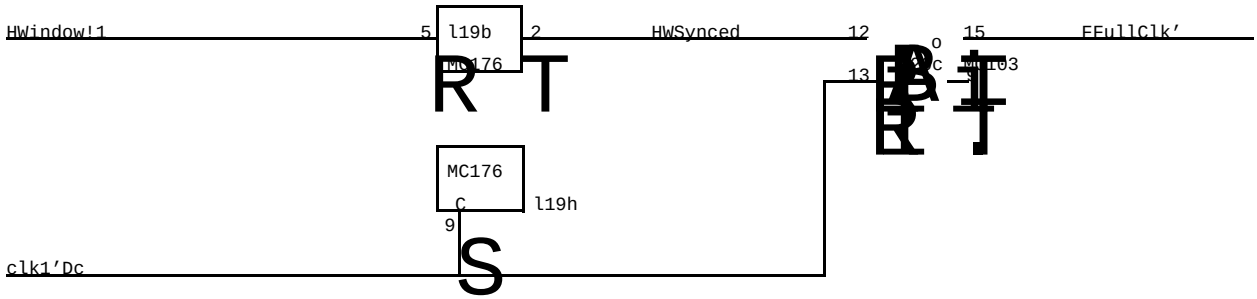


XEROX PARC	Project		File	Designer	Rev	Date	Page
	Dorado	DDC Slow IO Interface	DispY18.sil	K. Pier	Da	7/19/79	18

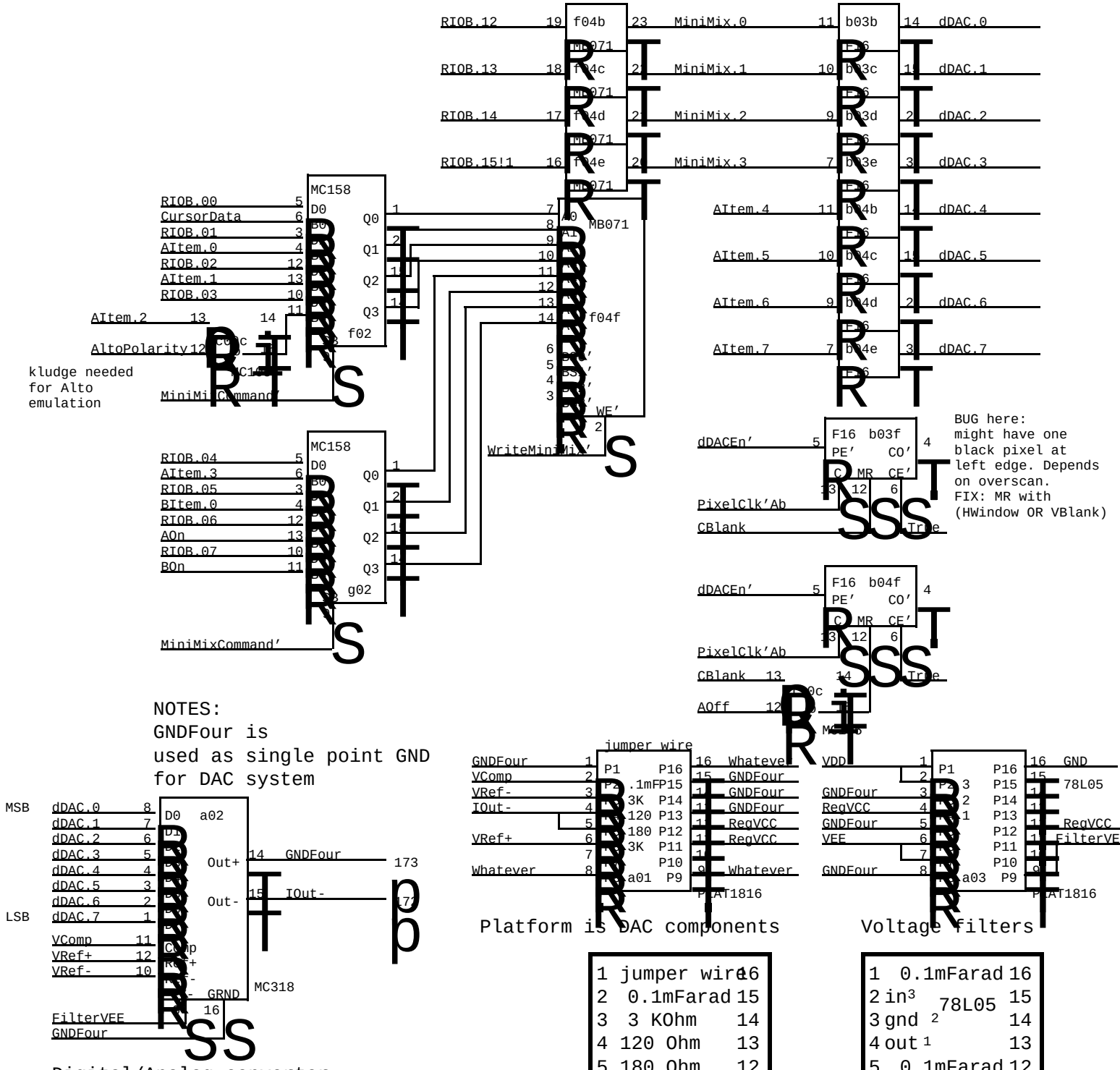




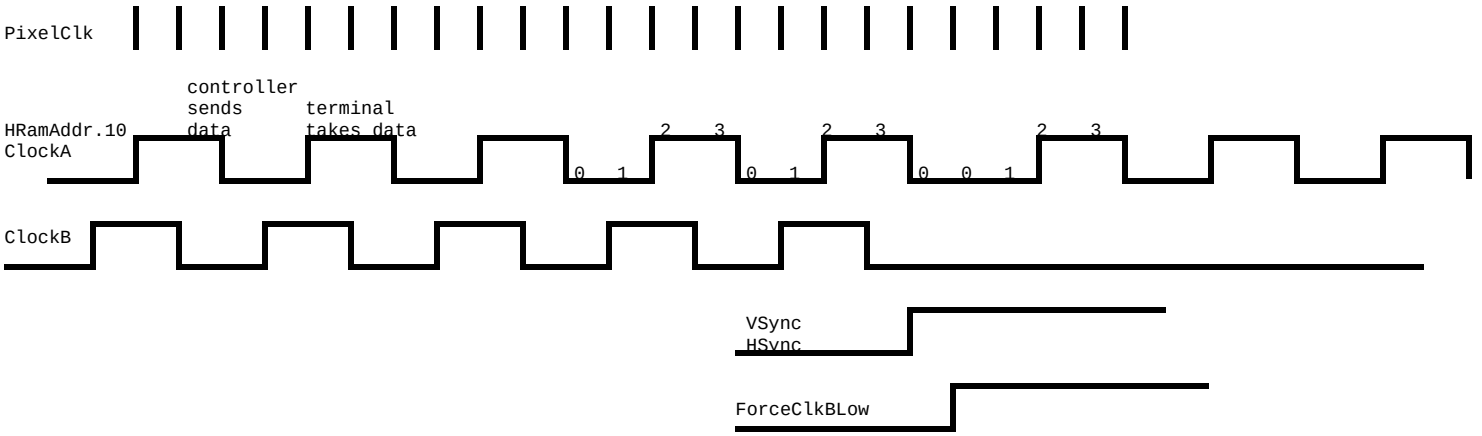




XEROX PARC	Project Dorado	DDC Alto Display Drivers	File DispY19.sil	Designer K. Pier	Rev Da	Date 3/26/81	Page 19

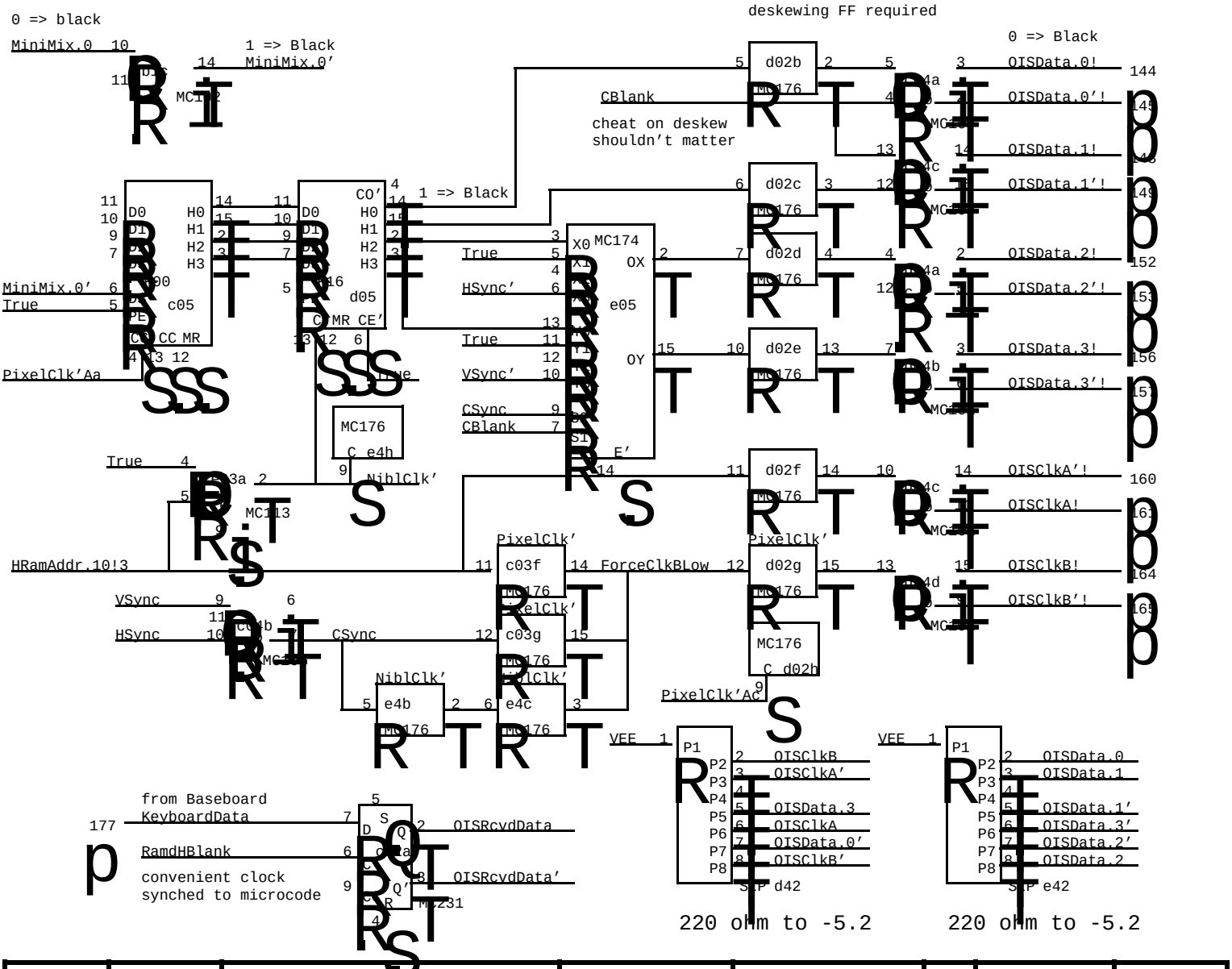


XEROX PARC	Project		File	Designer	Rev	Date	Page
	Dorado	DDC Mini Mixer	DispY20.sil	K. Pier	Da	11/02/79	20

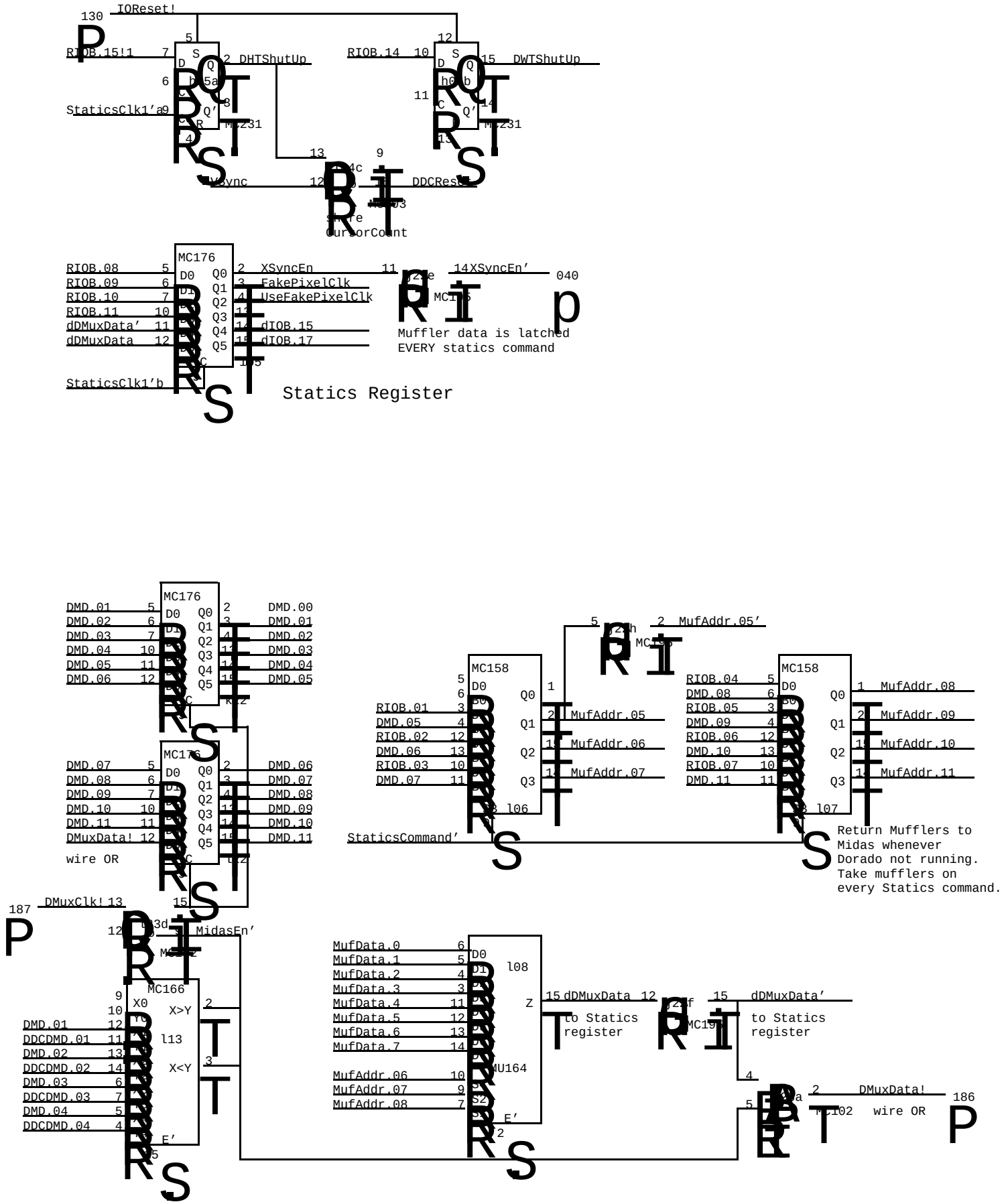


CLAIM: HRamAddr.10 is the waveform for ClockA. Delay it by one pixelclock, and invert, then you get the waveform for ClockB. ClockB is also jammed low by (HSync OR VSync) delayed by one PixelClk. To avoid hiccups in the phasing of ClockA with respect to ClockB, HSync should only be generated just after HRamAddr.10-11=3, that is, a hiccup would occur if HRamAddr.01-11 = 1 just before HSync occurred.

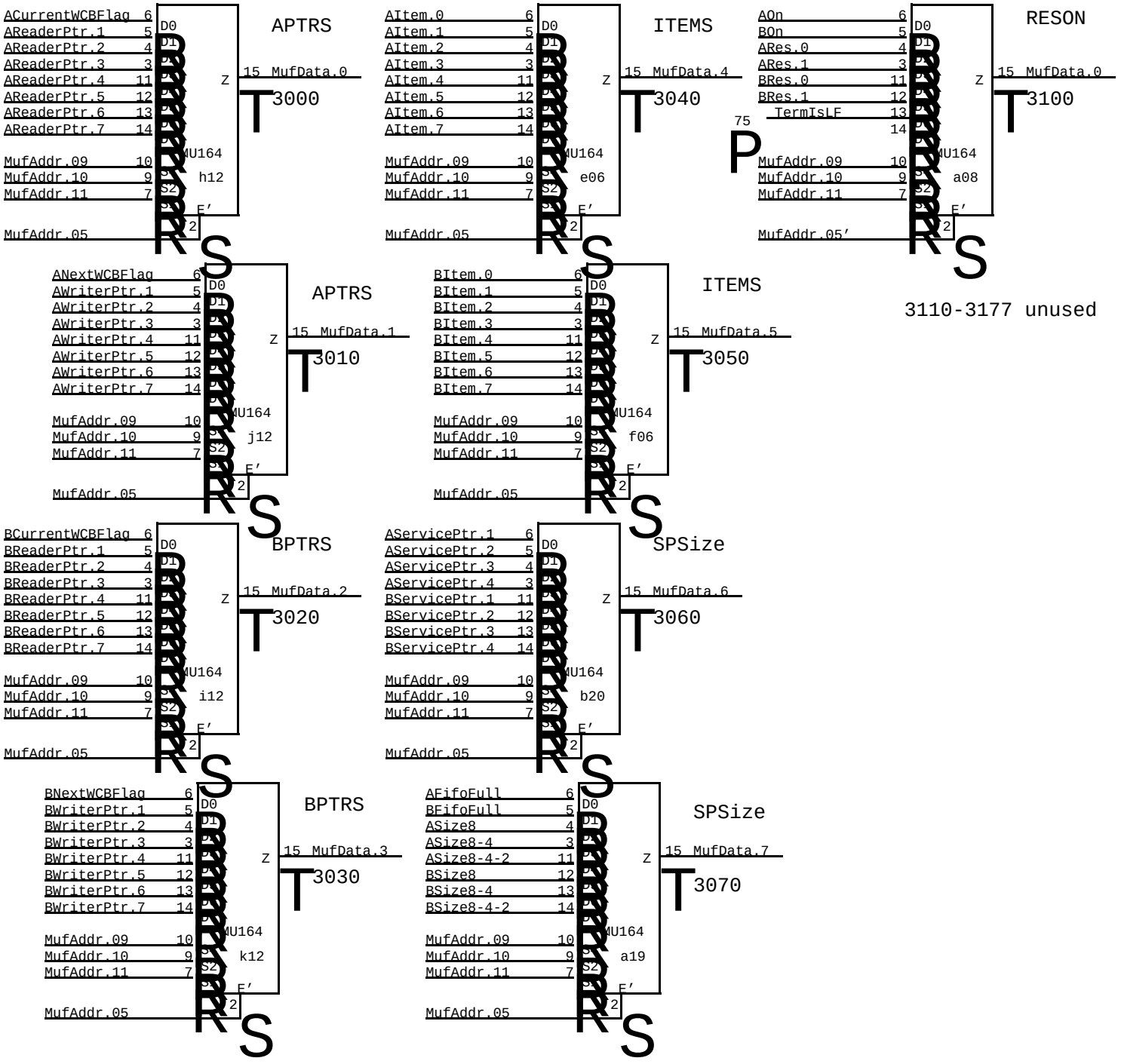
CBlank must be phased so that it changes when HRamAddr.10 goes from 1 to 0. However, CBlank is delayed by two pixel clocks from RamdHBlank, so the HRam must be programmed to make RamdHBlank change on the 0 to 1 transition of HRamAddr.10. This is slightly confusing, so be careful.



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	DispY21.sil	K. Pier	Da	10/29/79	21
	DDC OIS Terminal Interface					

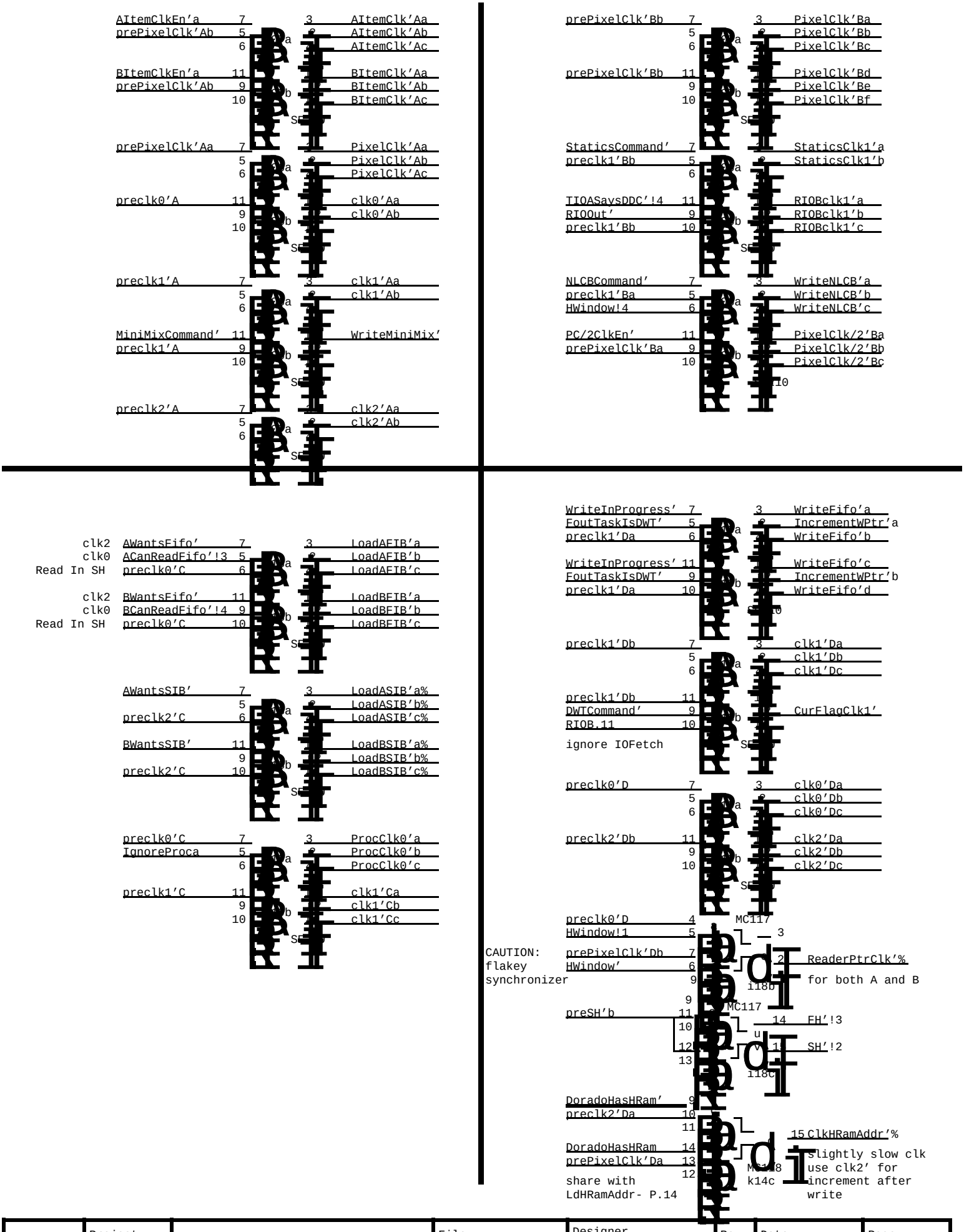


XEROX PARC	Project Dorado	DDC Statics Register and Muffler Control	File DispY22.sil	Designer K. Pier	Rev Da	Date 7/19/79	Page 22

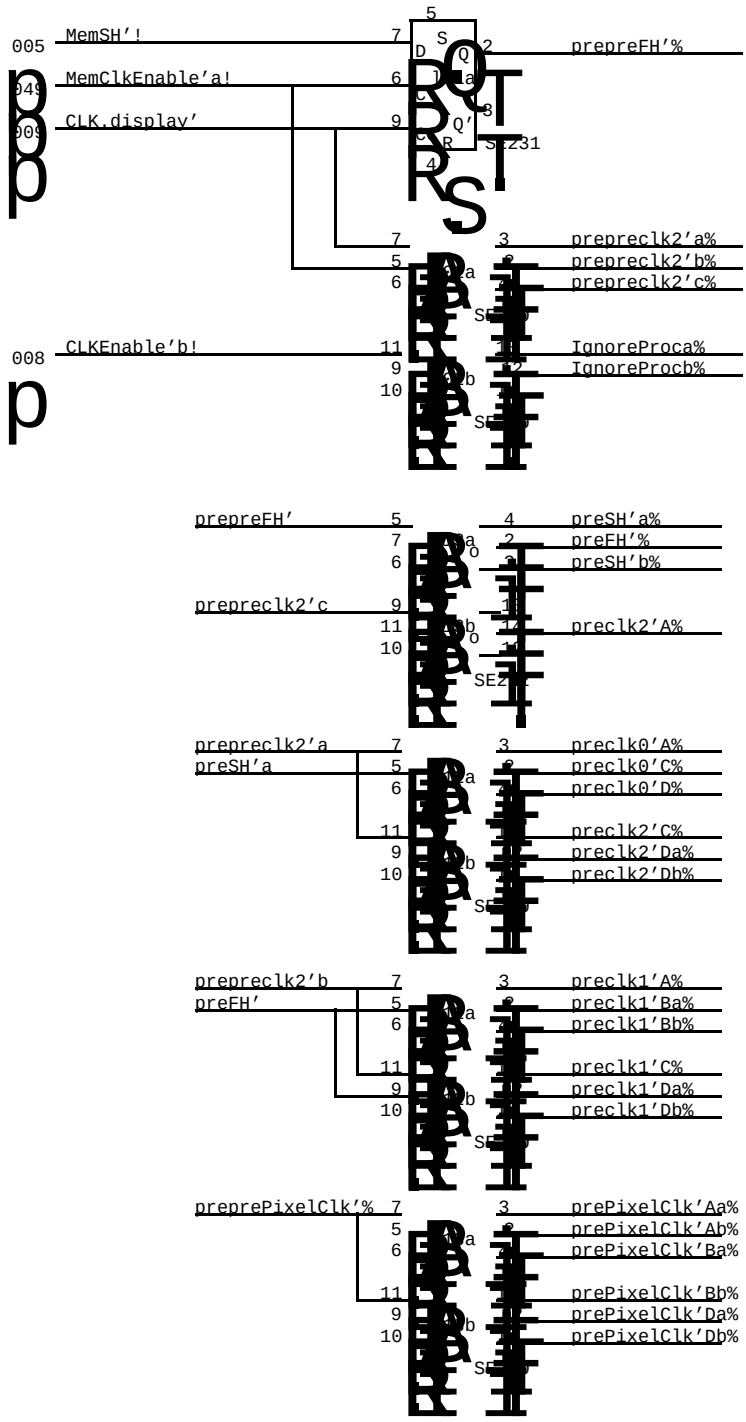


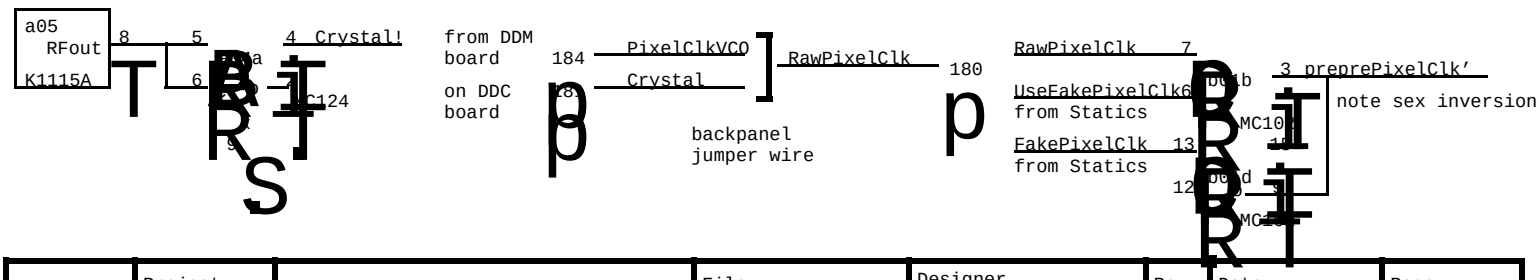
All SIPs are standard 100 ohm terminators with legs broken as shown

XEROX PARC	Project Dorado	DDC Mufflers and SIPs	File DispY23.sil	Designer K. Pier	Rev Da	Date 10/22/81	Page 23



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado DDC Clock Drivers	DispY24.sil	K. Pier	Da	11/29/79	24





XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	DispY25.sil	K. Pier	Da	7/19/79	25

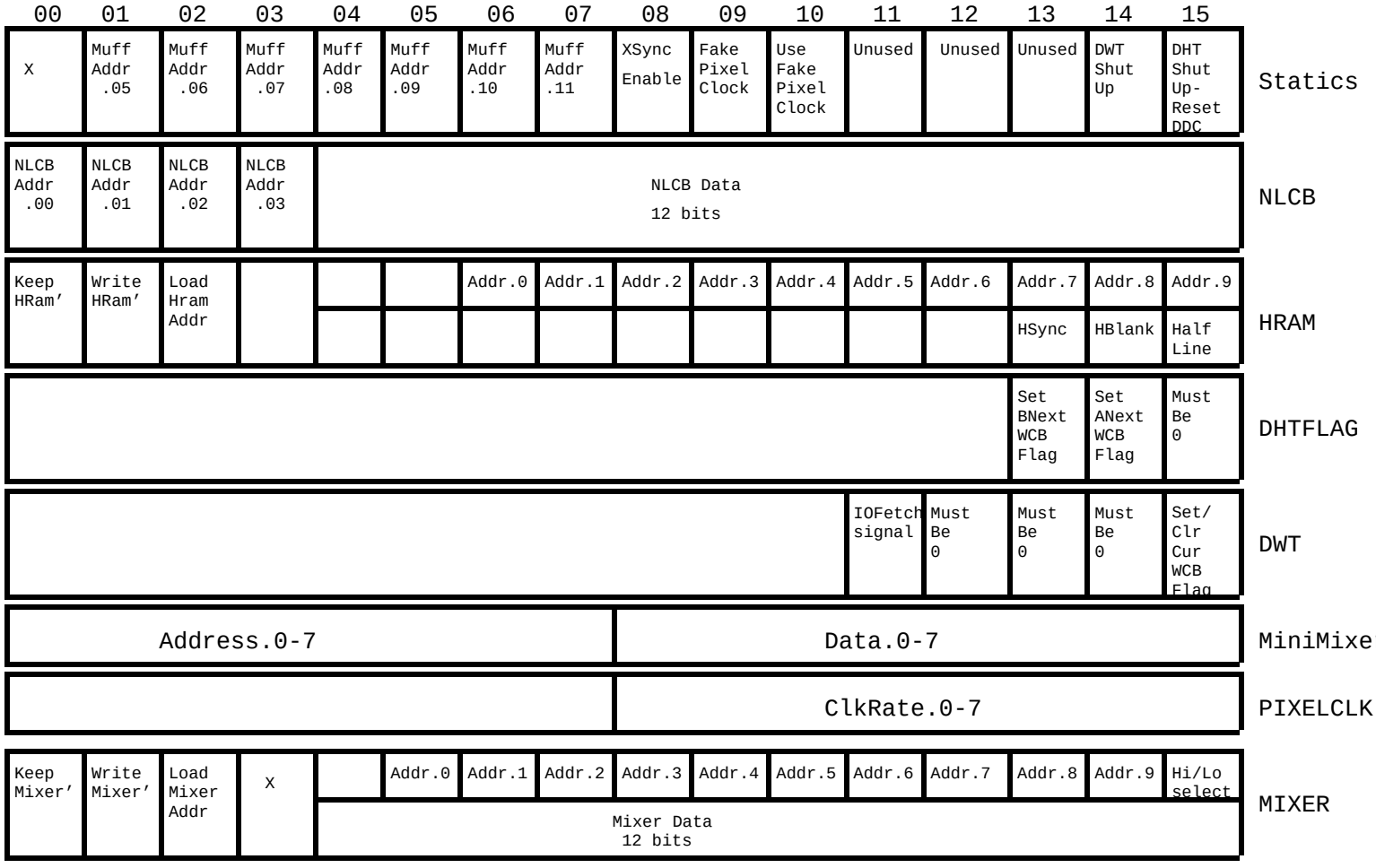
DDC
Pre Clock logic

	CONNECTOR		CONNECTOR		TIOA TW		CONNECTOR		IOBLo	CONNECTOR		IOBHi CLK	
	a 181	b 168	c 153	d 137	e 124	f 109	93 g	80 h	64 i	48 j	33 k	20 l	
1	DAC Plat	PCLK B>Ct 102		TIOA DEF 176 1	TIOA 176 1	DHTTw RdFifo 135	ALTO 74128	ALTO 125	RIOB 176 rc1	RIOB 176 rc1	RIOB 176 rc1	SE231	1
2	DAC 10518			OIS 176	TIOA=D 113	MMMux 158	MMMux 158	NLCB 145 W	DIOB 100	NLCB 145 W	NlcbAd F16 P2	SE210	2
3	DAC Plat	MMix F16 PC	OIS ICEn 176 PC	DWTTw 231 0	TIOA=D 113	ALTO 105	NLCB 145 W	CURSR 141 P	CURSR 141 P	CURSR 141 P	NlcbAd 197	CURSR 141 P	3
4	PCLK 124 BCD	MMix F16 PC	OIS 105	OIS 101	OIS 176	MMix	ClcbEn 161	VSyC 104	CURX F16 P	CURX F16 P	CURX F16 P	CURX 103	4
5	PCLK Xtal	LSR 104	OIS F00	OIS F16	OIS 174	MMix	ClcbEn 161	STAT 231 sc1	STAT 176 sc1		195 RIOB′	CURSR 104	5
6	AdICEN 121	BdICEn 121	PC MMix	0,1	MU AITEM	MU BITEM	ASIZE F16 P2	ARES F16 P2	sc1 rc1	NLCB 1 PC/2		MIDAS 158	6
7	ARESC F16 P	BRESC F16 P	2 210 B	ABITEMCLK	AITEM 104	BITEM 104	BSIZE F16 P2	BRES F16 P2	PC PC		PULSE 195	MIDAS 158	7
8	MU ABOFF OIS RES	LSR 118	ASRC F16 I	BSRC F16 I	AITEM 104	BITEM 104	HWNDO 135 P2	BWDTH F16 P	BWDTH F16 P	BWDTH F16 P	BWDTH 103	MIDAS 164	8
9	ASYNC 231 2	ASYNC 231 2	ASYNC 105	BSYNC 231 2	ASYNC 135 I	BSYNC 135 I	MODE F16 P2	ABOFF 135 P	AWDTH F16 P	AWDTH F16 P	AWDTH F16 P	176 PC P	9
10	ASR I F00	BSR I F00	ASR F00	BSR I F00	ASR I F00	BSYNC 105	VCW F16 P2	BLMarg F16 P	BLMarg F16 P	BLMarg F16 P	BLMarg 105	HRmOut F16 P	10
11	ASR I F00	BSR I F00	ASR I F00	BSR I F00	BSR I F00	BSR I F00	WANT 117	ALMarg F16 P	ALMarg F16 P	ALMarg F16 P	ALMarg 105	AWDTH 103	11
12	ASR I F00	BSR I F00	ASR I F00	BSR I F00	ASR I F00	pc0′ pc2′ SE210	pc1′pc1′ SE210	MU ARP AF	MU BRP BF	MU AWP AF	MU BWP BF		12
13	ASIB 176	BSIB 176	AFIB F00	BFIB F00	BFIB F00	pc2 FHSH SE212	ppc′ ppc′ SE210	HRAddr F16 H	HRAddr F16 H	HRAddr F16 H	HRAddr 103	MIDAS 166	13
14	ASIB 176	BSIB 176	AFIB F00	AFIB F00	BFIB F00	COMM′ 176 1	flags 117	HRam 415 HW	HRam 415 HW	HRam 415 HW	HRamC 118	HRamC 118	14
15	ASIB 176	BSIB 176	AFIB F00	BFIB F00	IP	NFlags 231 1	CFlags 231 cf	DHasHR 231 1,p2	AFULL 149	BFULL 176 1	AFULL 176 1	BFULL 149	15
16	ASIB 176	BSIB 176	AFIB F00	BFIB F00	IP	IP			ARP rpc F16	BRP rpc F16	AWP wpc F16	BWP wpc F16	16
17	ASIB 176	BSIB 176	AFIB F00	BFIB F00	IP	IP	FIFO	FIFO	ARP rpc F16	BRP rpc F16	AWP wpc F16	BWP wpc F16	17
18	ASIB 176	BSIB 176	ABSIB 2 ABSIB 2	ABFIB 0	IP	IP			FHSH rpc 0 117	1, cflg 1	FAM 174	PTRS 103	18
19	MU BA-SZE	ABSize 103	PROC0′ 1′		IP	IP	FIFO	FIFO	fifo 1 wpc 1	2 0	FAM 174	Sync 176	19
20		MU SP	AFIB F00	BFIB F00	IP	IP			FA 2 231	FAM FH 174 SH	FAM 174	IncSP 103 C	20
21			AFIB F00	BFIB F00	IP	IP	FIFO	FIFO	FA 2 231	FA 2 231			21
22	CTDWT 117 C		OIS 231	IP	IP	IP			FA 2 231	d 195	MIDAS 176	MIDAS 176	22
23	102 C	clk0 0 176 FG	GETS 231 1	BLKD B 135 1	ASP 1 F16	BSP 1 F16	FIFO	FIFO	FOUT 1 176	FOUT 1 176	FOUT 1 176	MIDAS 102 BC	23
24	NEXT 113	SUBT 106 A	105	195	WSpace F16 0	HELD 231 0	IOInOut 1660	TIOA=D 161	FOUT 0 176	FOUT 0 176	FOUT 0 176 f	FTsk 113	24
	a 11	b 26	c 39	d 55	e 70	Hold f 86	99 g	114 h	129 i	143 j	159 k	174 l	
	NEXT	SubI BLK	FIN			IOin/out	CONNECTOR		IOR FNXT	FOUT		FTsk DMux	

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	DDC Board Layout	DispY26.sil	K. Pier	Da	3/26/81	26

DDC Slow IO System

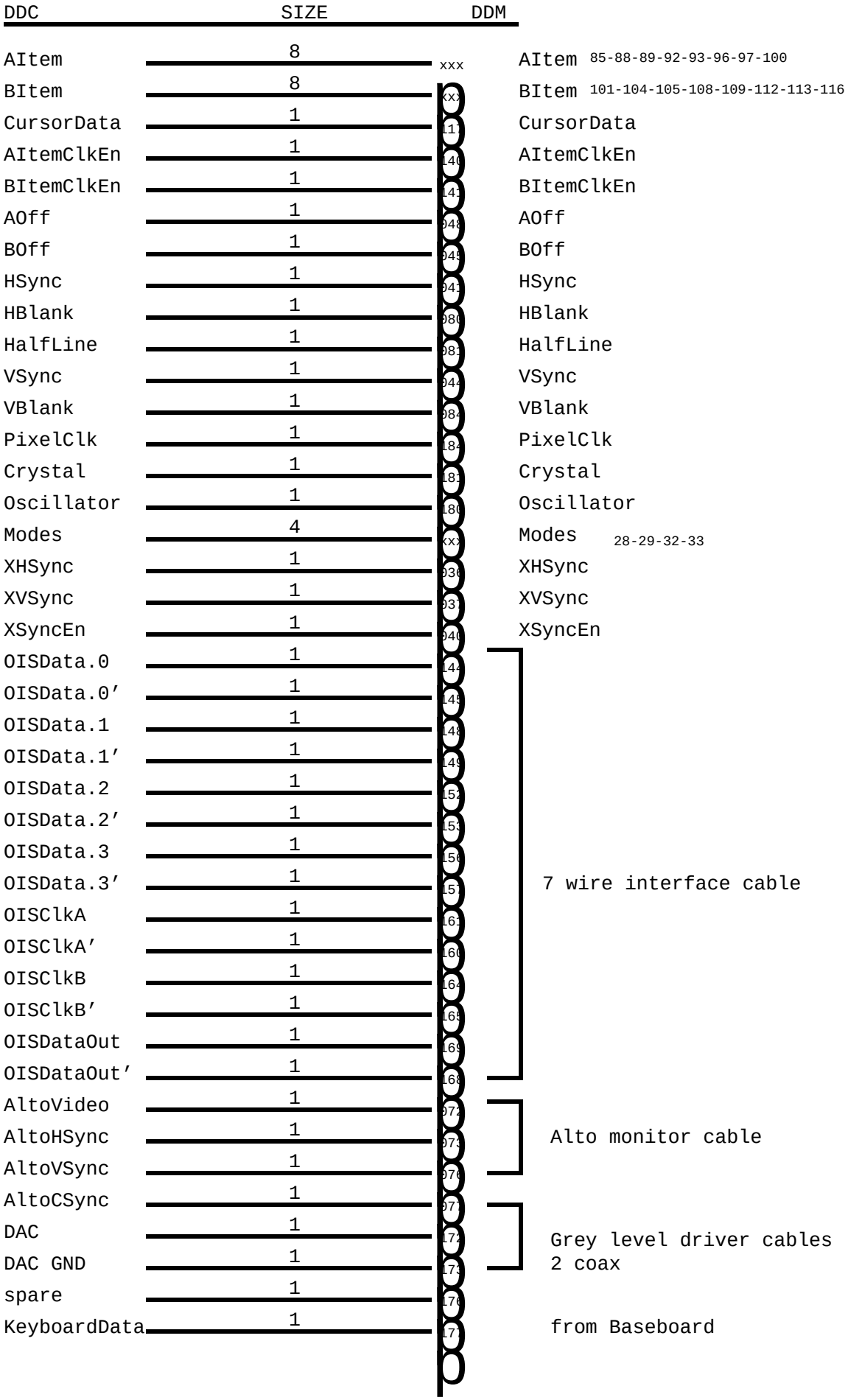
DEVICE	TIOA	I/0	TASK	FORMAT and COMMENTS
STATICS	377	O	DHT, EMU	See Below
NLCB	376	O	DHT, EMU	NLCBAddr.0-3,,Data.4-15
HRAM	375	O	DHT, EMU	Keep,Write,LoadAddr,0,Data.4-15
DHTFLAG	374	O	DHT	....,ANextWCBFlagSet,BNextWCBFlagSet,0 bits 13,14,15
DWT	373	O	DWT	IOFetch signal,....,Set/Clr CWCBFlagANDClrNWCBFlag bit 11, ... , bit 15
MiniMixer	372	O	DHT, EMU	address,,data always writes MiniMixer RAM
STATUS	370	I	DHT, EMU	Selected muffler input returned in bit 15
PIXELCLK	367	O	DHT, EMU	Pixel clock rate located on mixer board
MIXER	366	O	DHT, EMU	Keep,Write,LoadAddr,0,Data.4-15 located on mixer board



XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	DDC Slow IO System Formats	DispY27.sil	K. Pier	Da	7/19/79	27

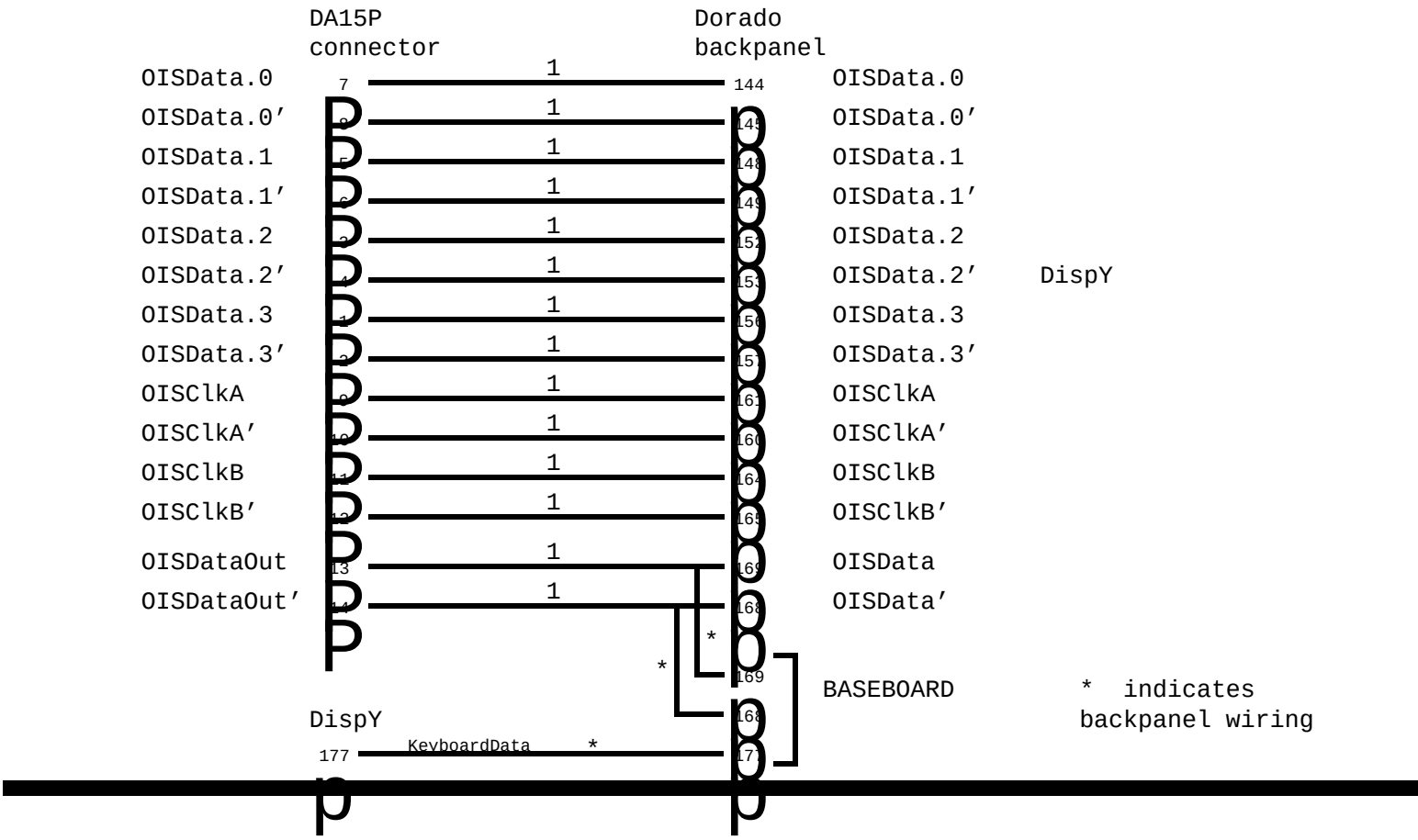
Next Line Control Block Format

Address	Name	Format
0	VCW vertical control word	0...0, VBlank, VSync, EvenField
1	AMargin	LMarg[00..11]
2	AWidth	Width[00..11]
3	AFifoAddr	FifoAddr[0..7] *must be even
4	AScan	0...0,Polarity,Resolution[0..1],Size8,Size4,Size2,S
5	ModeControl	0..0,24Bit,AByPass,BByPass,A8B2
6	reserved	
7	reserved	
10	unused	
11	BMargin	LMarg[00..11]
12	BWidth	Width[00..11]
13	BFifoAddr	FifoAddr[0..7] *must be even
14	BScan	0...0,Polarity,Resolution[0..1],Size8,Size4,Size2,S
15	CursorX	CursorXCount[0..11]
16	CursorLo	CursorLoByte[4..11]
17	CursorHi	CursorHiByte[4..11]

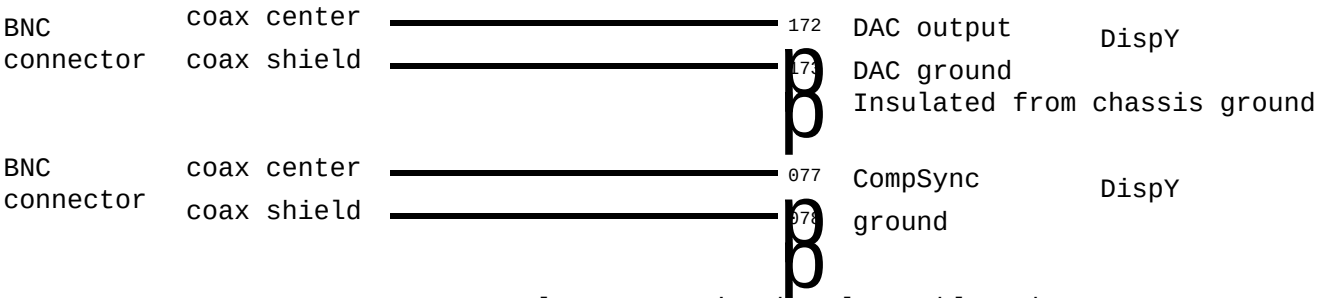


XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	DDC to DDM Interface	DispY29.sil	K. Pier	Da	8/13/79	29

Seven Wire Interface Cable



Grey level cabling



Note: CompSync currently appears in the Alto cable. The Alto display doesn't make use of CompSync. We could simply replace the CompSync pair in the Alto cable with the coax. We then have the capability to attach a local Alto type display and a remote display.

Six BNC connectors mounted on the "square" side. Cabling not yet defined.

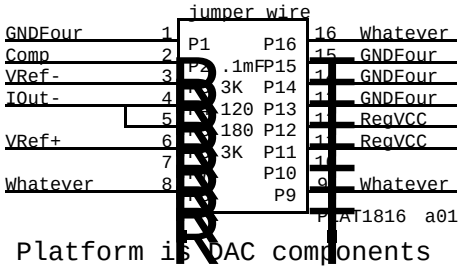
1. Plug an MC10318 D/A converter into location a02 .
2. Plat1816 in locations a01 and b02 are discrete components, shown below.
3. SIPs are 100 ohm terminator package with legs broken:

location	break legs
g41	3,4,5
g42	none
k51	4,5
k52	3

See page 23.

4. SIPs at locations d42 and e42 are 220 ohm value instead of 100 ohm.

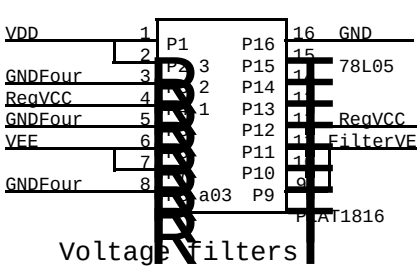
5. Crystal oscillator K1115A, location a05, value 20 MHz.



Platform is DAC components

1	jumper wire		16
2	0.1mFarad		15
3	3 KOhm		14
4	120 Ohm		13
5	180 Ohm		12
6	3 KOhm		11
7			10
8			09

location a01



Voltage Filters

1	0.1mFarad		16
2	in	78L05	15
3	gnd		14
4	out		13
5	0.1mFarad		12
6	12 mHnry		11
7	2 ohm		10
8	+ 22 mF		09

location a03

See Page 20.