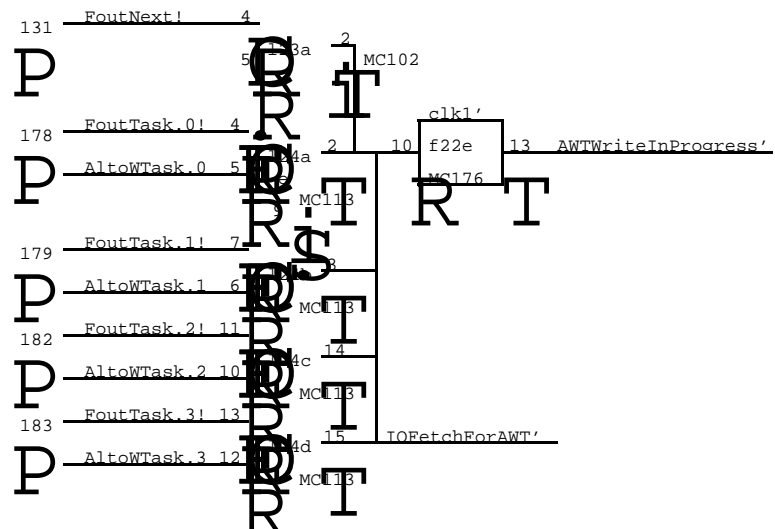
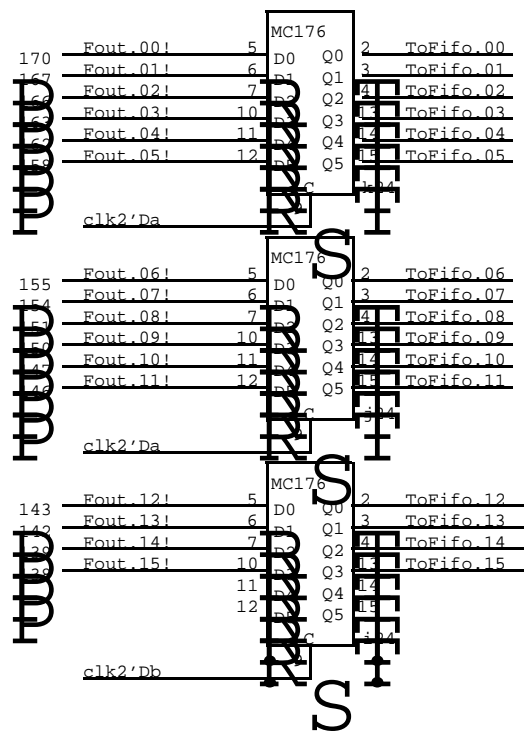
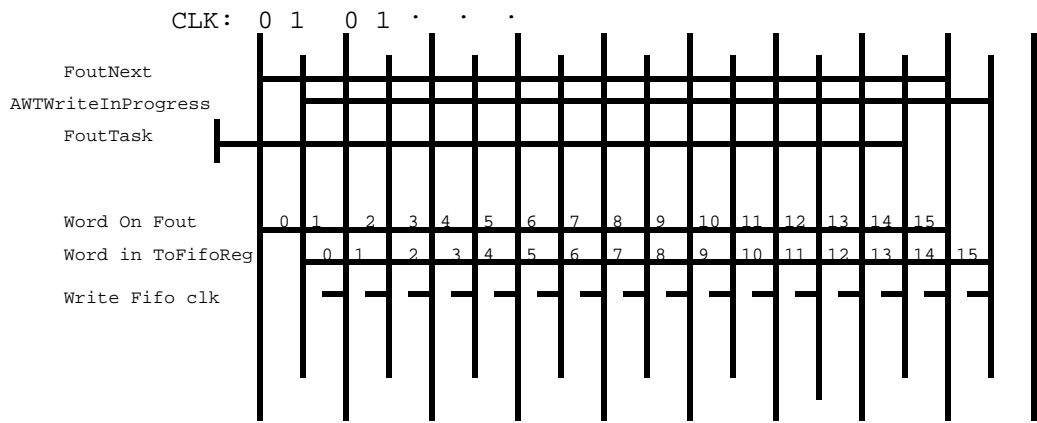


D O R A D O S C H E M A T I C S

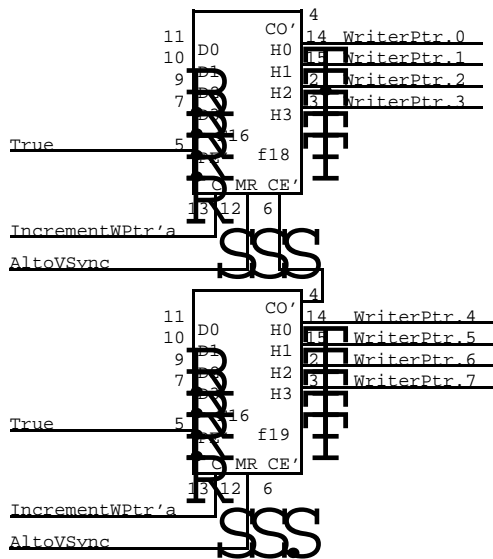
D i s p l a y M

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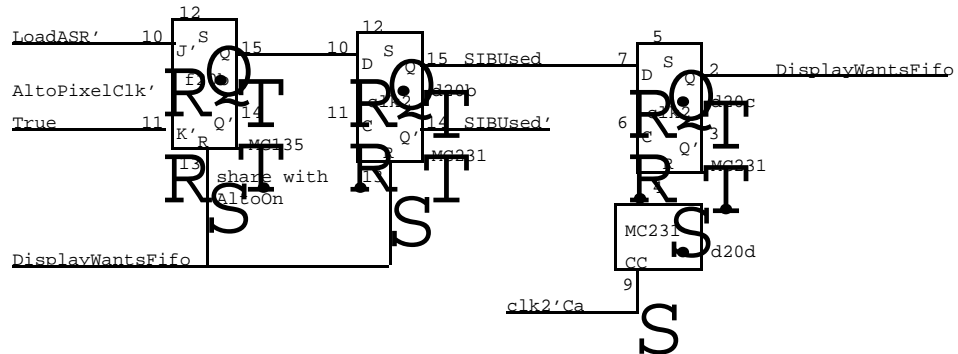
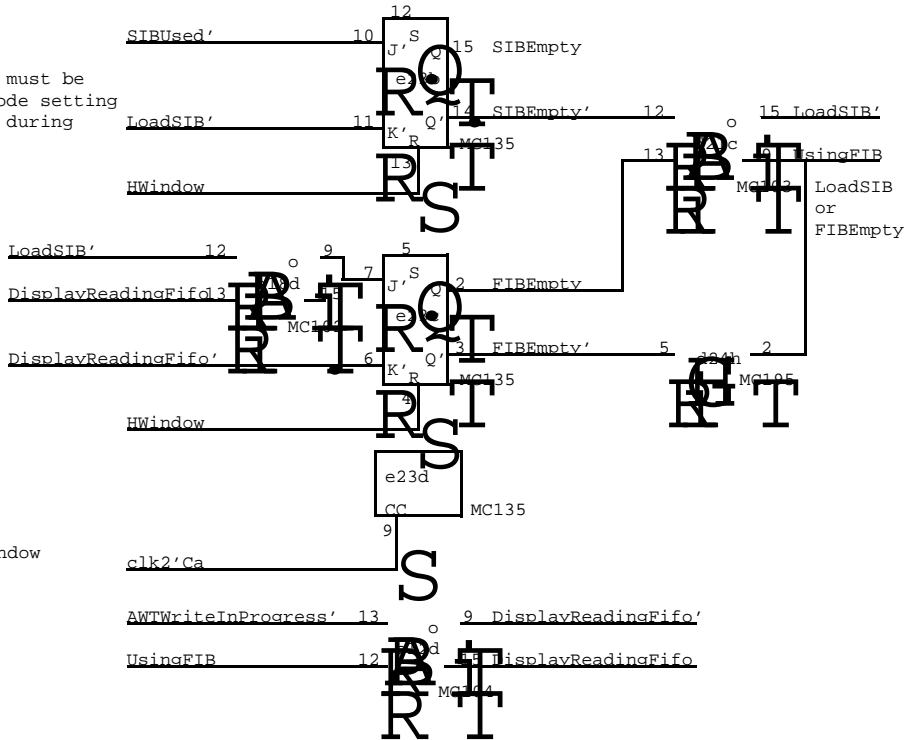
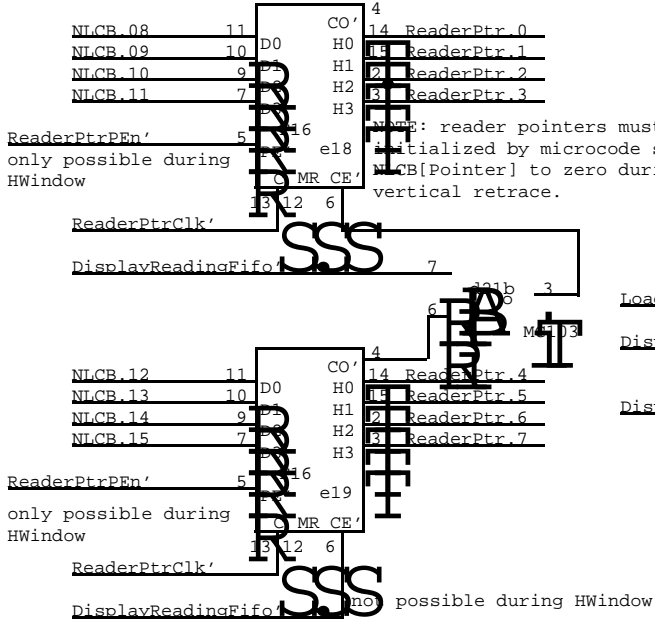
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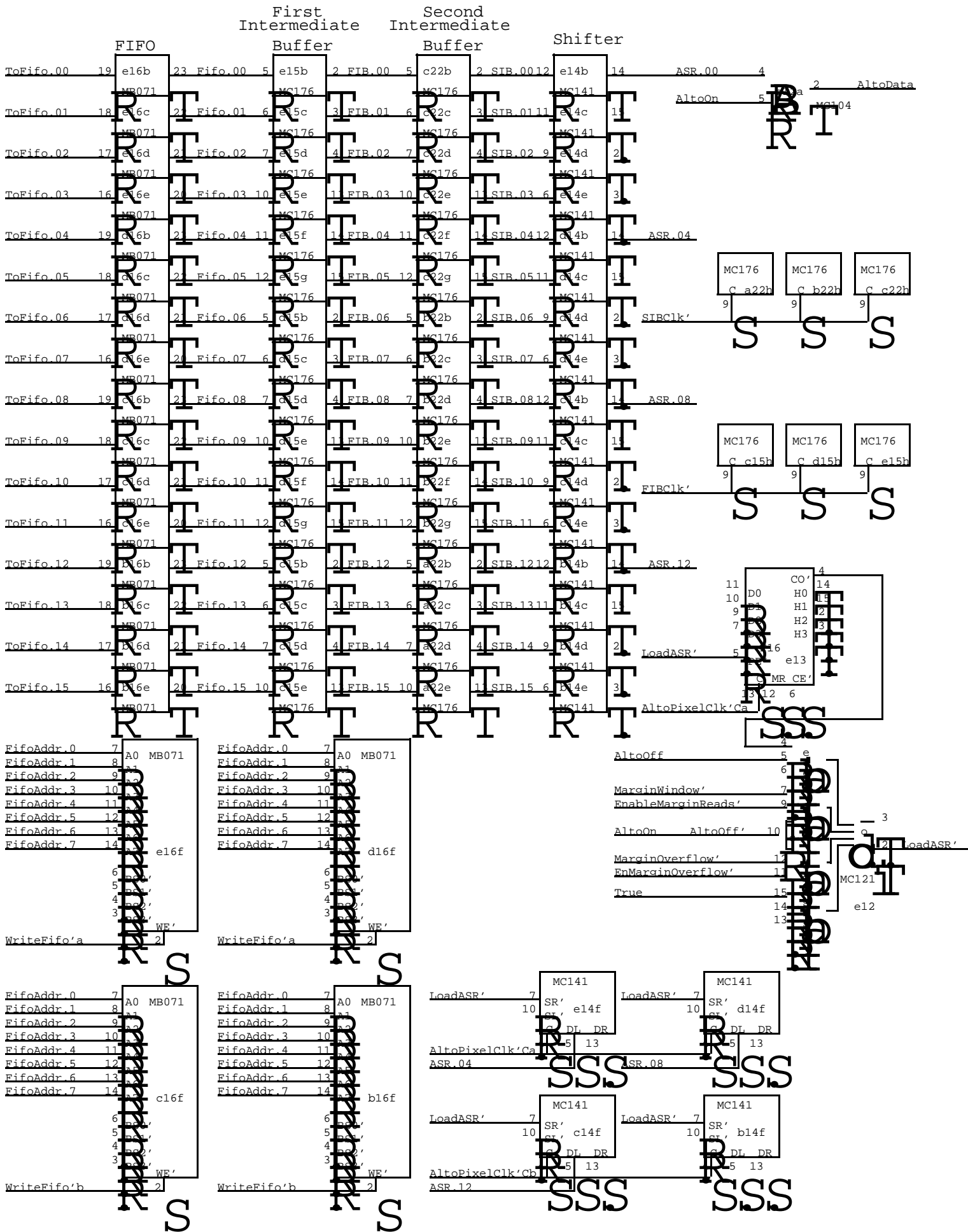


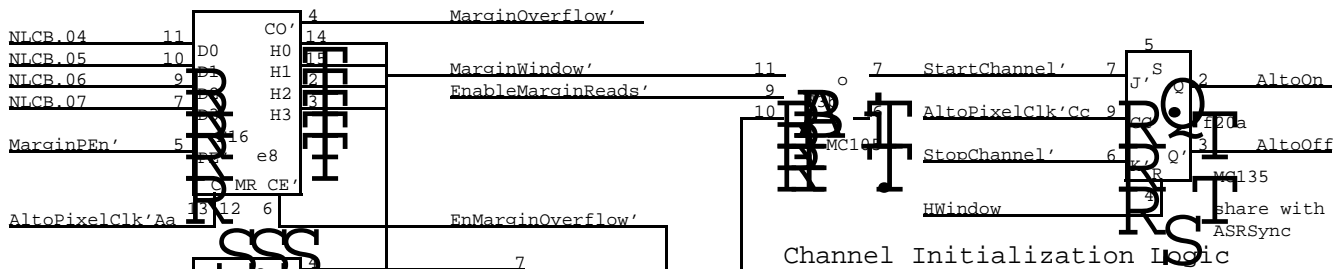
Writer Pointer



Reader Pointer

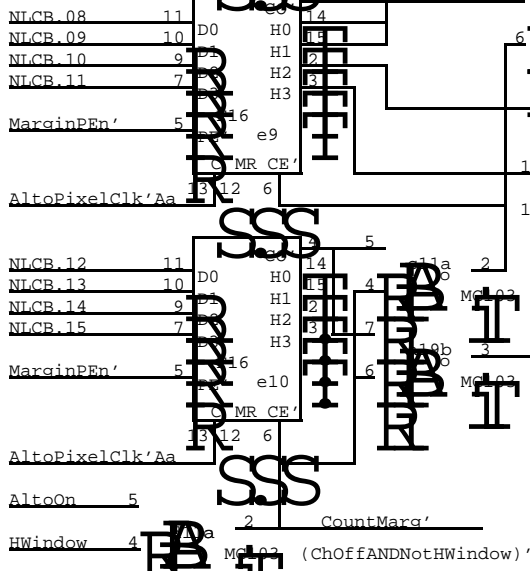




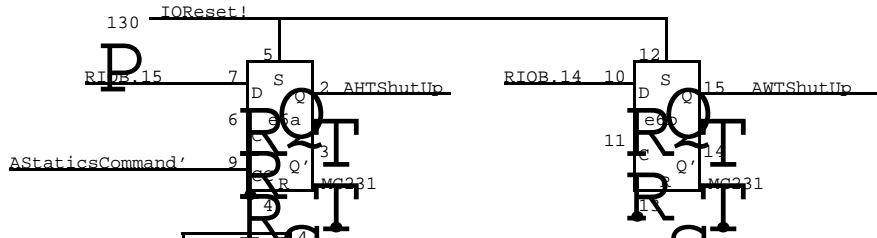


Left Margin Counter

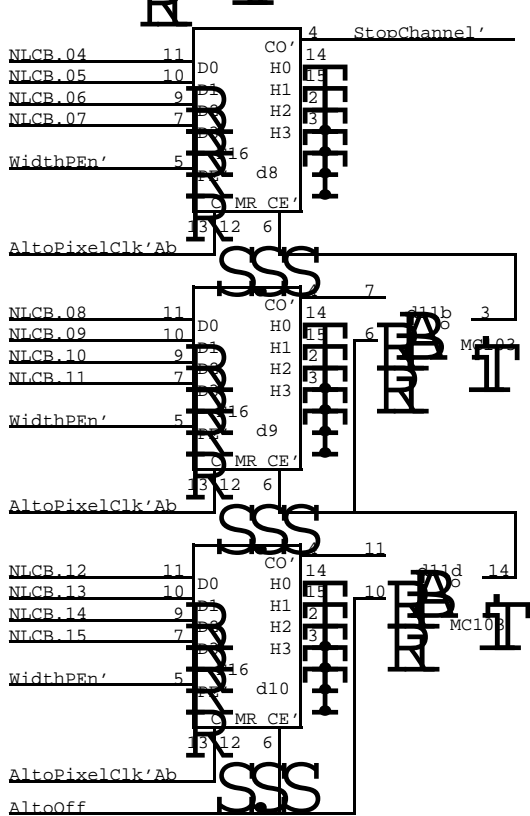
Counter loaded from NLCB. Starts counting after HWindow Overflow => initial read, 37B=>second read, 77B=>third and start the channel. Stop counting while channel is on. Resumes counting when channel goes off, but will not overflow. EnableMarginReads' again before end of scanline.



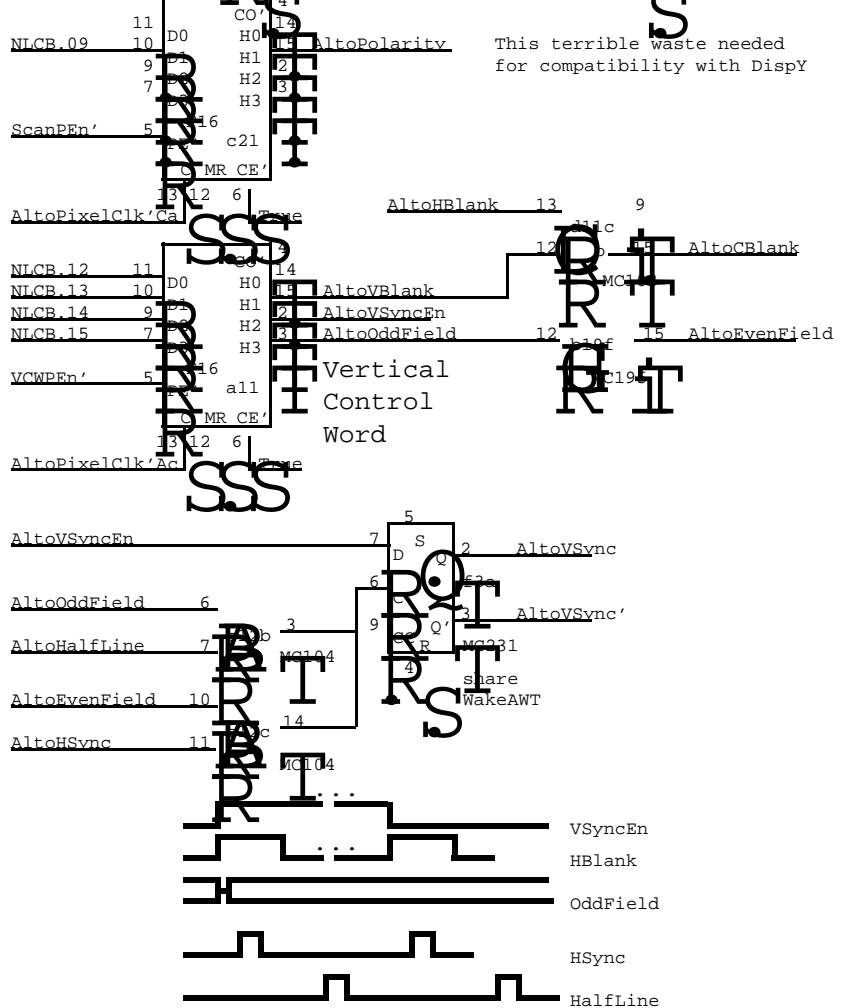
DCB Width Counter
Stop channel when counter value is > 7400B

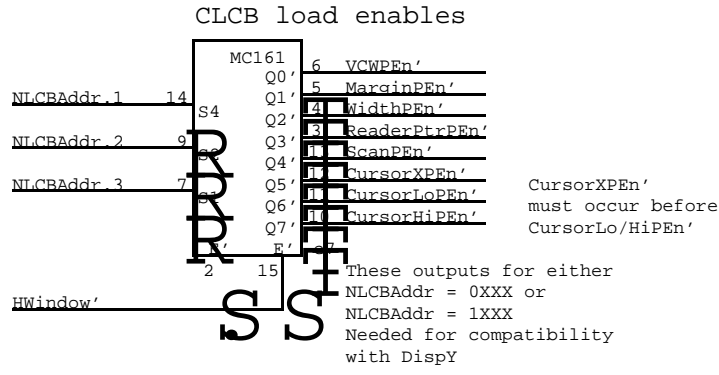
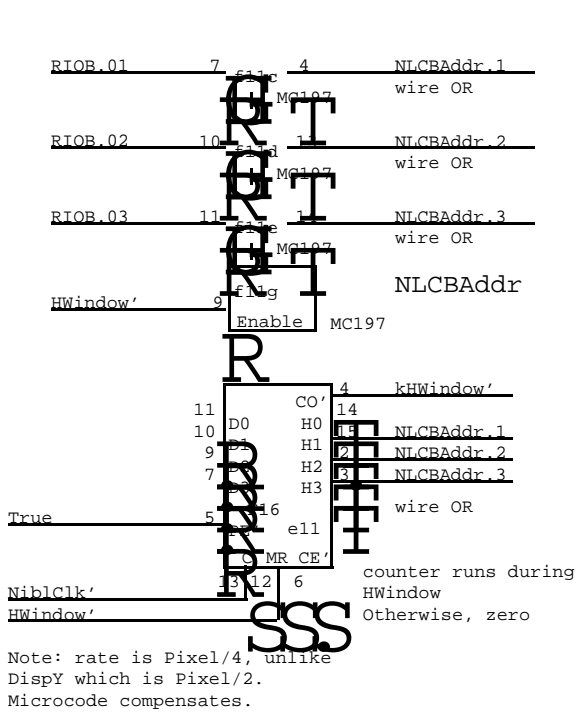


This terrible waste needed for compatibility with DispY

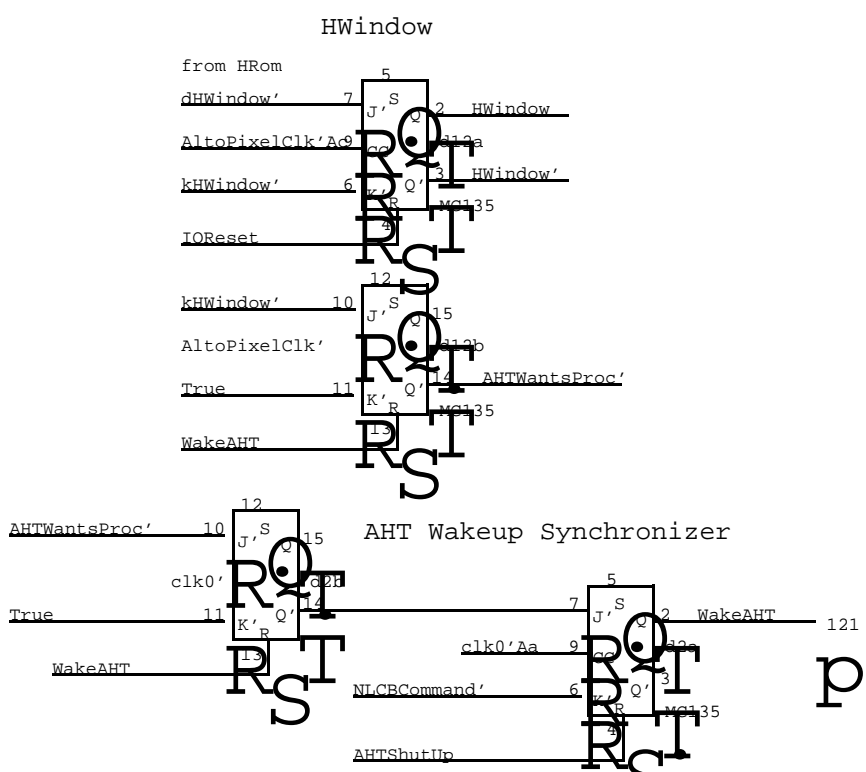
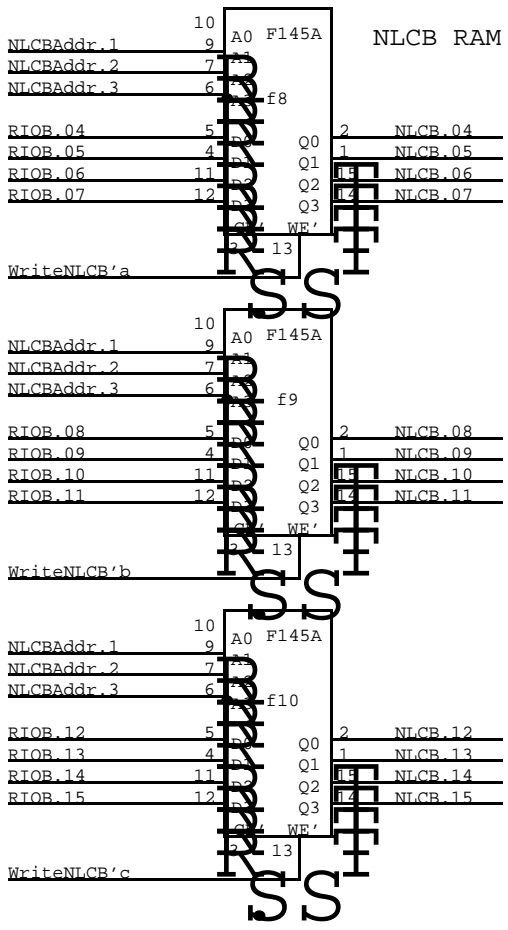


Vertical Control Word



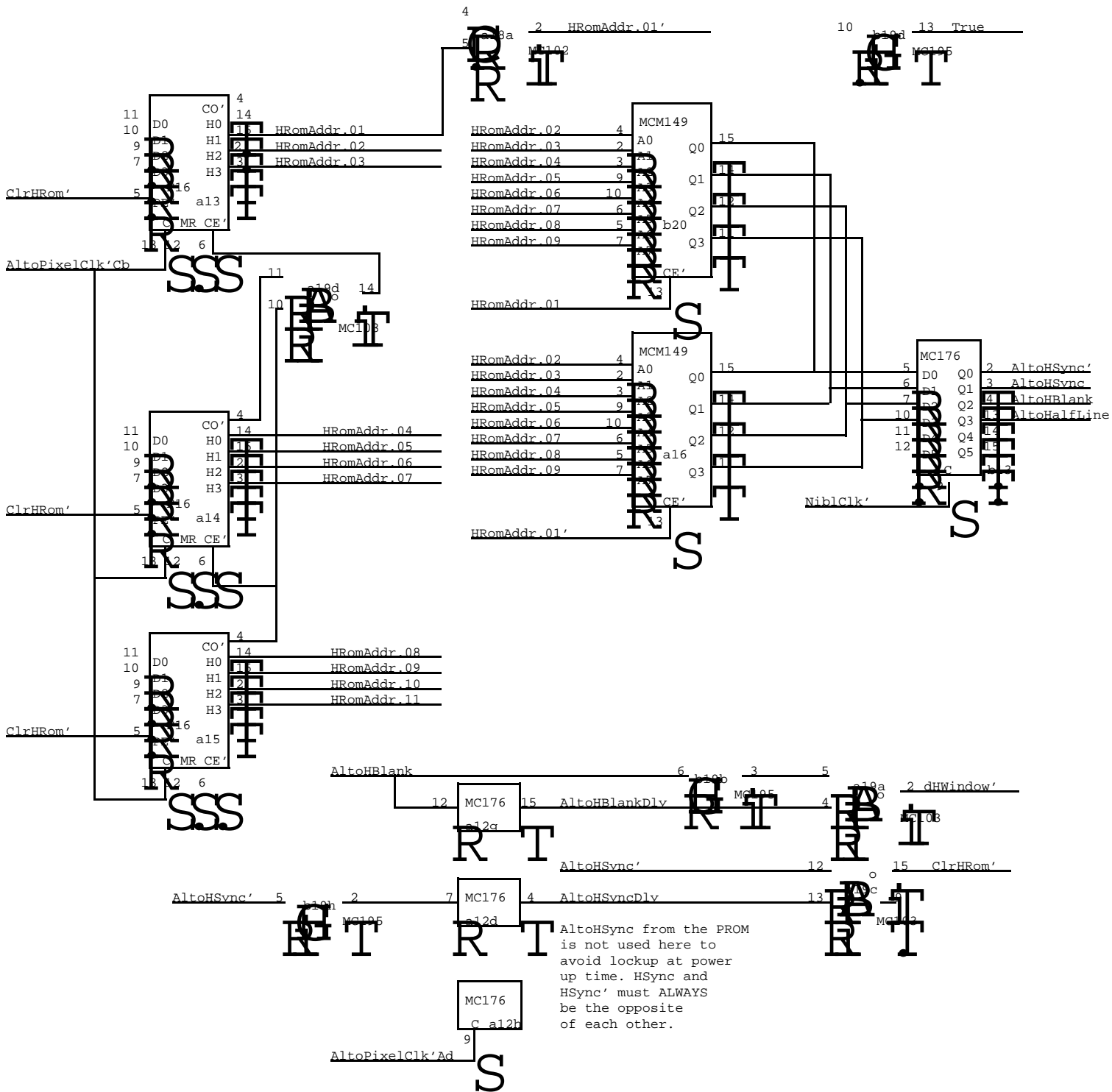


NOTE:
 There are only 8 entries in NLCB.
 The MSB (NLCBAddr.0) is ignored.
 Outputs to 0XXX or 1XXX write words 0XXX of NLCB. During HWindow, CLCB entries are redundantly written twice, first when counter goes 00-07 and again when counter goes 10-17.



For convenience, use NLCBCommand to kill wakeup. Assumes AHT will always do some NLCB command whenever it is awakened. Default would be to redundantly load NLCB[0] with same data.

requires minimum 4 instruction loop



NEXT Word Control Block Flag (NextWCBFlag)
 Current Word Control Block Flag (CurrentWCBFlag)

A Word Control Block is a pair of values called
 Address and MunchCount, for either the CURRENT
 or the NEXT scanline.

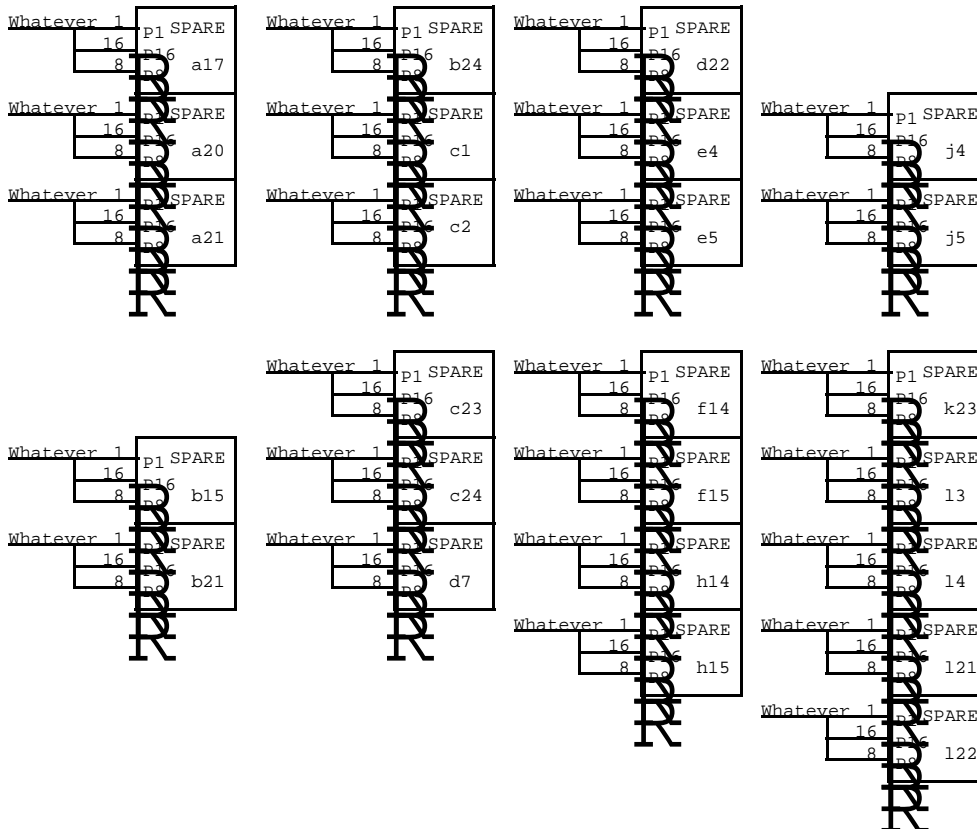
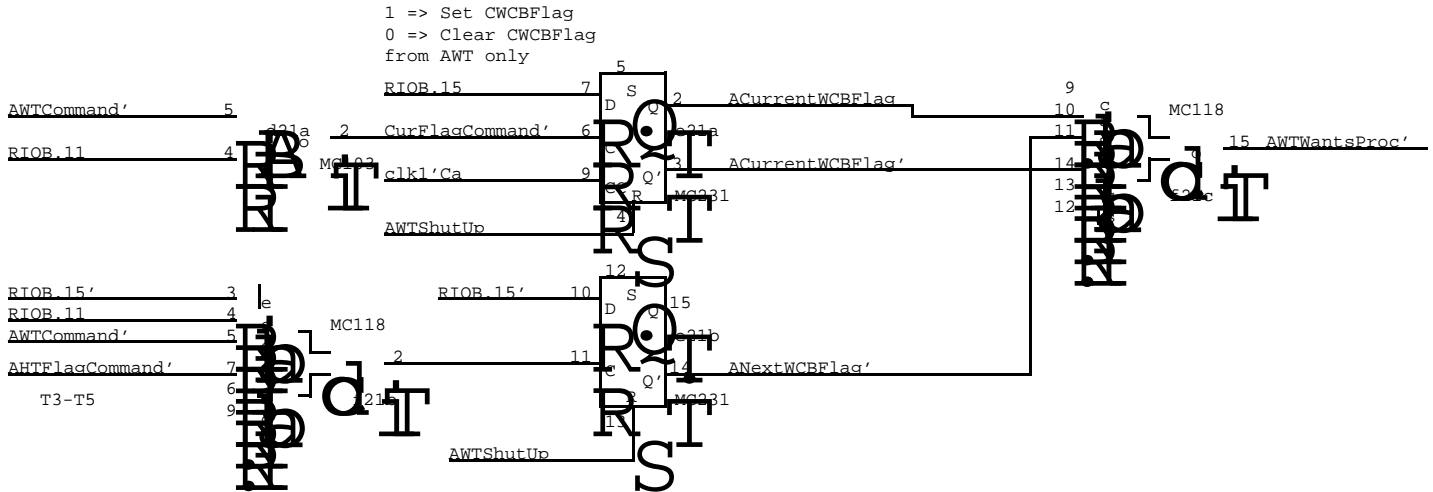
For AWT Commands:		For AHT commands:	
RIOB	Means	RIOB	Means
=1c	Set CWCBFlag and Clear NWCBFlag	=0c	Set ANextWCBFlag
=0c	Clear CWCBFlag		

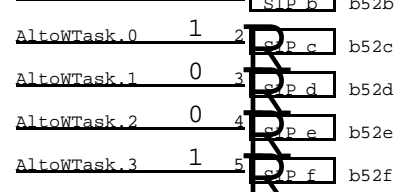
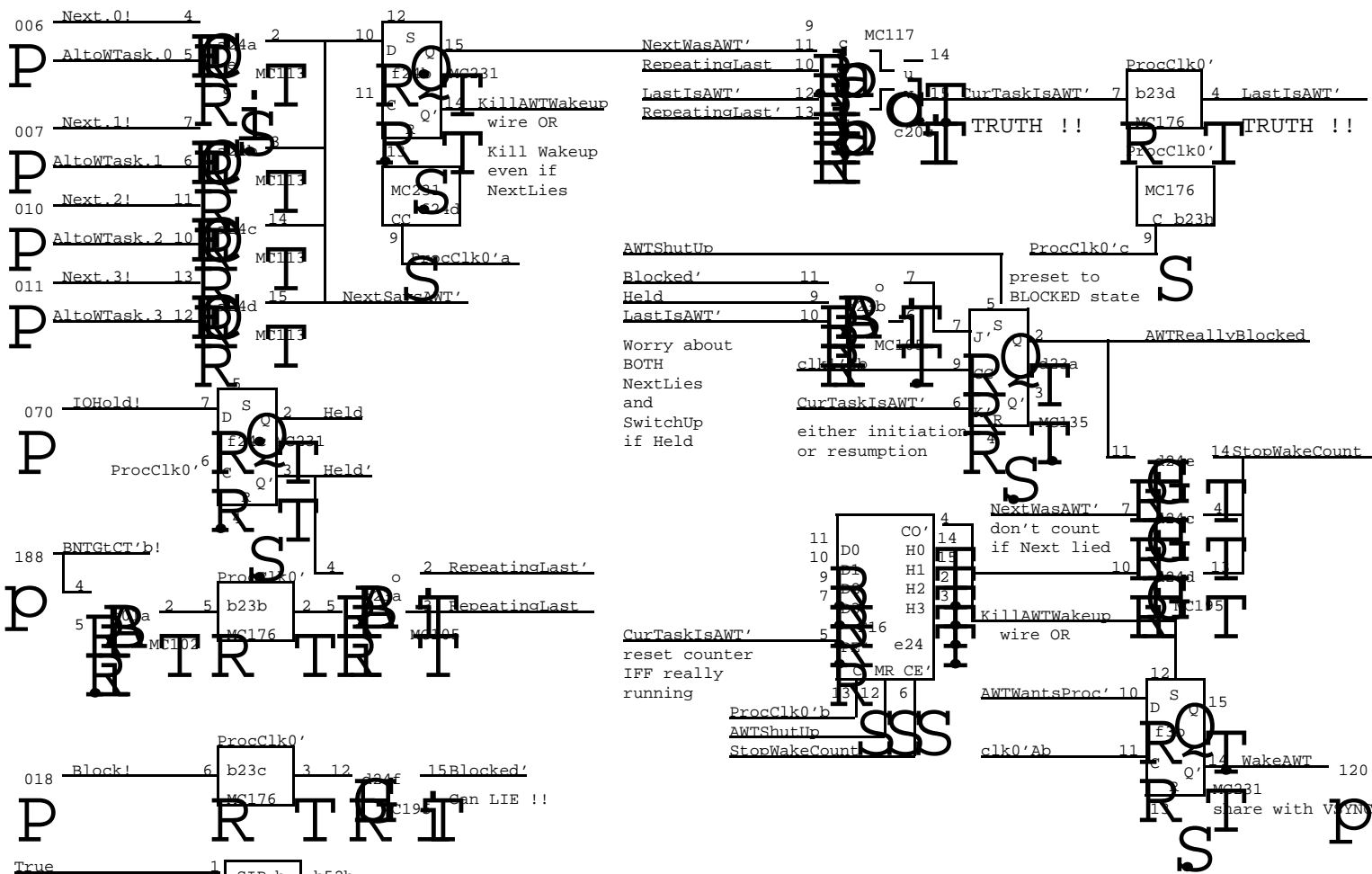
Flag management	SET	CLEARED
	NextWCBFlag	by AHT when it has filled the NextWCB
CurrentWCBFlag	by AWT when it has copied NextWCB into CurrentWCB	by AWT when it has sent out all the data from the CurrentWCB

WakeUp conditions:

WakeAHT: at end of every HWindow

WakeAWT: (CurrentWCBFlag) OR (NextWCBFlag AND NOT(CurrentWCBFlag))

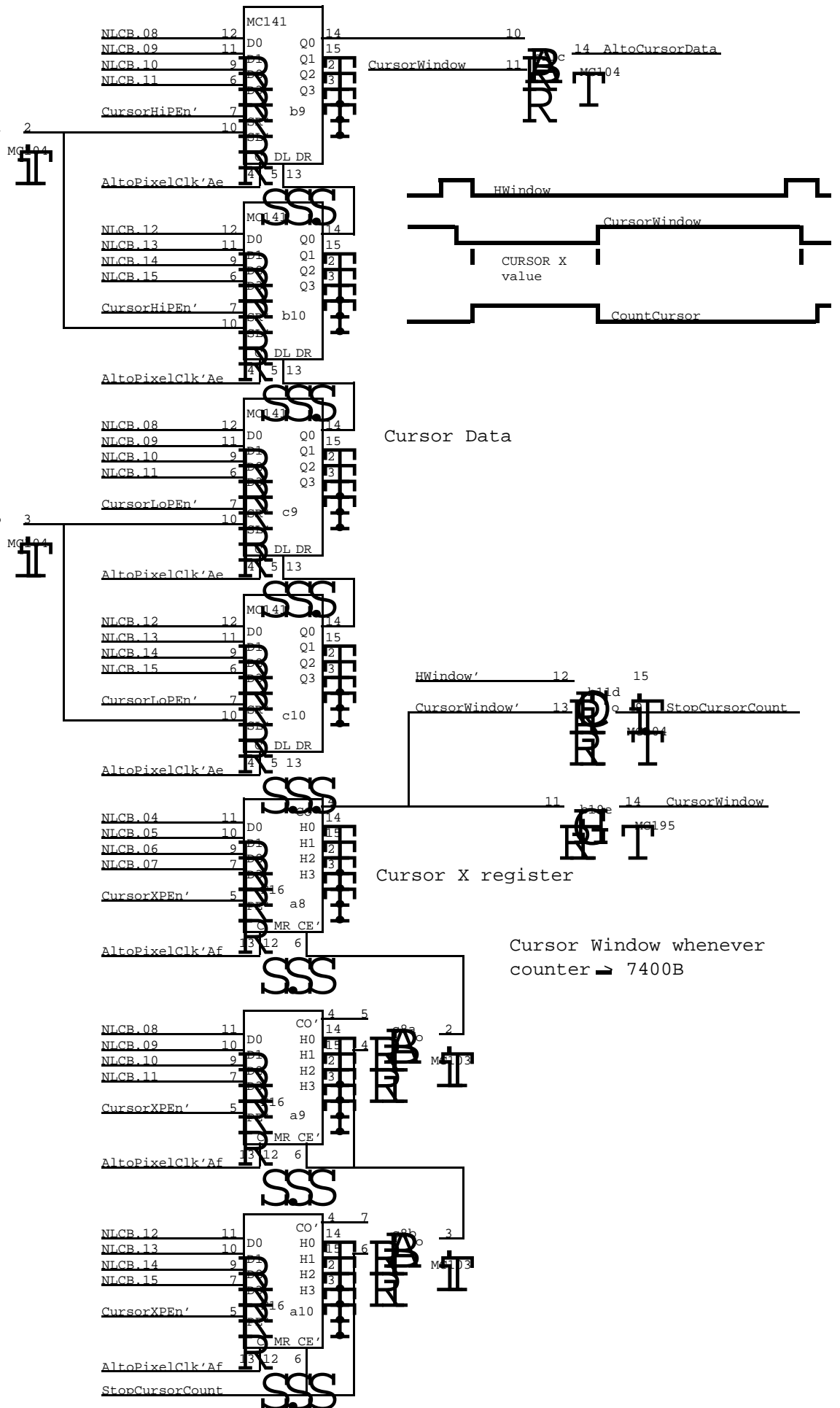




For AWT Task = 11B
cut legs 3 and 4

CursorHiPEn' 5
 CursorWindow' 4
 during HWindow
 CursorWindow must
 go inactive
 before loading
 CursorHi/lo with
 new data, so
 CursorX is loaded
 before CursorHi/Lo

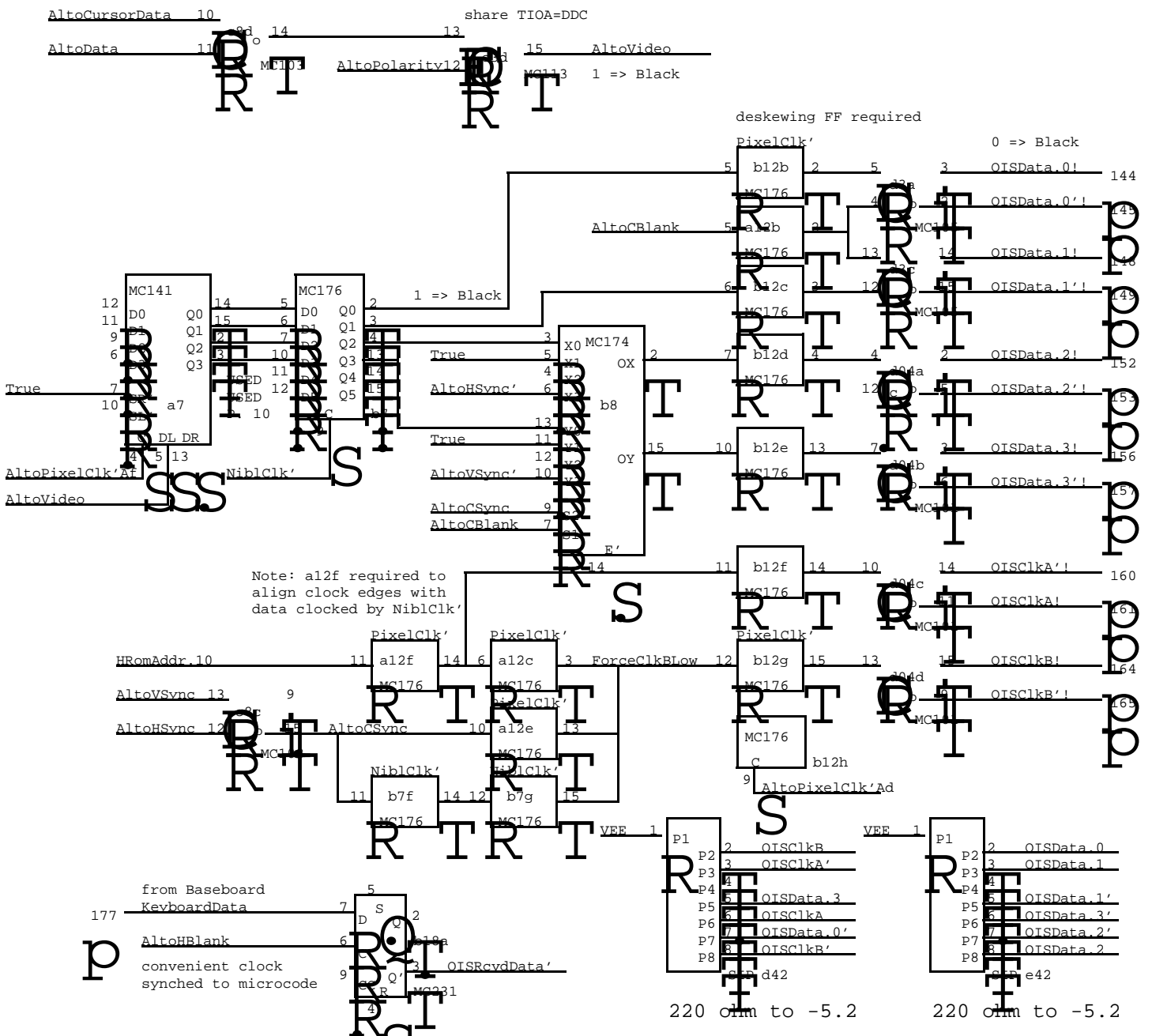
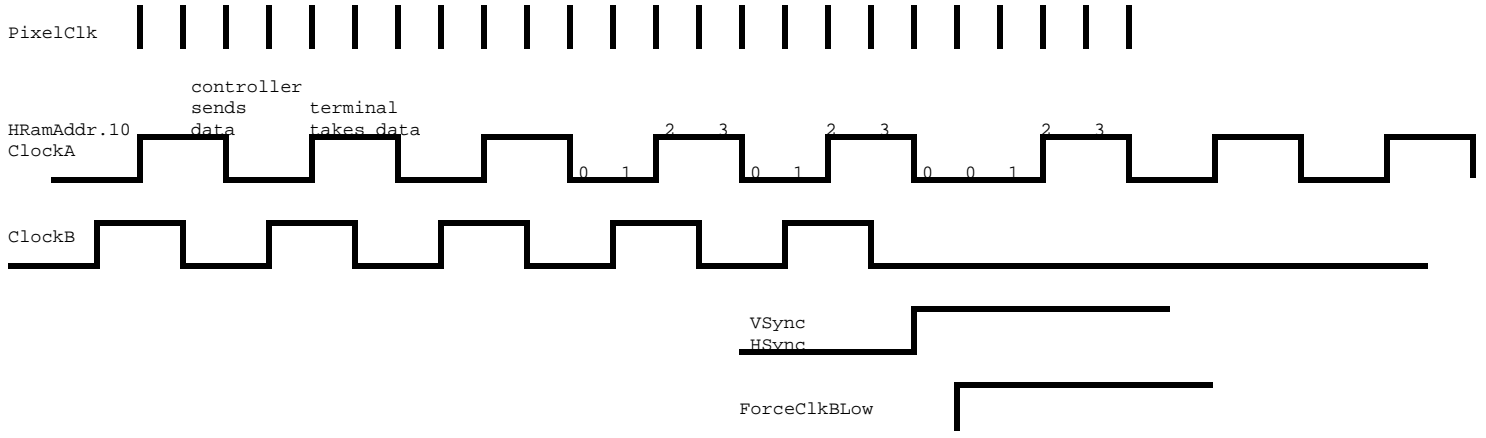
CursorLoPEn' 7
 CursorWindow' 6



Cursor Data

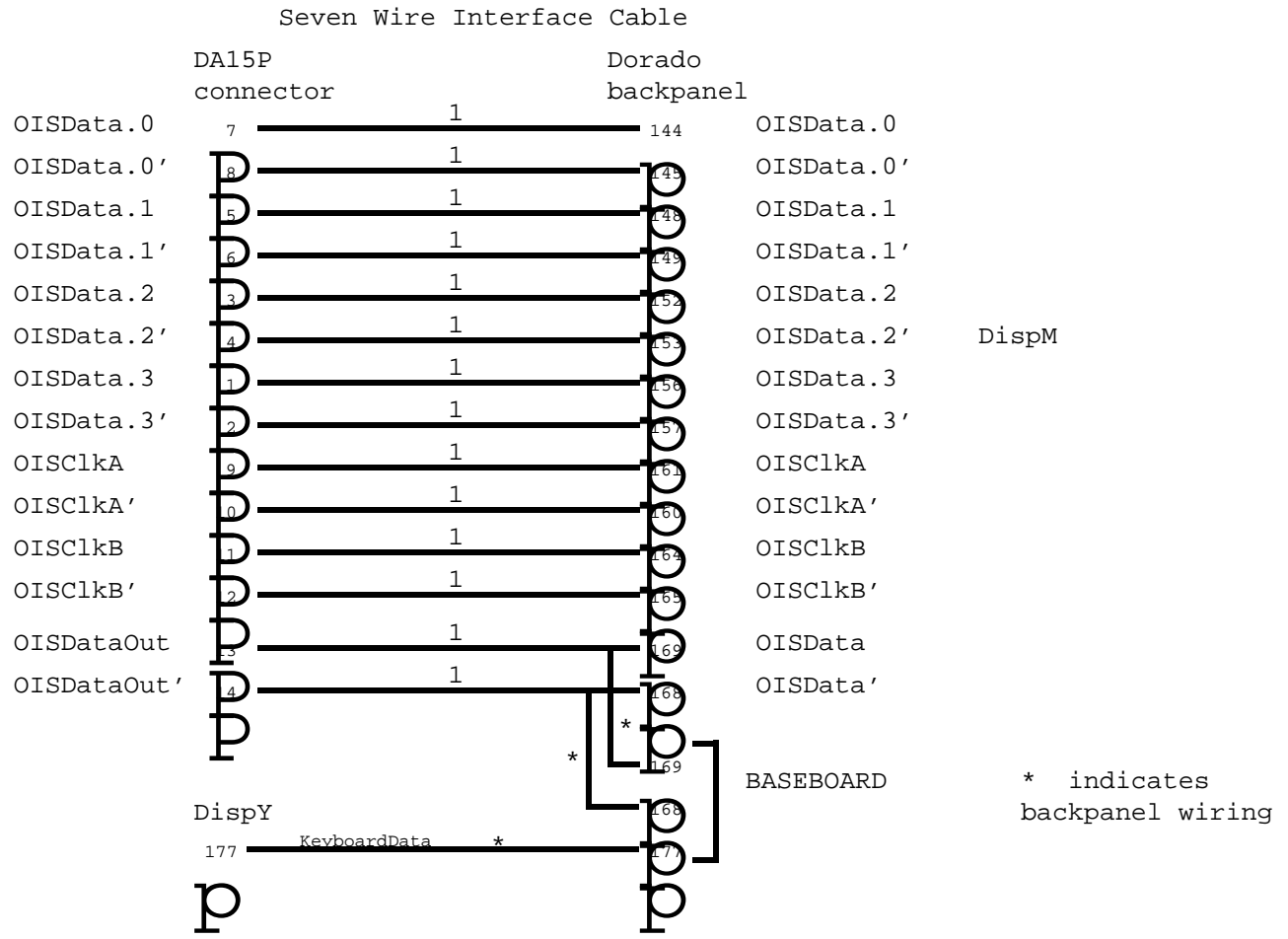
Cursor X register

Cursor Window whenever counter → 7400B

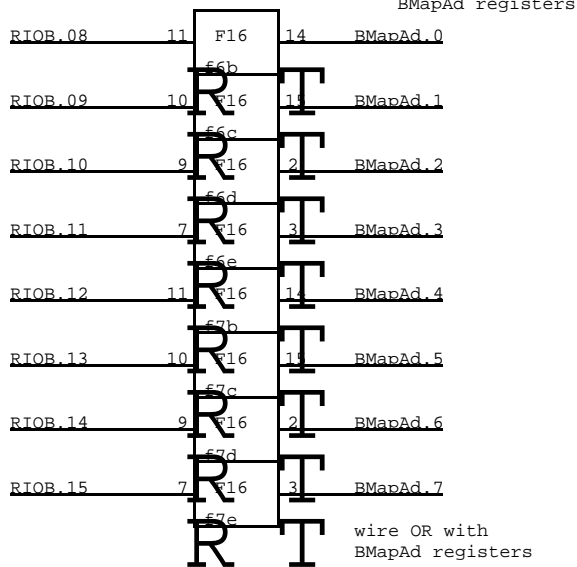


Alto Display Controller
Next Line Control Block Format

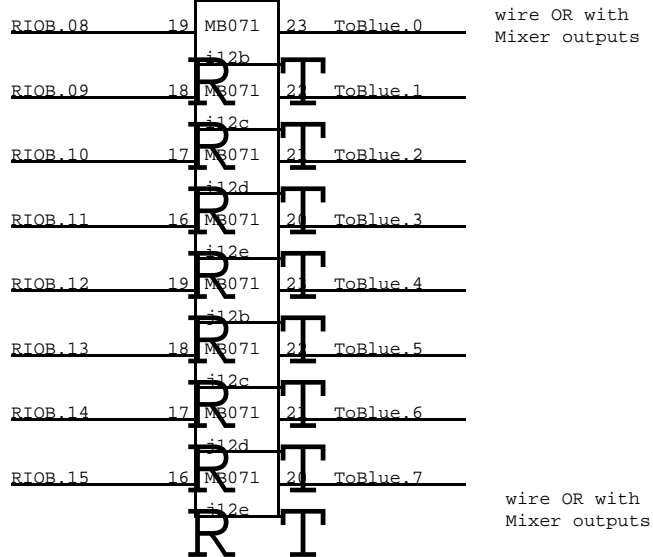
Address	Name	Format
0	VCW vertical control word	0,..0, VBlank, VSync, OddField
1	Margin	LMarg[00..11]
2	Width	Width[00..11]
3	FifoAddr	FifoAddr[0..7] *must be even
4	Scan	AltoPolarity,0,0,0,0,0,0,
15	CursorX	CursorXCount[0..11]
16	CursorLo	CursorLoByte[4..11]
17	CursorHi	CursorHiByte[4..11]



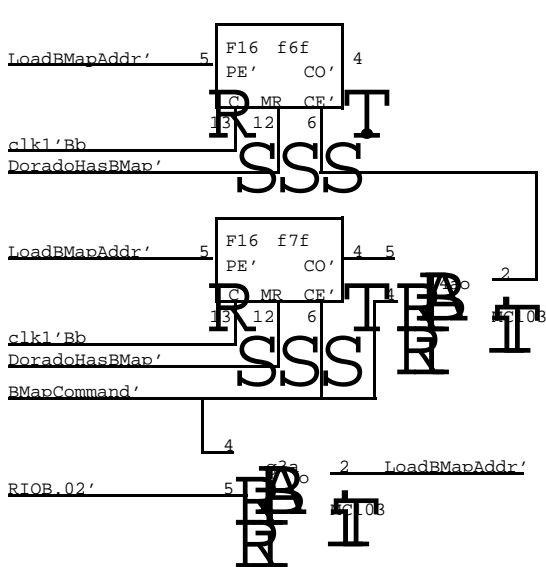
Dorado BMap address wire OR with BMapAd registers



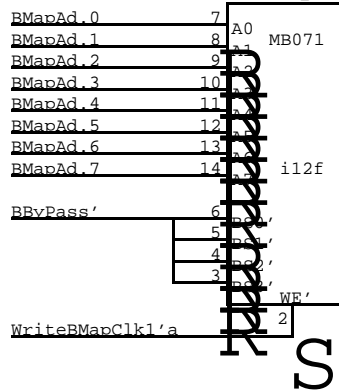
B Map



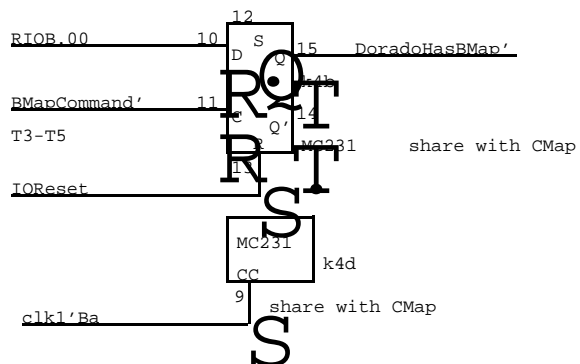
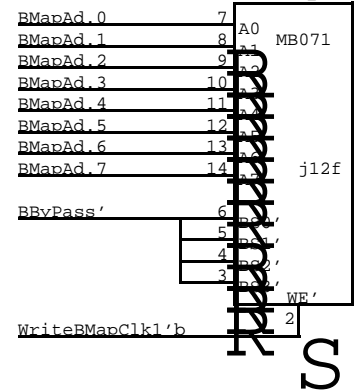
Dorado BMap address



B Map

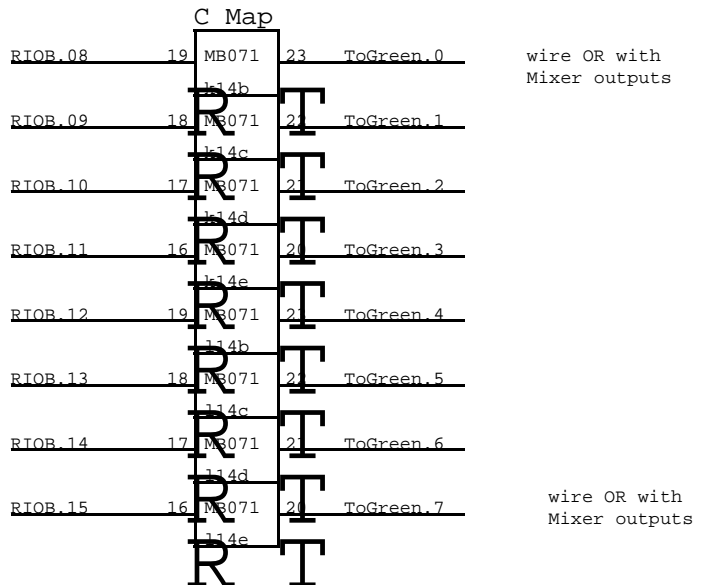
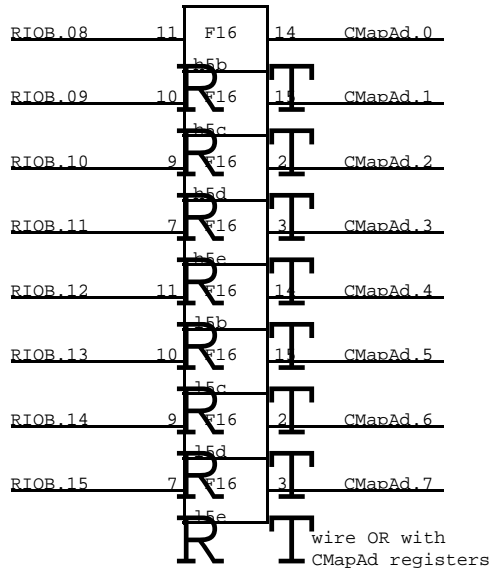


B Map

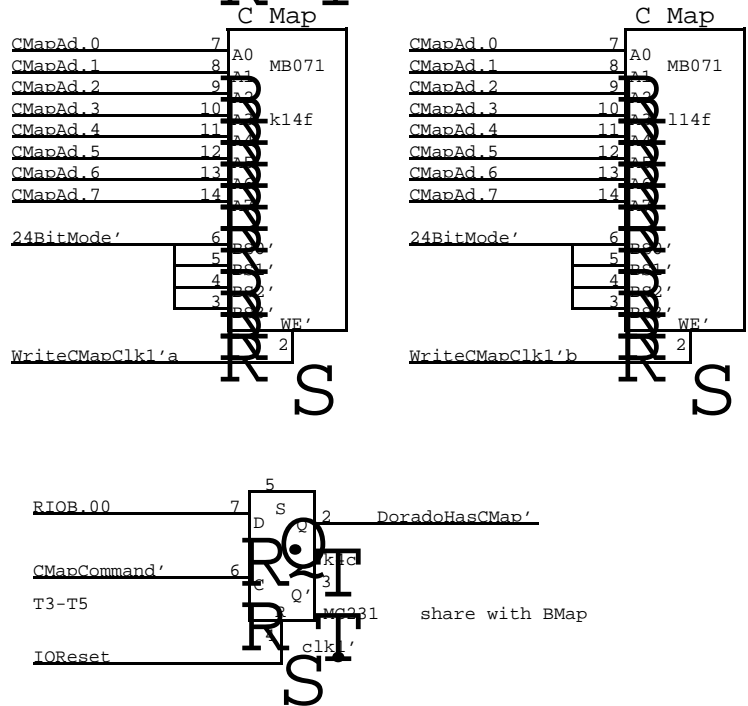
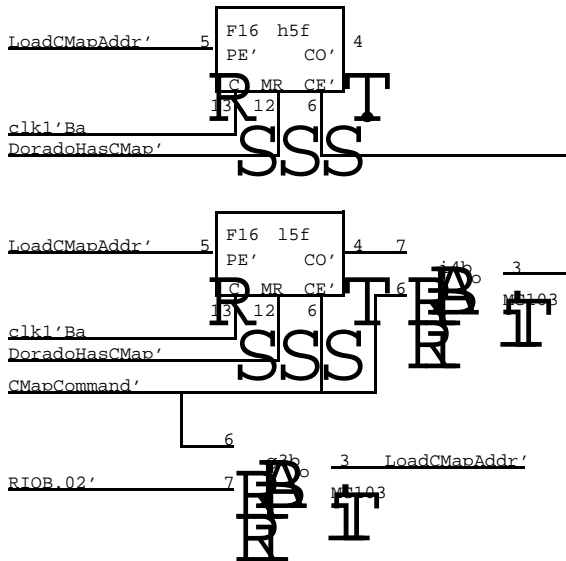


NOTE: in order to read/write BMap, BByPass mode must be ON and the B Channel must be OFF. This is inconvenient, but it does the right thing for real time mode switching.

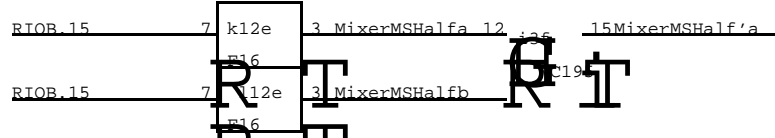
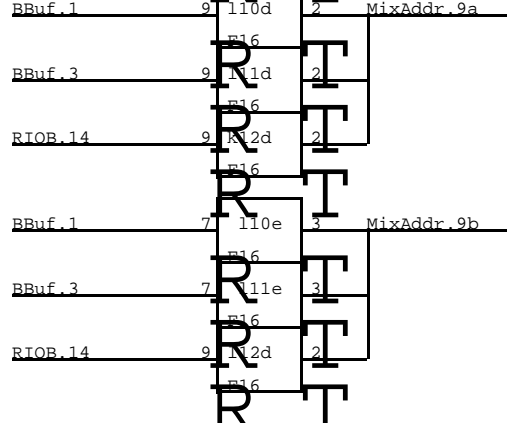
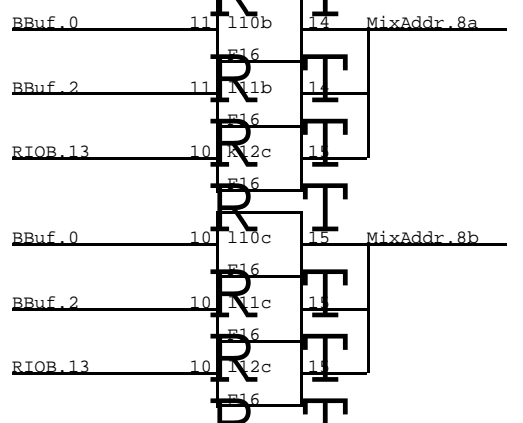
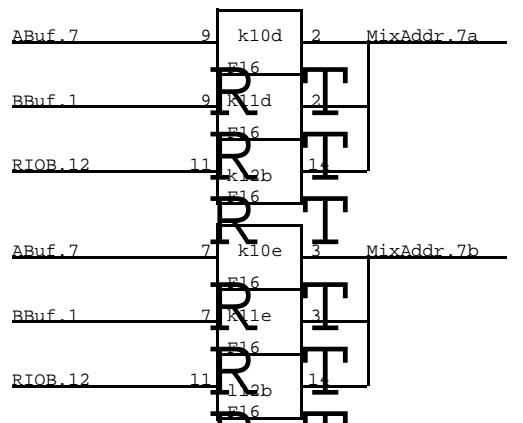
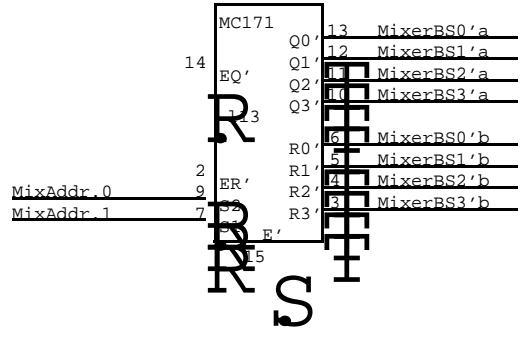
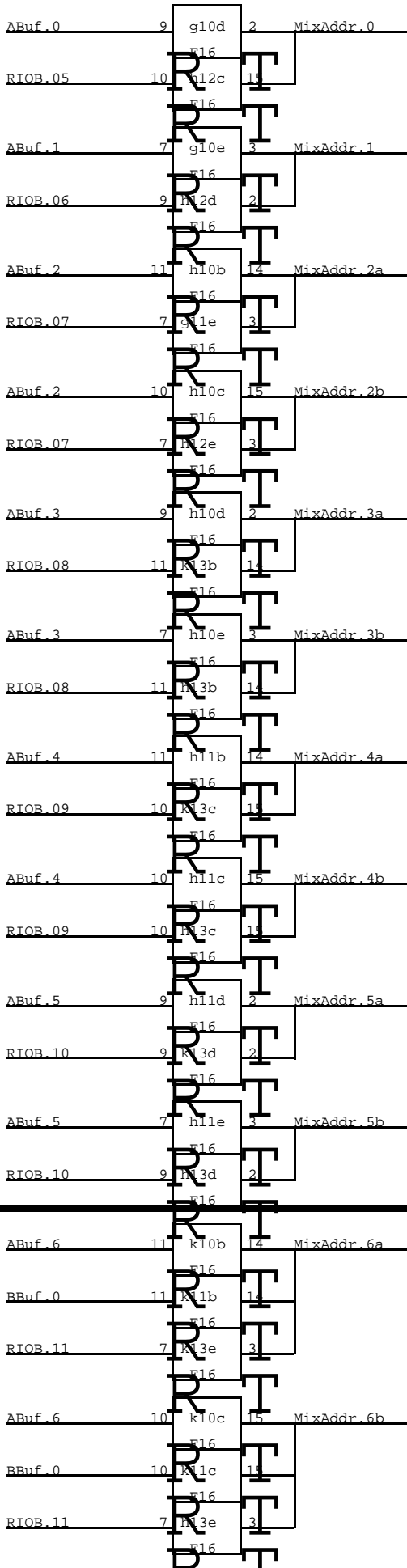
Dorado CMap address wire OR with CMapAd registers

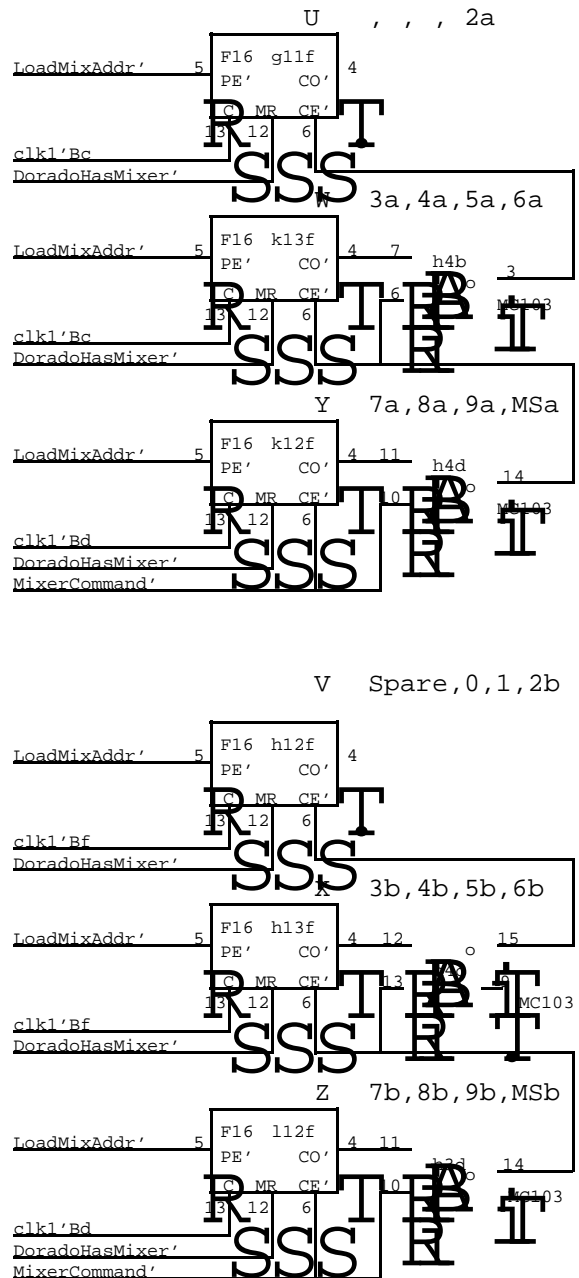
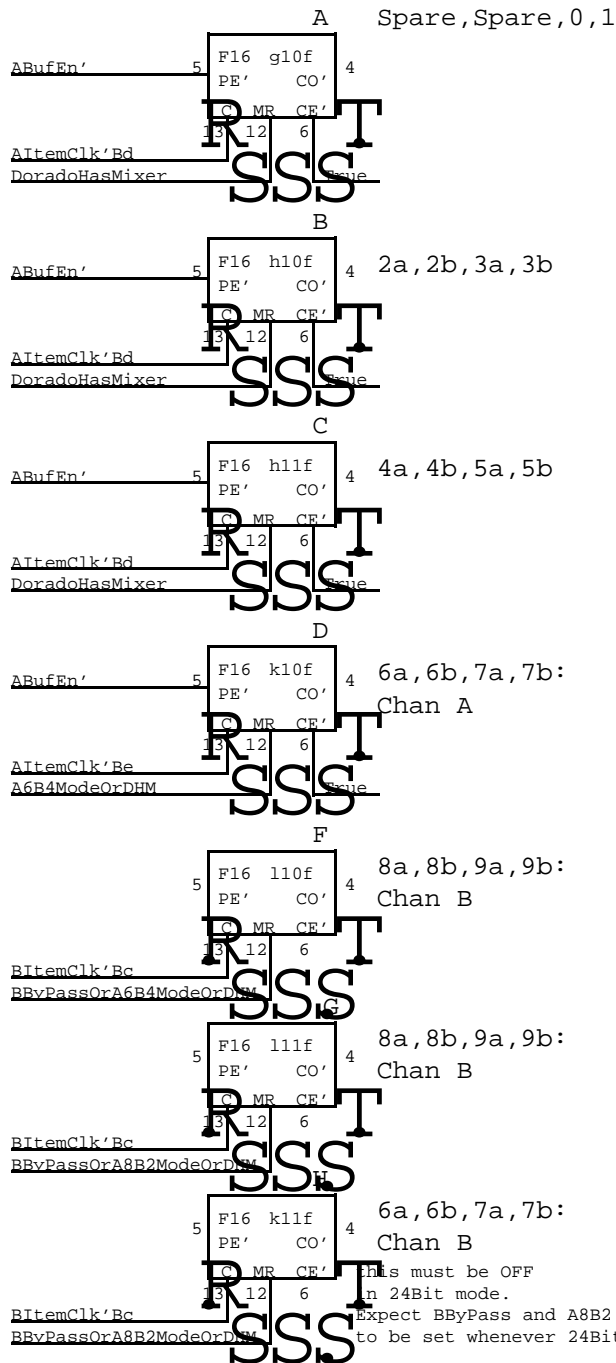


Dorado CMap address



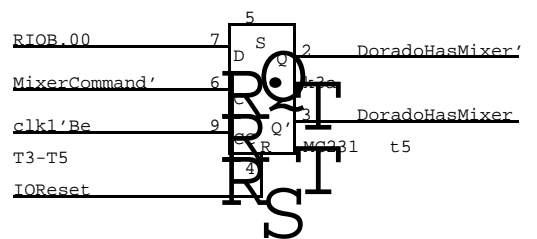
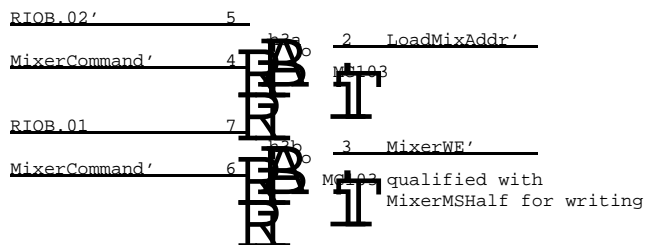
NOTE: in order to read/write CMap, 24BitMode must be ON and The A channel must be OFF. This is inconvenient, but it does the right thing for real time mode switching.

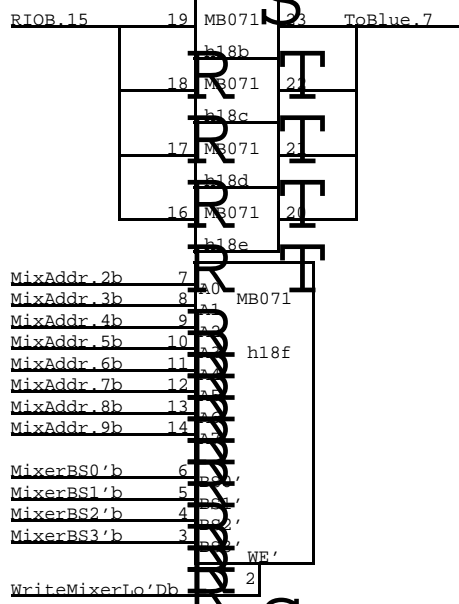
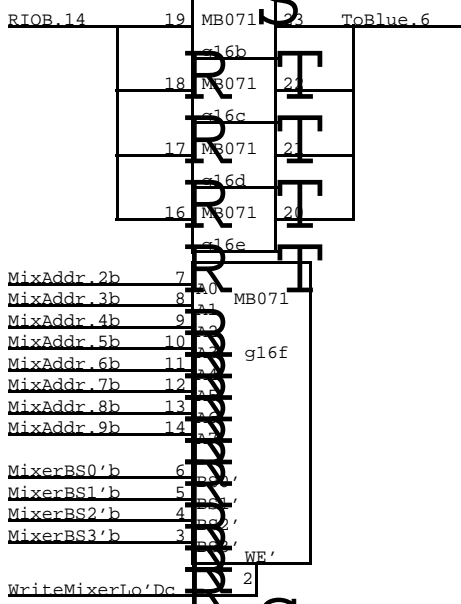
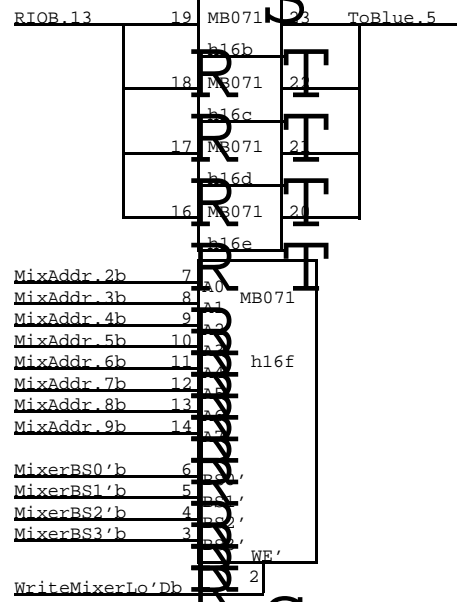
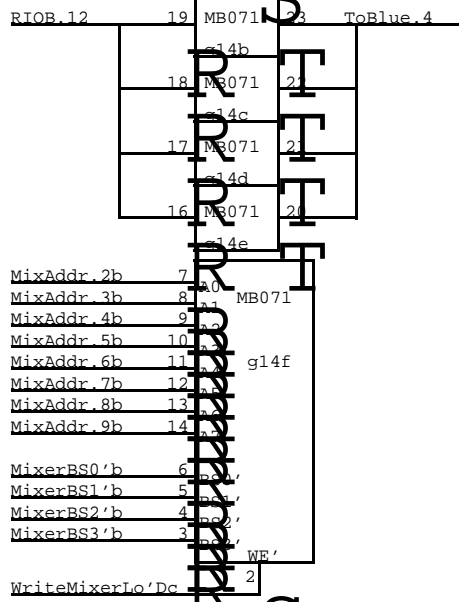
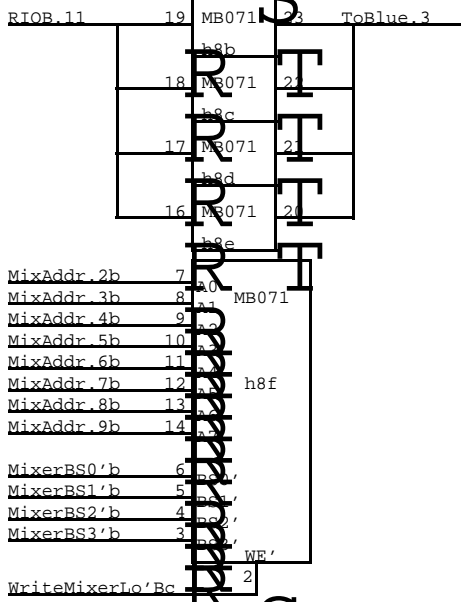
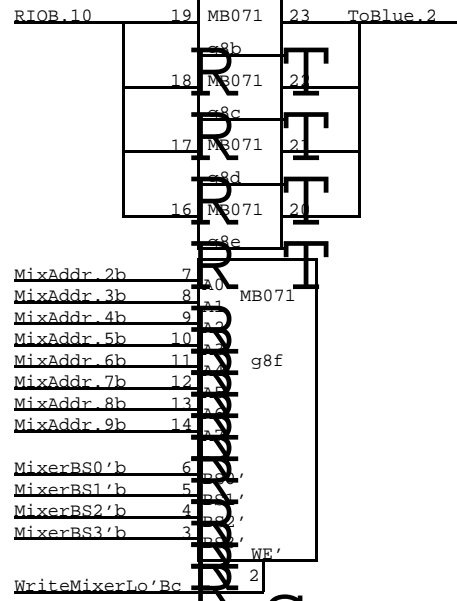
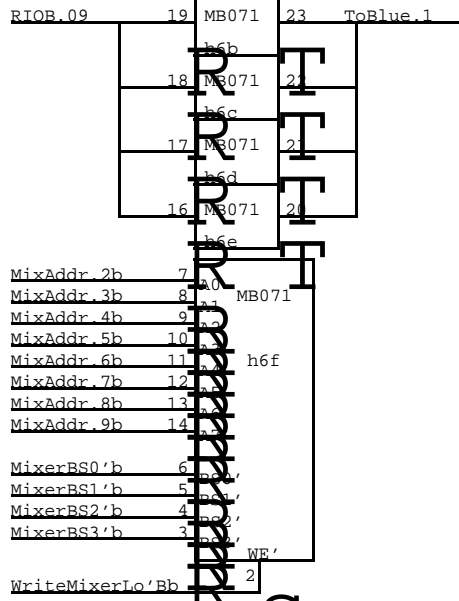
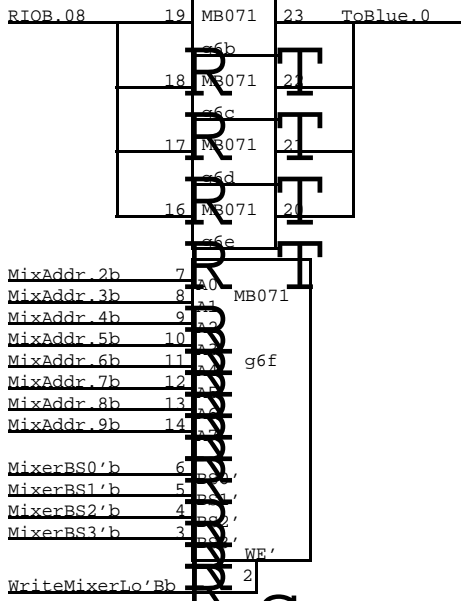


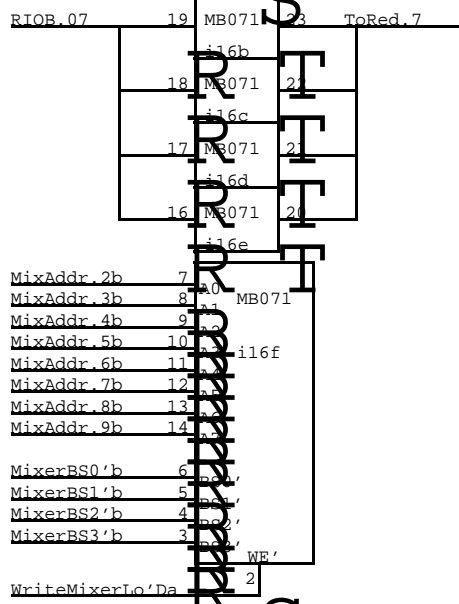
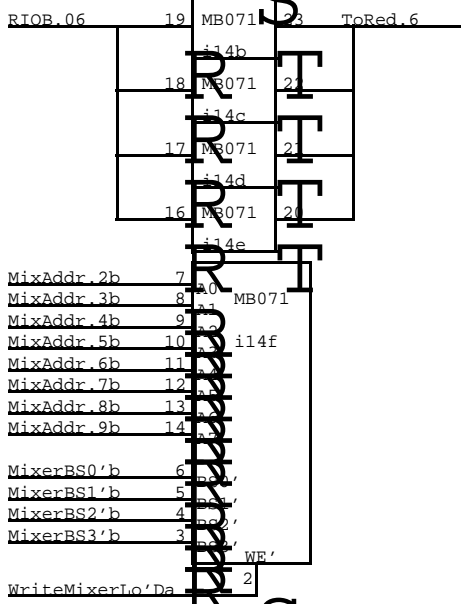
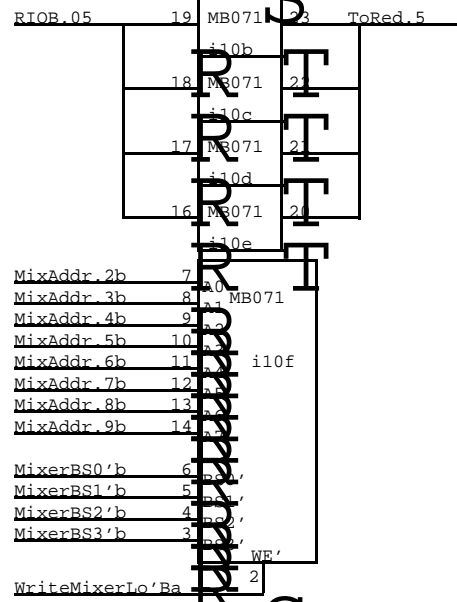
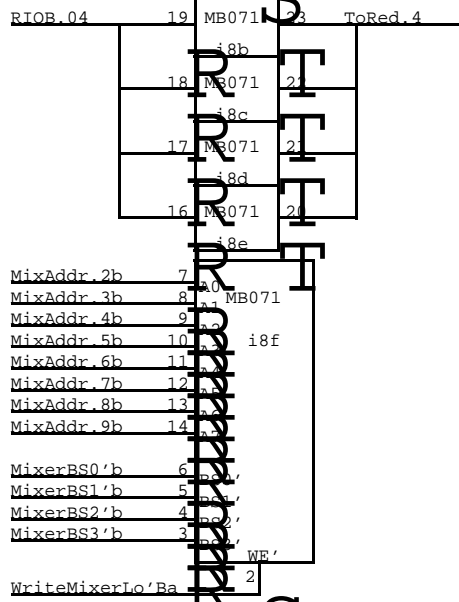
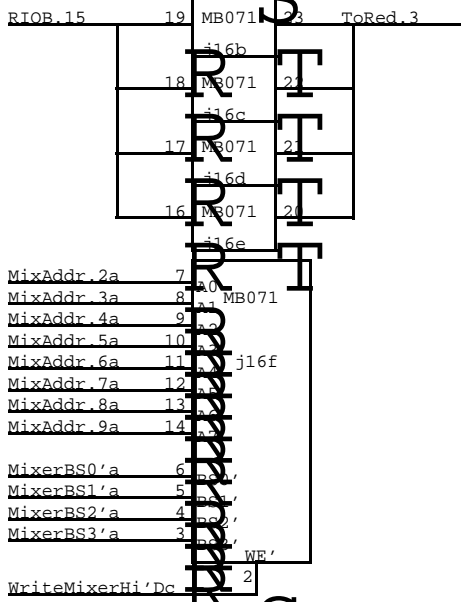
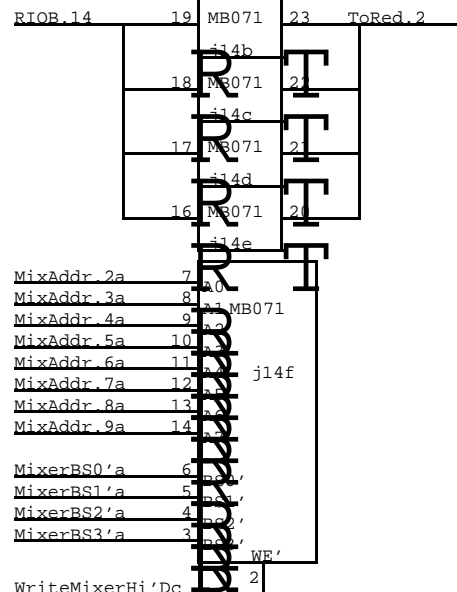
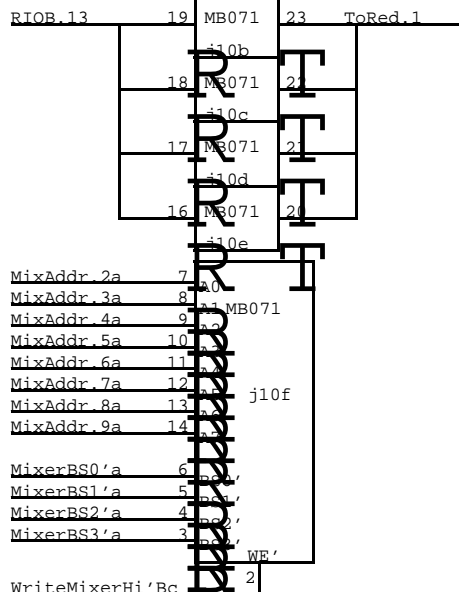
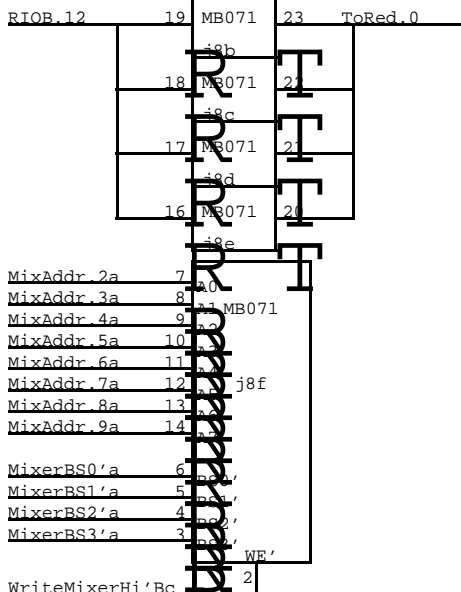


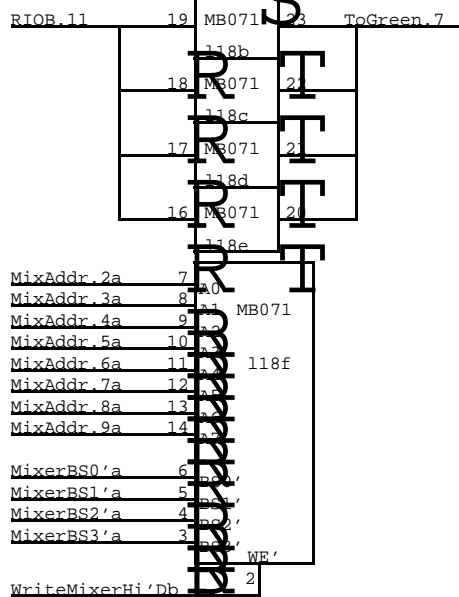
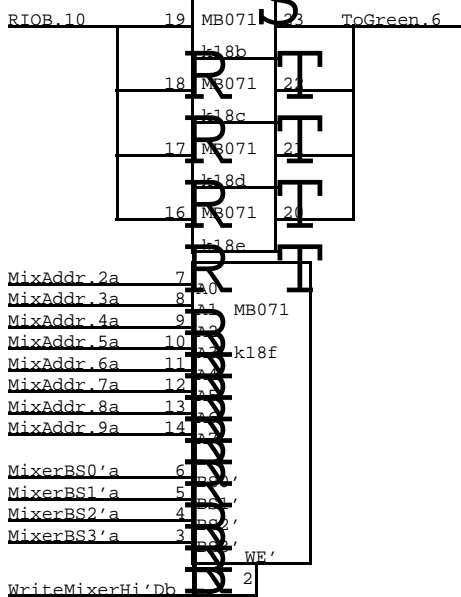
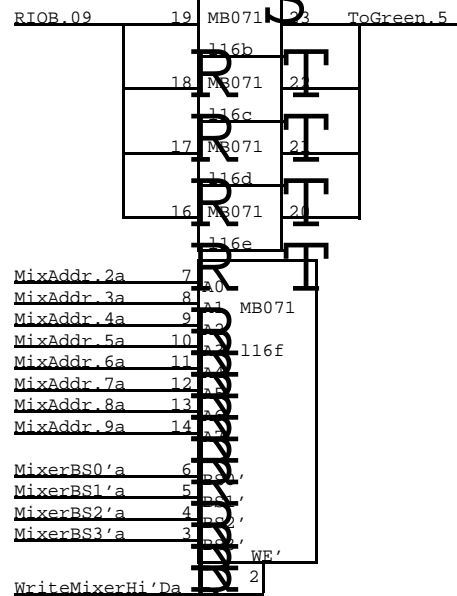
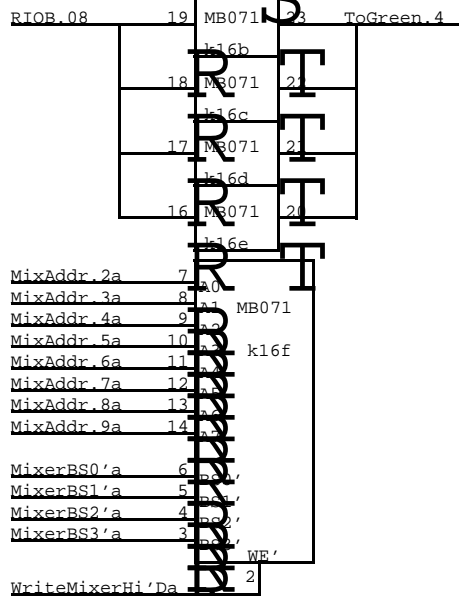
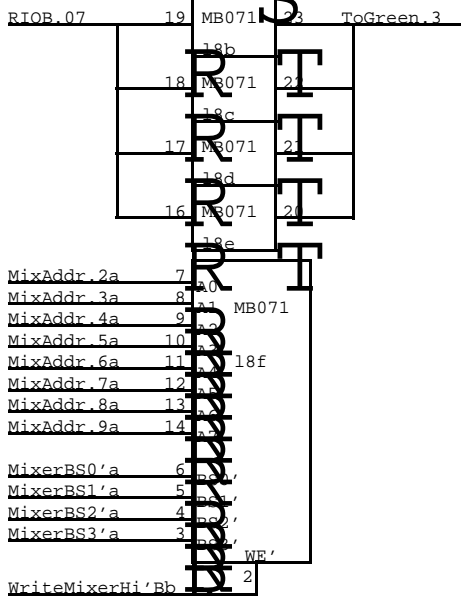
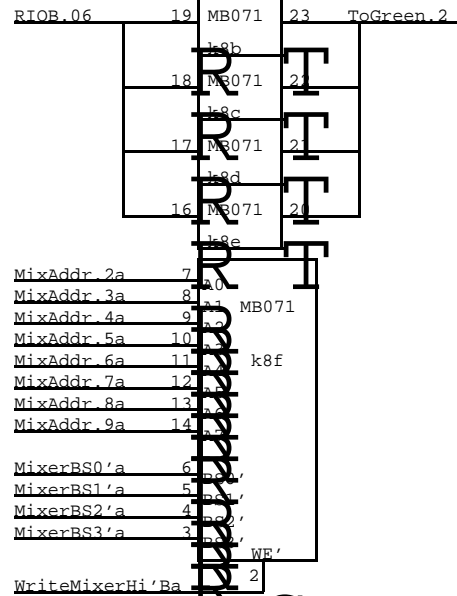
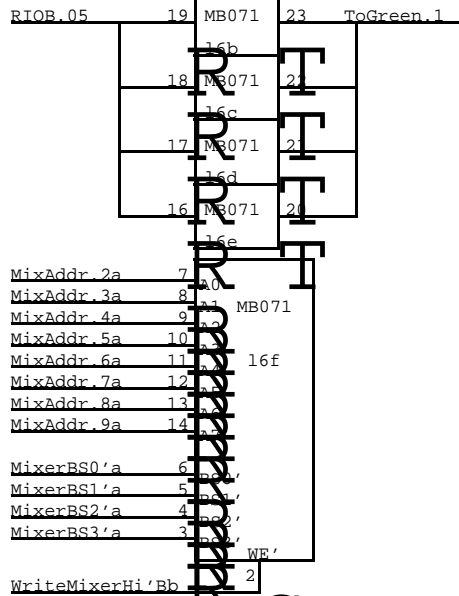
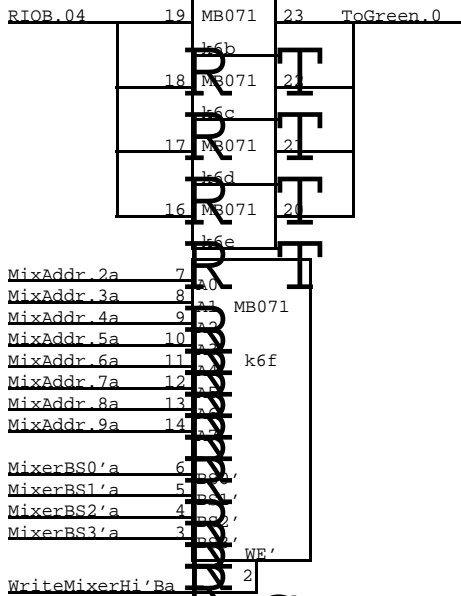
NOTE: B Channel must be started by microcode one pixel clk tick earlier than A channel for 24BitMode to align properly.

NOTE: Pixel clock must run at 2X rate for 24BitMode to work across entire screen !!

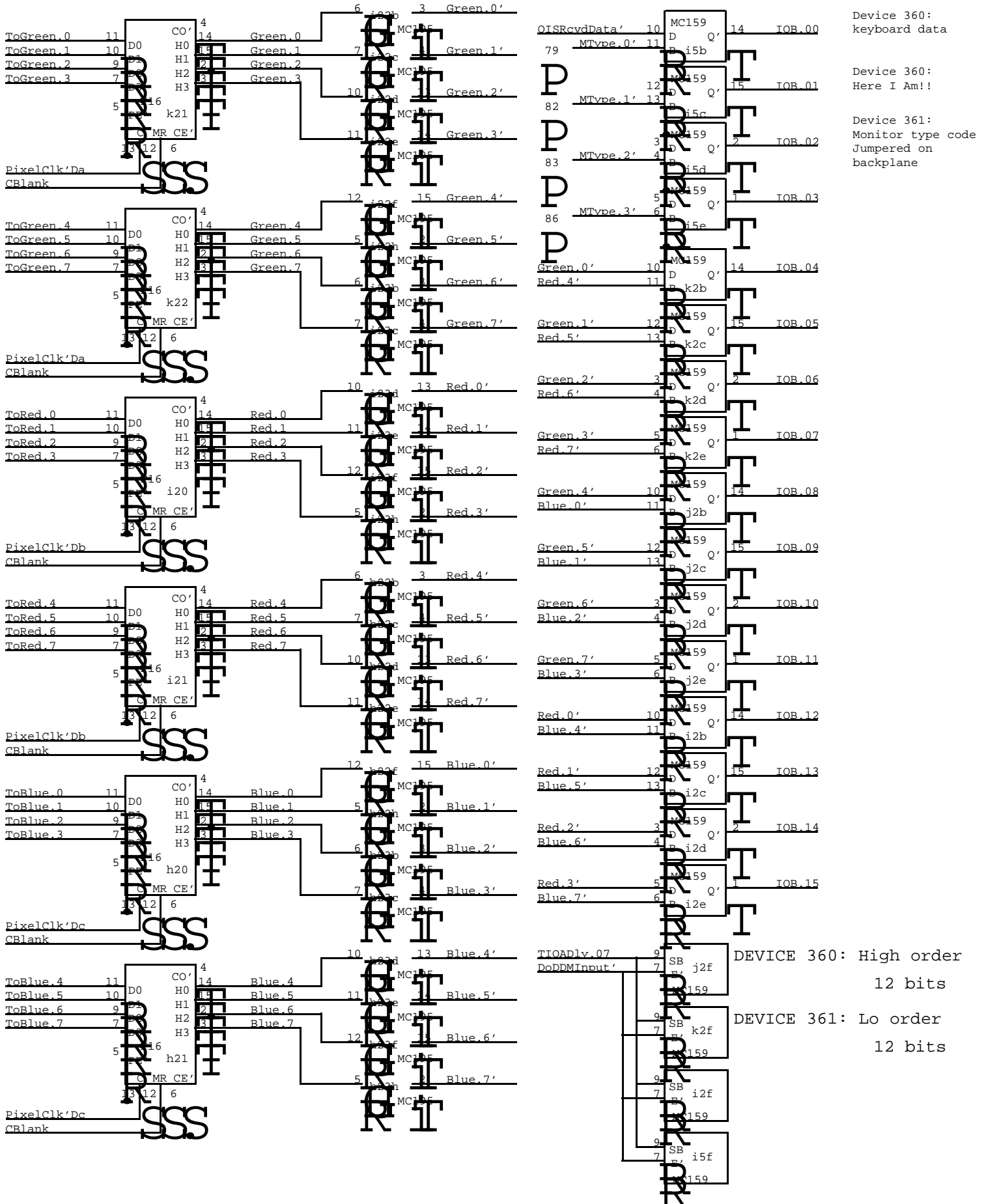


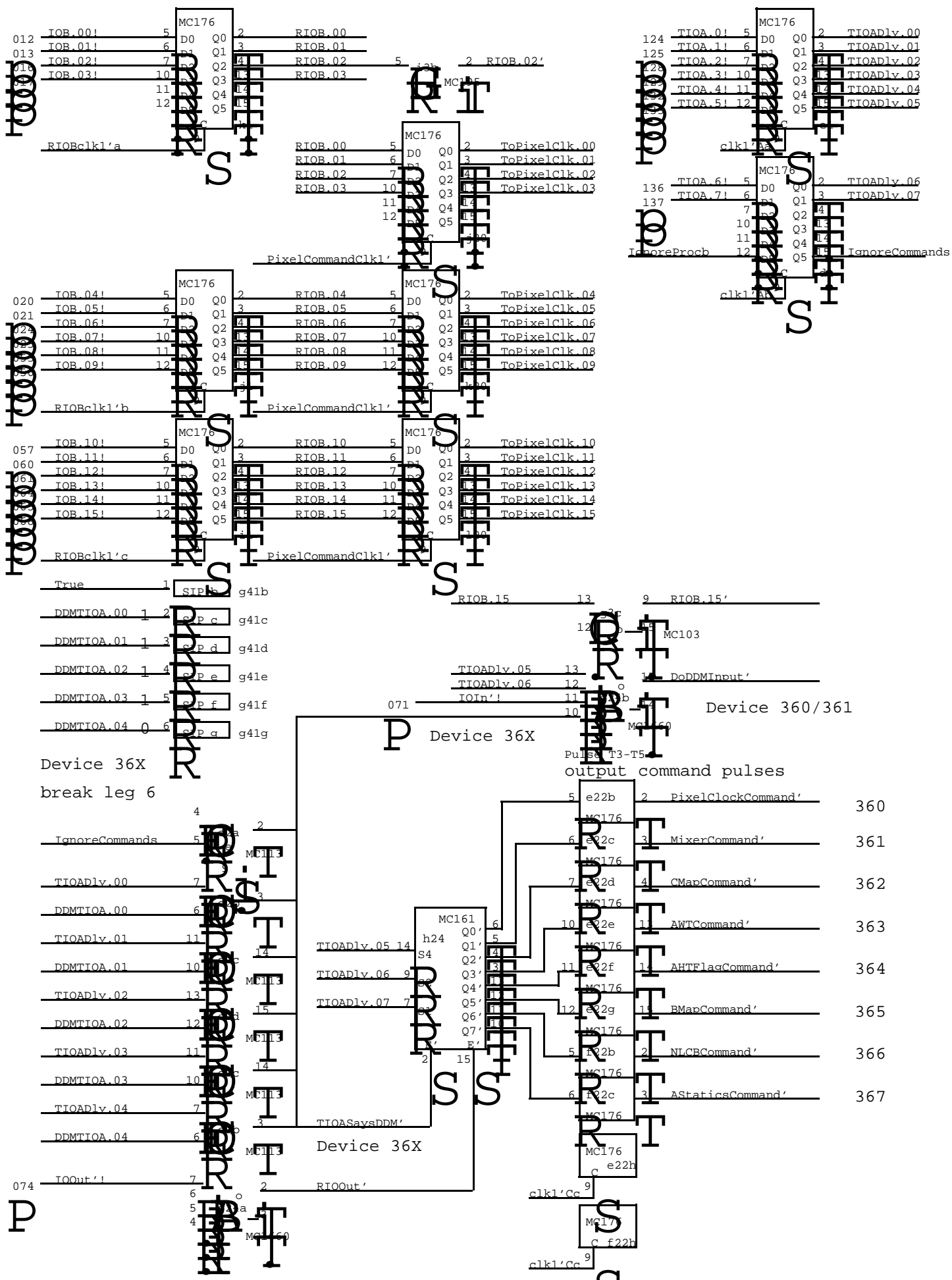




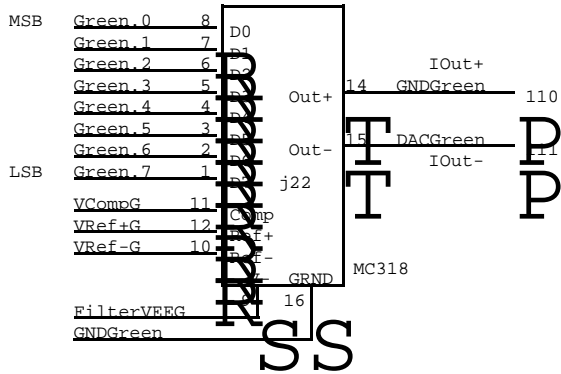


No Parity supplied
Use InputNoPE



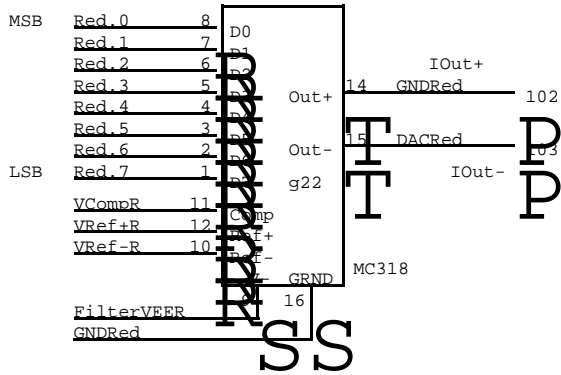


NOTES:
 GNDGreen is
 used as single point GND
 for DAC system



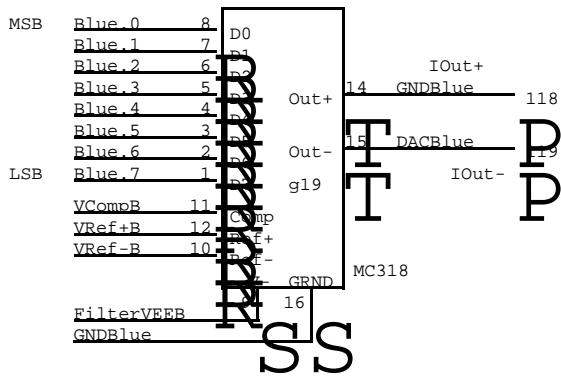
Digital/Analog converter

NOTES:
 GND RED is
 used as single point GND
 for DAC system

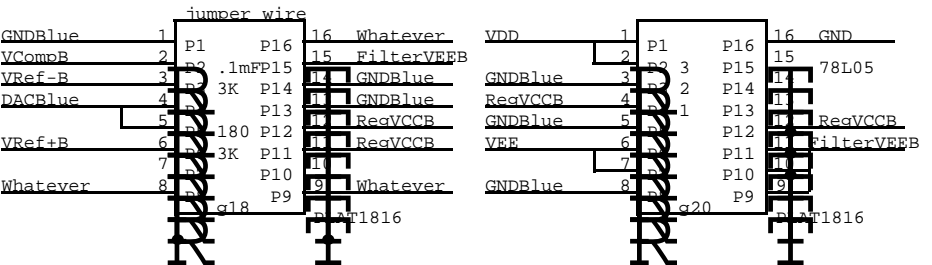
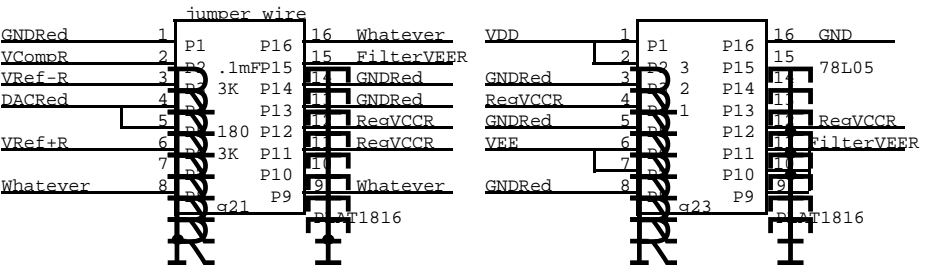
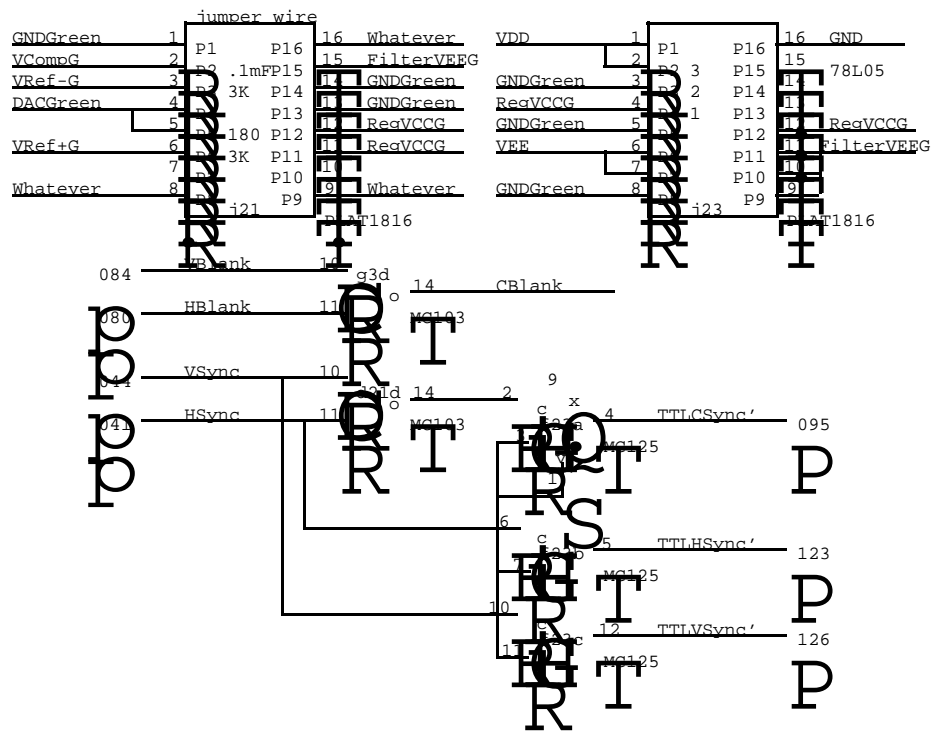


Digital/Analog converter

NOTES:
 GNDBLue is
 used as single point GND
 for DAC system



Digital/Analog converter

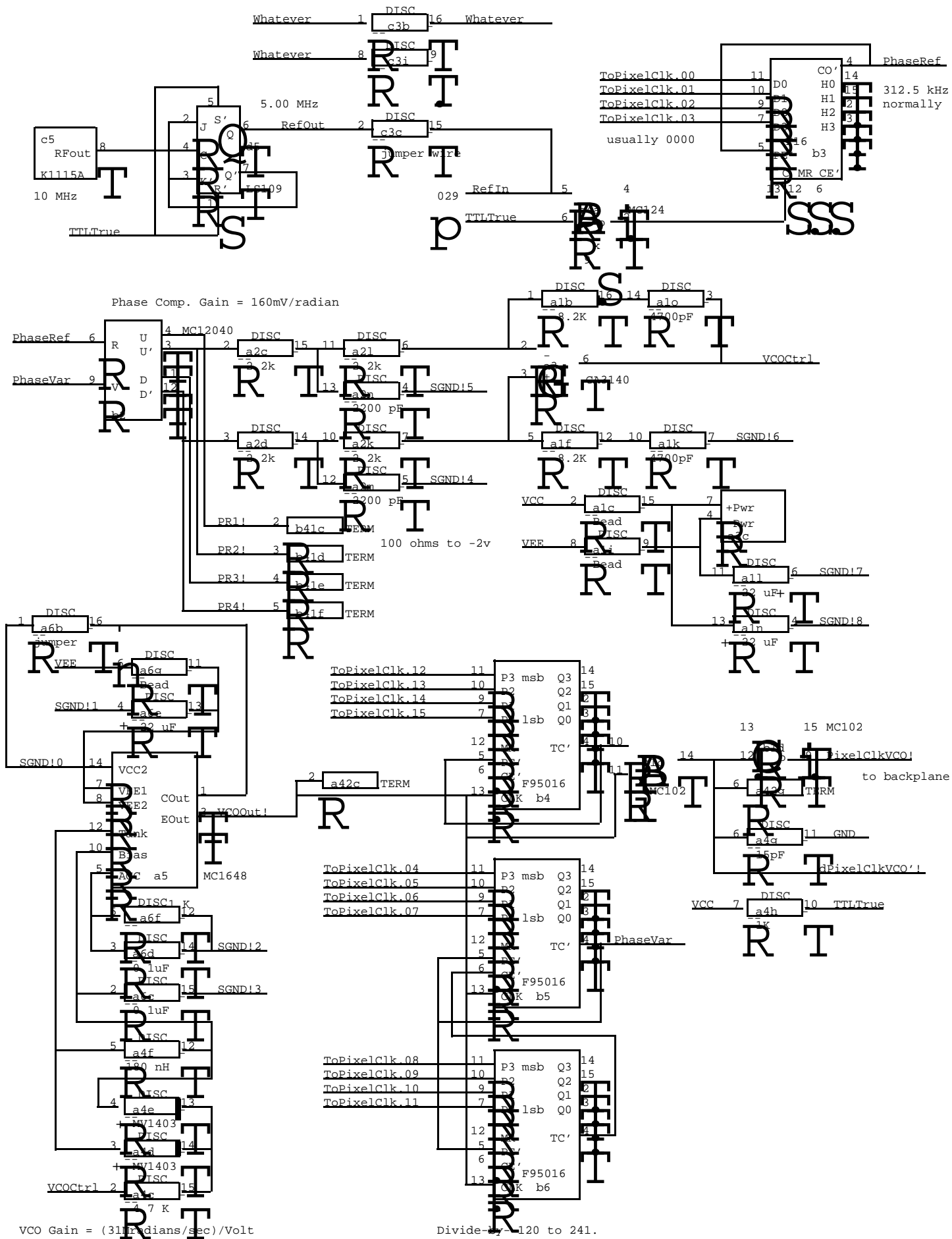


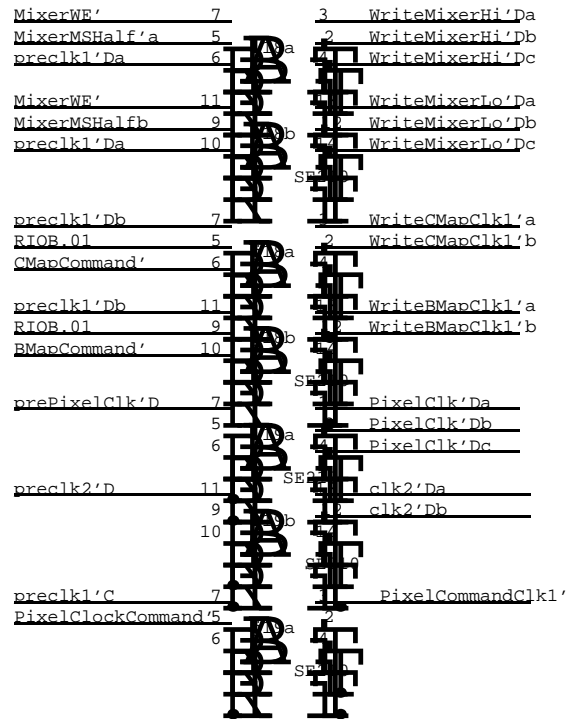
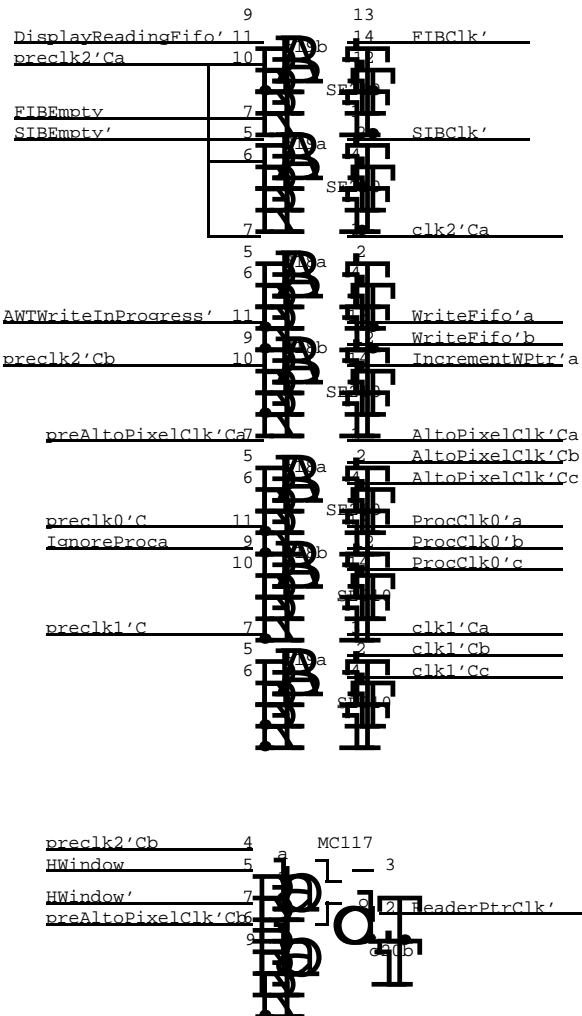
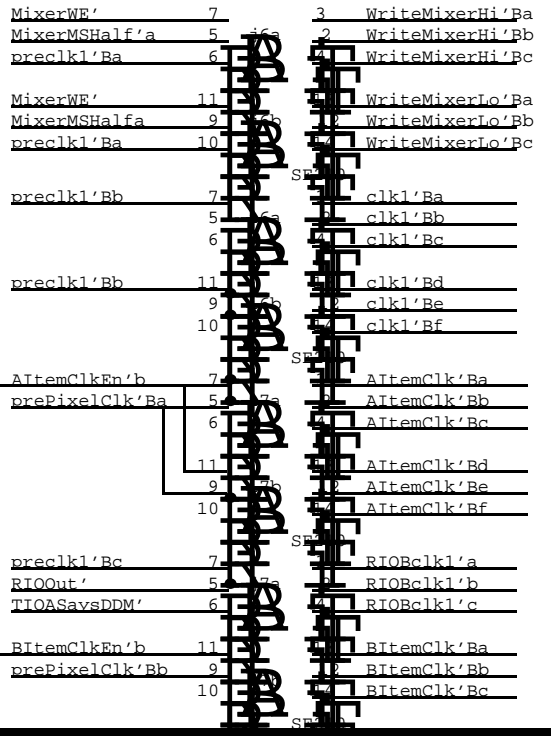
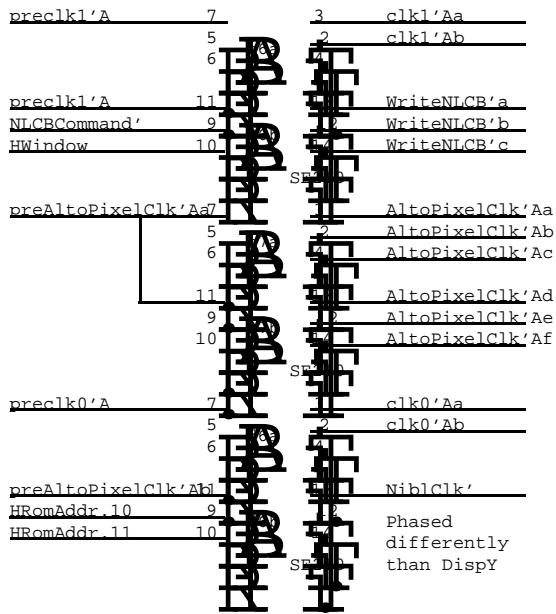
1	jumper wire	16
2	0.1mFarad	15
3	3 KOhm	14
4		13
5	180 Ohm	12
6	3 KOhm	11
7		10
8		09

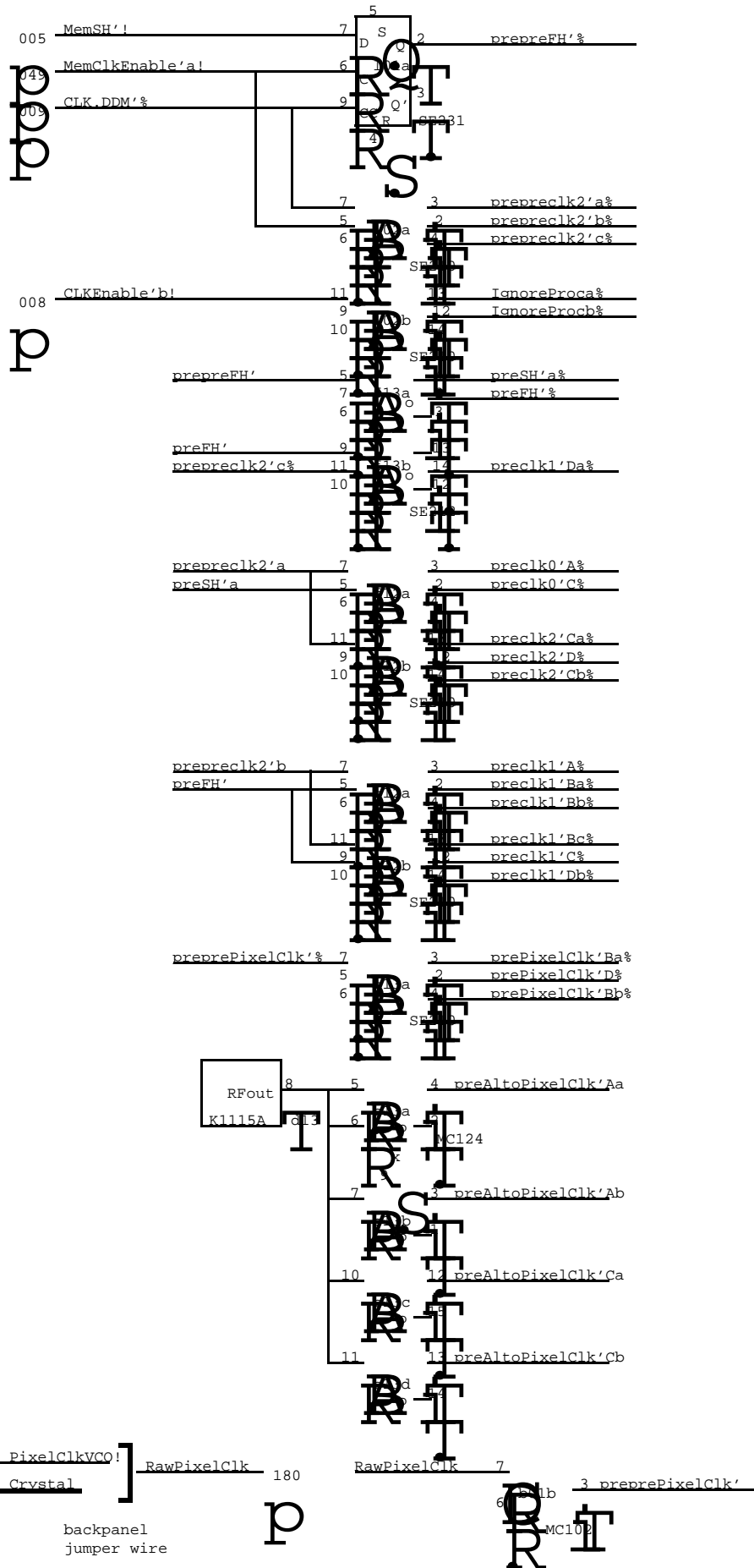
1	0.1mFarad	16
2	in ³	78L05 15
3	gnd ²	14
4	out ¹	13
5	0.1mFarad	12
6	12 mHnry	11
7	2 ohm	10
8	+ 22 mF	09

locations g18,g21,j21

locations j23,g23,g20







C	CONNECTOR		CONNECTOR		TIOA	TW	CONNECTOR		IOBLo	CONNECTOR		IOBHi	CLK	C
B>Ct	a 181	b 168	c 153	d 137	e 124	f 109	93 g	80 h	64 j	48 i	33 k	20 l	19	B
1	DISC VCO 23	PCLK 8,25,23,23 102		TIOA 176 21	TIOA 176 21	BBuf F16 12	ABuf F16 12	ABuf F16 12	RIOB 176 21	RIOB 176 21	RIOB 176 21	25 SE231		1
2	DISC VCO 23	12040 VCO 23		WakeAHT 135	TIOA=D 113	BBuf F16 12	CBuf F16 12	CBuf F16 12	DIOB 159 20	DIOB 159 20	DIOB 159 20	25 SE210		2
3	3140 VCO 23	F16 VCO 23	DISC 23	OISDrvr 10,4,10 105	TIOA=D A,21,21,10 113	WakeAWT AVSync 231	MapLd 13,14,21, 103 22	MixLd 16,16,20, 103 16	Modes B,12,12 195 12,15,	DHM 21 105 12	DHMix 231 16,B			3
4	DISC VCO 23	95016 VCO 23	VCO 124 23	OISDrvr 101 10		BMapAd F16 12	ABufEn 231 12,B	ORs 12,16,16, 103 16	13,14,12,D 103		DHMap 231 13,14			4
5	1648 VCO 23	95016 VCO 23	K1115 VCO 23	LS109 VCO 23		BMapAd F16 12	CMapAd F16 12	DCMapAd F16 14	IOB 159 20		CMapAd F16 12	DCMapAd F16 14		5
6	DISC VCO 23	95016 VCO 23	Clock 210 24	Clock 210 24	ShutUp 231 4	DBMapAd F16 13	Mixer B0 17	Mixer B1 17	Clock 210 24	Clock 210 24	Mixer G0 19	Mixer G1 19		6
7	AltoStoP 141 10	Nibble 176 10	Clock 210 24		CLCBDecd 161 5	DBMapAd F16 13	--	--	Clock 210 24	Clock 210 24	--	--		7
8	CursorX F16 9	OIS 174 10	OIS 9,9,10,10 103	Width F16 4	LMarg F16 4	NLCB 145A 5	Mixer B2 17	Mixer B3 17	Mixer R4 18	Mixer R0 18	Mixer G2 19	Mixer G3 19		8
9	CursorX F16 9	CursorHi 141 9	CursorLo 141 9	Width F16 4	LMarg F16 4	NLCB 145A 5	--	--	--	--	--	--		9
10	CursorX F16 9	CursorHi 141 9	CursorLo 141 9	Width F16 4	LMarg F16 4	NLCB 145A 5	MixAddr F16 15	MixAddr F16 15	Mixer R5 18	Mixer R1 18	MixAddr F16 15	MixAddr F16 15		10
11	VCW F16 4	Cursor 104 9	Width 4,4,6,4 103	LMarg 103 4	NLCBAddr F16 5	NLCBAddr 197 5	MixAddr F16 15	MixAddr F16 15	--	--	MixAddr F16 15	MixAddr F16 15		11
12	PixelClk 176 10	OISSkew 176 10	3,4,4,2 104	HWindow 135 5	LoadASR 121 3	Clock 210 25	Clock 210 25	MixAddr F16 15	BMap 13	BMap 13	MixAddr F16 15	MixAddr F16 15		12
13	HRomAddr 6	HRomOut 176 6	TTLtoEcl 25	Xtal K1115 25	LoadASR F16 3	Clock 212 25	Clock 210 25	MixAddr F16 15	--	--	MixAddr F16 15	Bsel 171 15		13
14	HRomAddr 6	ASR 141 3	ASR 141 3	ASR 141 3	ASR 141 3		Mixer B4 17		Mixer R6 18	Mixer R2 18	CMap	CMap		14
15	HRomAddr 6		FIB 176 3	FIB 176 3	FIB 176 3		--		--	--	--	--		15
16	HRomAddr 6	Fifo 3	Fifo 3	Fifo 3	Fifo 3	FifoAd 158 2	Mixer B6 17	Mixer B5 17	Mixer R7 18	Mixer R3 18	Mixer G4 19	Mixer G5 19		16
17						FifoAd 158 2	--	--	--	--	--	--		17
18	6,4,4,2 102	OISRevd 231 10,B	Clock 210 24	Clock 210 24	RPtr 2	WPtr 2	Bldac Plat 22	Mixer B7 17	Clock 210 24	Clock 210 24	Mixer G6 19	Mixer G7 19		18
19	6,4,6,6 103	6,4,6 9,4,6 195	Clock 210 24	Clock 210 24,B	RPtr 2	WPtr 2	Bldac 10318	--	Clock 210 24	Clock 210 24	--	--		19
20		HRom MC149 6	RdrPtrClk CTisAWT 117 24,8	ASRSync 231 2		AOn ASRSync 135 2,4	Bldac Plat 22	Blue 20	Red 20		PXLCLK 176 21 176 21	176 21		20
21			SCAN F16 4	7,2,2,22 103	Flags 231 7	Flags 118 7	RdDac Plat 22	Blue 20	Red 20	GrDac Plat 22	Green 20			21
22	SIB 176 3	SIB 176 3	SIB 176 3		CMND 176 21	CMND 176 21	RdDac 10318	Color' 195 20	Color' 195 20	GrDac 10318	Green 20			22
23	8,8,C 105	ProcClk0 176 8		blocked 135 8	ASRSync 135 2	TTLCSync 22 125	RdDac Plat 22	Color' 195 20	Color' 195 20	GrDac Plat 22		1,B,C,D 102		23
24	NextAWT 112 8			WakeCnt B,4*8,2 195	WakeCnt F16 8	Hold 231 8	IOInOut 1660 21	TIOA=D 161 21	Fout 176 1	Fout 176 1	Fout 176 1	FtTsk 113 1		24

C	a 11	b 26	c 39	d 55	e 70	Hold f 86	99 g	114 h	129 i	143 j	159 k	174 l	D
E	Next	Subt	Blk	Fin	IOin/out	CONNECTOR	IOB FNXT	FOUT	FTsk	DMux	E		

Project	Reference	File	Designer	Rev	Date	Page
Dorado	DispM Board Layout	DispM26.sil	K. Pier	Ch	11/09/82	26

DispY	SIZE	DispM
AItem	8	AItem 85-88-89-92-93-96-97-100
BItem	8	BItem 101-104-105-108-109-112-113-116
CursorData	1	CursorData
AItemClkEn	1	AItemClkEn
BItemClkEn	1	BItemClkEn
AOff	1	AOff
BOff	1	BOff
HSync	1	HSync
HBlank	1	HBlank
HalfLine	1	HalfLine
VSync	1	VSync
VBlank	1	VBlank
RawPixelClk	1	RawPixelClk
Crystal	1	Crystal
PixelClkVCO	1	PixelClkVCO
Modes	3	Modes 28-32-33
XHSync	1	XHSync
XVSync	1	XVSync
XSyncEn	1	XSyncEn
ABypass	1	RefIn

Red GND	1	102	DispM to coax/BNC connectors
Red	1	103	
Green GND	1	104	
Green	1	105	
Blue GND	1	106	
Blue	1	107	
TTLCSync'	1	108	
TTLCSync' GND	1	109	

MType.0	1	079	Monitor type field Jumper resistors on backplane
MType.1	1	080	
MType.2	1	081	

DispM ControlA

121 WakeTHT (TWReg4) twisted pair 56

120 WakeTHT (TWReg9) twisted pair 128

Plus seven wire interface cable. See page 11.

DDC Slow IO System

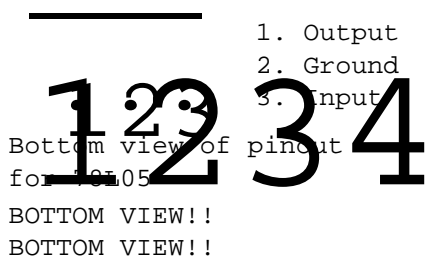
DEVICE	TIOA	I/O	TASK	FORMAT and COMMENTS
AStatics	367	0	AHT	
NLCB	366	0	AHT	
BMap	365	0	CHT, EMU	Keep,Write,LoadAddr,0,DataOrAddr8-15
AHTFlag	364	0	AHT	
AWT	363	0	AWT	
CMap	362	0	CHT, EMU	Keep,Write,LoadAddr,0,DataOrAddr8-15
MIXER	361	0	CHT, EMU	Keep,Write,LoadAddr,0,Data.4-15
PIXELCLK	360	0	CHT, EMU	Pixel clock rate
STATUS	361	I	CHT, EMU	MType.0-3,Green.0-7,Red.0-3
STATUS	360	I	CHT, EMU	Keyboard,1,1,1,Red.4-7,Blue.0-7

00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15

				Pixel Clock Rate								Clock Divider			PIXELCLK	
Keep Mixer'	Write Mixer'	Load Mixer Addr	X	Addr.0	Addr.1	Addr.2	Addr.3	Addr.4	Addr.5	Addr.6	Addr.7	Addr.8	Addr.9	Hi/Lo select	MIXER	
Mixer Data 12 bits																
Keep BMap'	Write BMap'	Load Bmap Addr	X	Address.0-7 OR Data.0-7											BMap	
Keep CMap'	Write CMap'	Load CMap Addr	X	Address.0-7 OR Data.0-7											CMap	
														AWT Shut Up	AHT Shut Up	AStatics
NLCB Addr 00	NLCB Addr 01	NLCB Addr 02	NLCB Addr 03	NLCB DATA 12 Bits											NLCB	
										IOFetch				Set/Clr Cur WCB Flag	AWT	
													X	Must Be 0	AHTFlag	

1	jumper wire	16
2	0.1mFarad	15
3	3 KOhm	14
4	120 Ohm	13
5	180 Ohm	12
6	3 KOhm	11
7		10
8		09

1	0.1mFarad	16
2	in ³ 78L05	15
3	gnd ²	14
4	out ¹	13
5	0.1mFarad	12
6	12 mHnry	11
7	2 ohm	10
8	+ 22 mF	09



locations

g18,g21,j21

3 identical copies

locations

j23,g23,g20

3 identical copies

SIP in location g41 is 100 ohm terminator with leg 6 cut (making DDMTIOA = 360B)

SIP in location b52 is 100 ohm terminator with legs 3 and 4 cut for Task 9D=11B

SIPs in locations d42 and e42 are 220 ohm value instead of 100 ohm (terminators for 7 wire in

Crystal oscillators, type K1115A:
 location c5, value 10 MHz, for VCO
 location d13, value 20 Mhz for Alto
 value 50 MHz for LF

Horizontal PROM, type MC149
 location a16 and b20 for LF display
 location b20 ONLY for Alto style display
 programmed for each monitor type

1	8.2 KOhm	16
2	Bead	15
3	4700 pF	14
4	22 microF	13
5	8.2 KOhm	12
6	+ 22 microF	11
7	4700 pF	10
8	Bead	09

location a1

1		16
2	2.2 KOhm	15
3	2.2 KOhm	14
4	2200pF	13
5	2200pF	12
6	2.2 KOhm	11
7	2.2 KOhm	10
8		09

location a2

1		16
2	4.7 KOhm	15
3	+MV1403-	14
4	+MV1403-	13
5	180 nH	12
6	15 pF	11
7	1 KOhm	10
8		09

location a4

1	jumper wire	16
2	0.1microF	15
3	0.1microF	14
4	+ 22 microF	13
5	1 KOhm	12
6	Bead	11
7		10
8		09

location a6

1		16
2	jumper wire	15
3		14
4		13
5		12
6		11
7		10
8		09

location c3

Rev.	Date	Page	Revisions
Ch	11/07/82	7, 21, 23, 26 30 31	Expanded pixel clock buffer. Added 120 ohm resistor to position 4 of Platform for g18, g21 Added Revision Record Page