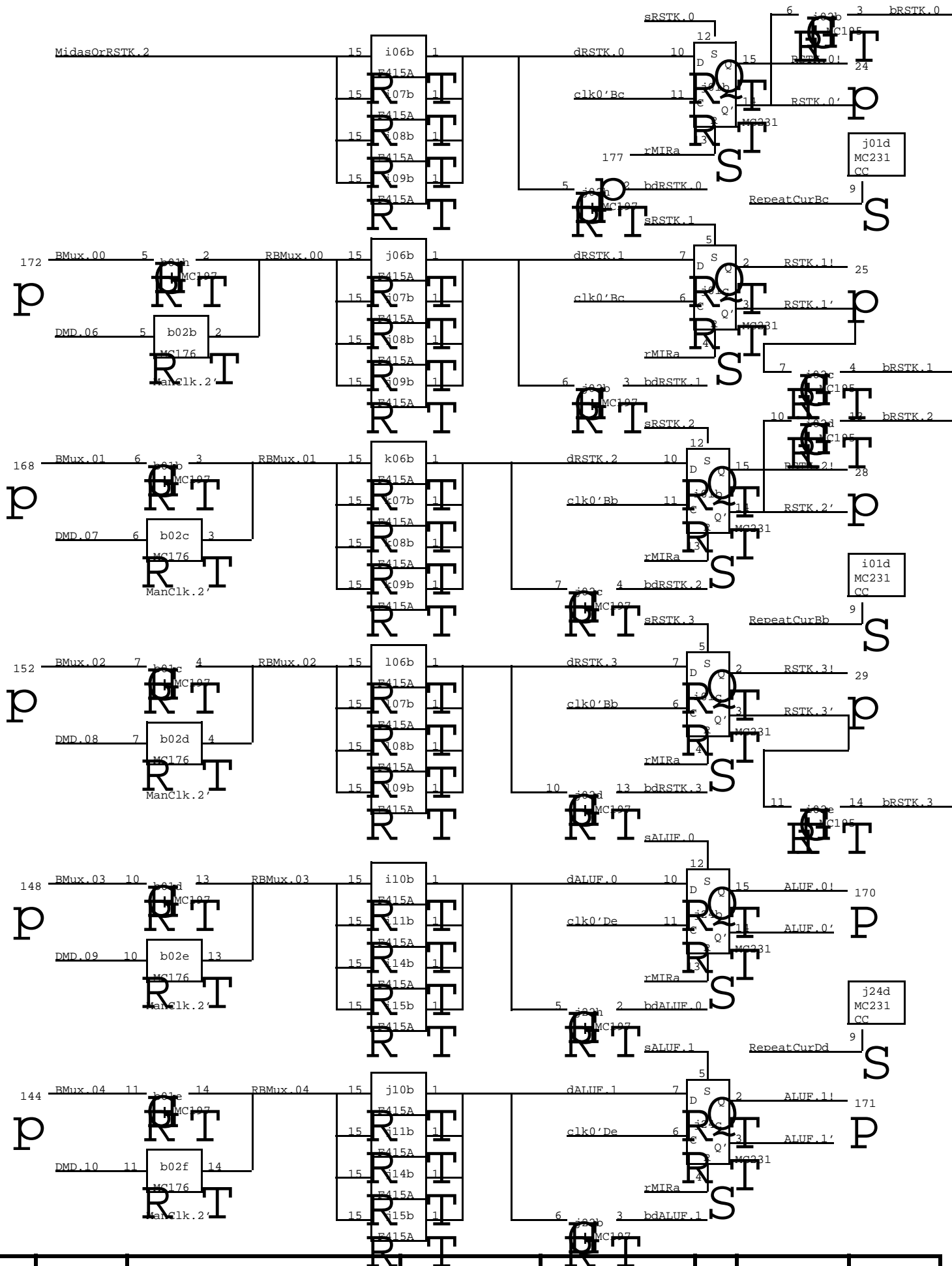


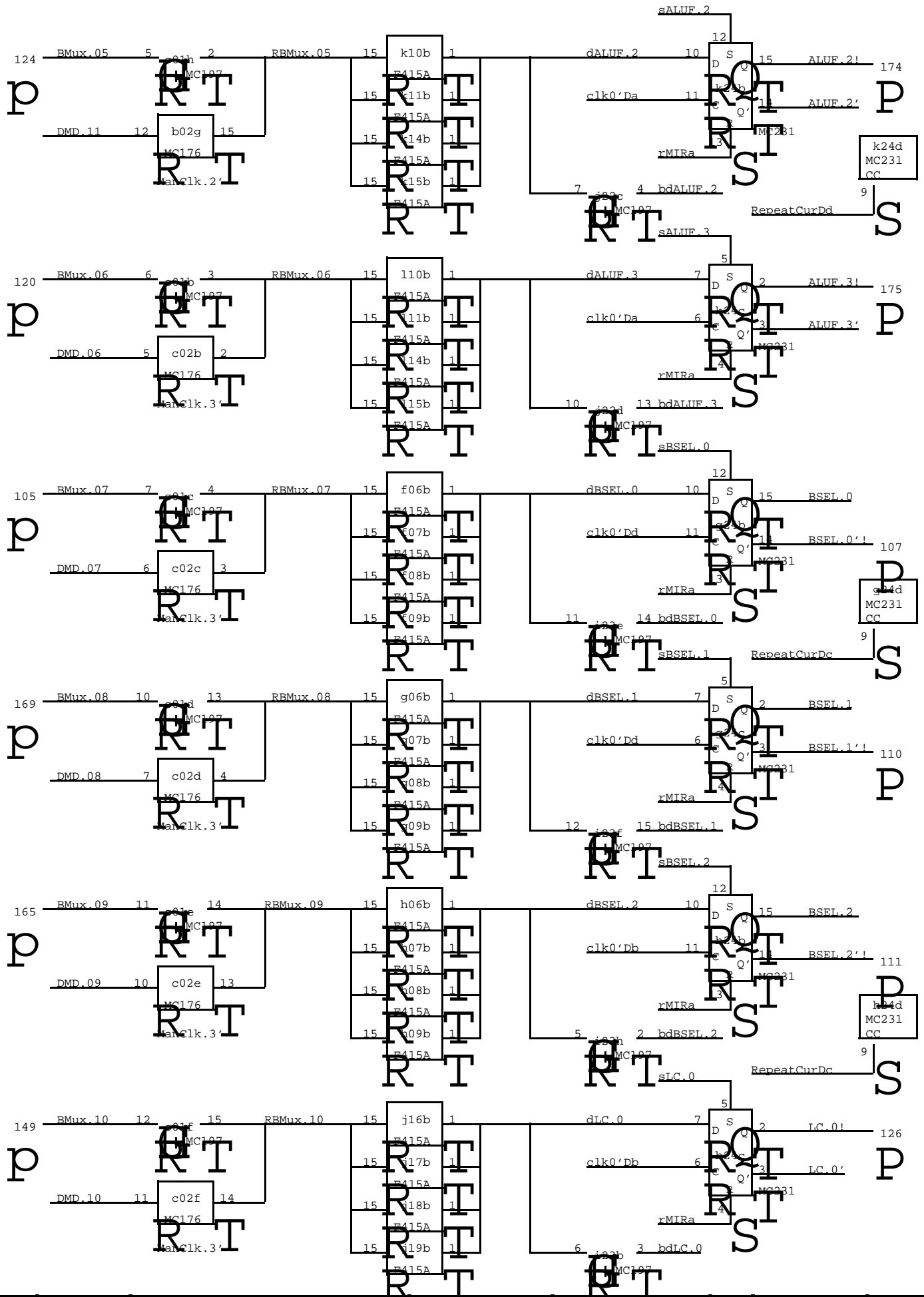
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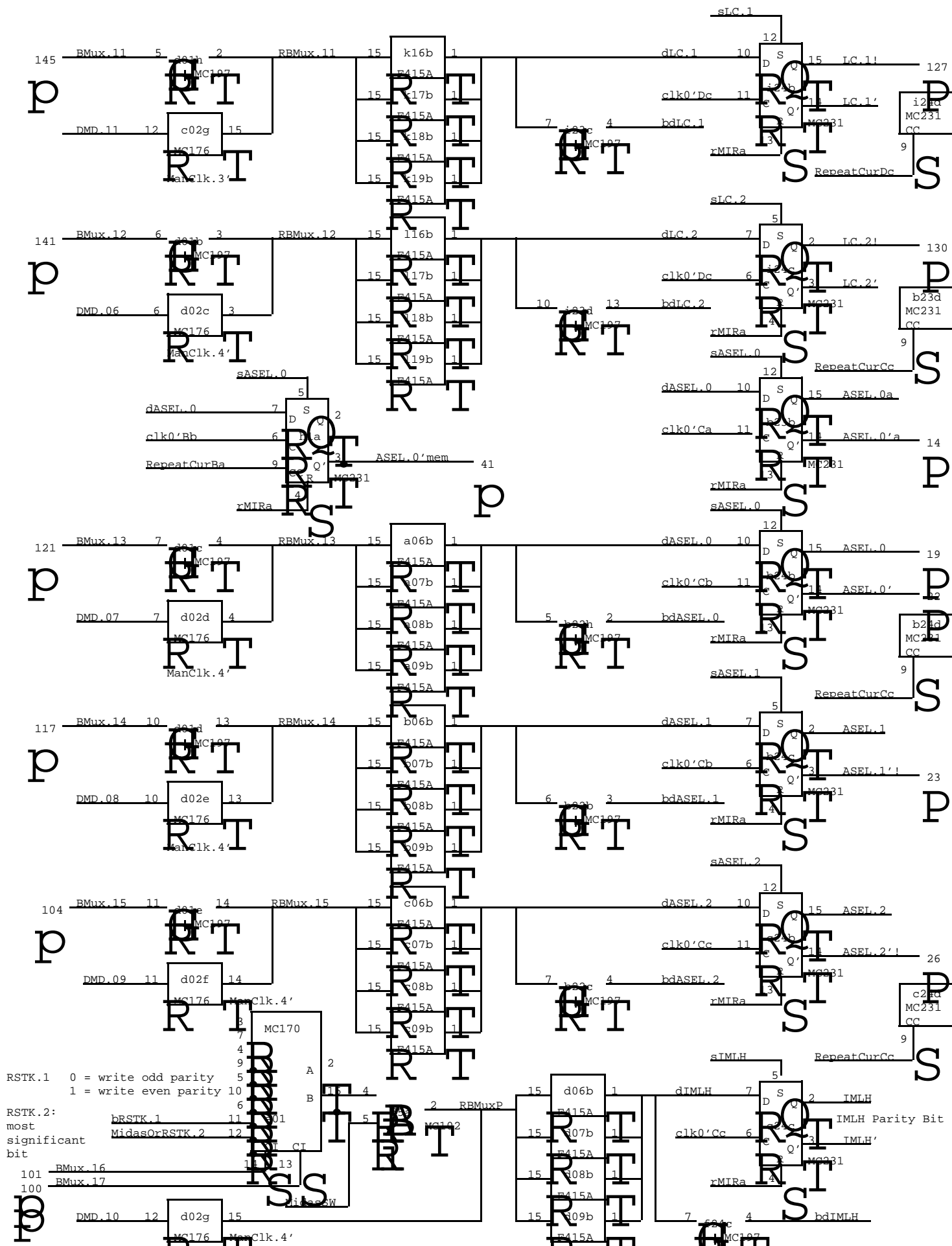
C o n t r o l   B

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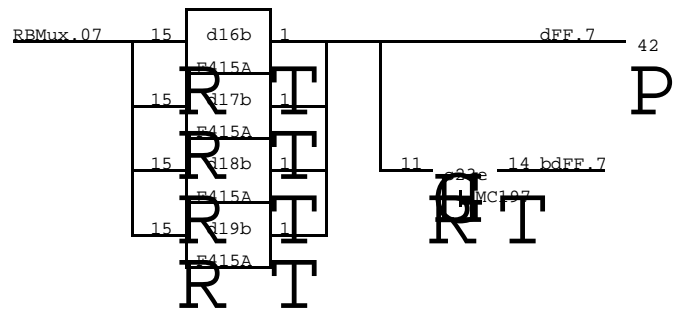
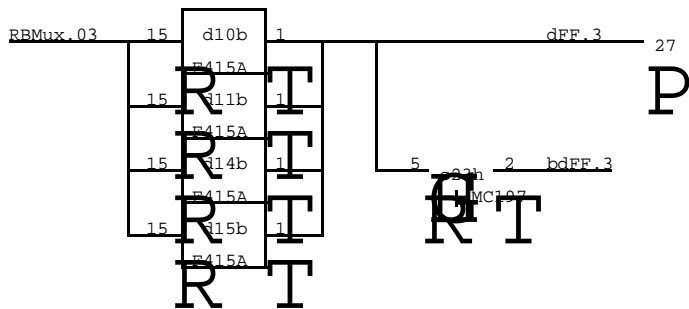
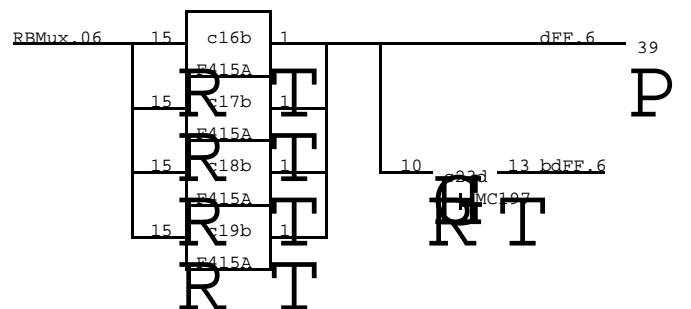
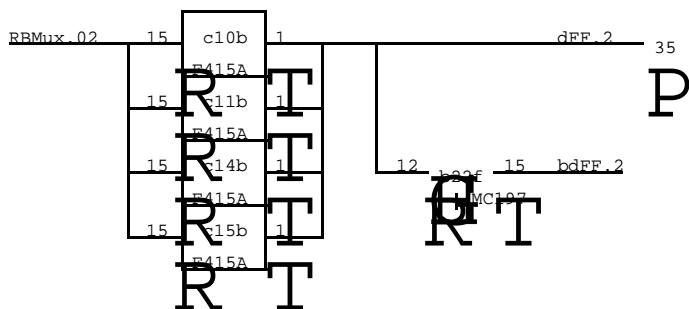
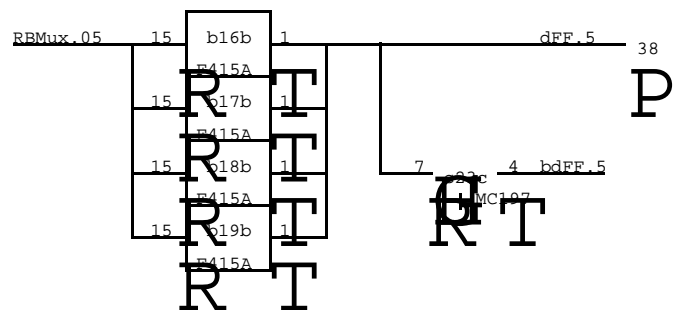
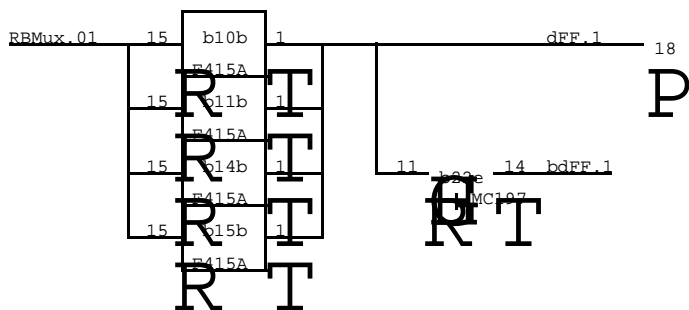
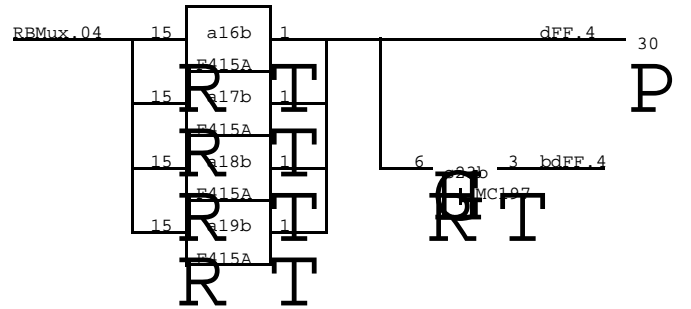
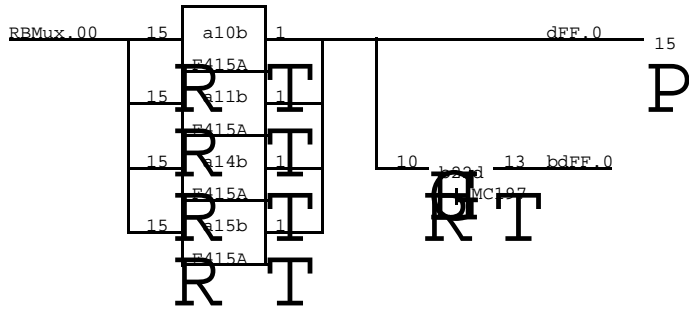
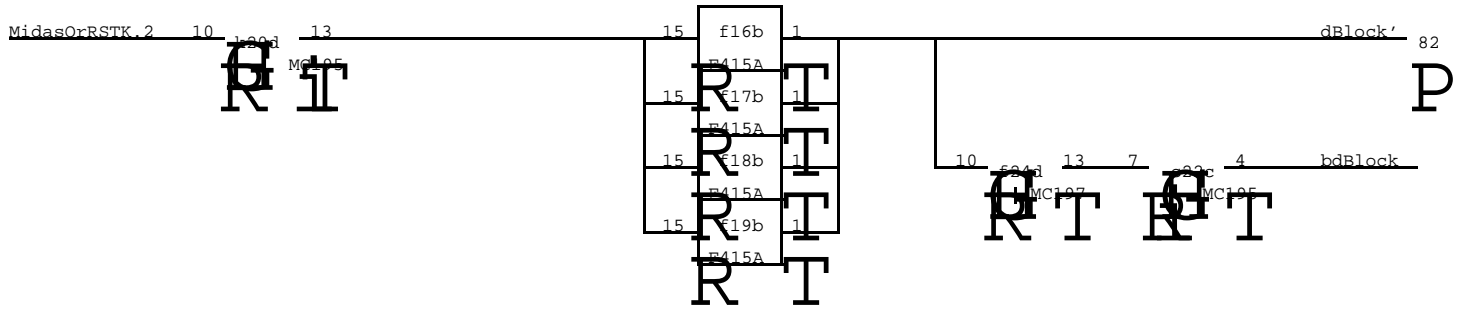


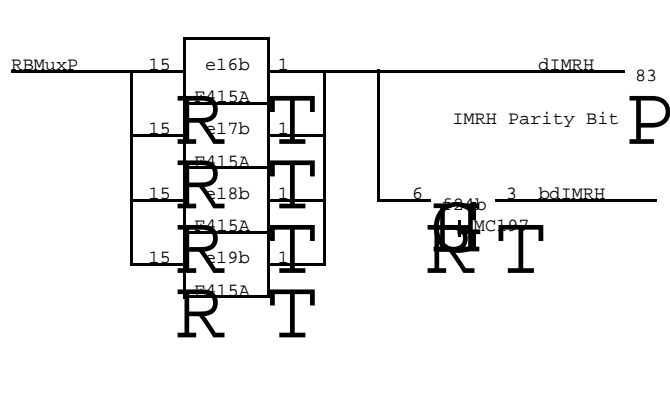
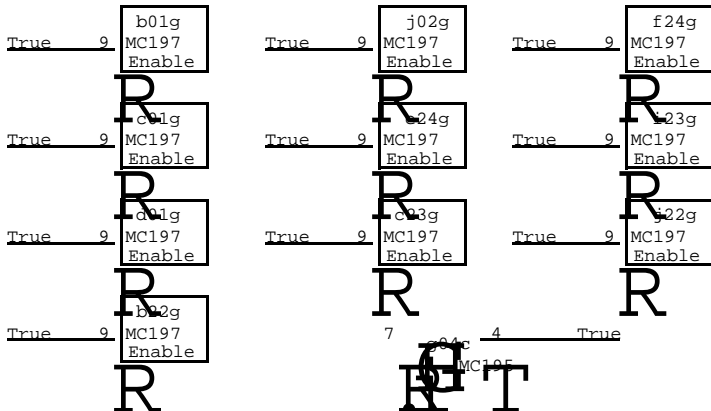
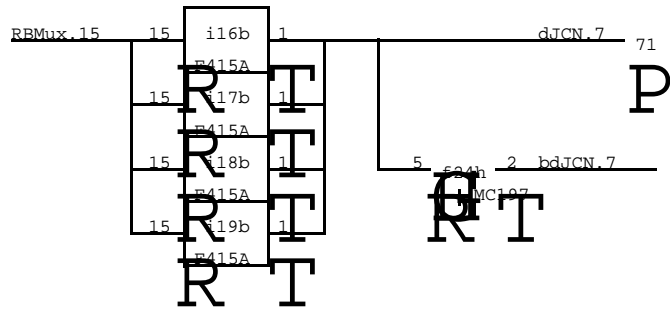
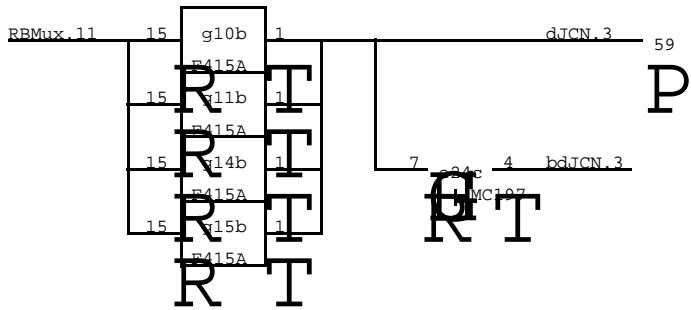
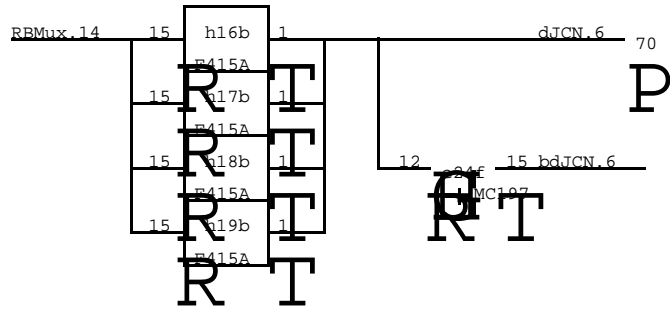
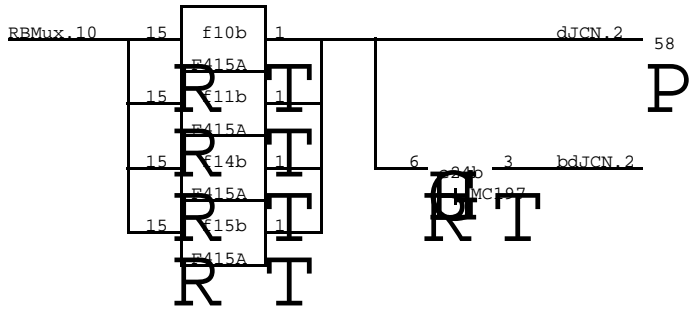
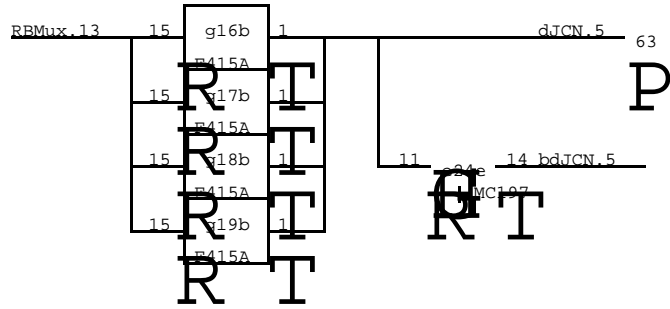
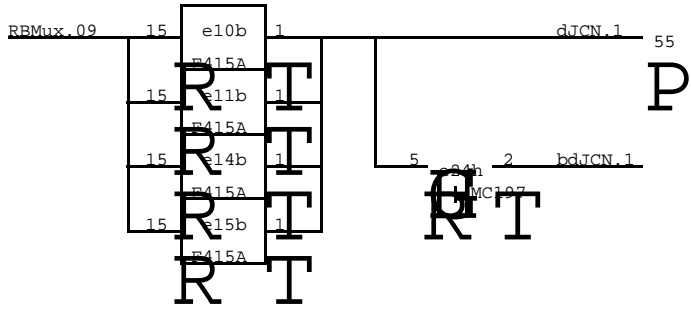
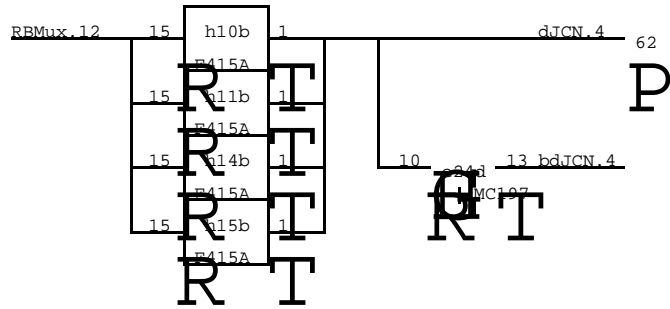
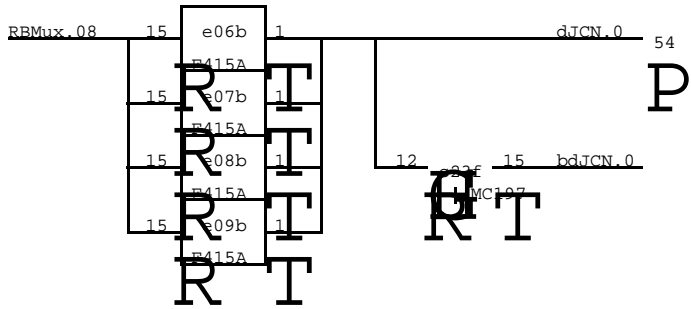


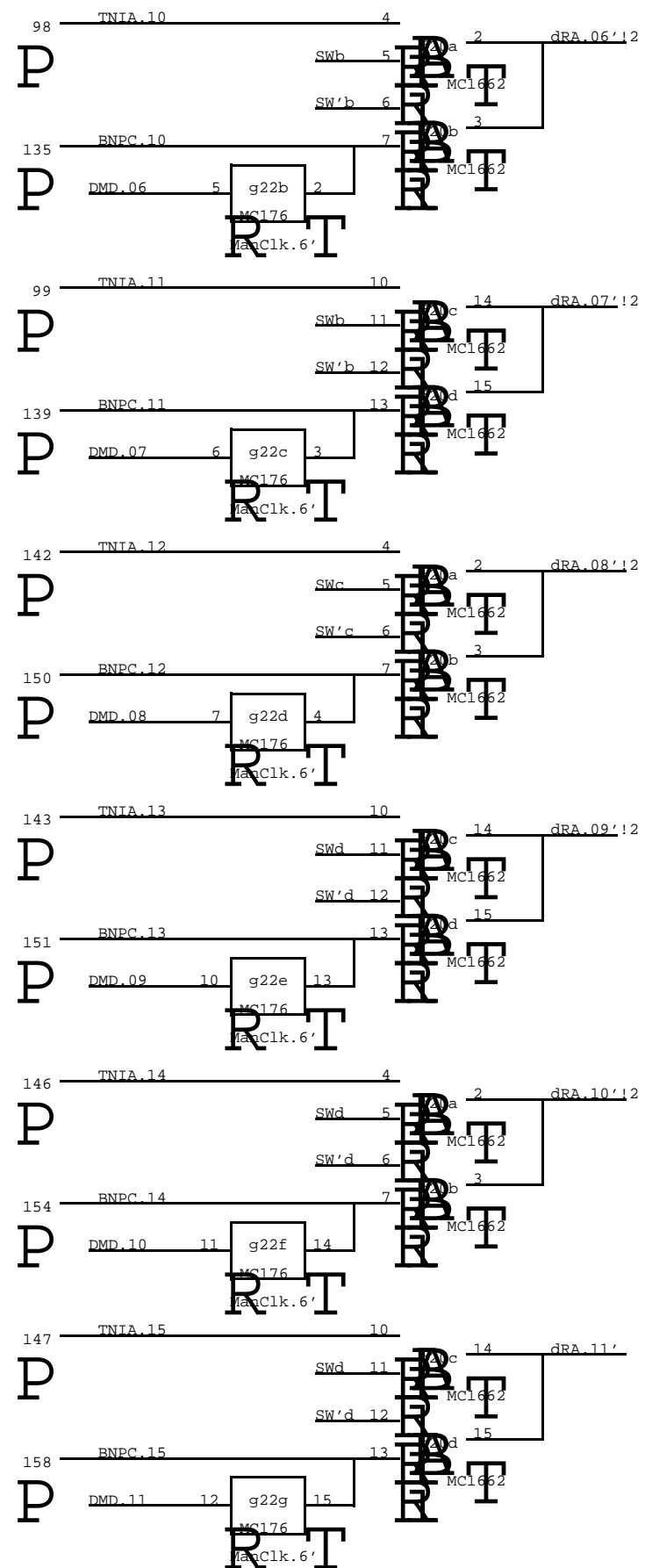
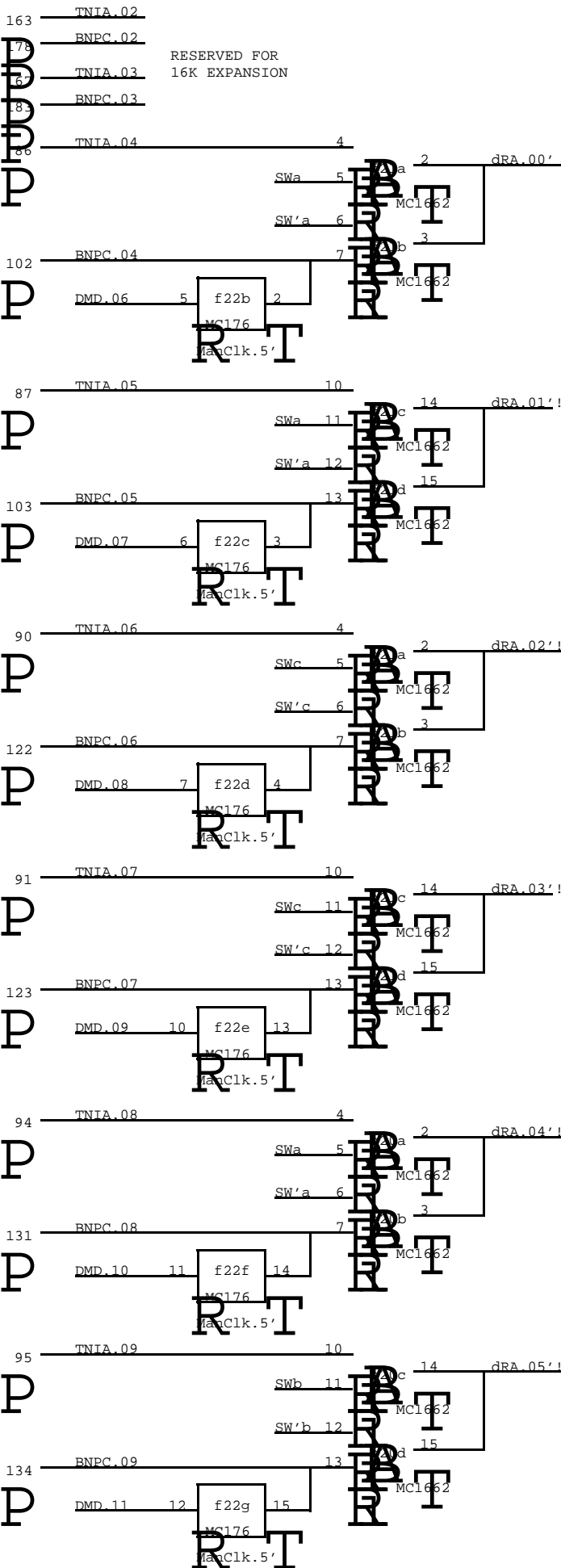


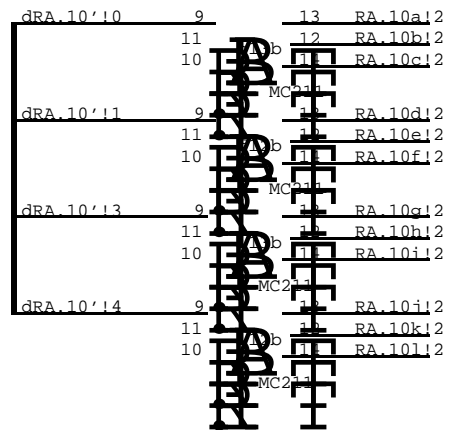
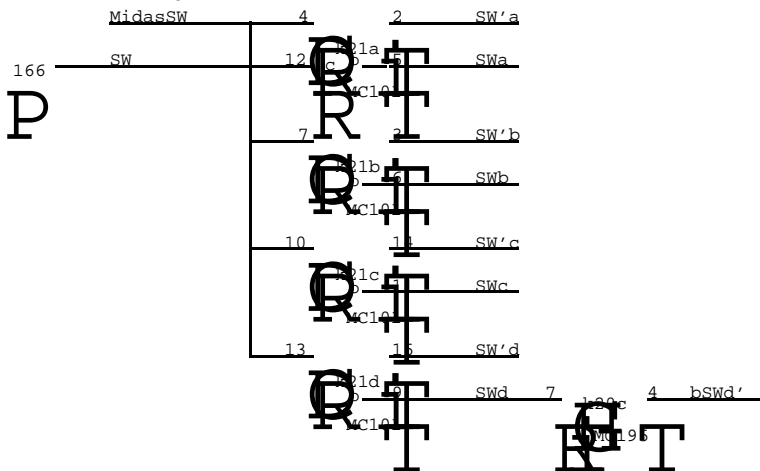
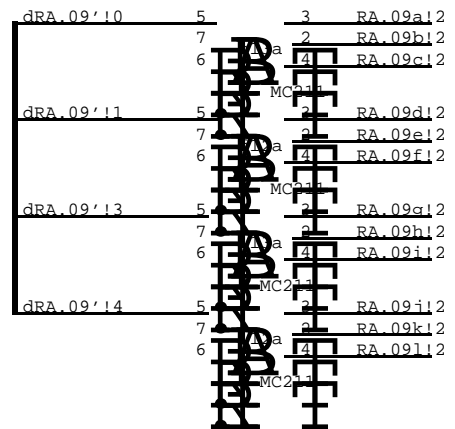
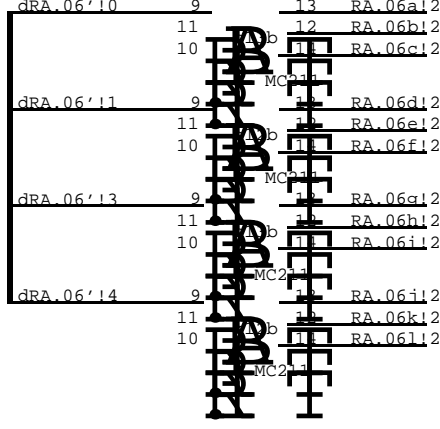
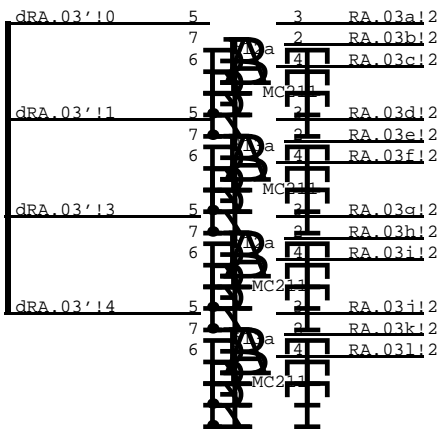
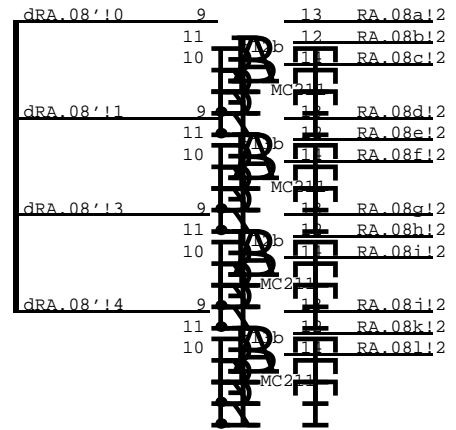
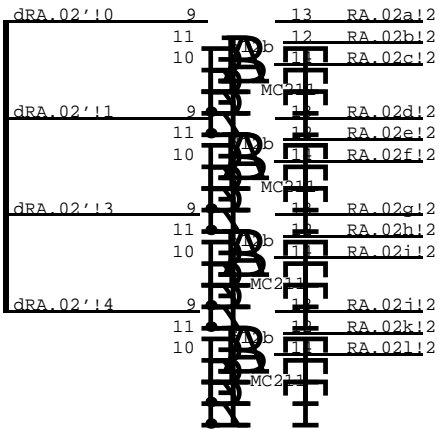
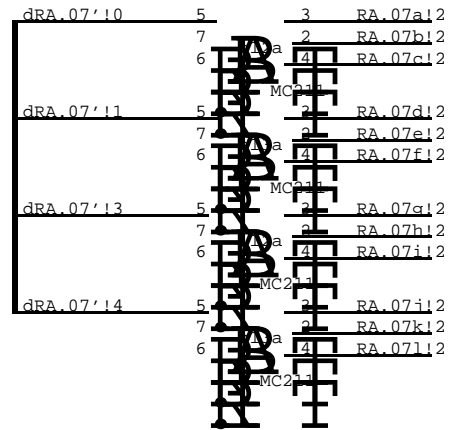
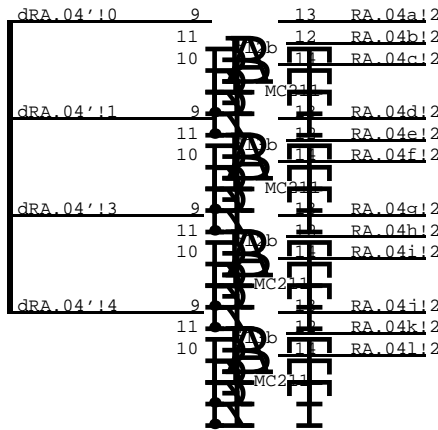
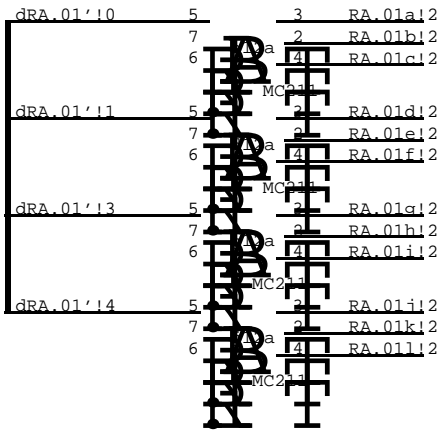
RSTK.1 0 = write odd parity  
 1 = write even parity

RSTK.2:  
 most significant bit

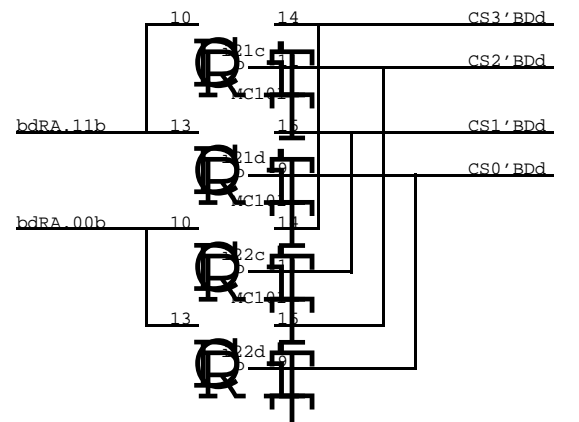
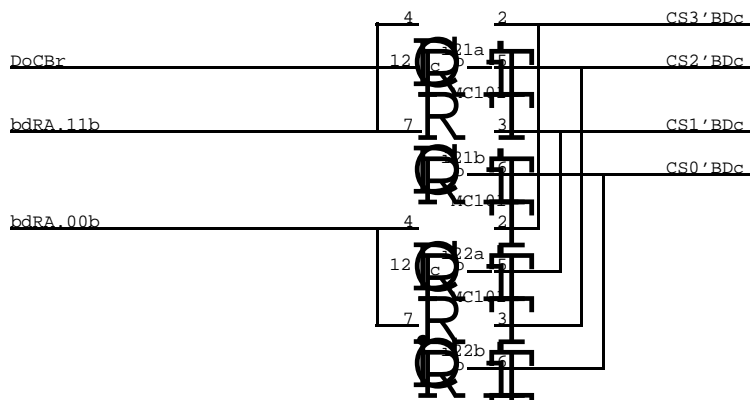
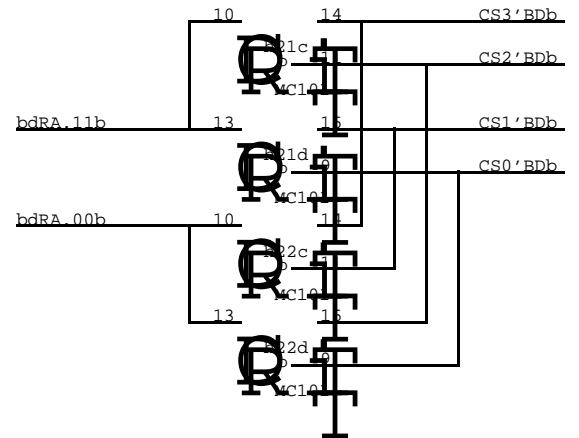
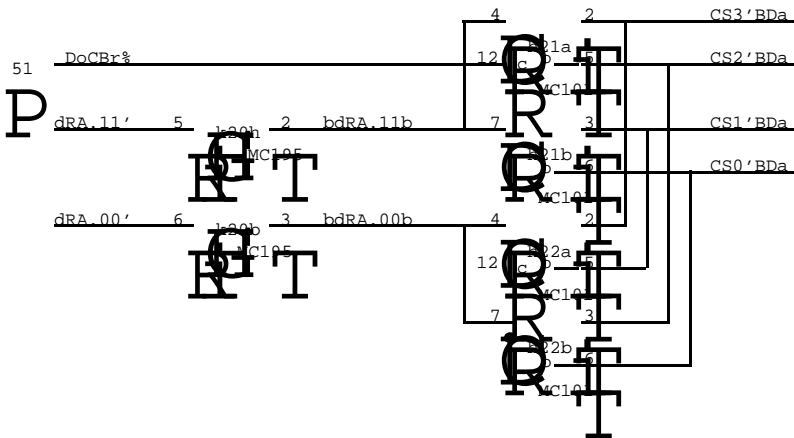
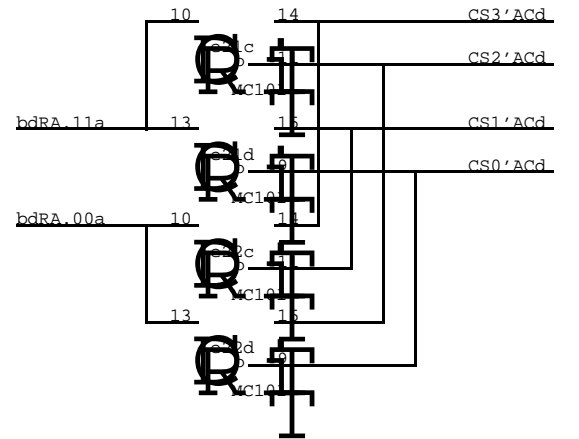
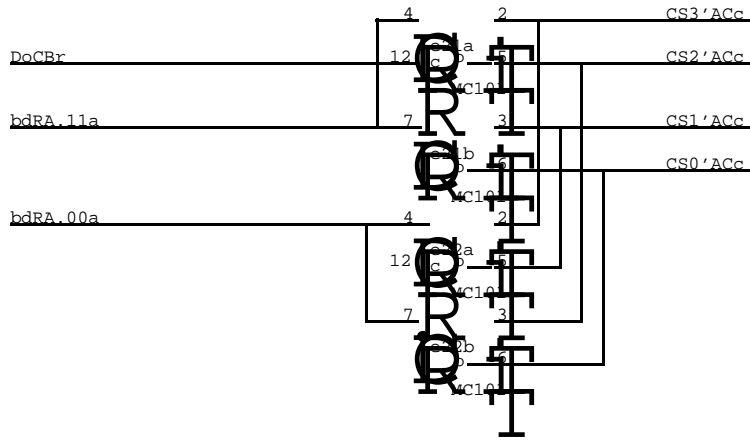
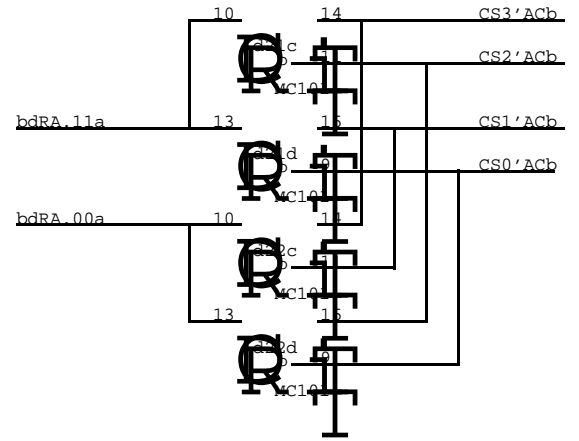
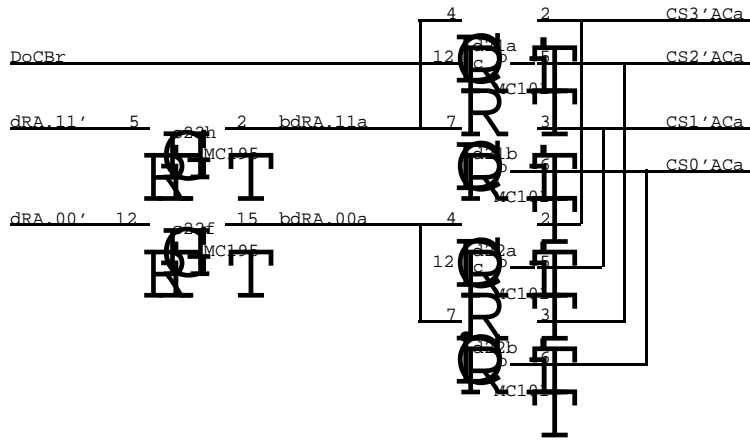




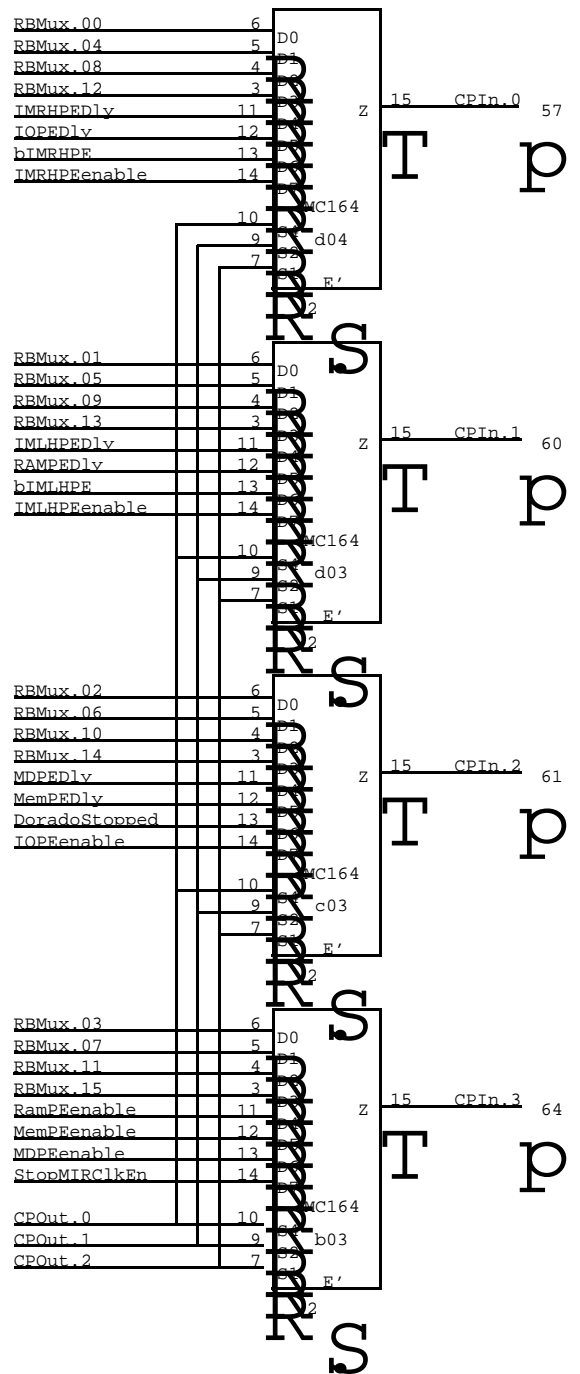
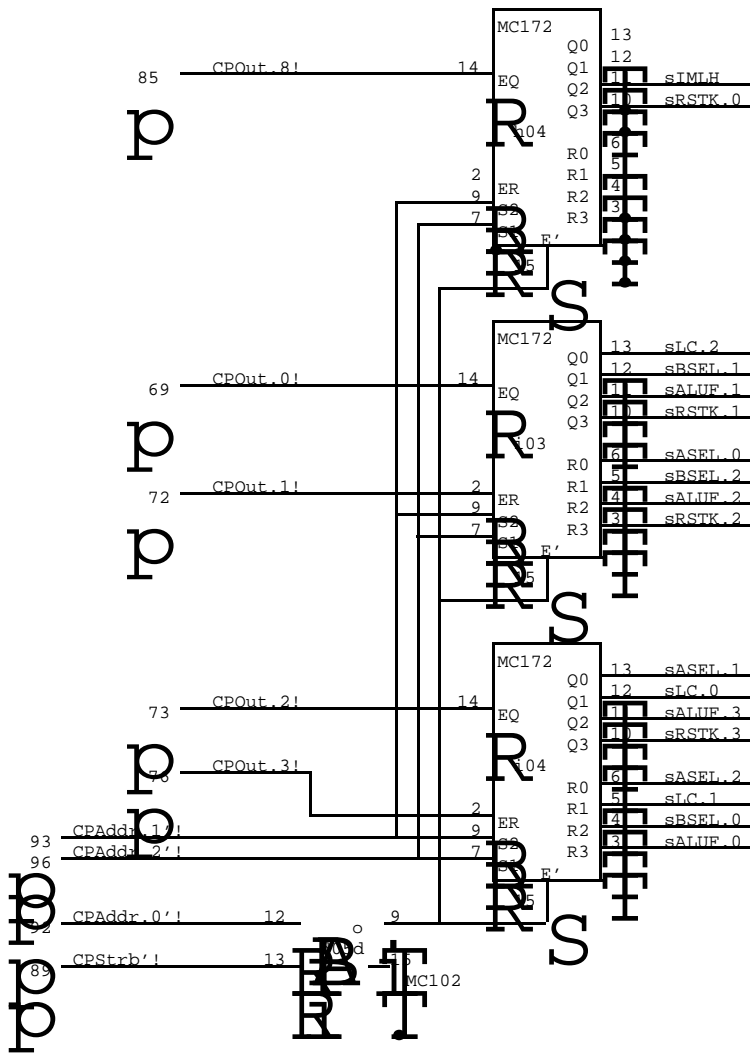


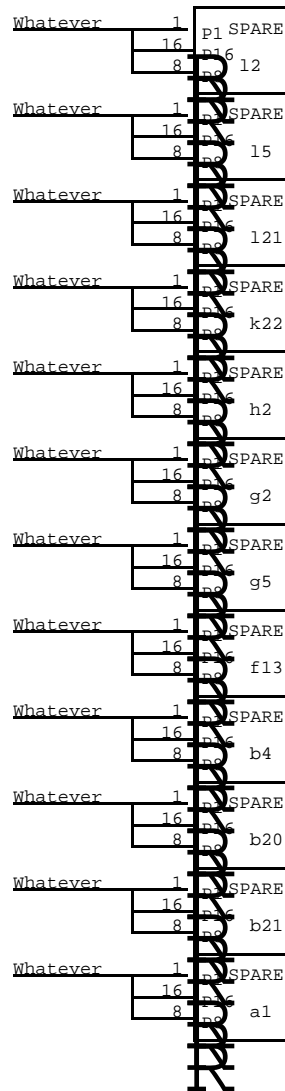
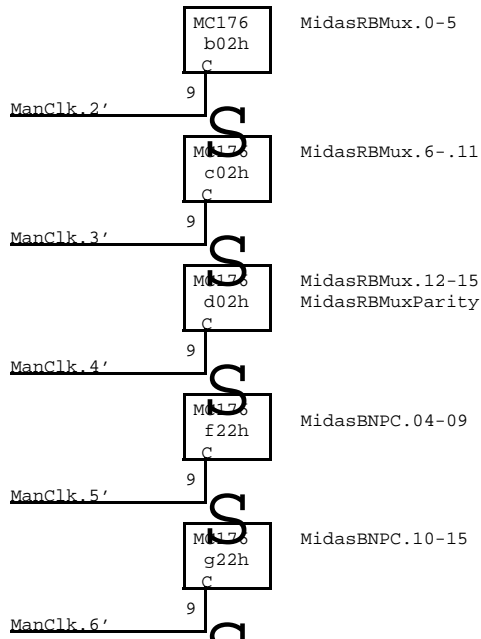
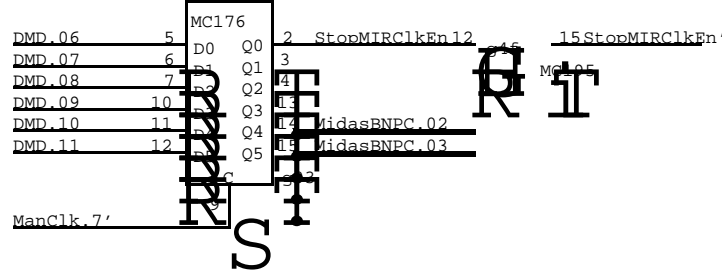
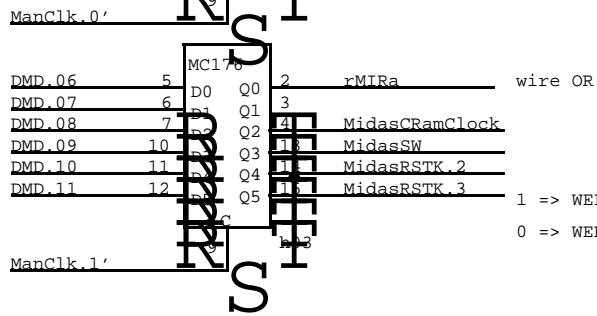
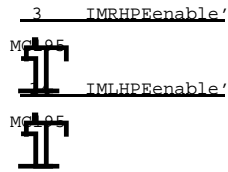
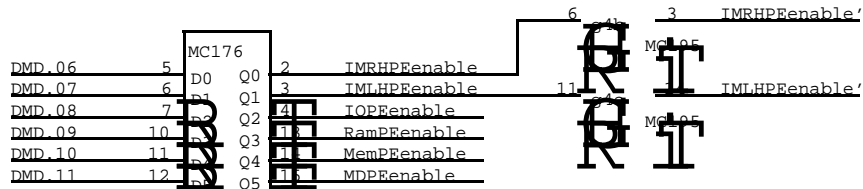




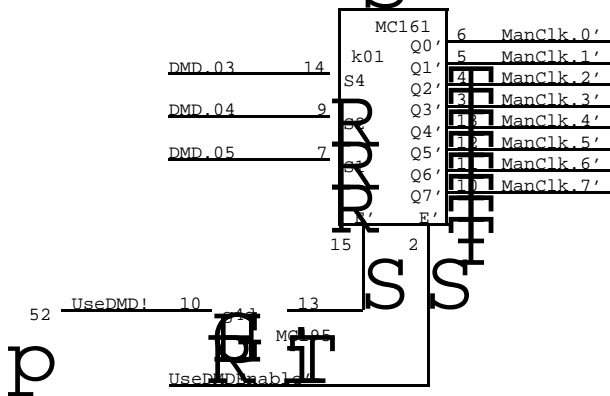




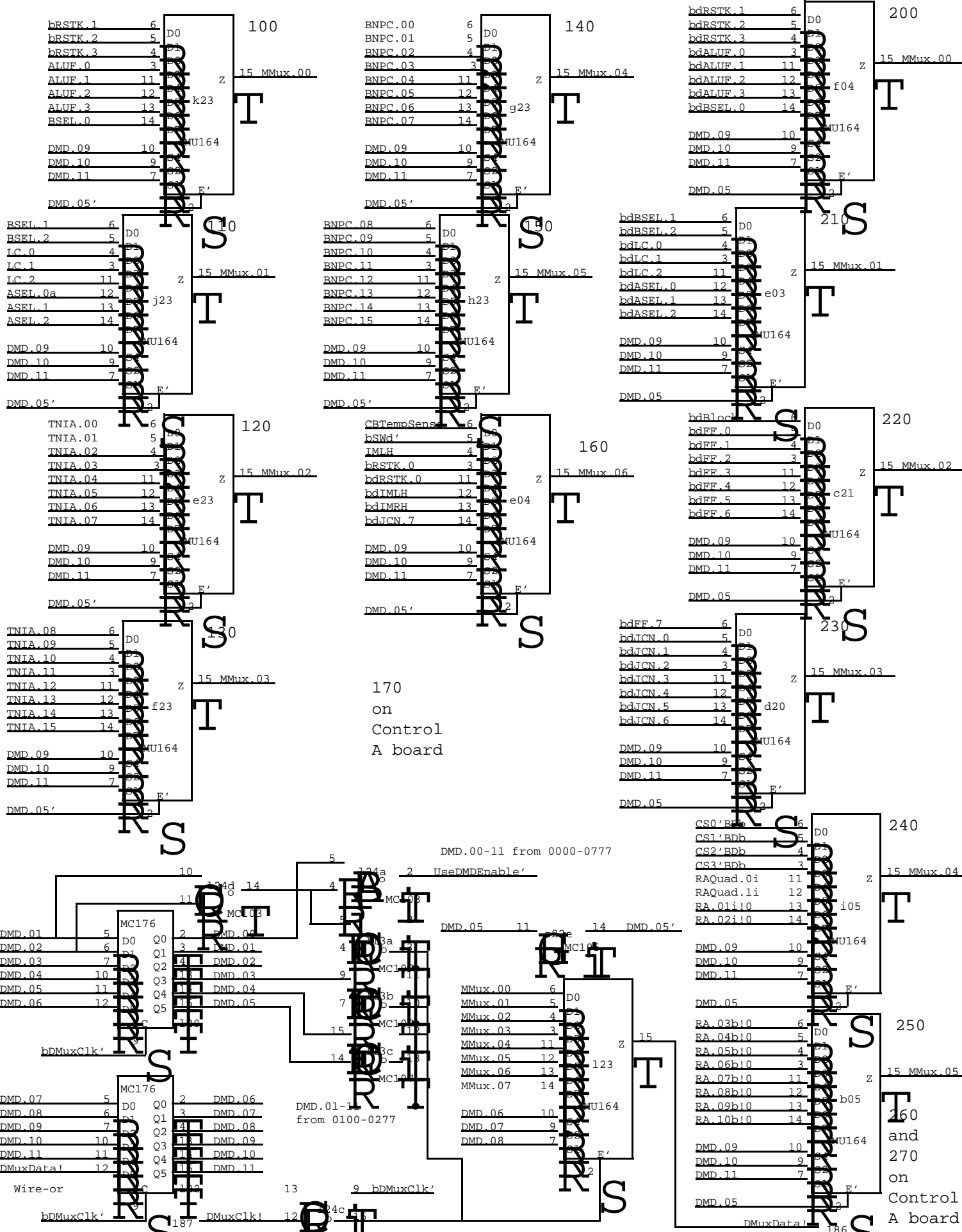


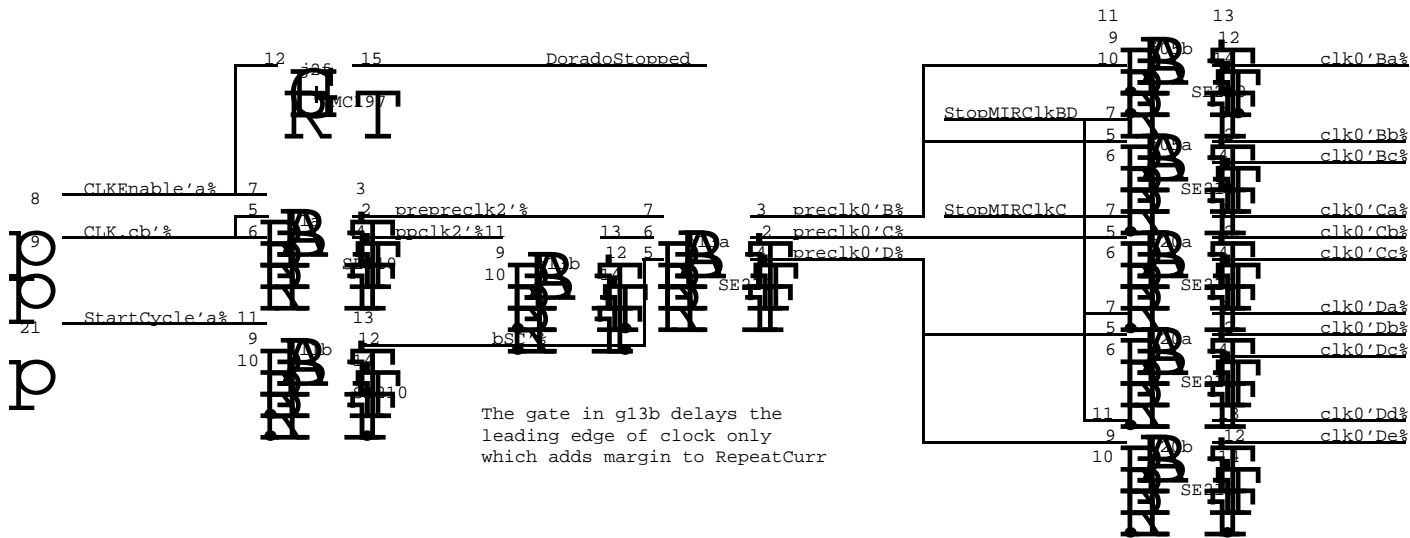


Multiwire spares



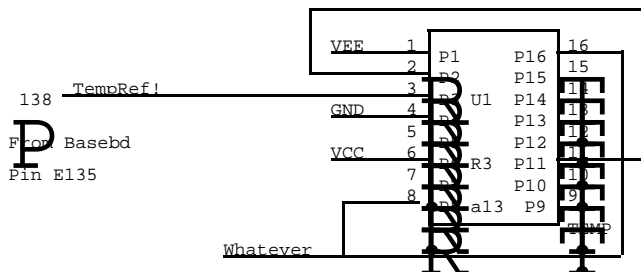
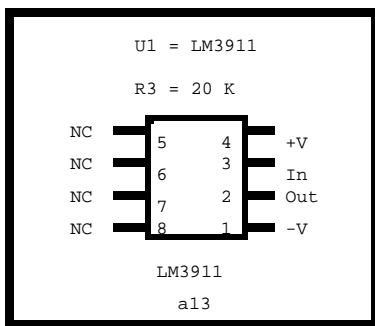
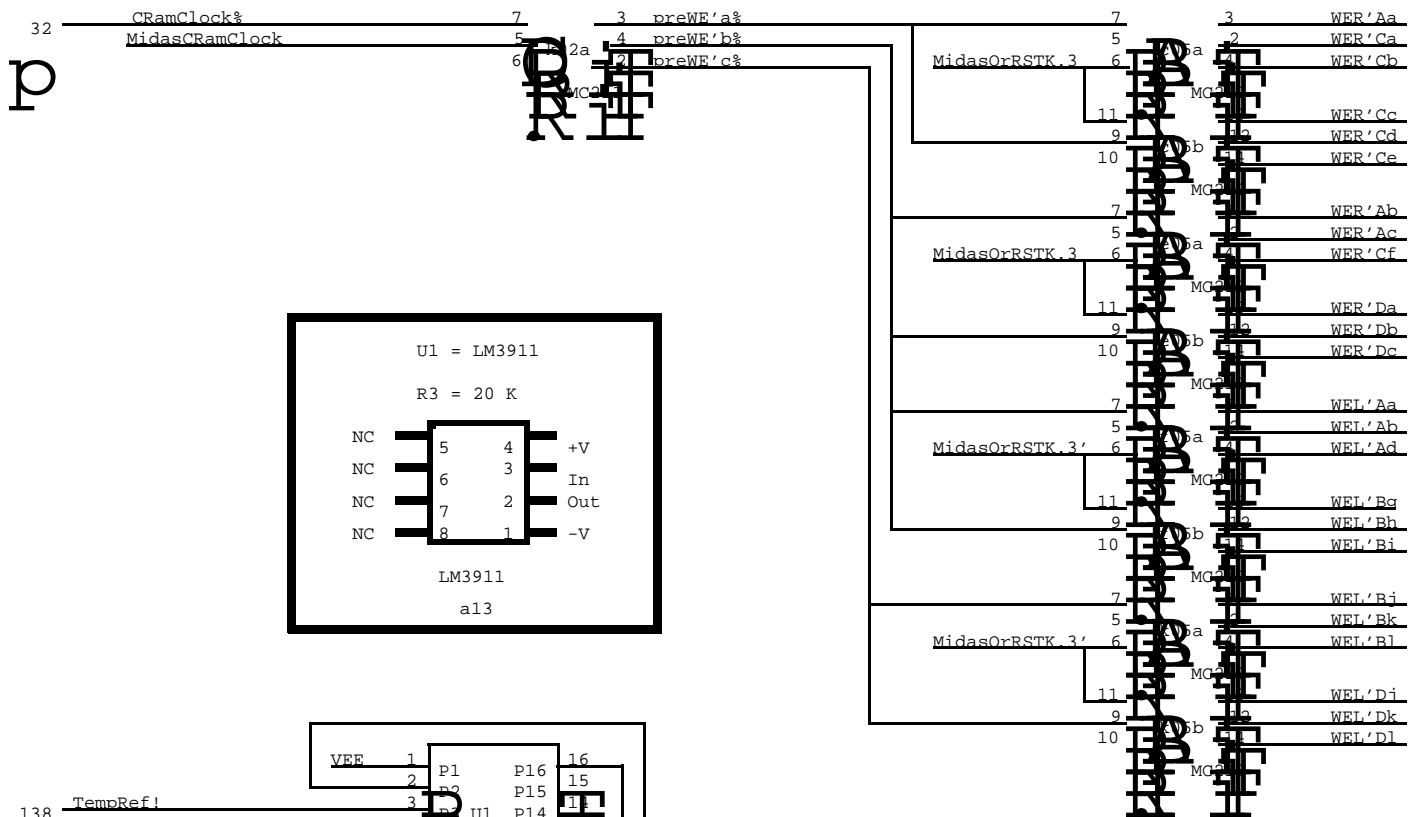
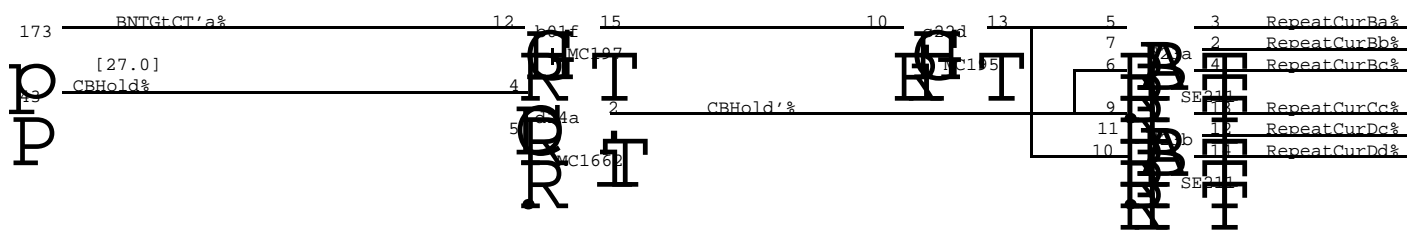
p





The gate in g13b delays the leading edge of clock only which adds margin to RepeatCurr

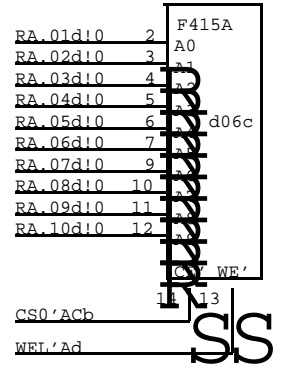
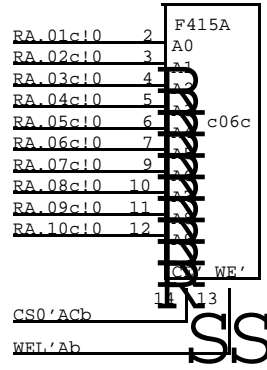
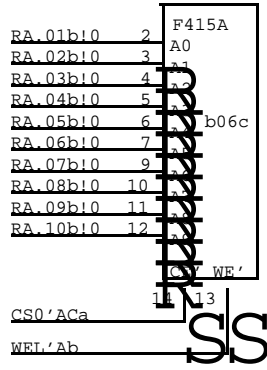
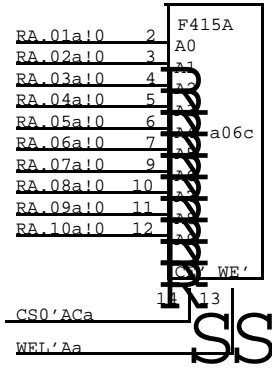
[by 32.5]



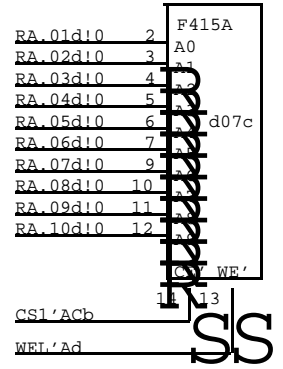
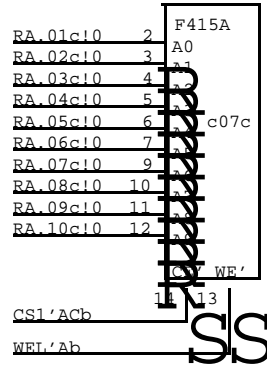
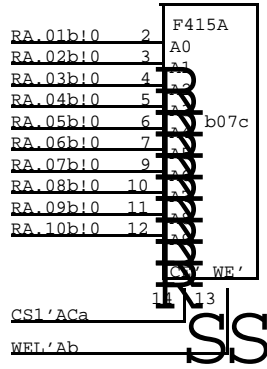
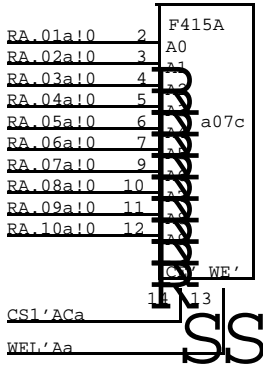
CBTempSense!  
To Muffler Input

XEROX	Project	D1 Control Store	File	Designer	Rev	Date	Page
PARC/CSL	Dorado	Clocks	ContB13.sil	Pier	Da	7/12/79	13

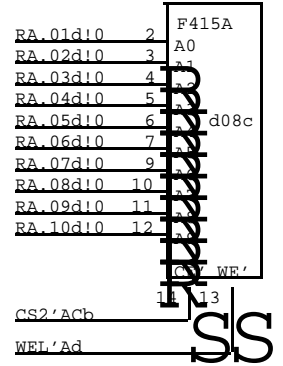
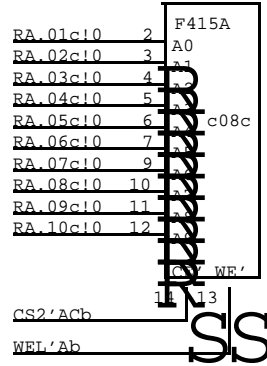
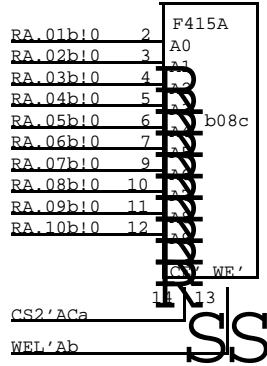
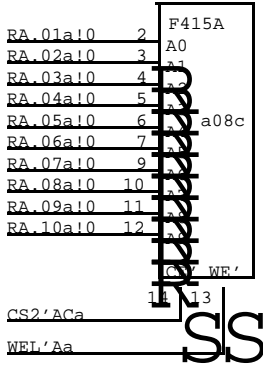
0 to 3777 Even



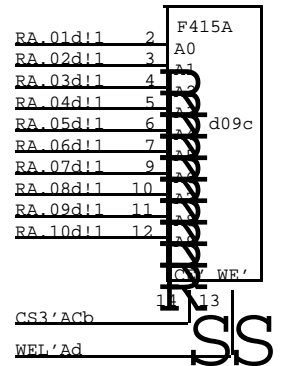
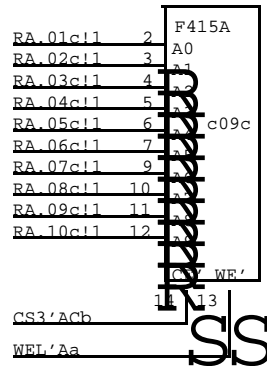
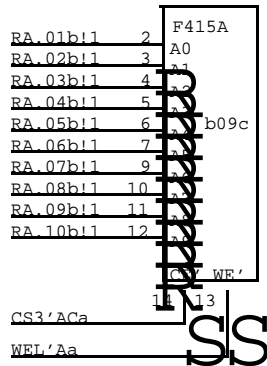
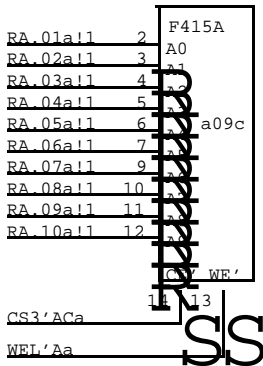
0 to 3777 Odd



4000 to 7777 Even



4000 to 7777 Odd

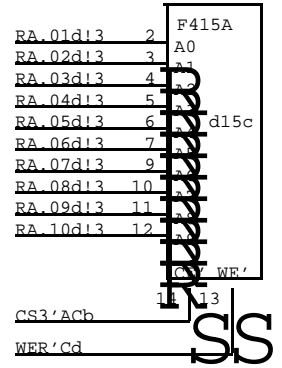
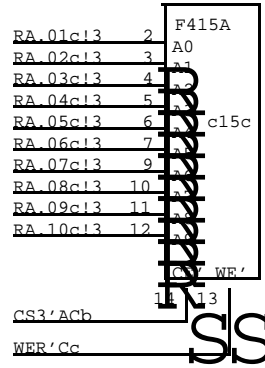
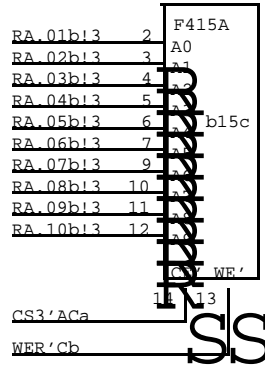
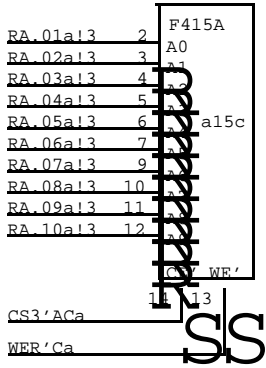
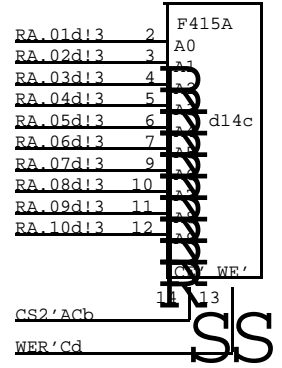
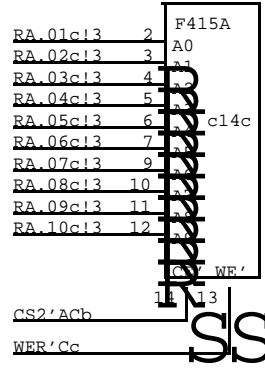
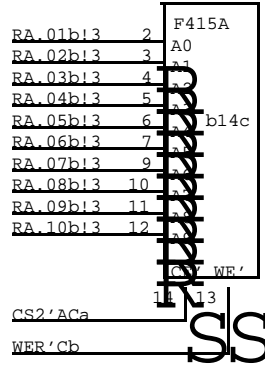
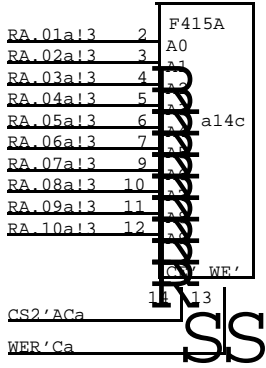
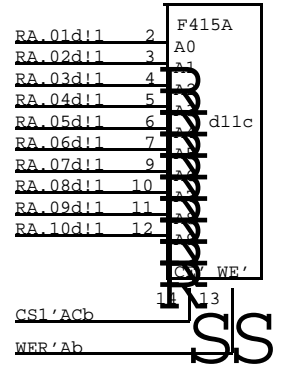
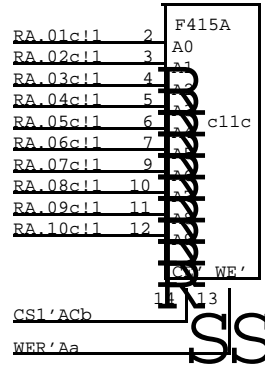
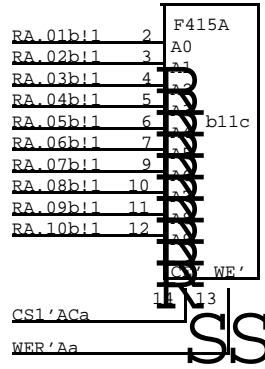
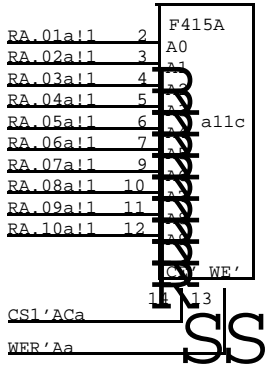
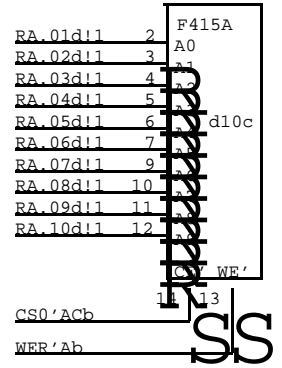
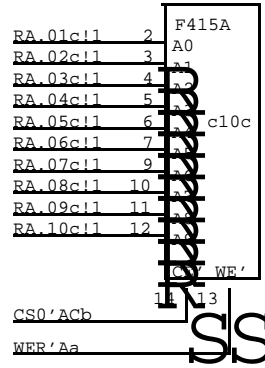
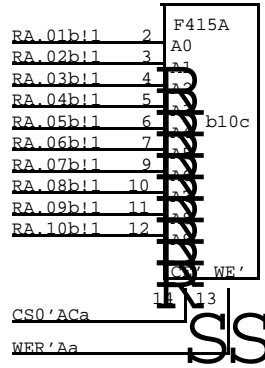
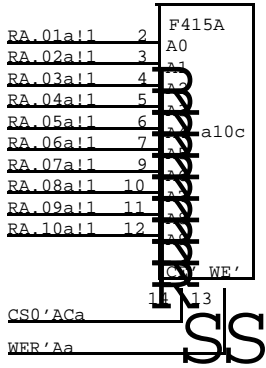


ASEL.0

ASEL.1

ASEL.2

IMLH



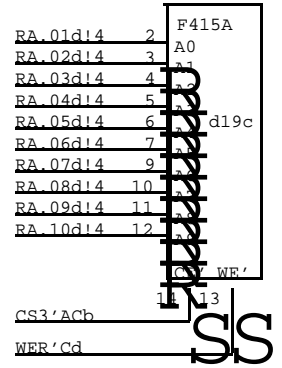
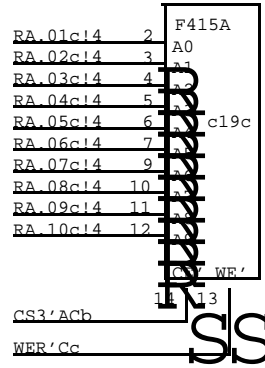
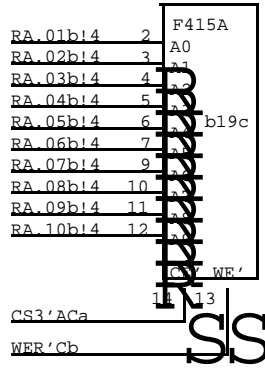
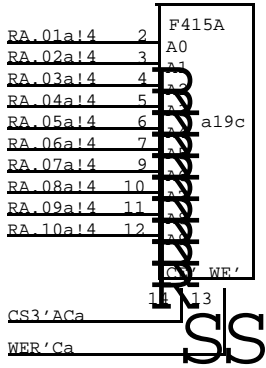
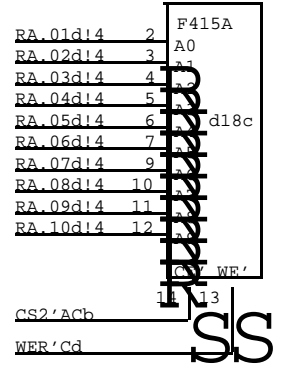
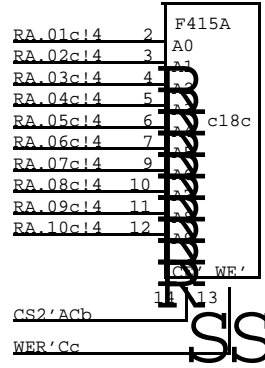
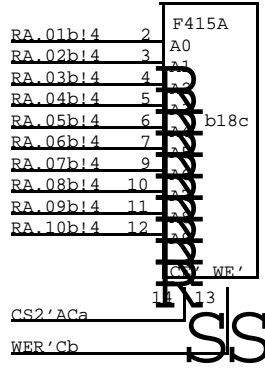
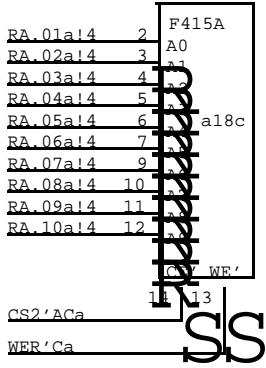
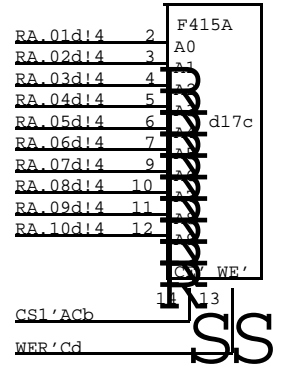
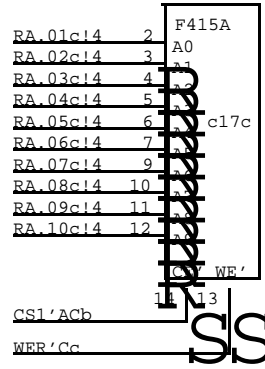
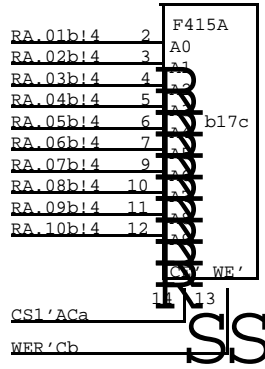
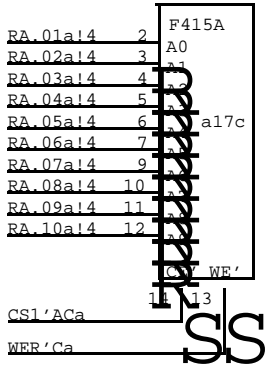
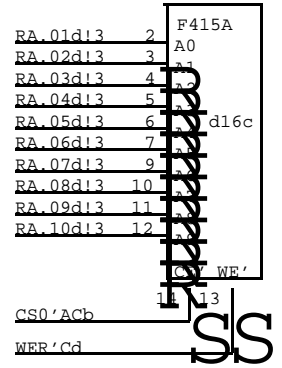
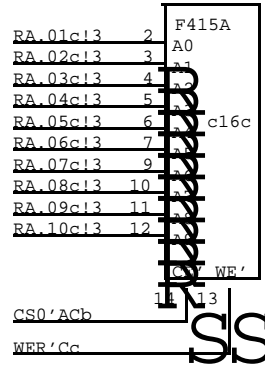
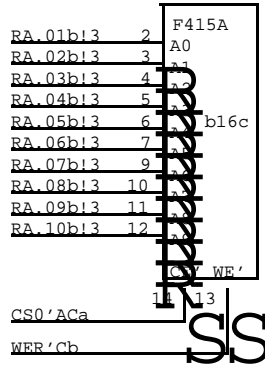
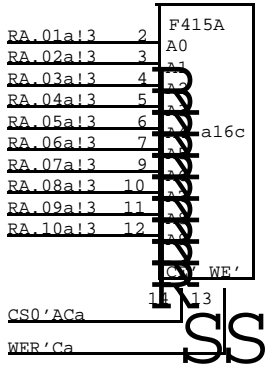
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FF.3



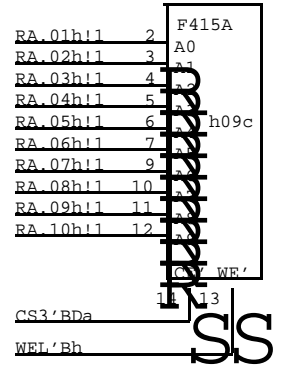
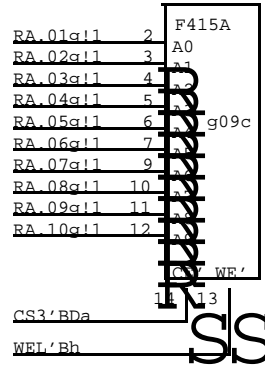
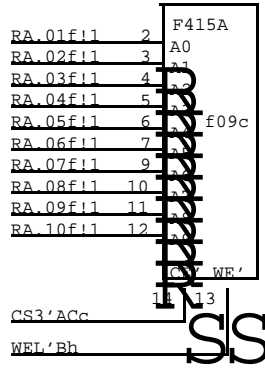
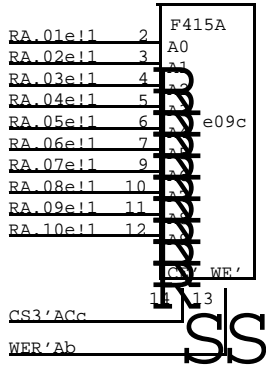
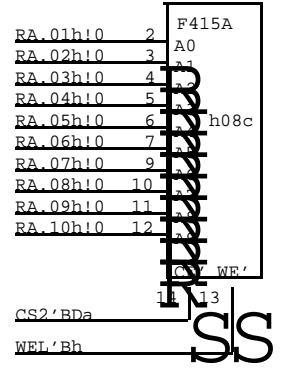
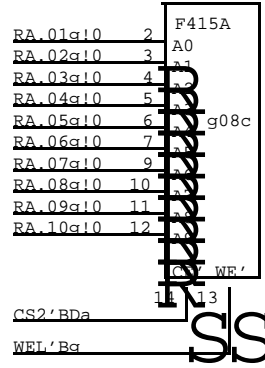
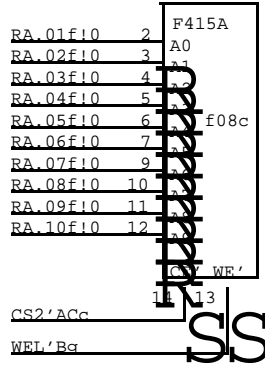
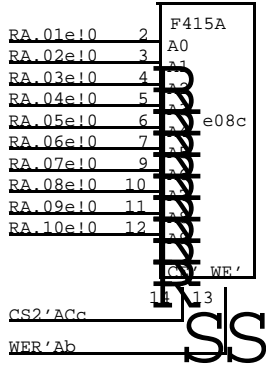
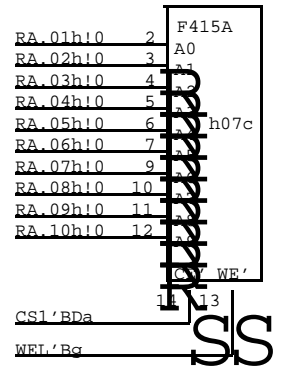
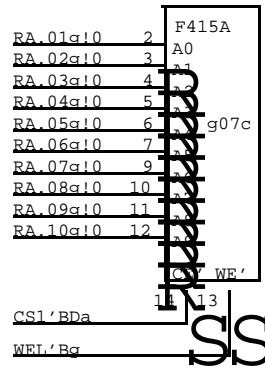
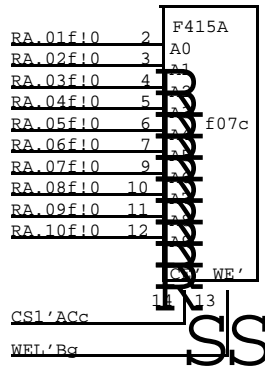
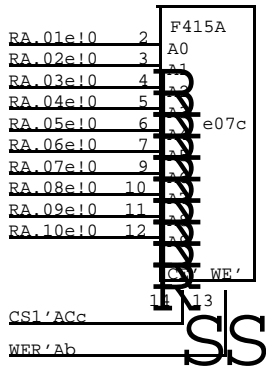
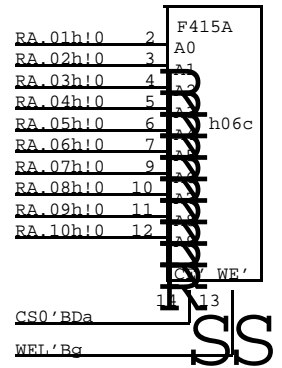
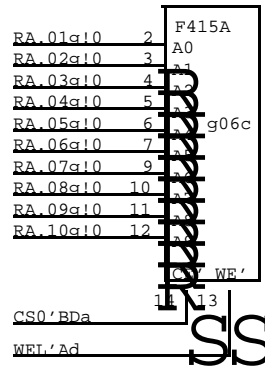
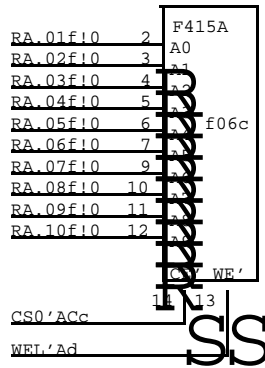
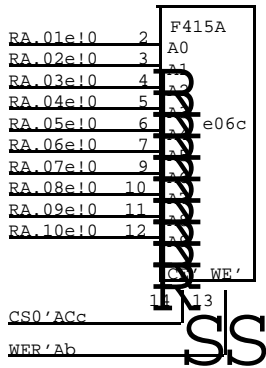


FF.4

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FF.7

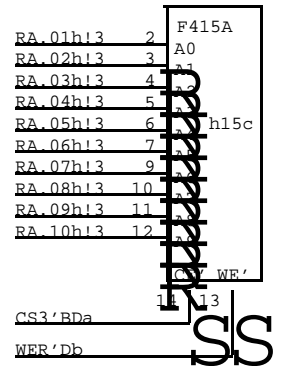
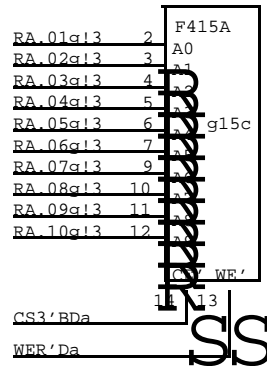
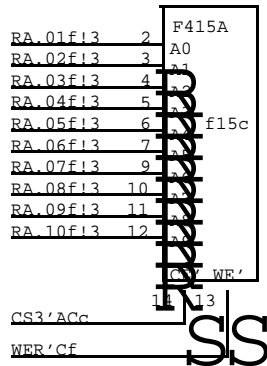
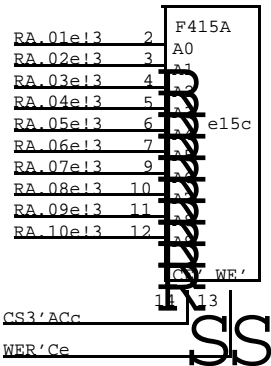
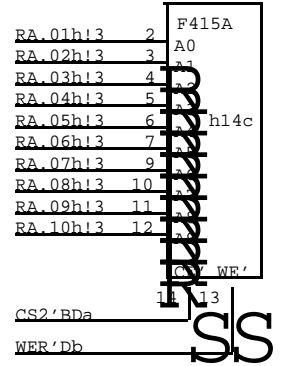
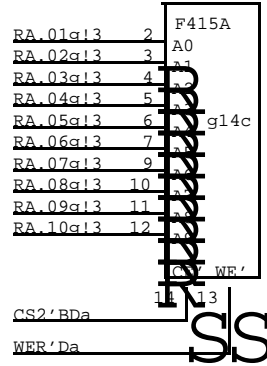
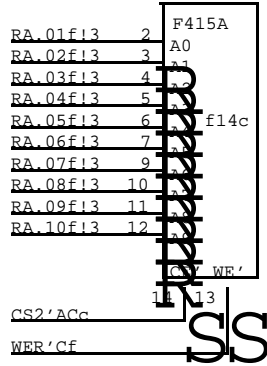
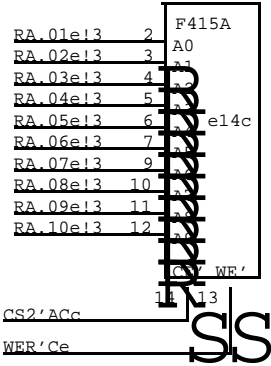
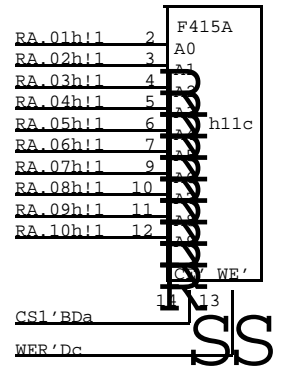
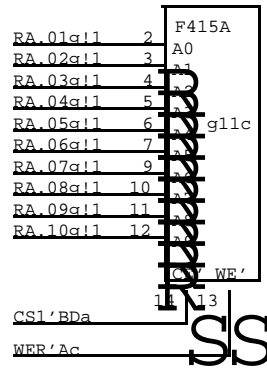
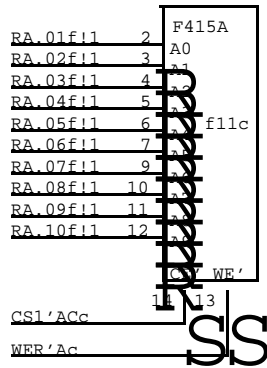
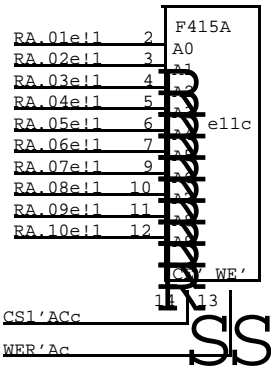
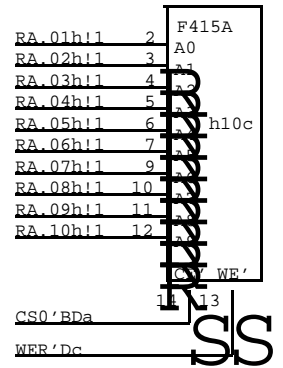
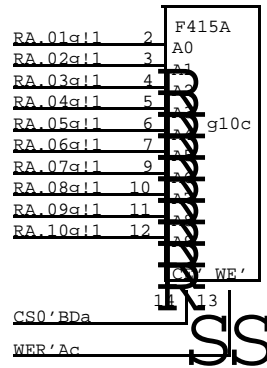
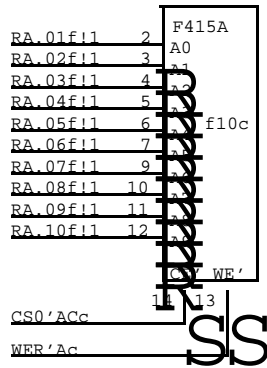
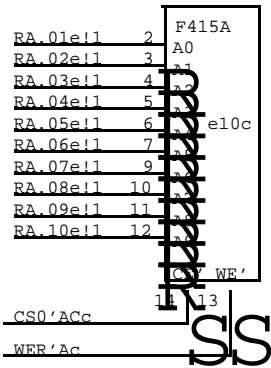


JCN.0

BSEL.0

BSEL.1

BSEL.2

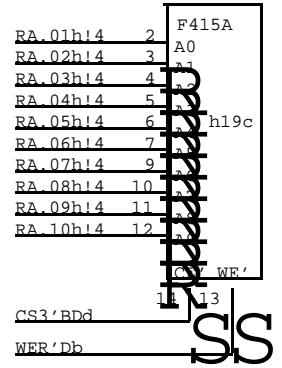
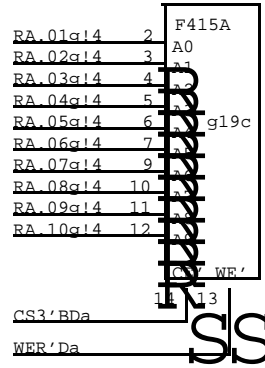
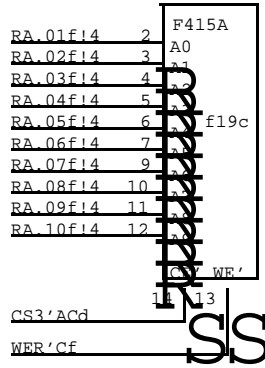
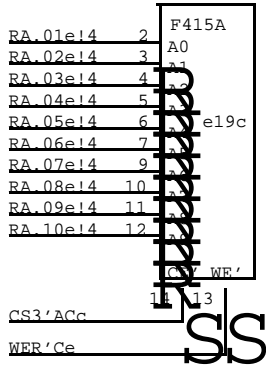
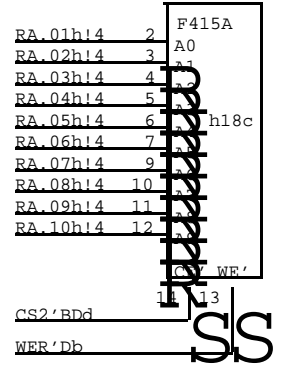
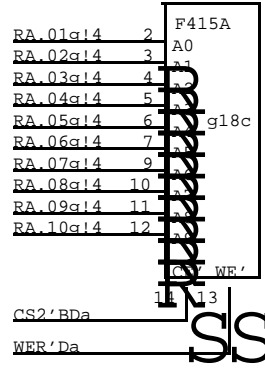
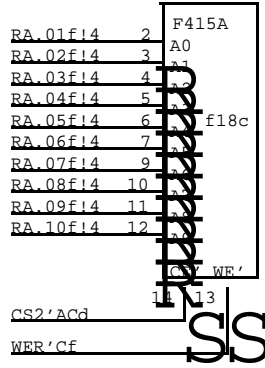
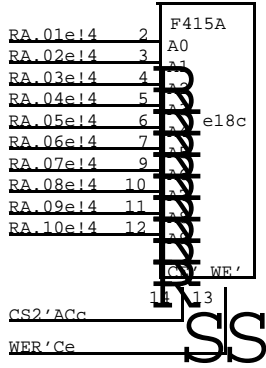
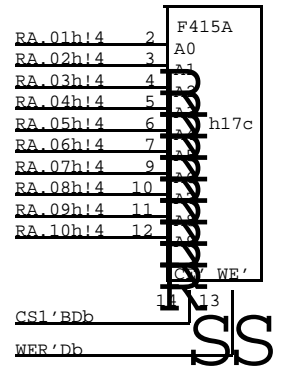
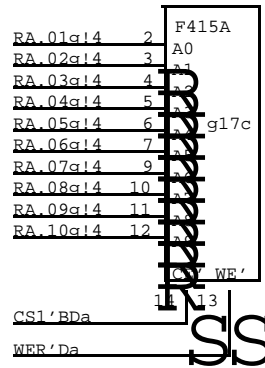
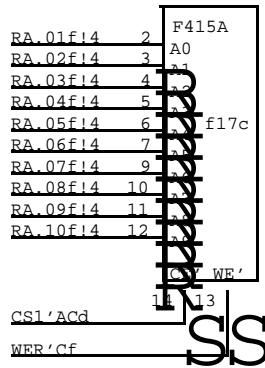
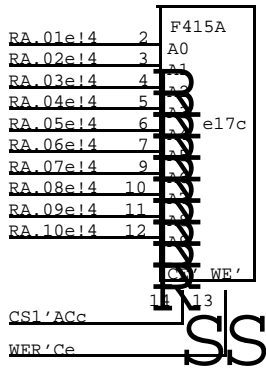
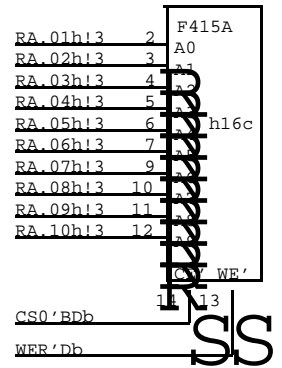
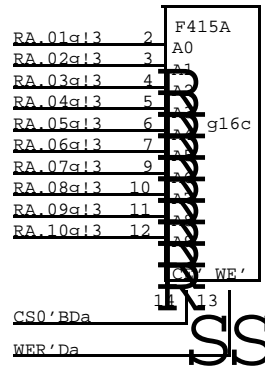
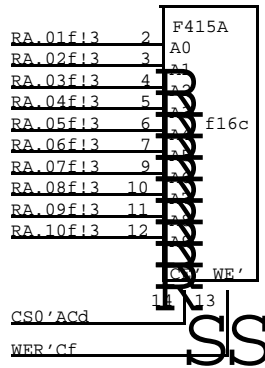
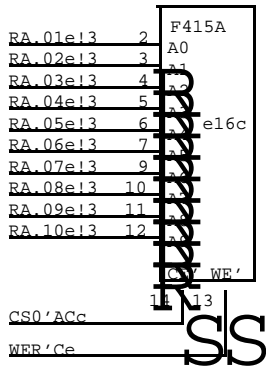


JCN.1

JCN.2

JCN.3

JCN.4



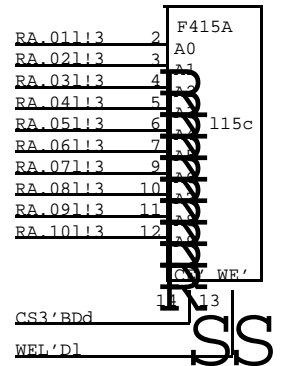
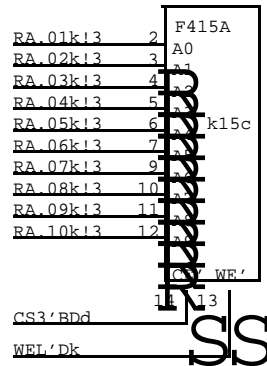
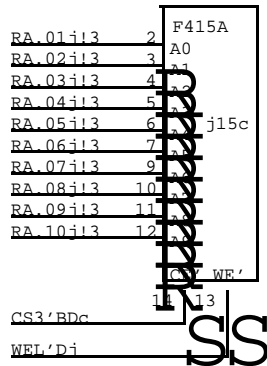
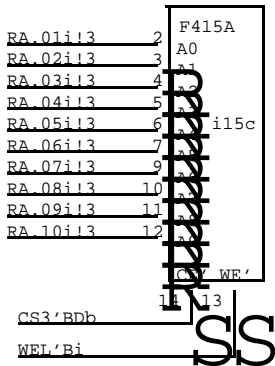
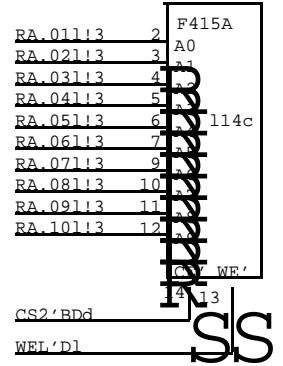
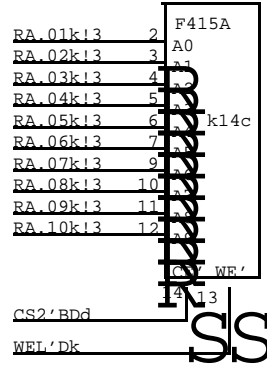
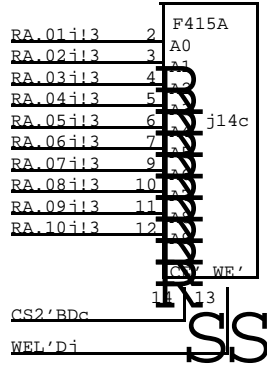
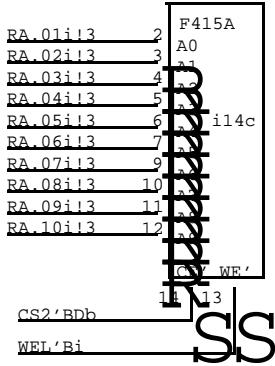
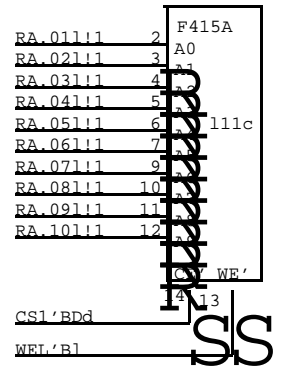
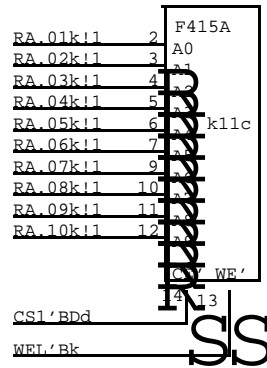
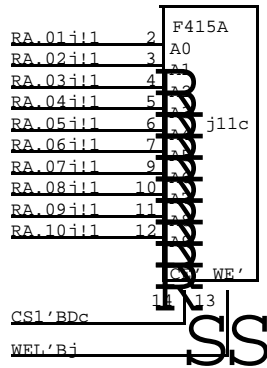
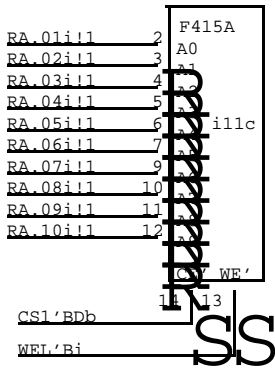
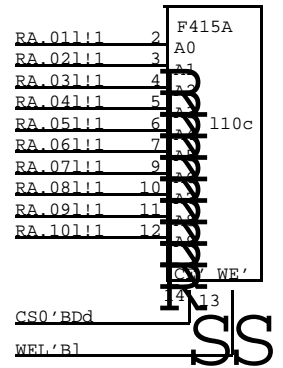
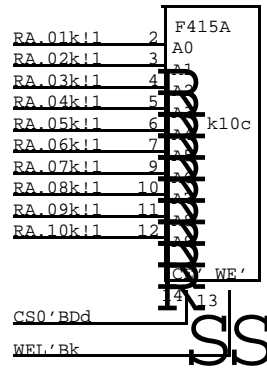
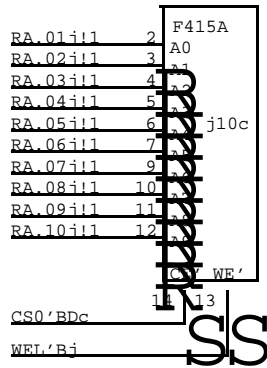
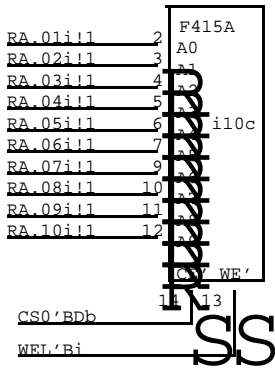
IMRH

BLK'

JCN.5

JCN.6





ALUF.0

ALUF.1

ALUF.2

ALUF.3



A	a 181	b 168	c 153	d 137	e 124	f 109	93 g	80 h	64 i	48 j	33 k	20 l	B
1	BMrcvr 1,1,1,1,1,1 197	BMrcvr 197	BMrcvr 3,3,3,3,3,4 197	PAR TREE 170	dIMOut 08 & 09 174	dIMOut 03 174	ASEL,0' 3,b mem 231	RSTK2-3 231	RSTK0-1 231	Man Clk 161	CLK 210		1
2	ManClk2 1,1,1,1,1,1 176	ManClk3 2,2,2,2,2,2 176	ManClk4 3,3,3,3,3,3 176	dIMOut 10 & 11 174	dIMOut 06 & 07 174			1,1,1,1 9,9 195	bdRSTK.x 1,1,1,1, 197	CRAMClk 11,9 211			2
3	CPI.3 164	CPI.2 164	CPI.1 164	MU bdxxx 164	dIMOut 04 & 05 174	ManClk.7 176	MidasSW 176	SetMIR 172	Err bRSTK 105	ERROR 104	STUFF 121		3
4		PEEnbl 176	CPI.0 164	MU dxxx 164	MU dxxx 164	13,5,13 13,13,h 195	SetMIR 172	SetMIR 172				5*9,G 176	4
5	MU RA 164	WER 'A & 'C 210	CBStrb/Par 3,b,c,10 102	WER 'A & 'D 210	WEL 'A & 'B 210		MU CPBus 164	MU RA,CS 164	Clk0'Bx 11,b 210	WEL 'B & 'D 210			5
6	F415A 0000 to 3777 Even		F415A 0	F415A 0	F415A 0	F415A 0			F415A 0				6
7	ASEL 0000 to 3777 Odd		IMLH 1	JCN 1		BSEL 1			RSTK 1				7
8	0 4000 to 7777 Even	1 2	2 2	3 2	0 2	0 2	1 2	2 2	0 2	1 2	2 2	3 2	8
9	4000 to 7777 Odd												9
10													10
11	FF 1			JCN 1	JCN 1	JCN 1	JCN 1		ALUF 1				11
12	RA 211	RA 211	RA 211	RA 211	RA 211	RA 211	RA 211	RA 211	RA 211	RA 211	RA 211	RA 211	12
13	TEMP SENSE	RA 211	RA 211	RA 211	RA 211		preclk0 11,b 210	RA 211	RA 211	RA 211	RA 211	Midas 107	13
14	0 2	1 2	2 2	3 2	1 2	2 2	3 2	4 2	0 2	1 2	2 2	3 2	14
15													15
16	F415A 0		F415A 0	F415A 0	F415A 0		F415A 0		F415A 0				16
17	FF 1			IMRH 1	BLK' 1		JCN 1		LC 1				17
18	4 2	5 2	6 2	7 2			5 2	6 2	7 2	0 2	1 2	2 2	18
19													19
20		CLK0'Cx 11,b 210	MU bdxxx 164	dRA 04' & 05' 1662	dRA 06' & 07' 1662	dRA 08' & 09' 1662	dRA 10' & 11' 1662	CLK0'Dx 210	PRITY 170	INV 8,7,4,d,e,g 195	Midas 176		20
21		MU bdxxx 164	CSEL 101	CSEL 101	dRA 00' & 01' 1662	dRA 02' & 03' 1662	CSEL 101	CSEL 101	PRITY 170	MidasSW 101			21
22	dXXXBuf 3,3,3,4,4,4 197	INV 8,4,4,11, 195	CSEL 101	CSEL 101	MidasBNPC ManClk5 176	MidasBNPC ManClk6 176	CSEL 101	CSEL 101	dXXXBuf 1,1,2,2,e,f 197		Midas 176		22
23	Local ASEL 3,c 231	dXXXBuf 4,4,4,4,4,5 197	RepeatCur 211	TNIA MU 164	TNIA MU 164	BNPC MU 164	BNPC MU 164	dXXXBuf 2,2,3,3,2,2 197	MU MIR 164	MU MIR 164	Midas 164		23
24	ASEL 0-1 231	ASEL 2 IMLH 231	b,c,d CbHold 1662	dXXXBuf 5,5,3,4,e,f 197	dXXXBuf 5,5,3,4,e,f 197	BSEL 0-1 231	BSEL2,LC0 231	LC 1-2 231	ALUF 0-1 231	ALUF 2-3 231	12,b,12 ,12 103		24
C	a 11	b 26	c 39	d 55	e 70	f 86	99 g	114 h	129 i	143 j	159 k	174 l	D