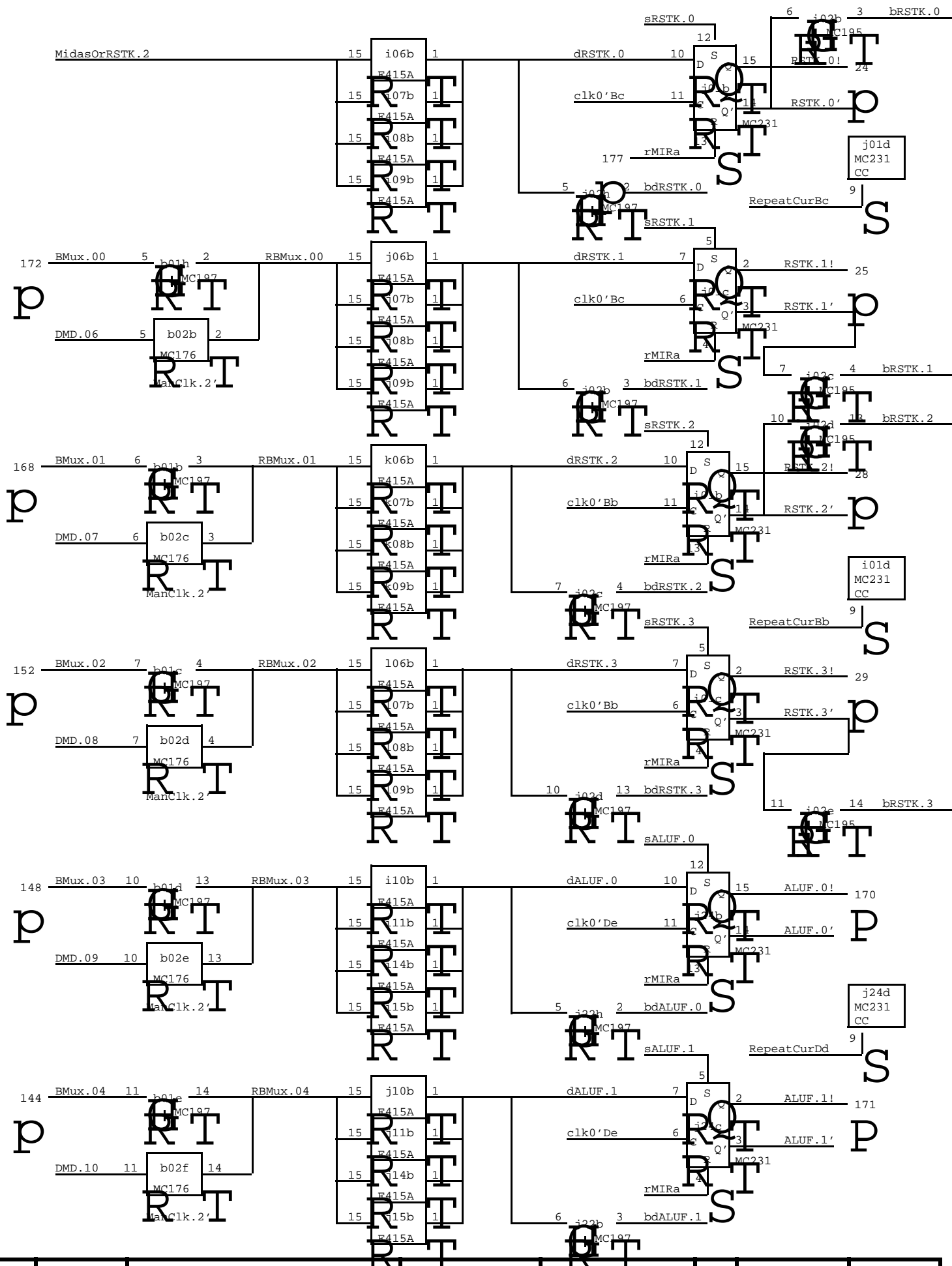


D O R A D O   S C H E M A T I C S

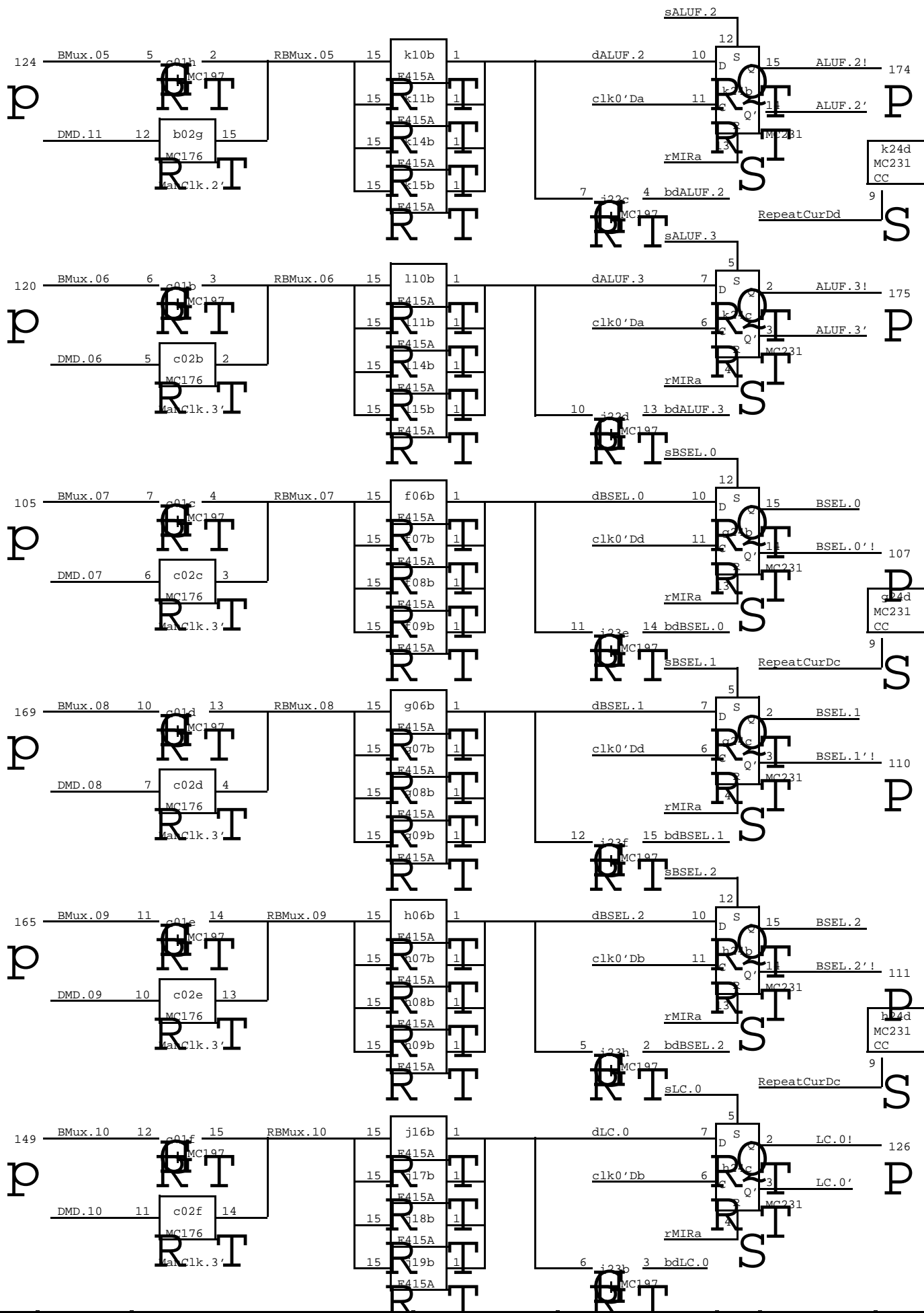
C o n t r o l   B

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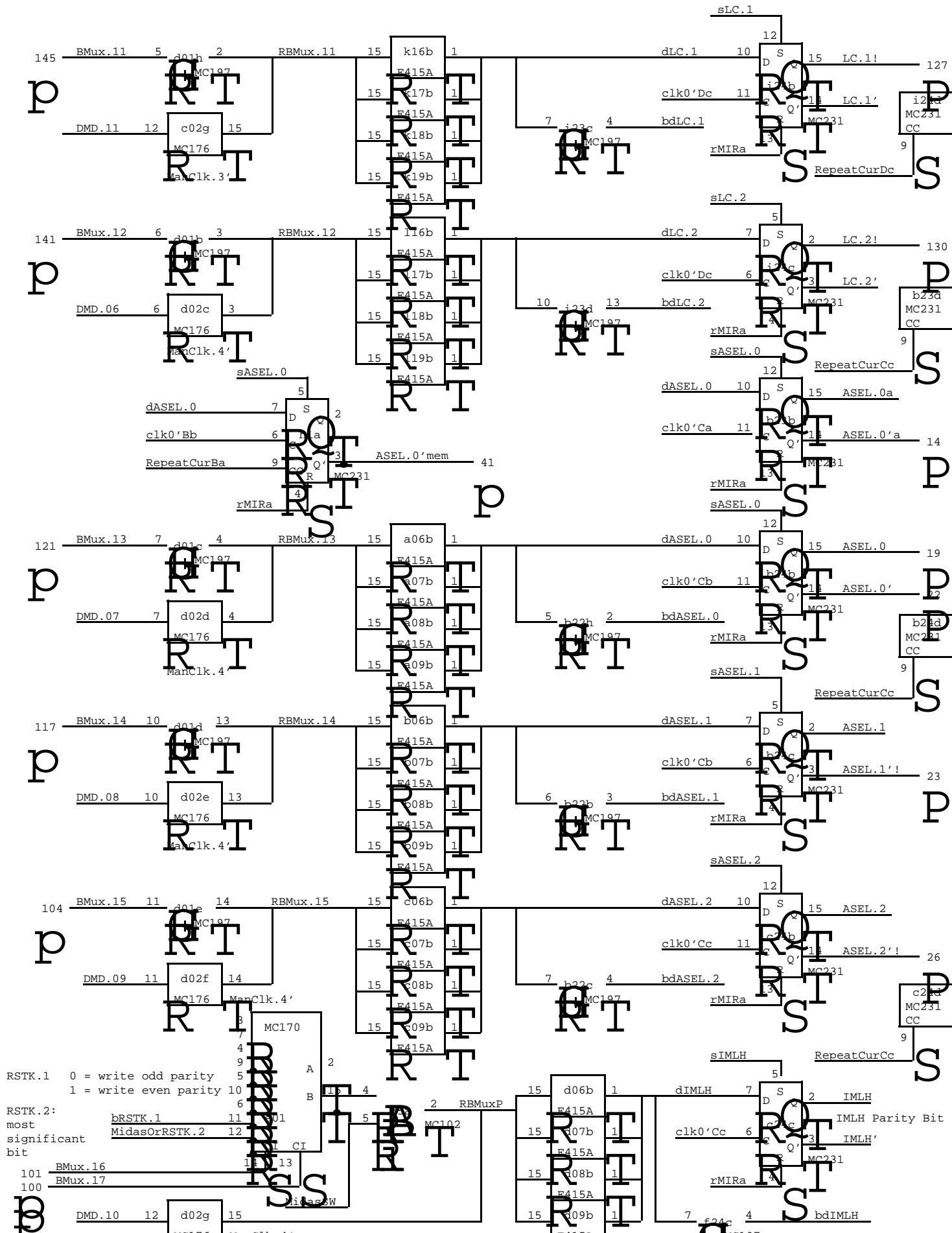
<u>TITLE</u>	<u>Page</u>
Control Store Bit Slice <u>00 to 05</u>	01
Control Store Bit Slice <u>06 to 11</u>	02
Control Store Bit Slice <u>12 to 17</u>	03
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XEROX PARC/CSL	Project Dorado	Dl Control Store Bit Slice 00-05	File ContB01.sil	Designer Pier	Rev Cd	Date 7/12/79	Page 01
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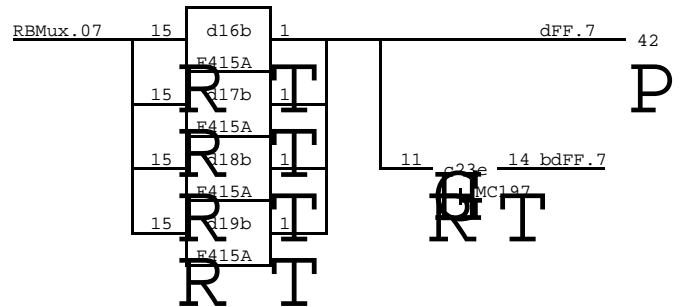
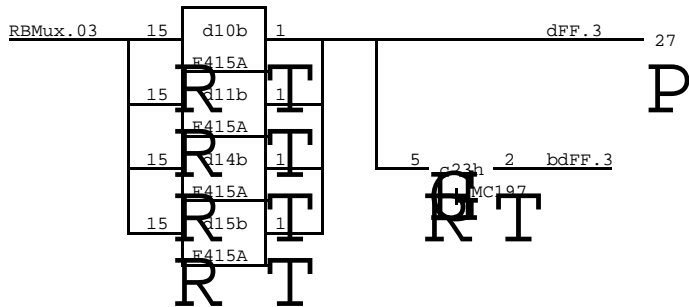
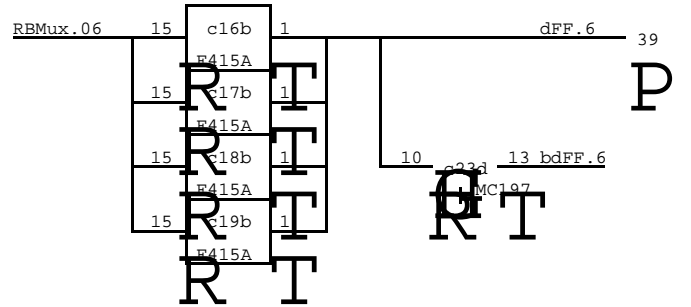
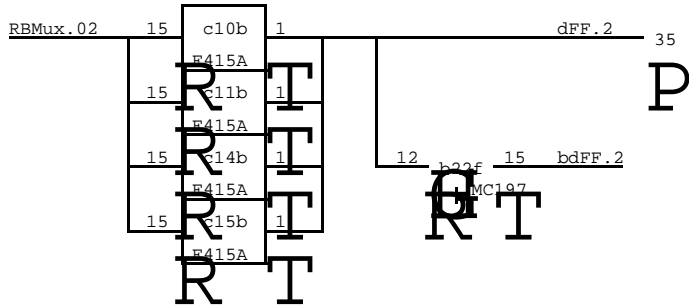
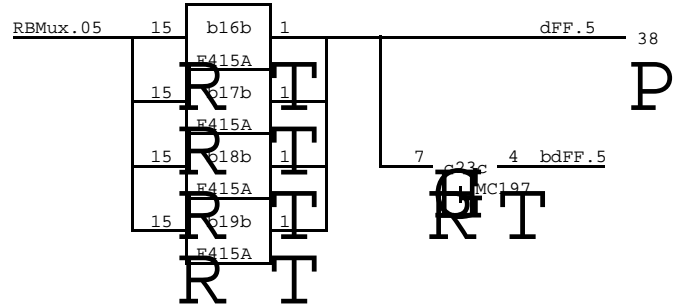
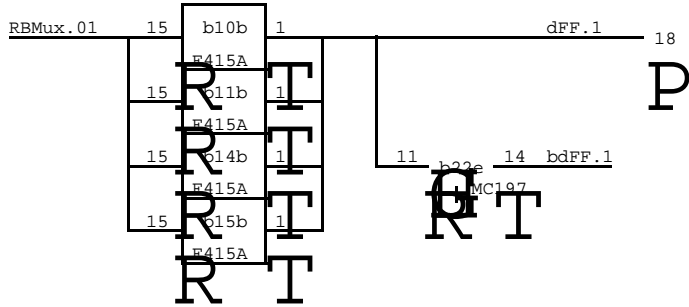
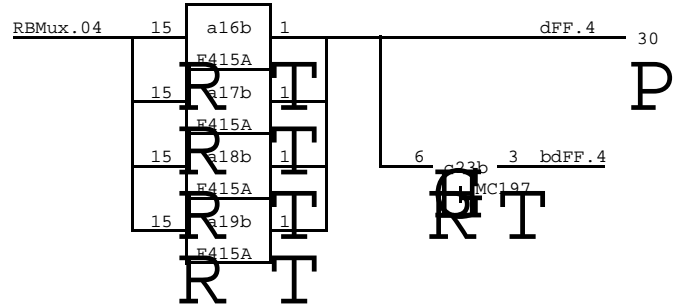
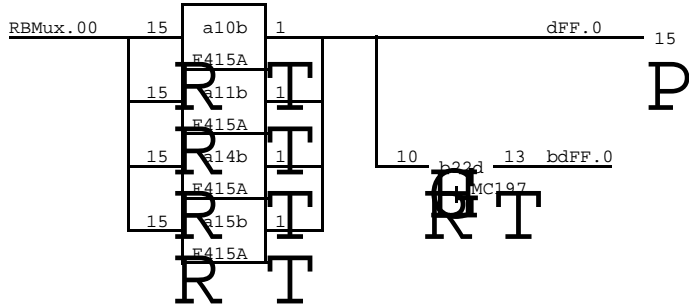
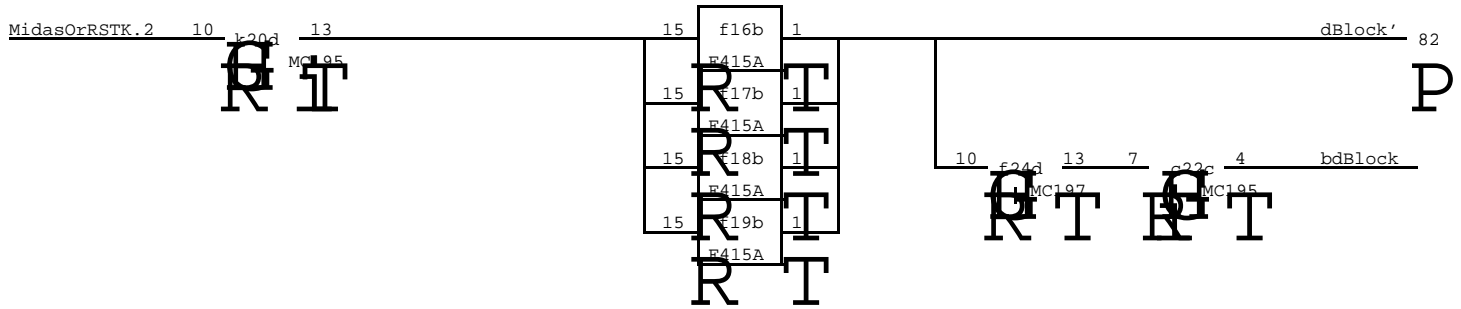


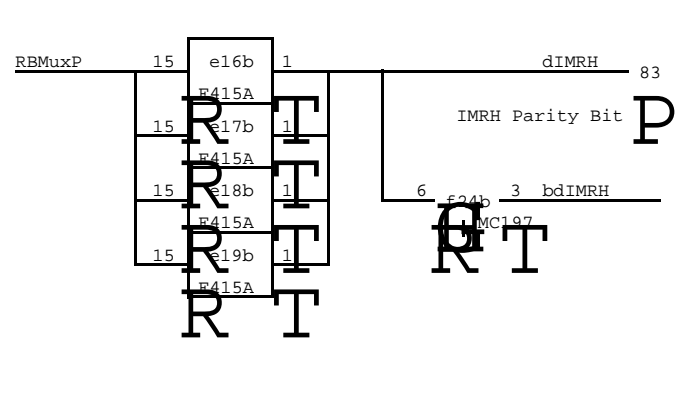
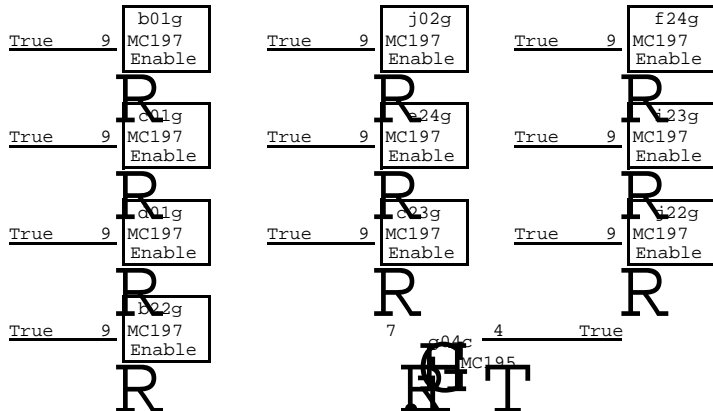
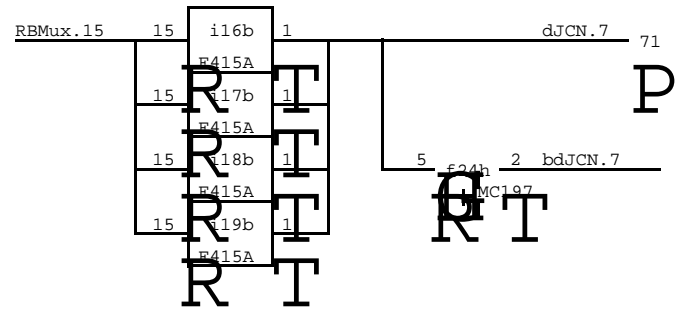
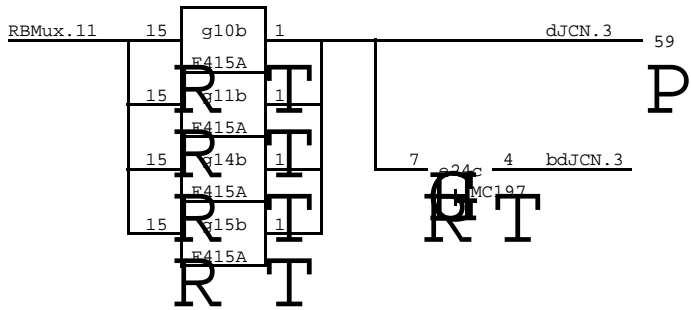
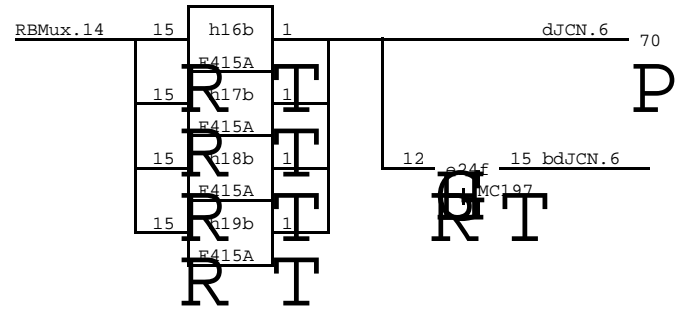
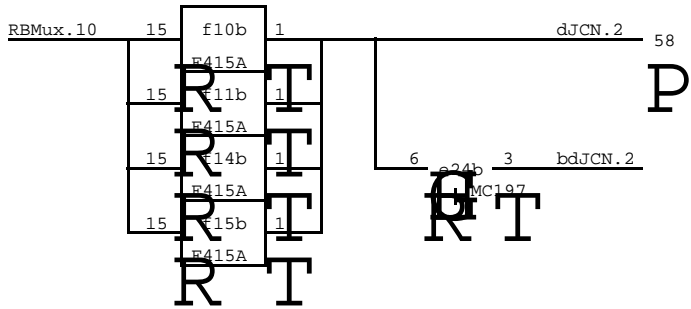
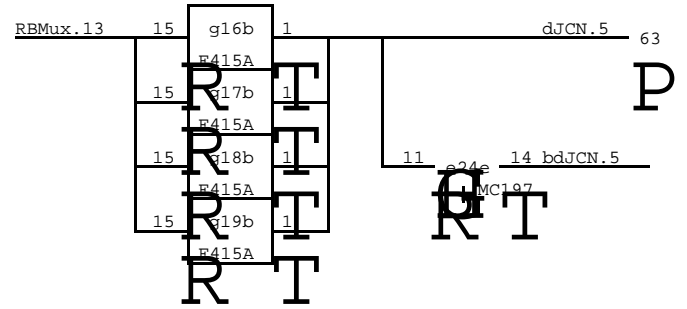
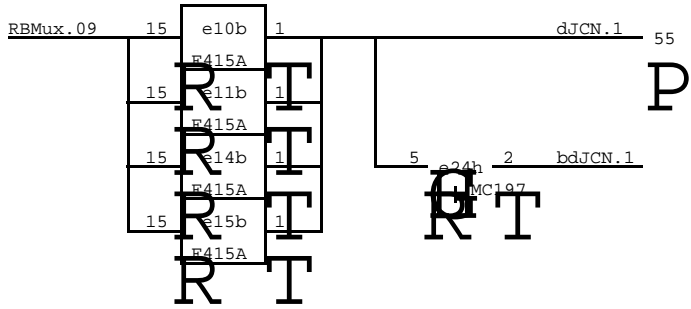
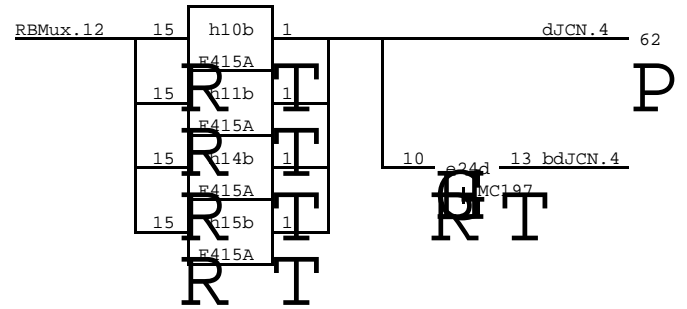
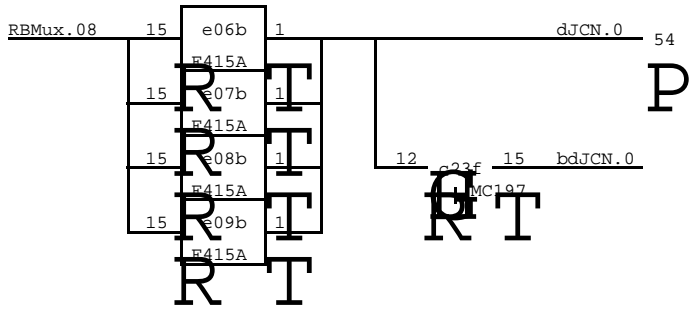
XEROX PARC/CSL	Project Dorado	D1 Control Store Bit Slice 06-11	File ContB02.sil	Designer Pier	Rev Cd	Date 7/12/79	Page 02
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RSTK.1 0 = write odd parity  
 1 = write even parity

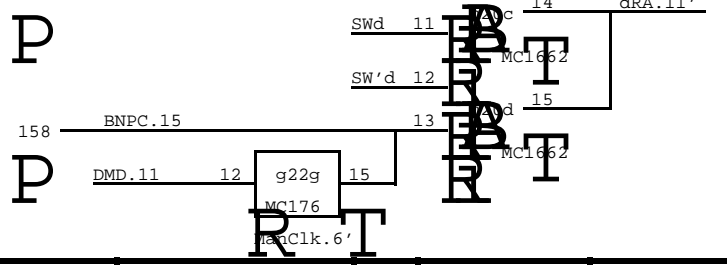
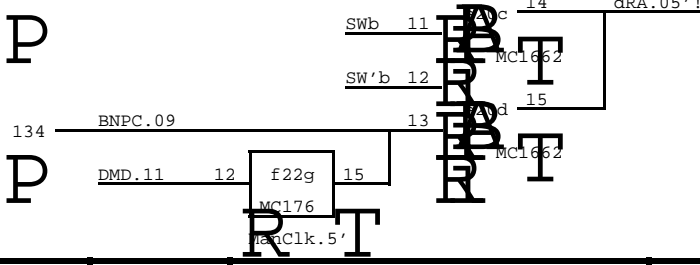
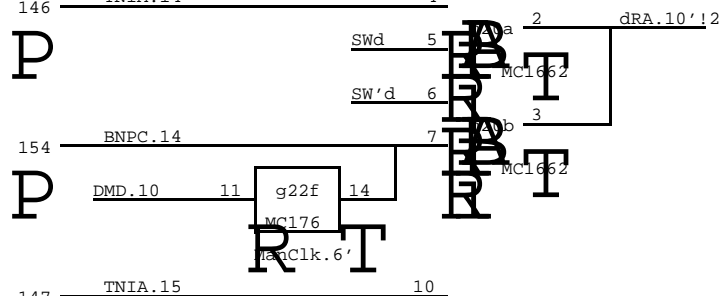
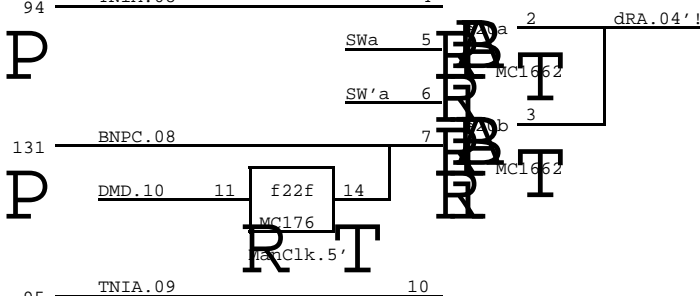
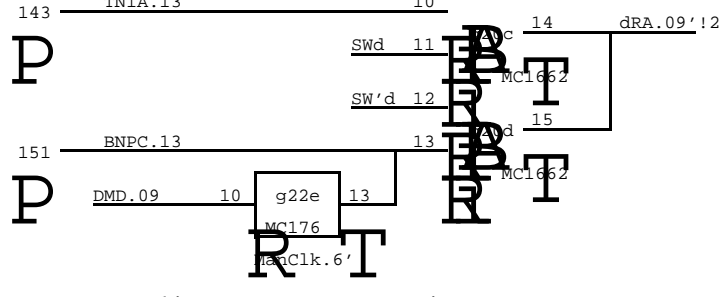
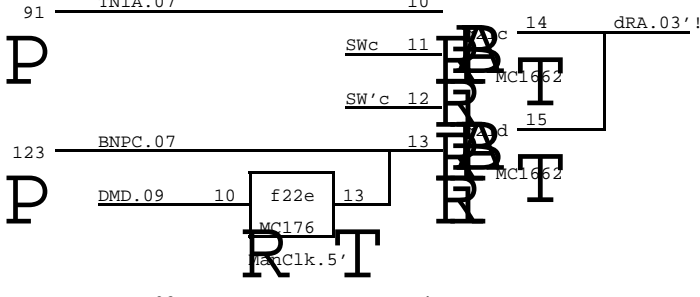
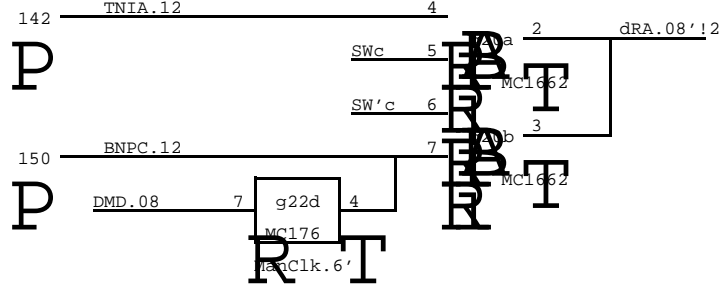
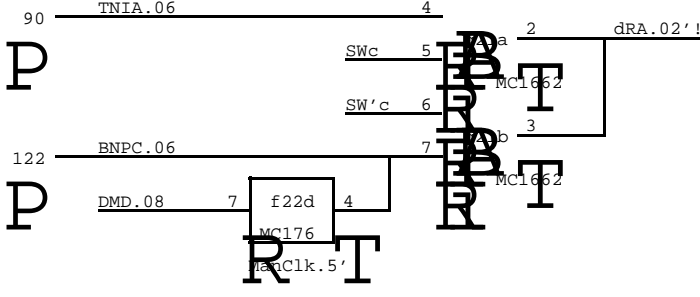
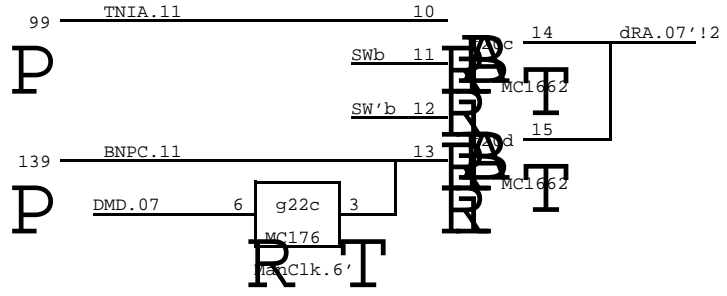
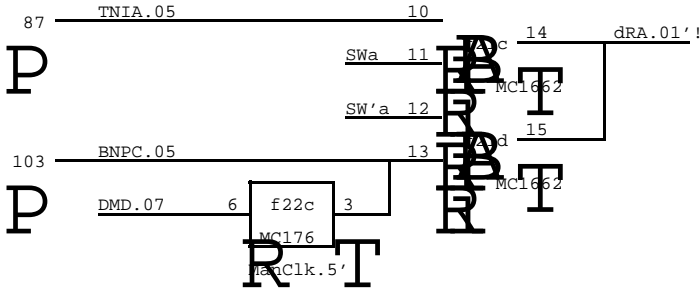
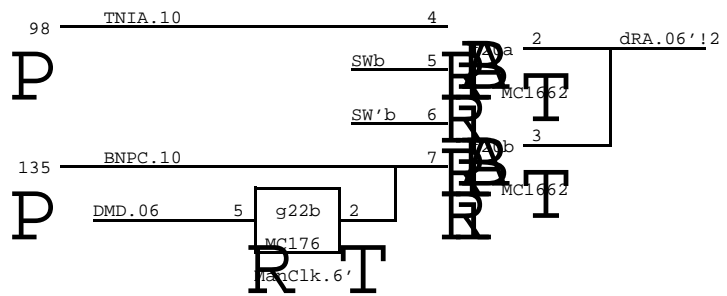
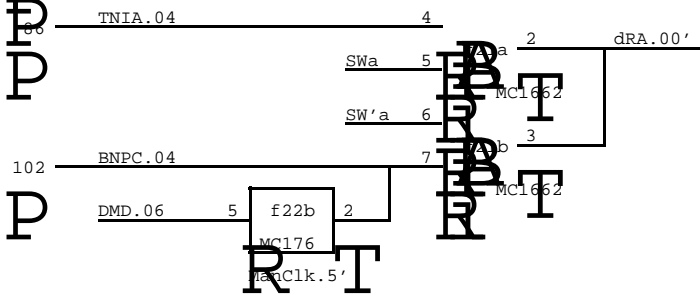
RSTK.2:  
 most significant bit

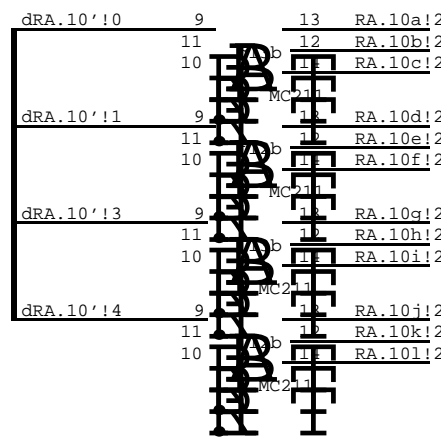
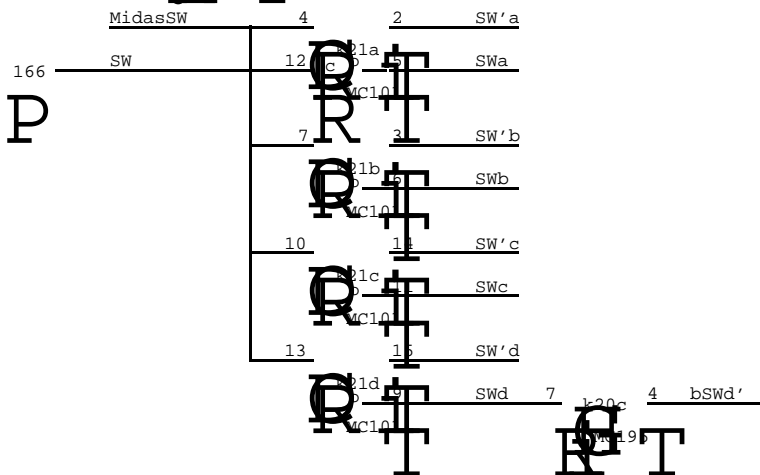
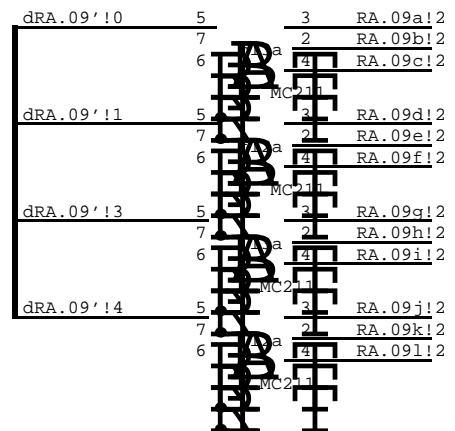
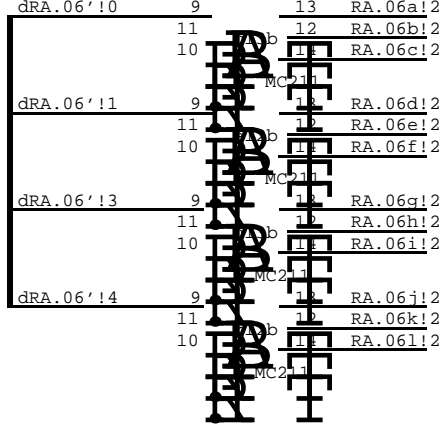
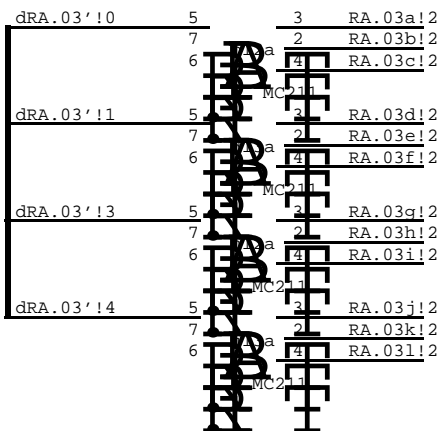
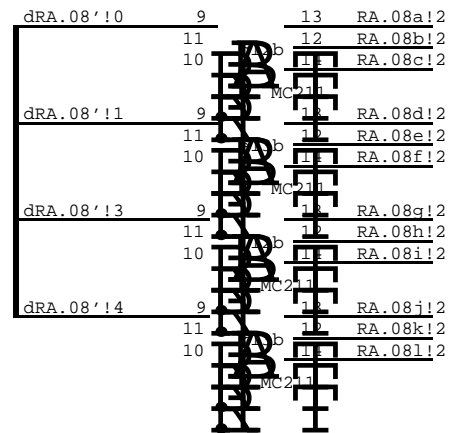
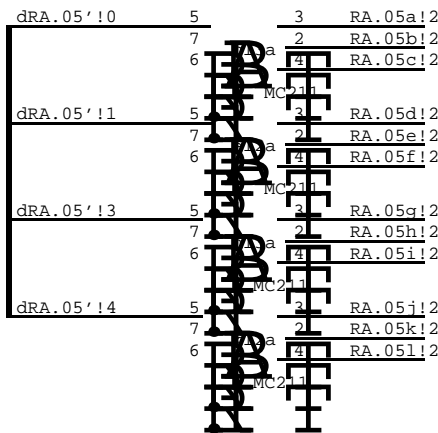
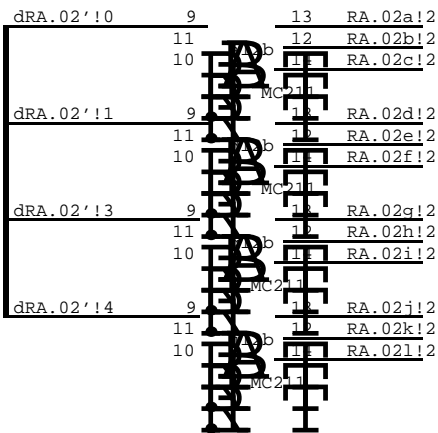
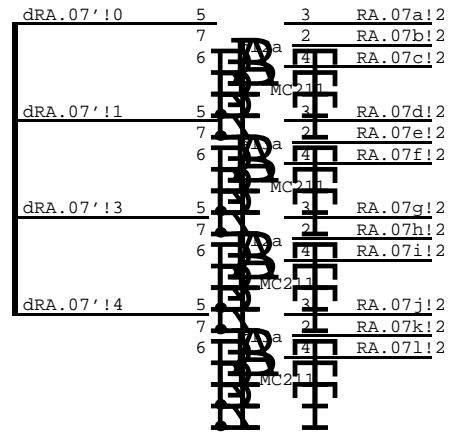
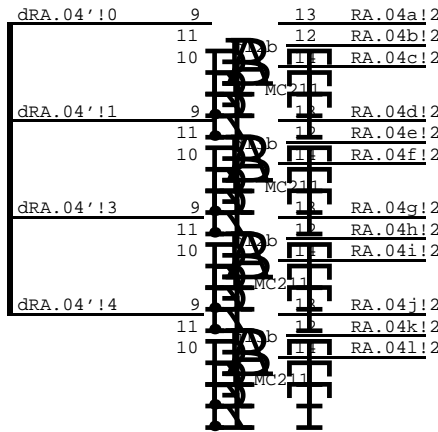
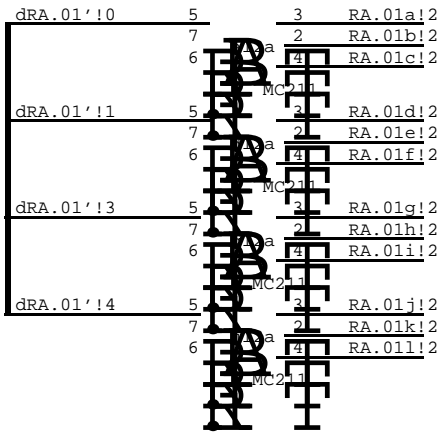




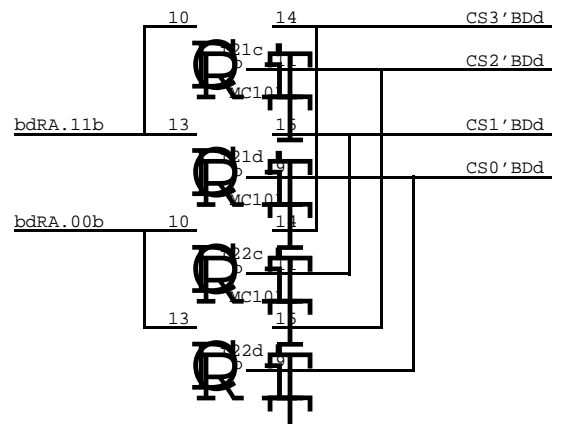
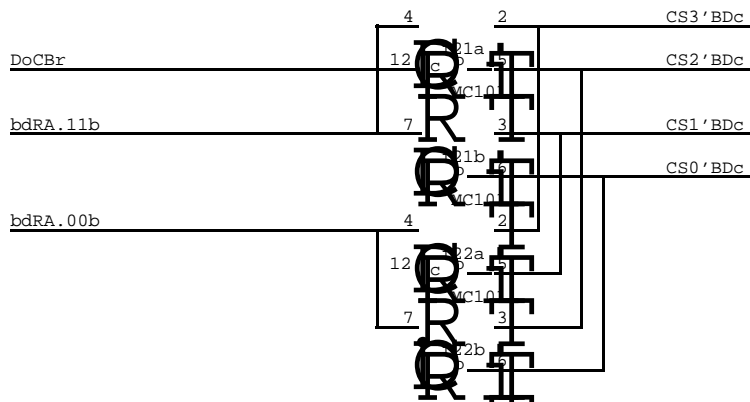
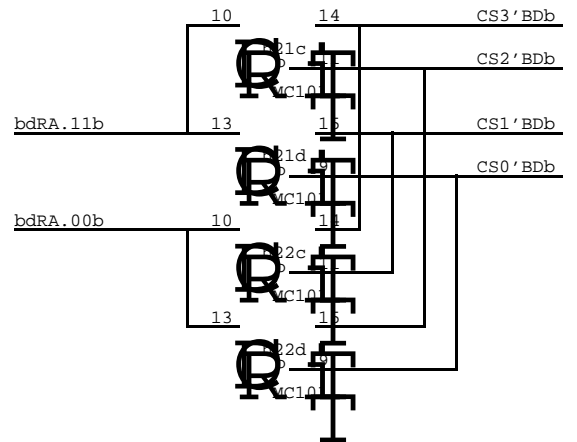
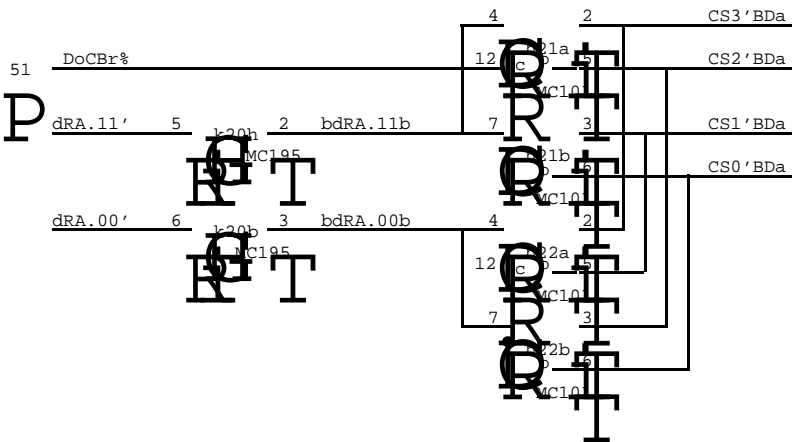
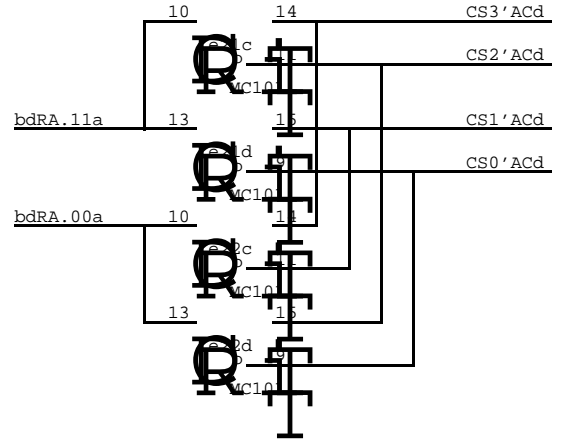
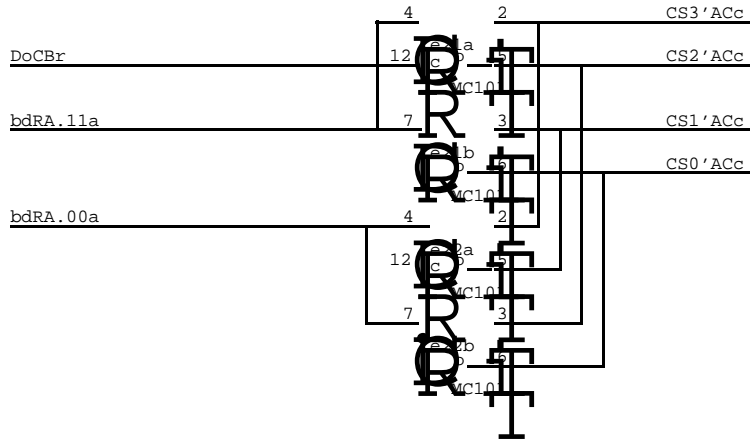
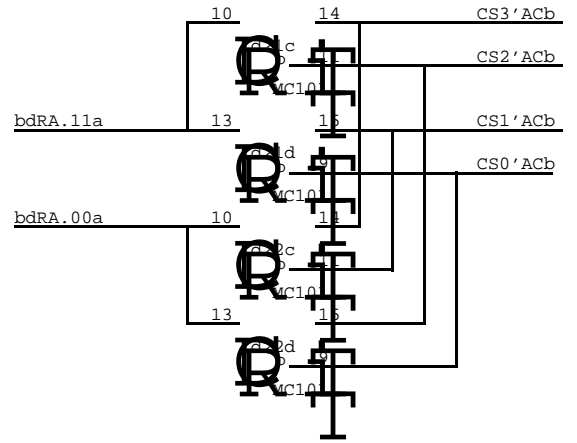
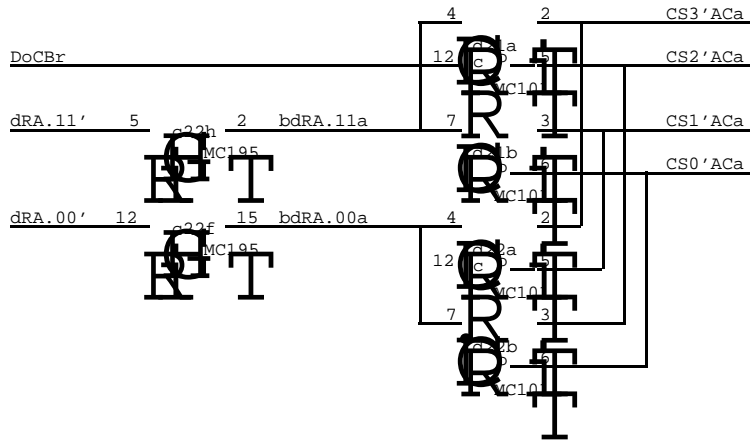
163 TNIA.02  
 175 BNPC.02  
 166 TNIA.03  
 183 BNPC.03

RESERVED FOR  
 16K EXPANSION

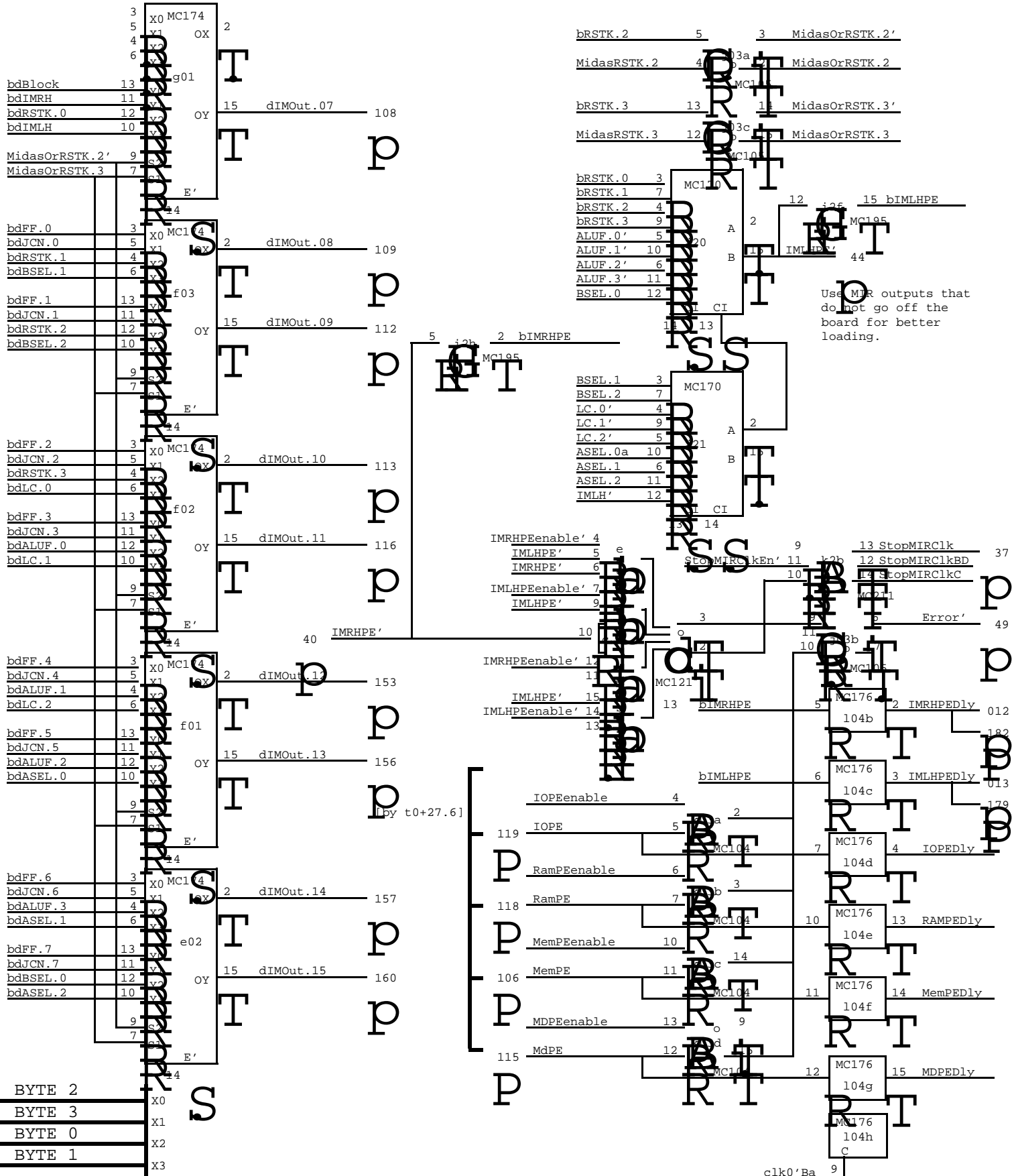


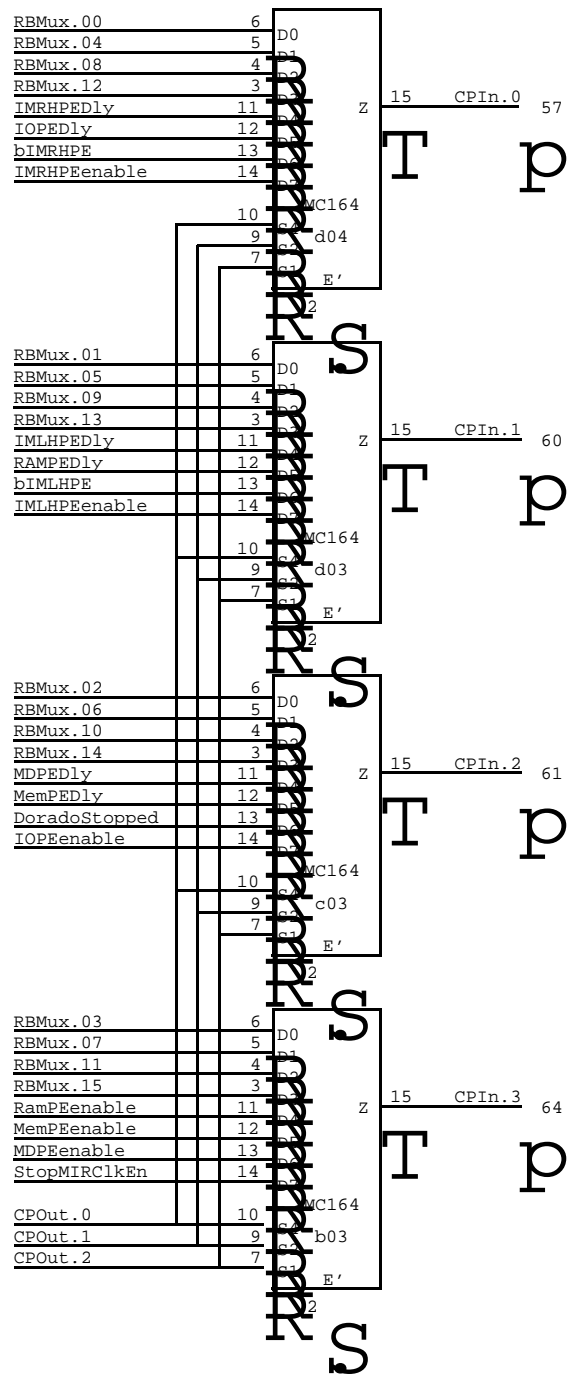
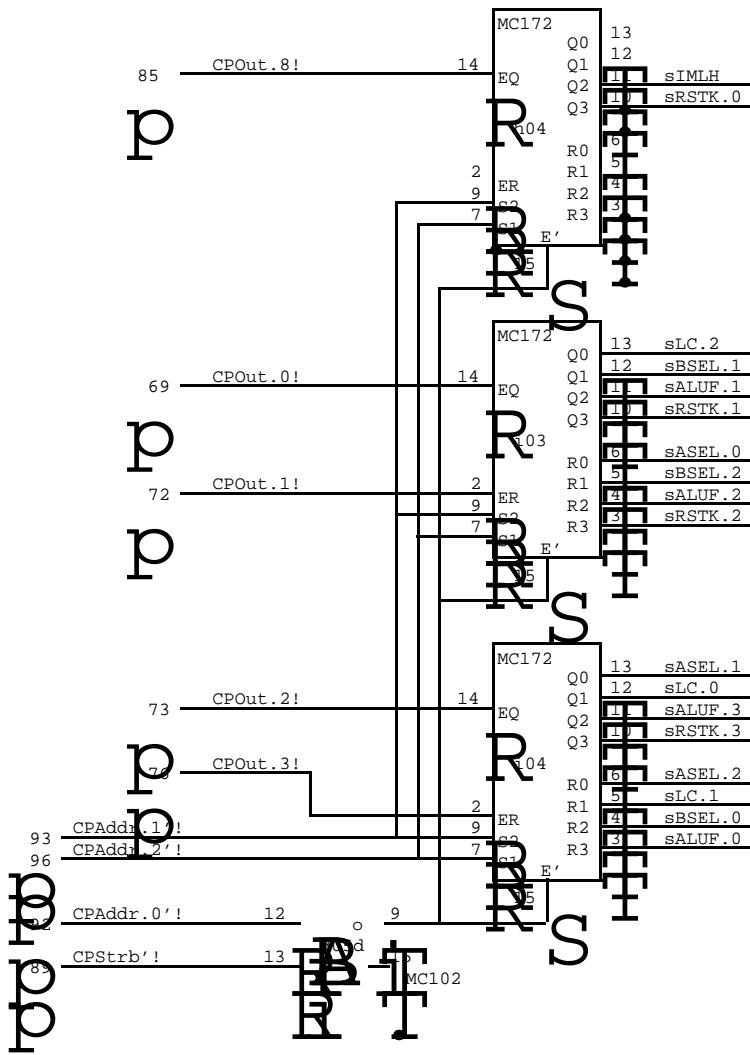


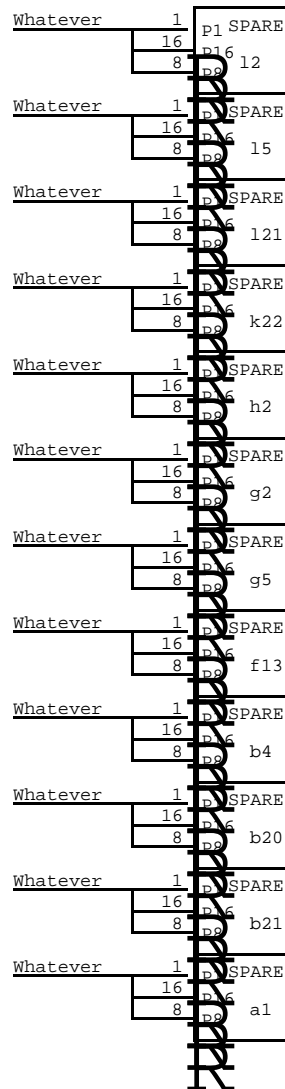
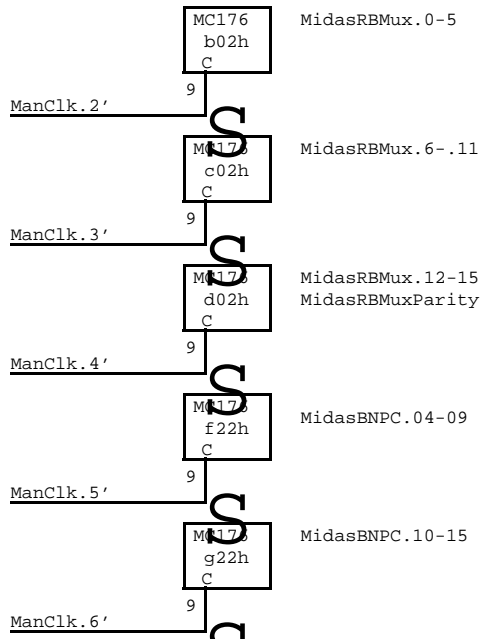
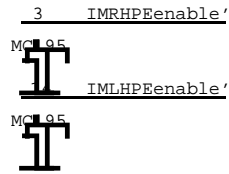
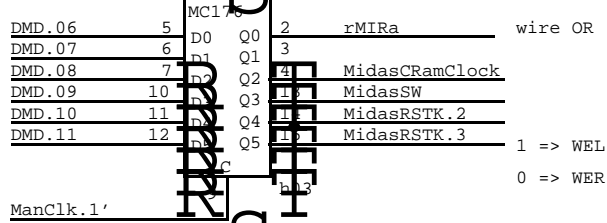
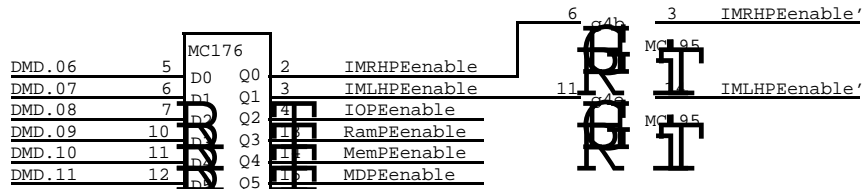




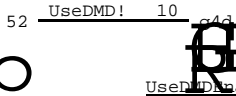
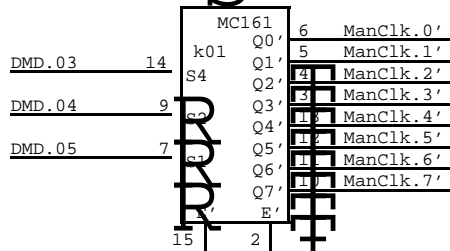
BYTE	RSTK		dIMOut									
	2	3	03	04	05	06	07	08	09	10	11	
0	0	0	RSTK.0	RSTK.1	RSTK.2	RSTK.3	ALUF.0	ALUF.1	ALUF.2	ALUF.3	BSEL.0	
1	0	1	IMLH	BSEL.1	BSEL.2	LC.0	LC.1	LC.2	ASEL.0	ASEL.1	ASEL.2	
2	1	0	BLOCK	FF.0							FF.7	
3	1	1	IMRH	JCN.0							JCN.7	

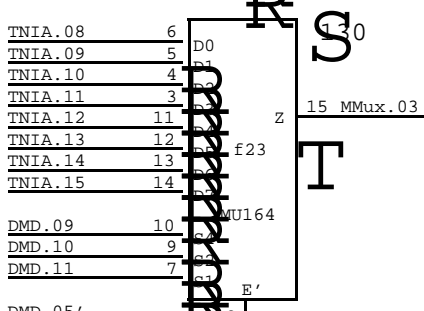
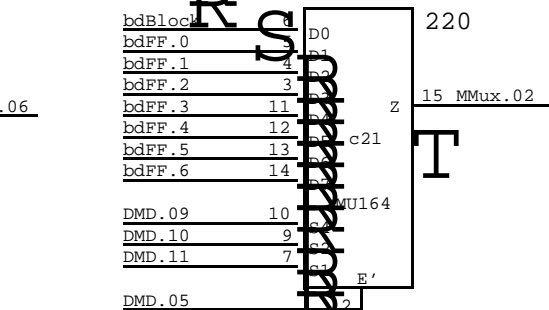
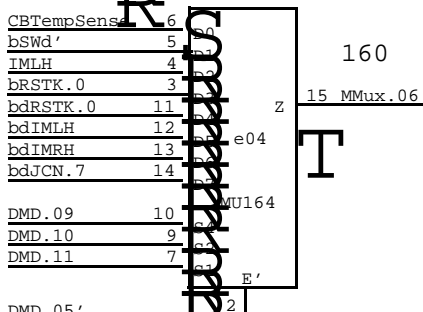
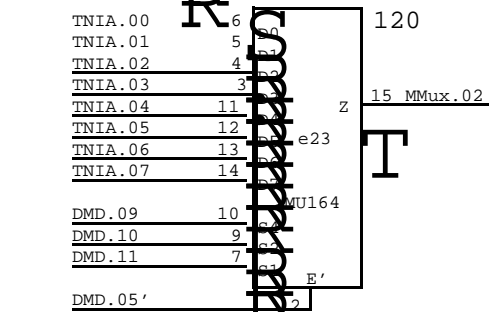
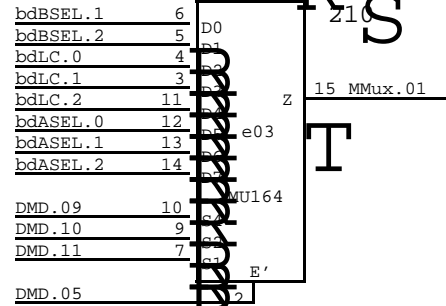
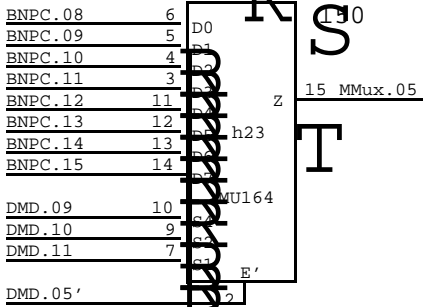
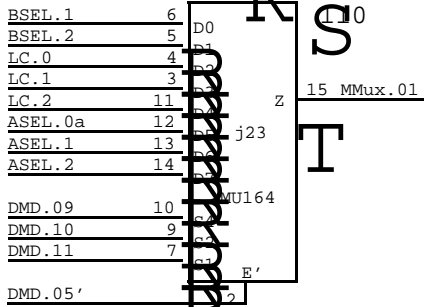
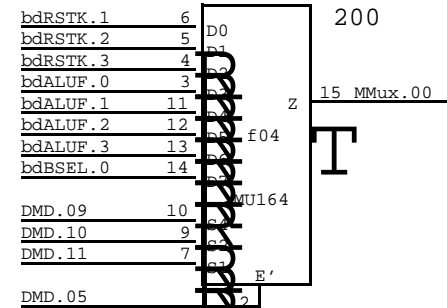
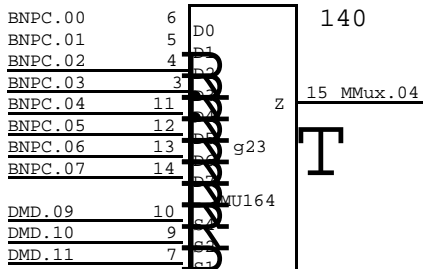
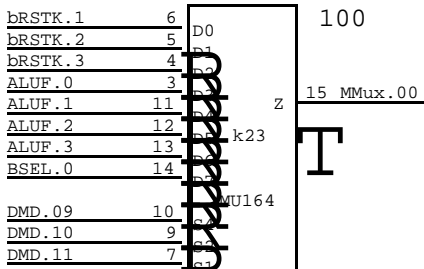




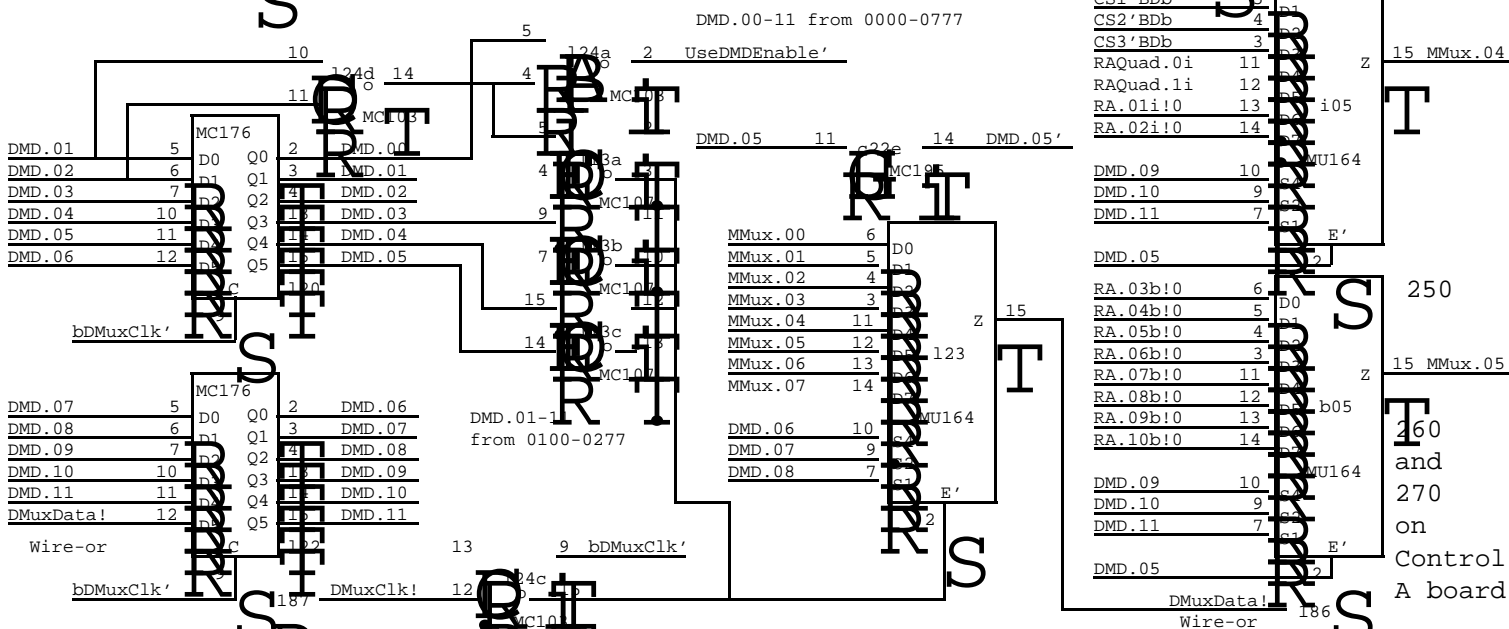
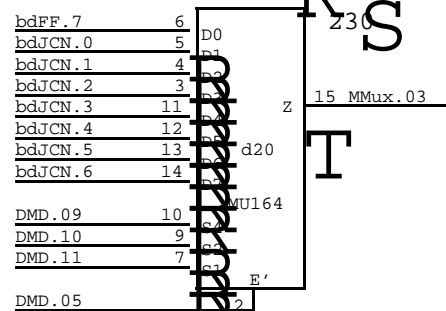


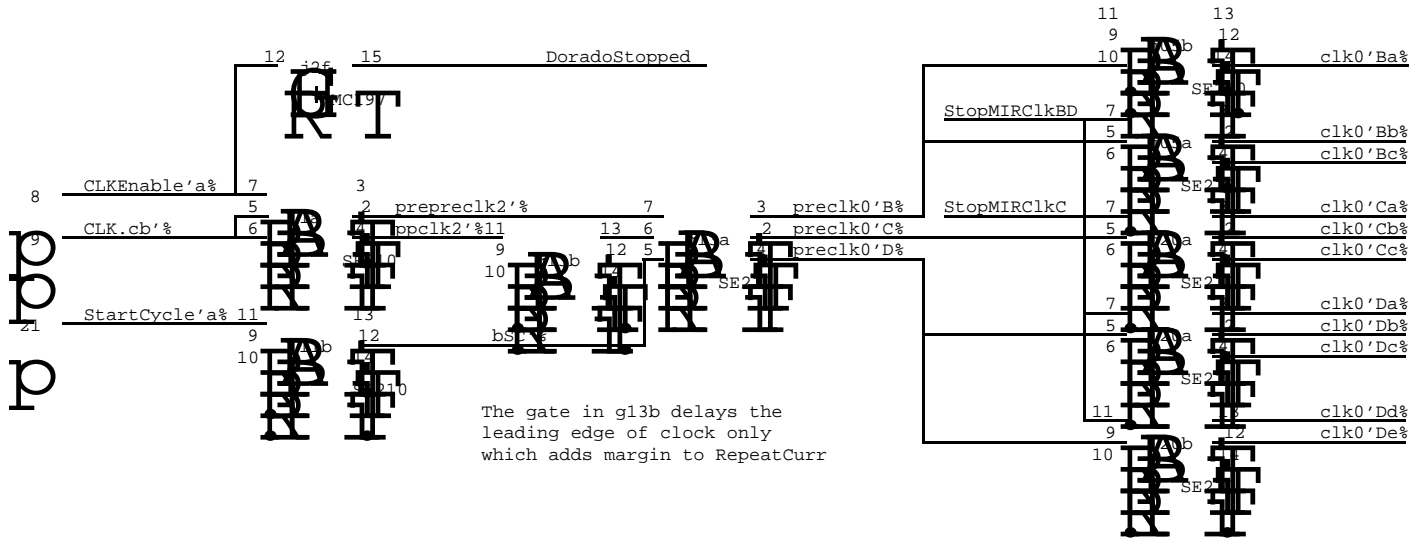
Multiwire spares



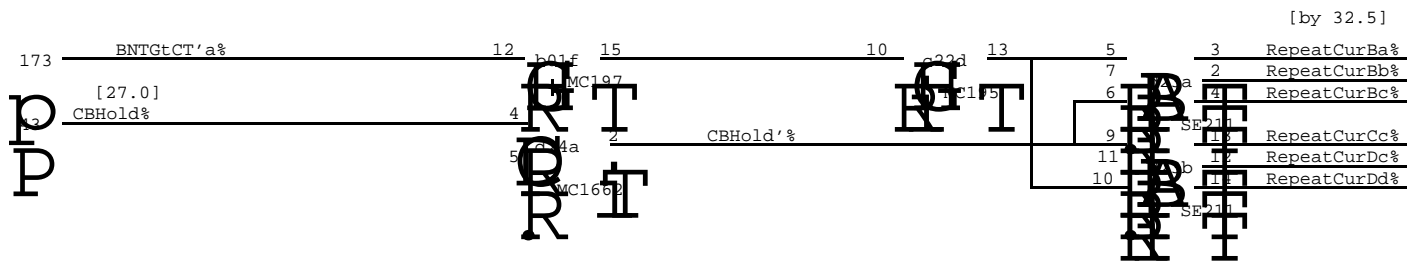


170  
on  
Control  
A board

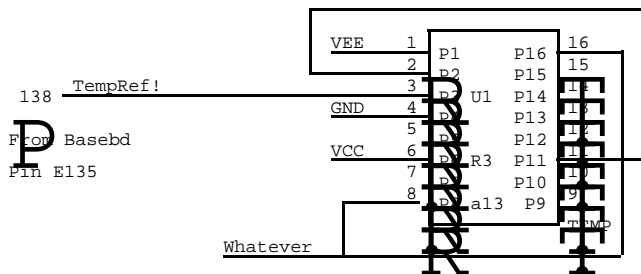
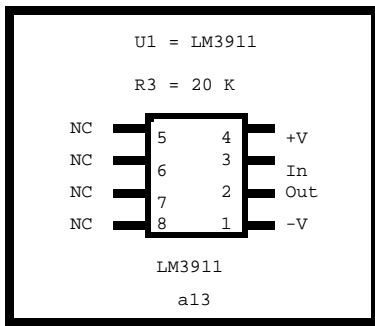
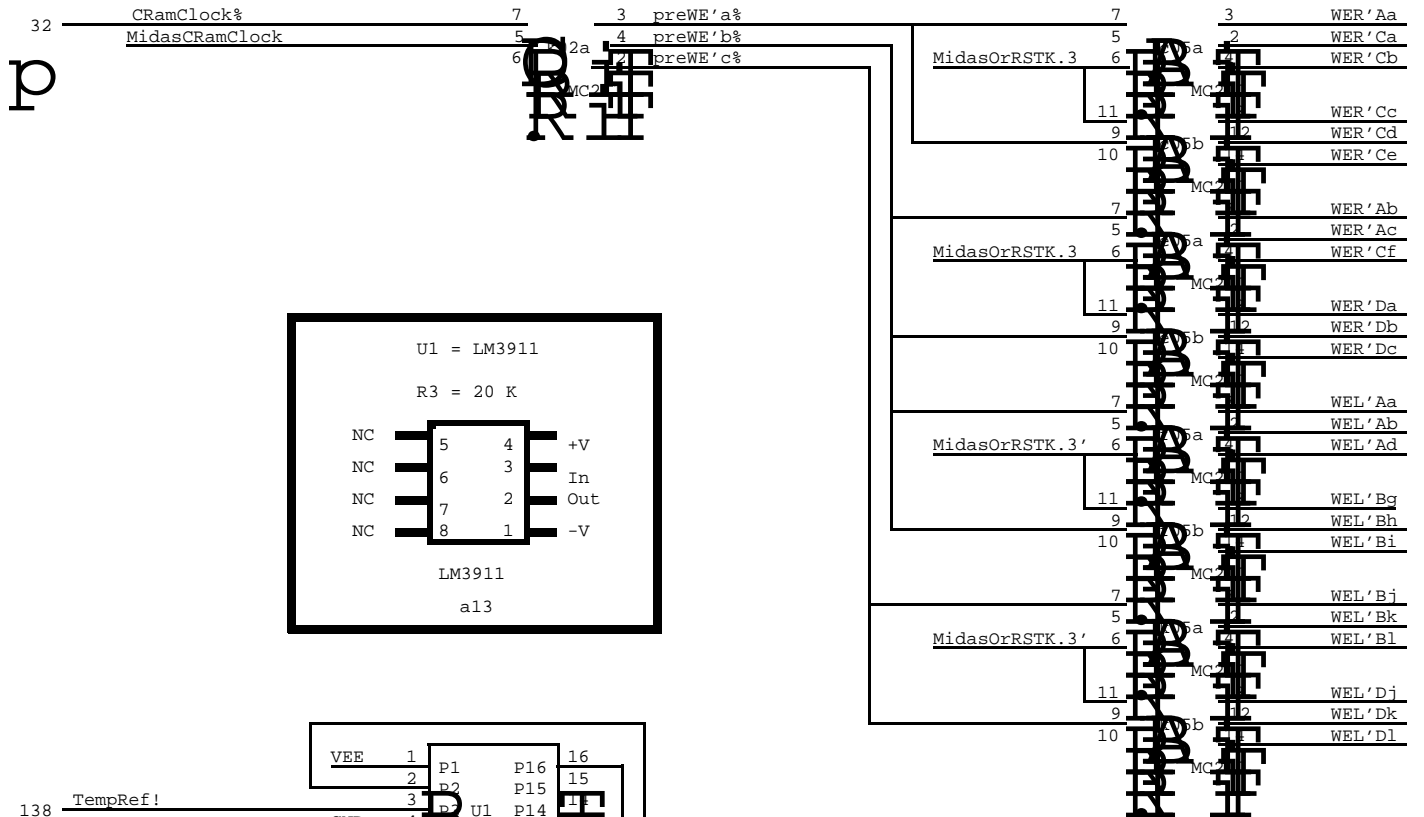




The gate in g13b delays the leading edge of clock only which adds margin to RepeatCurr

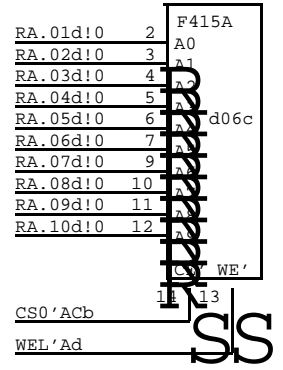
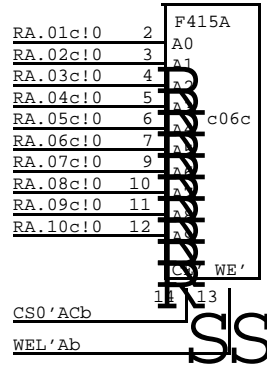
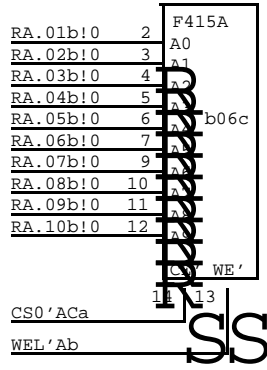
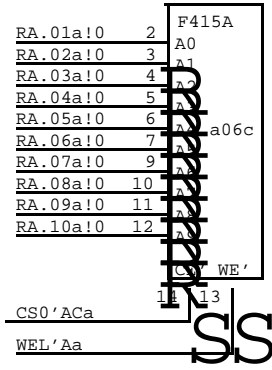


[by 32.5]

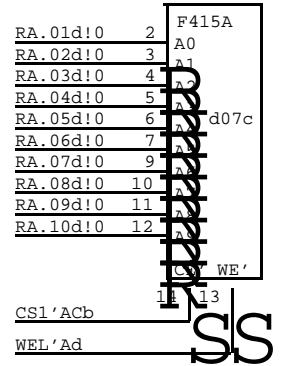
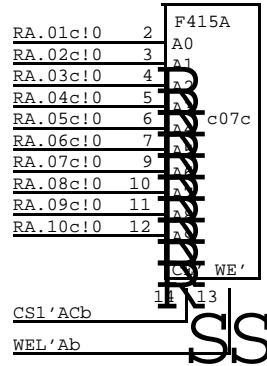
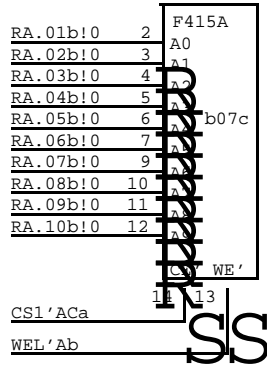
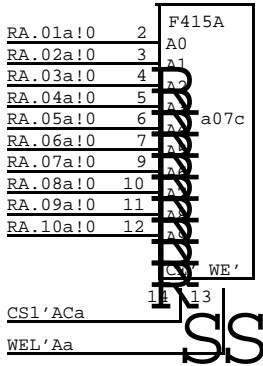


CBTempSense! 128  
To Muffler Input

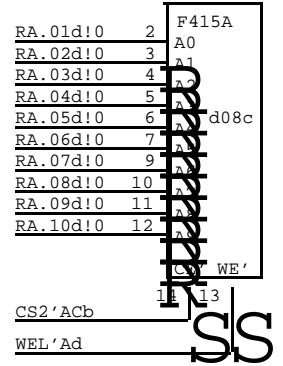
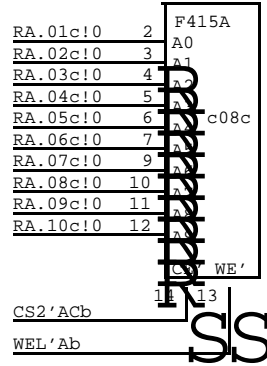
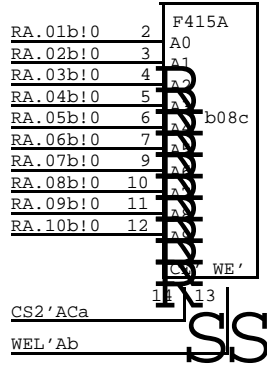
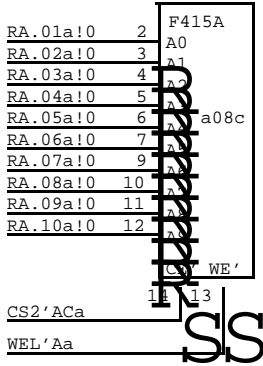
0 to 3777 Even



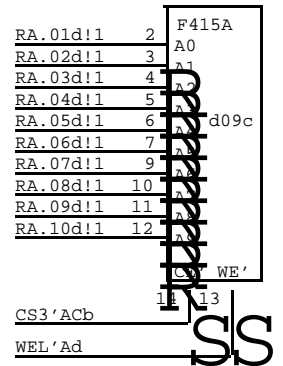
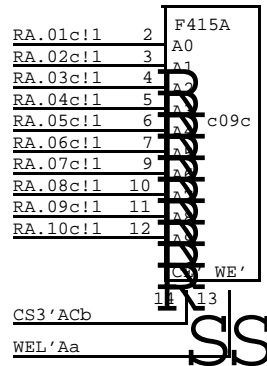
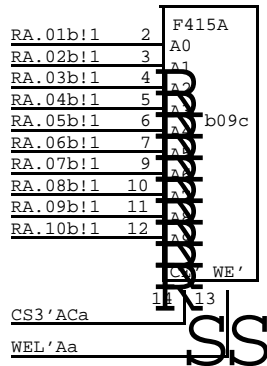
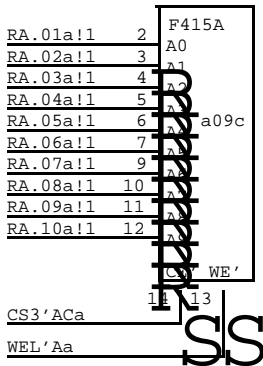
0 to 3777 Odd



4000 to 7777 Even



4000 to 7777 Odd

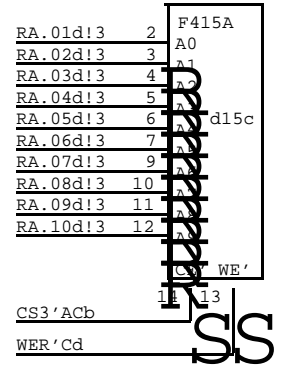
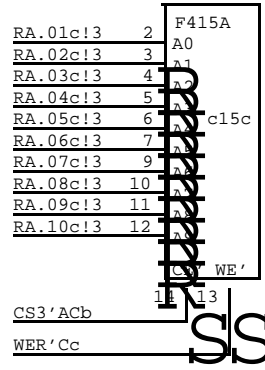
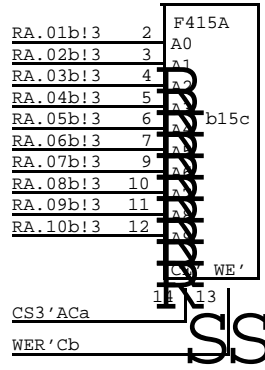
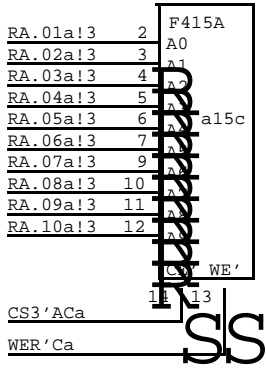
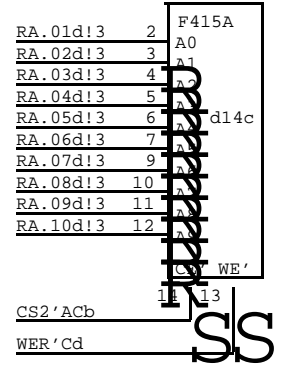
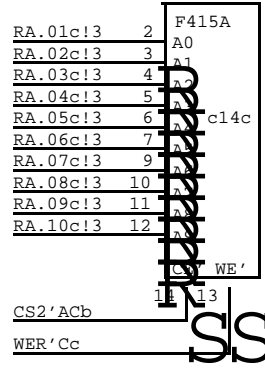
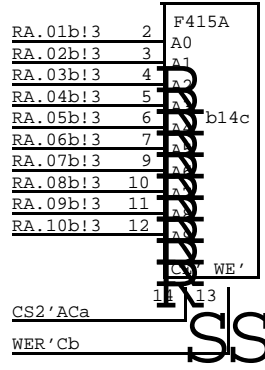
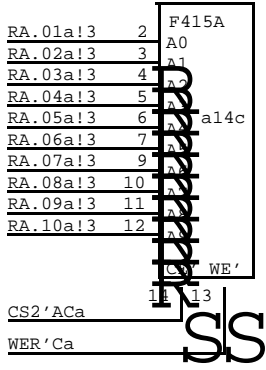
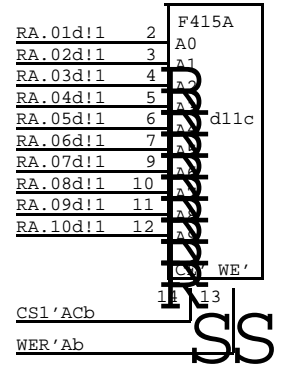
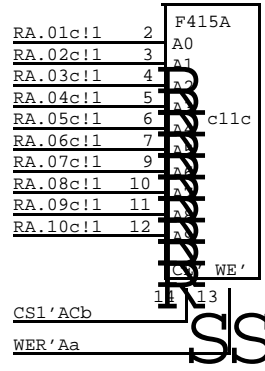
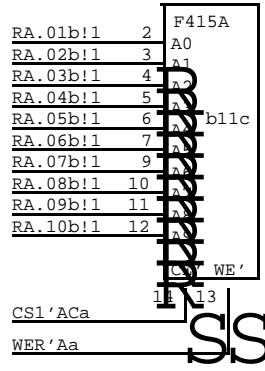
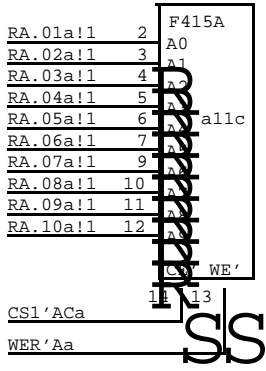
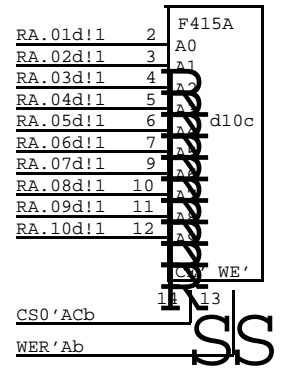
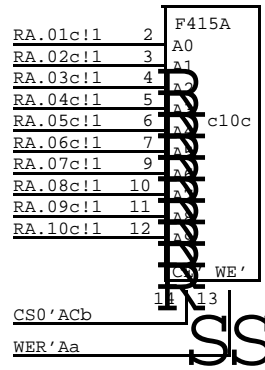
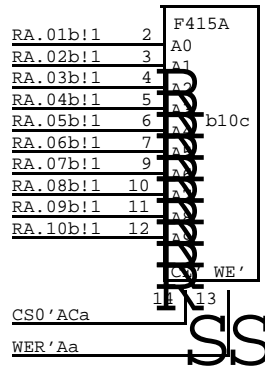
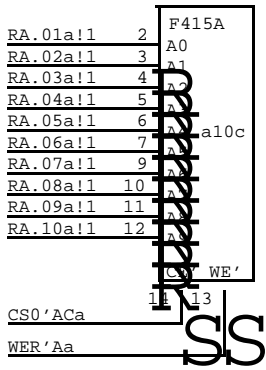


ASEL.0

ASEL.1

ASEL.2

IMLH



FF.0

FF.1

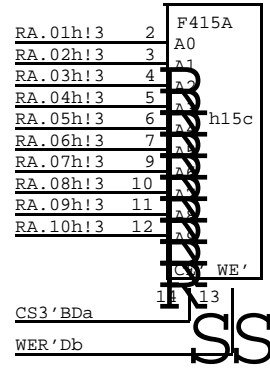
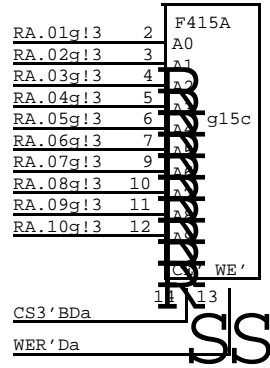
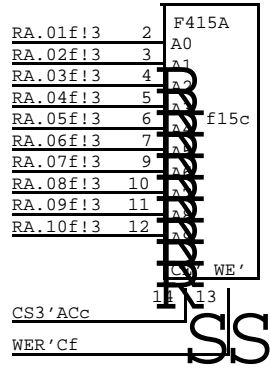
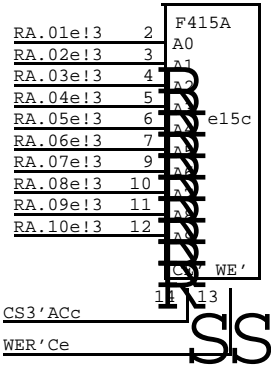
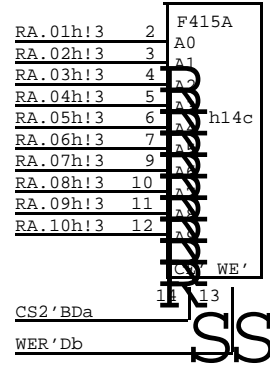
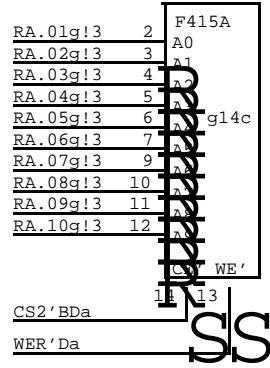
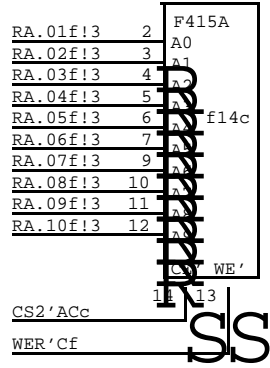
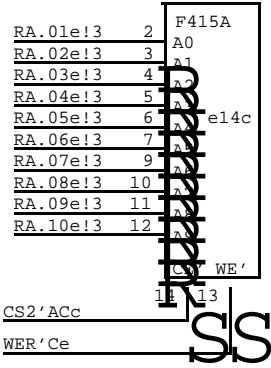
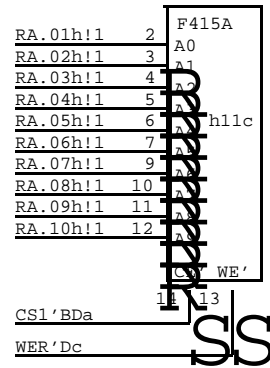
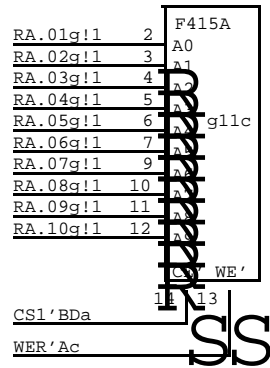
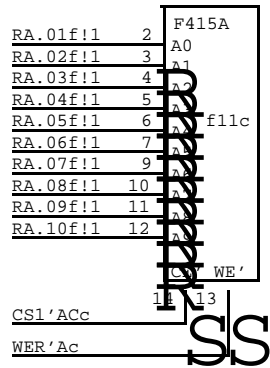
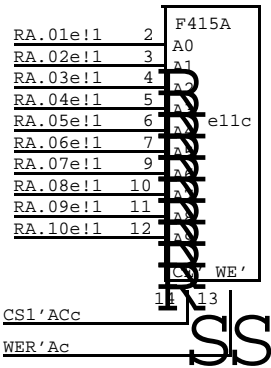
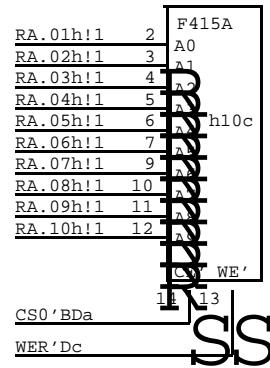
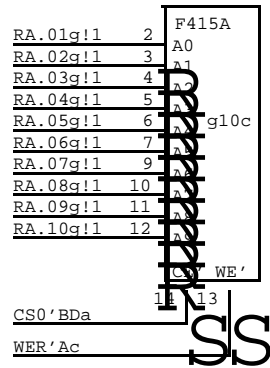
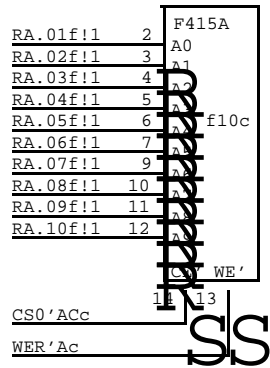
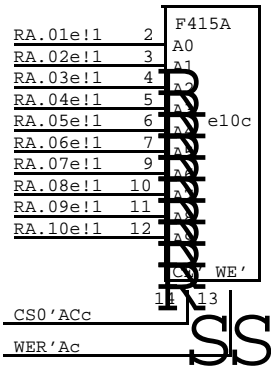
FF.2

FF.3







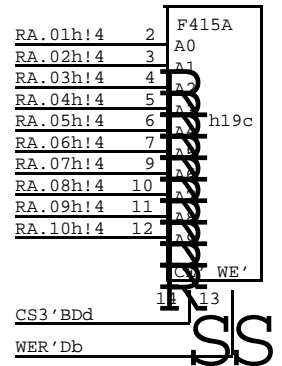
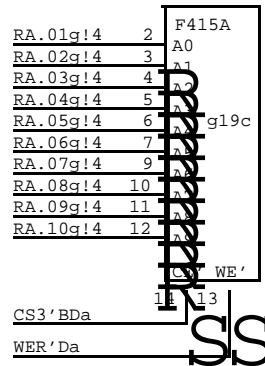
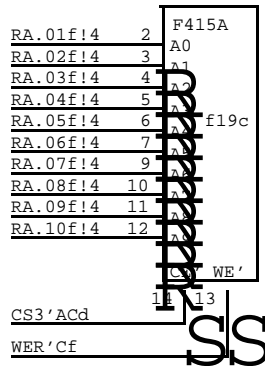
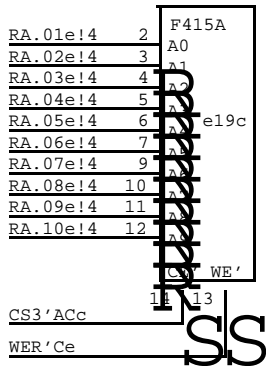
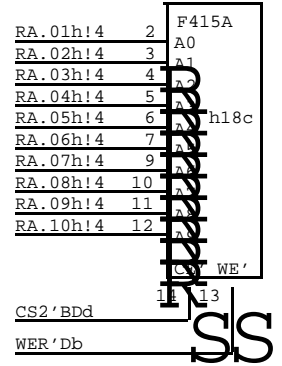
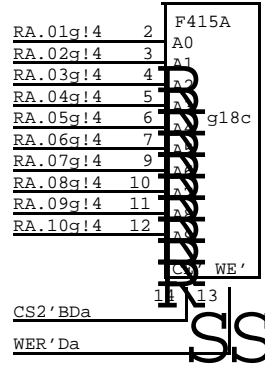
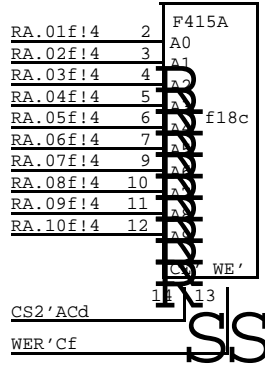
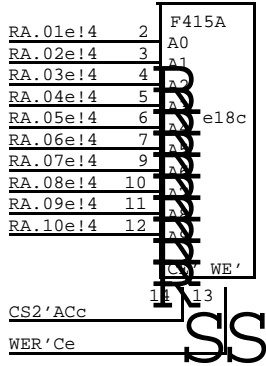
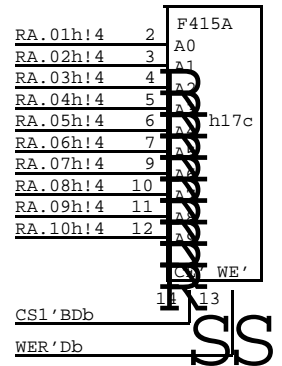
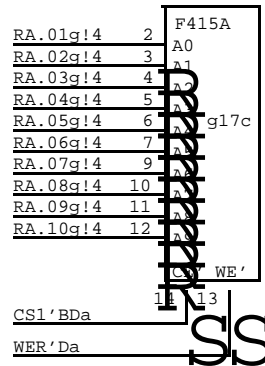
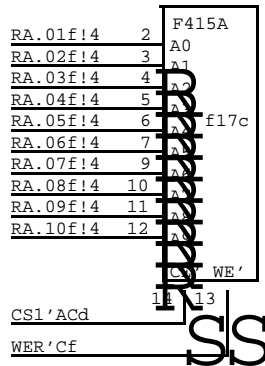
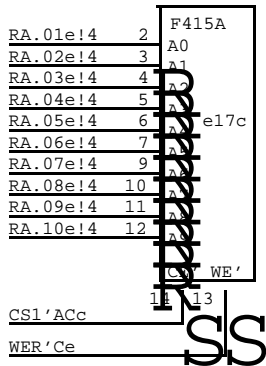
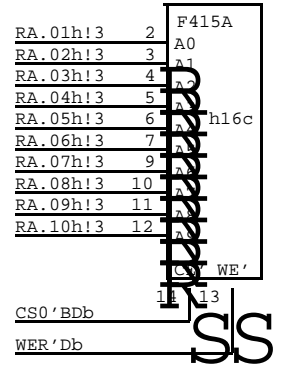
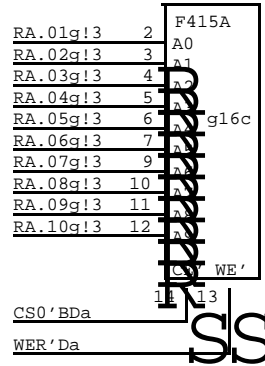
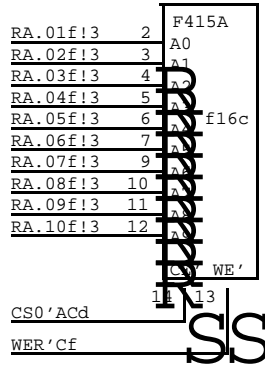
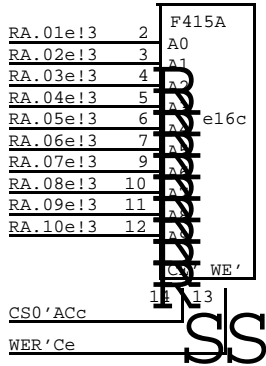


JCN.1

JCN.2

JCN.3

JCN.4



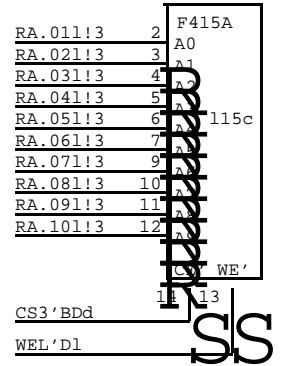
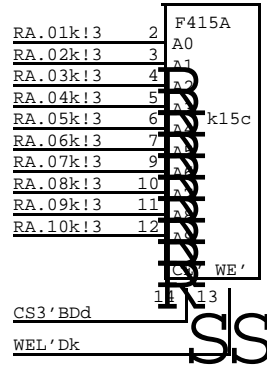
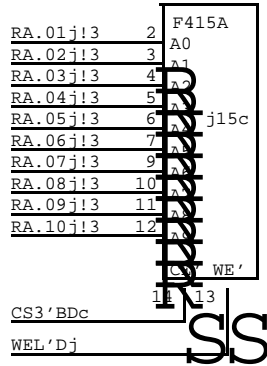
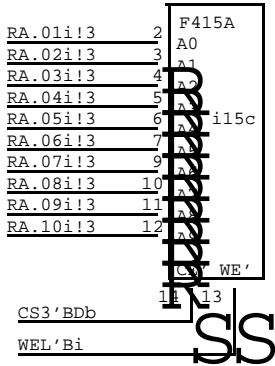
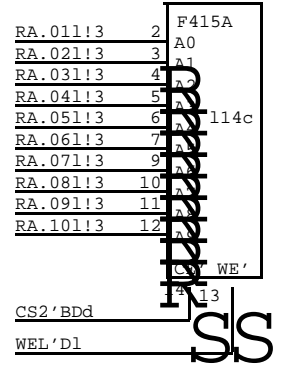
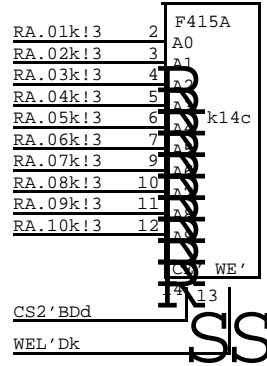
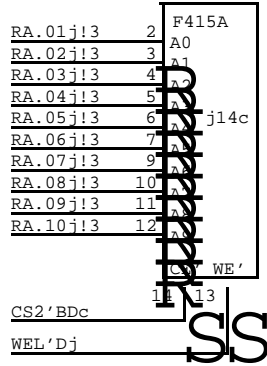
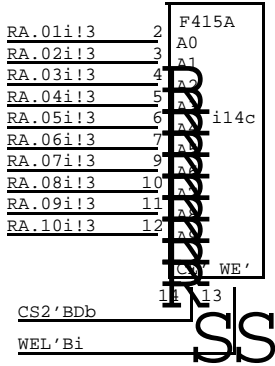
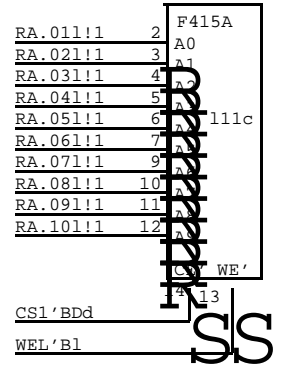
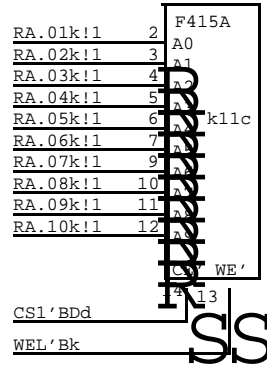
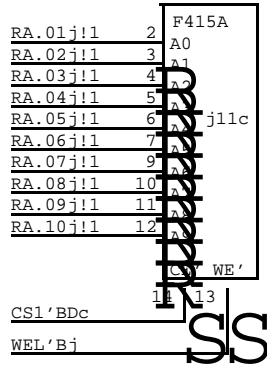
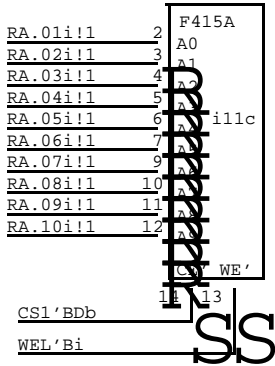
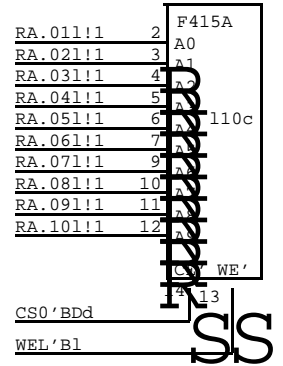
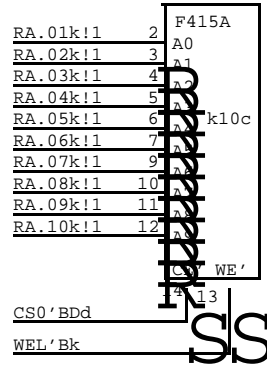
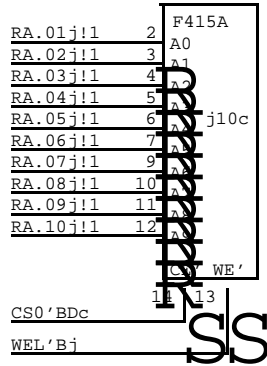
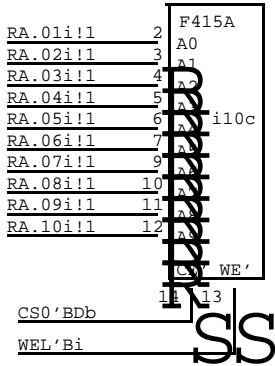
IMRH

BLK'

JCN.5

JCN.6



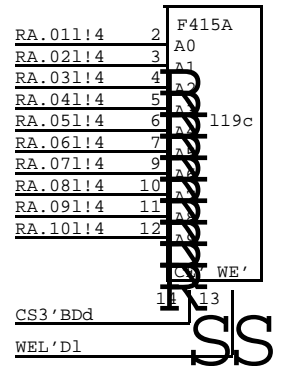
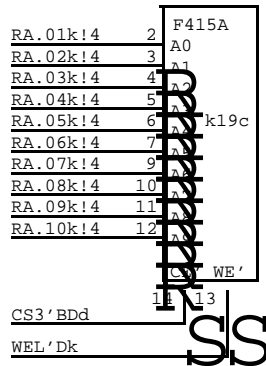
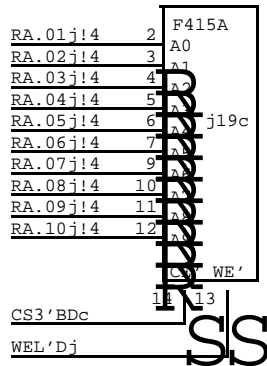
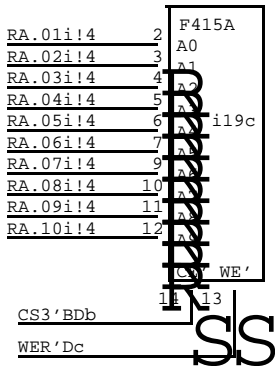
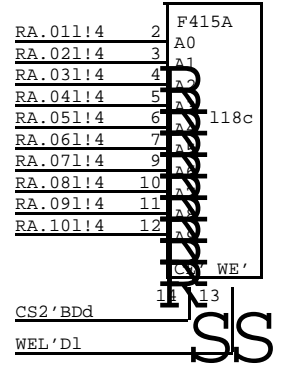
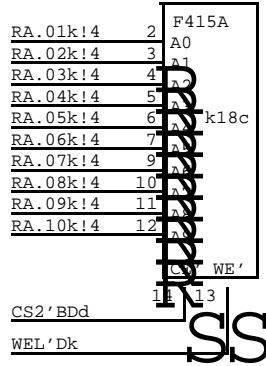
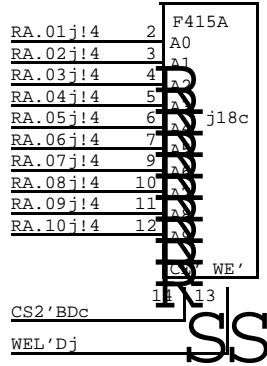
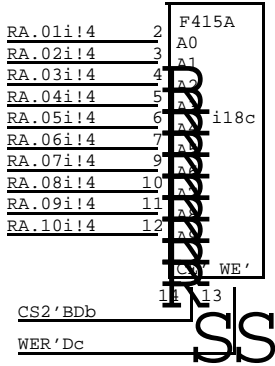
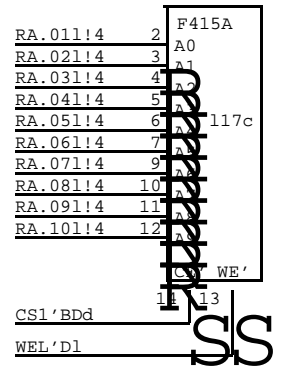
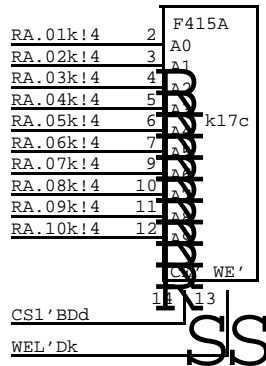
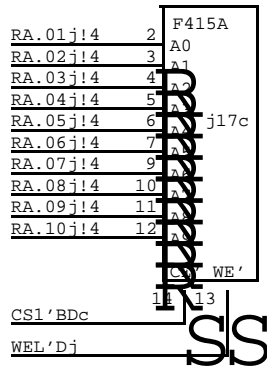
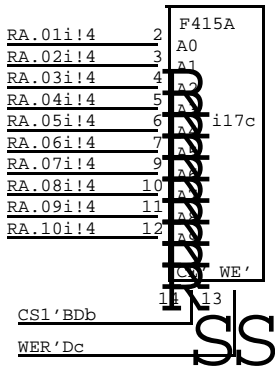
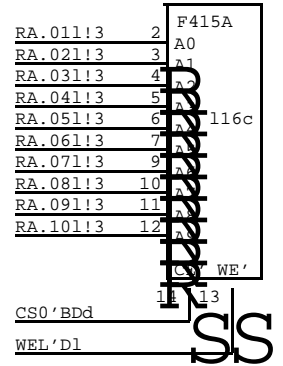
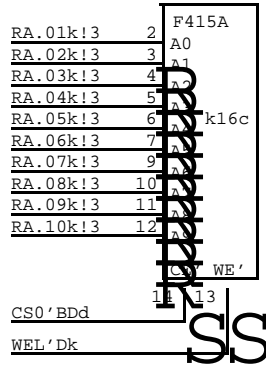
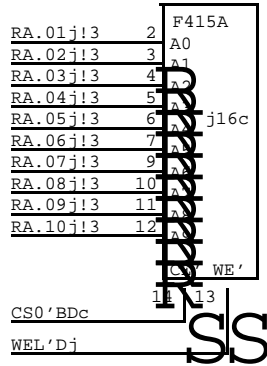
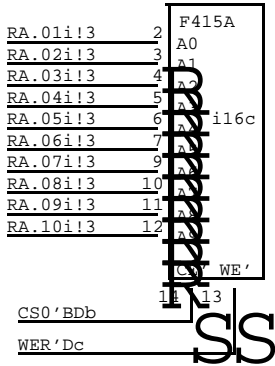


ALUF.0

ALUF.1

ALUF.2

ALUF.3



JCN.7

LC.0

LC.1

LC.2

A	a 181	b 168	c 153	d 137	e 124	f 109	93 g	80 h	64 i	48 j	33 k	20 l	B
1	BMrcvr 1,1,1,1,1,1 197	BMrcvr 197 2	BMrcvr 3,3,3,3,3,3 197	PAR TREE 170 3	dIMOut 08 & 09 174 9	dIMOut 03 174 9	ASEL,0' 3,b mem 231	RSTK2-3 231 1	RSTK0-1 231 1	Man Clk 161 13	CLK 210 11		1
2	ManClk2 1,1,1,1,1 176	ManClk3 2,2,2,2,2 176	ManClk4 3,3,3,3,3 176	dIMOut 10 & 11 174 9	dIMOut 06 & 07 174 9				1,1,1,1 9,9 195	bdRSTK.x 1,1,1,1, 197 11,h	CRAMClk 11,9 211		2
3	CPI.3 164 10	CPI.2 164 10	CPI.1 164 10	MU bdxxx 164 12	dIMOut 04 & 05 174 9	ManClk.7 176 13	MidasSW 176 13	SetMIR 172 10	Err brSTK 105 9	ERROR 104 9	STUFF 121 9		3
4		PEEnbl 176 13	CPI.0 164 10	MU dxxx 164 12	MU dxxx 164 12	13,5,13 13,13,h 195	SetMIR 172 10	SetMIR 172 10				5*9,G 176 9	4
5	MU RA 164 12	WER 'A & 'C 210 11	CBStrb/Pa 3,b,c,10 102	WER 'A & 'D 210 11	WEL 'A & 'B 210 11		MU CPBus 164 12	MU RA,CS 164 12	Clk0'Bx 11,b 210	WEL 'B & 'D 210 11			5
6	F415A 0000 to 3777 Even		F415A 0	F415A 0	F415A 0	F415A 0				F415A 0			6
7	ASEL 0000 to 3777 Odd		IMLH 1	JCN 1		BSEL 1				RSTK 1			7
8	0 4000 to 7777 Even	1 2	2	0 2	0 2	1 2	2 2	2 2	0 2	1 2	2 2	3 2	8
9	4000 to 7777 Odd		3	3	3	3	3	3	3	3	3	3	9
10	0	0	0	0	0	0	0	0	0	0	0	0	10
11	FF 1			JCN 1	JCN 1	JCN 1	JCN 1			ALUF 1			11
12	RA 211 7	RA 211 7	RA 211 7	RA 211 7	RA 211 7	RA 211 7	RA 211 7	RA 211 7	RA 211 7	RA 211 7	RA 211 7	RA 211 7	12
13	TEMP SENSE	RA 211 7	RA 211 7	RA 211 7	RA 211 7		preclk0 11,b 210	RA 211 7	RA 211 7	RA 211 7	RA 211 7	Midas 107 12	13
14	0 2	1 2	2 2	3 2	1 2	2 2	3 2	4 2	0 2	1 2	2 2	3 2	14
15	3	3	3	3	3	3	3	3	3	3	3	3	15
16	0	F415A 0	0	0	F415A 0	F415A 0	0	F415A 0	0	0	0	0	16
17	FF 1			IMRH 1	BLK' 1		JCN 1			JCN 1		LC 1	17
18	4 2	5 2	6 2	7 2			5 2	6 2	7 2	0 2	1 2	2 2	18
19	3	3	3	3	3	3	3	3	3	3	3	3	19
20			CLK0'Cx 11,b 210	MU bdxxx 164 12	dRA 04' & 05' 1662 6	dRA 06' & 07' 1662 6	dRA 08' & 09' 1662 6	dRA 10' & 11' 1662 6	CLK0'Dx 210 11	PRITY 170 9	INV 8,7,4,d,e, 195	Midas 176 12	20
21			MU bdxxx 164 12	CSEL 101 8	CSEL 101 8	dRA 00' & 01' 1662 6	dRA 02' & 03' 1662 6	CSEL 101 8	CSEL 101 8	PRITY 170 9	MidasSW 101 11		21
22	dXXXBuf 3,3,3,4,4 197	INV 8,4,4,11, 195 12,8	CSEL 101 8	CSEL 101 8	MidasBNPC ManClk5 176 6	MidasBNPC ManClk6 176 6	CSEL 101 8	CSEL 101 8	dXXXBuf 1,1,2,2,e,f 197			Midas 176 12	22
23	Local ASEL 3,c 231	dXXXBuf 4,4,4,4,4 197 4	RepeatCur 211 11	TNIA MU 164 12	TNIA MU 164 12	BNPC MU 164 12	BNPC MU 164 12	dXXXBuf 2,2,3,3,2 197 2	MU MIR 164 12	MU MIR 164 12	Midas 164 12		23
24	ASEL 0-1 231 3	ASEL 2 IMLH 231 3	b,c,d CbHold 1662 11	dXXXBuf 197 5	dXXXBuf 5,5,3,4,e,f 197 5	BSEL 0-1 231 2	BSEL2,LC0 231 2	LC 1-2 231 3	ALUF 0-1 231 1	ALUF 2-3 231 2	12,b,12 ,12 103		24
C	a 11	b 26	c 39	d 55	e 70	f 86	99 g	114 h	129 i	143 j	159 k	174 l	D