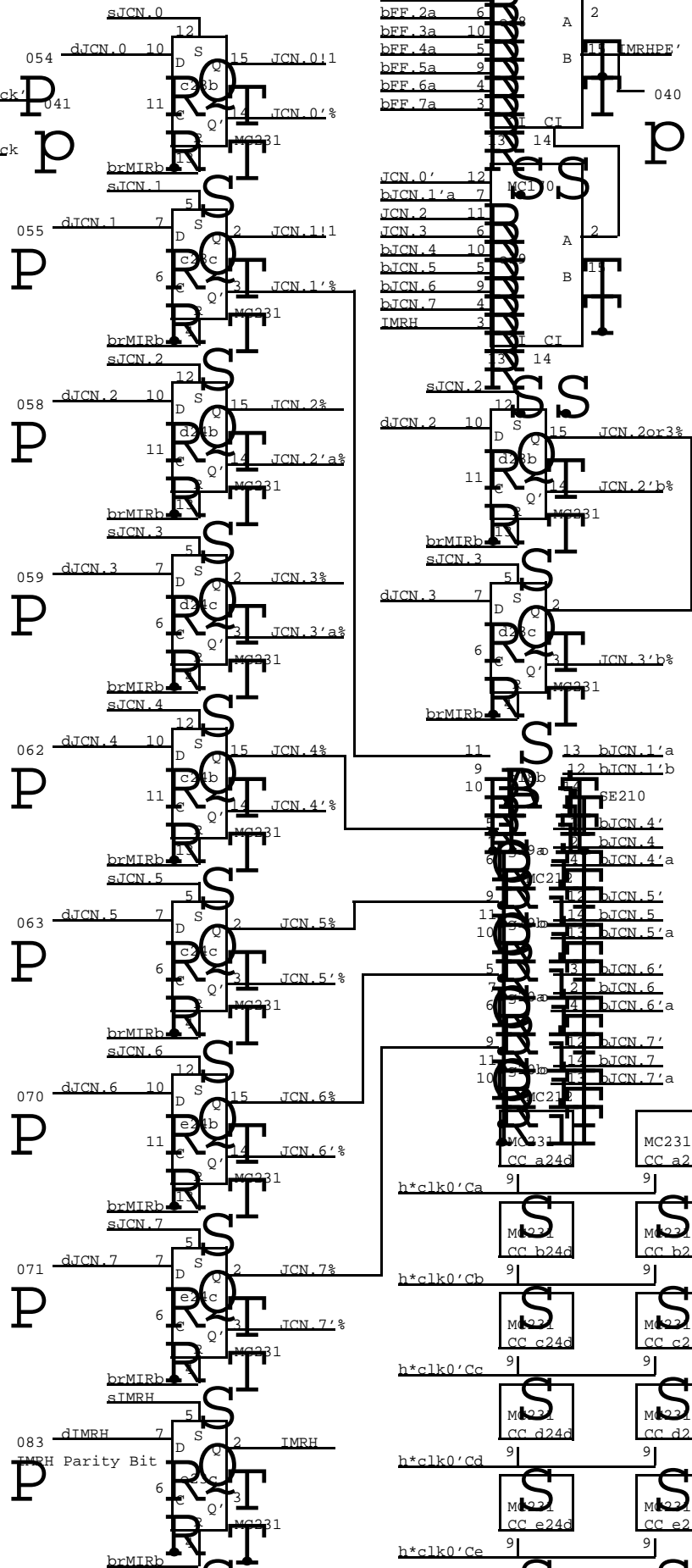
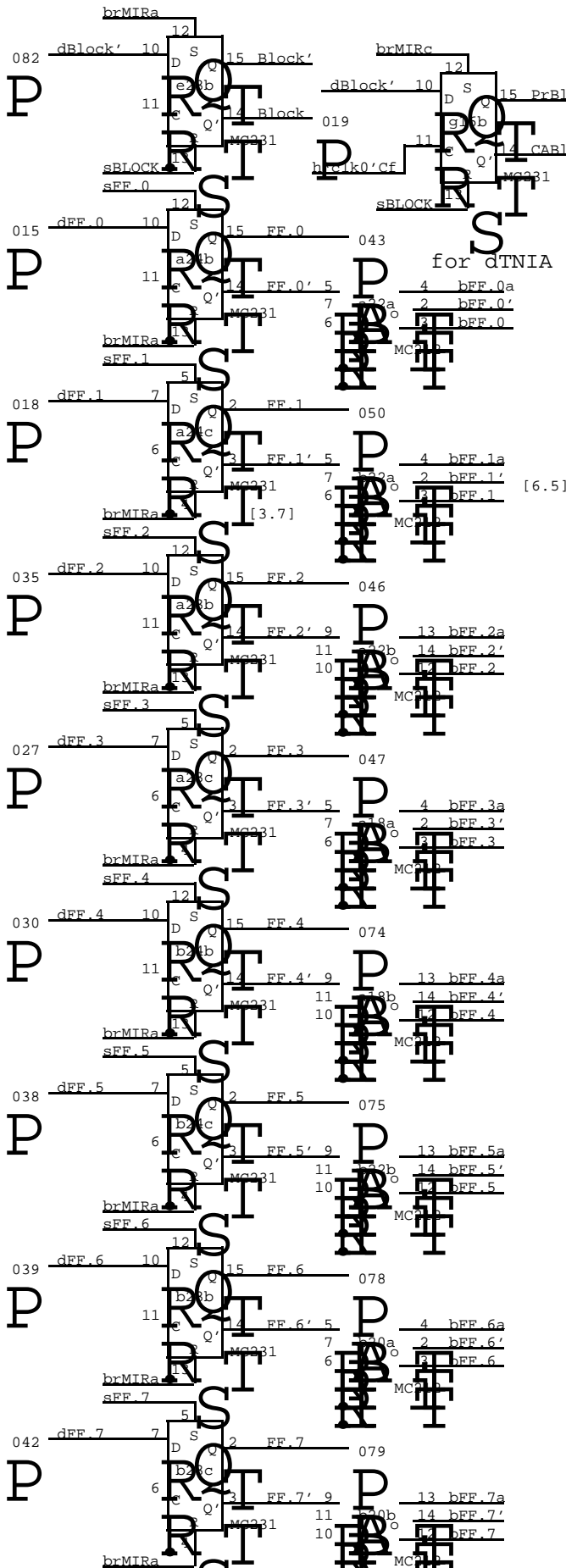


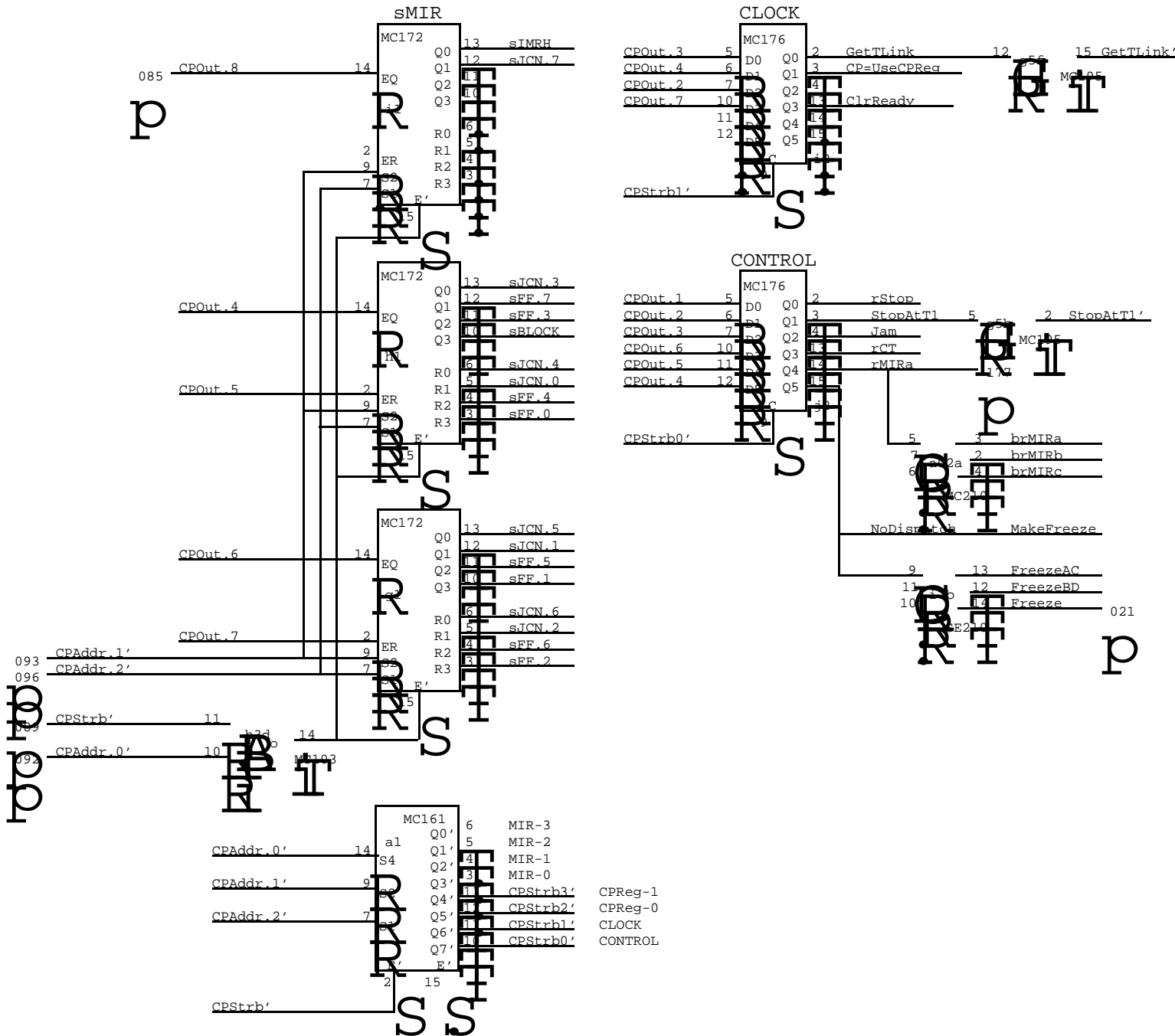
D O R A D O   S C H E M A T I C S

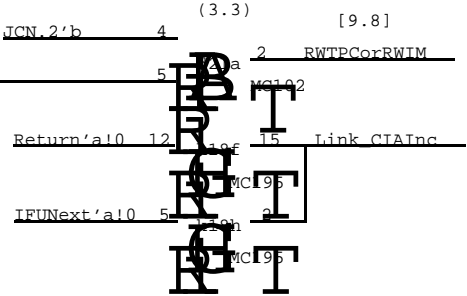
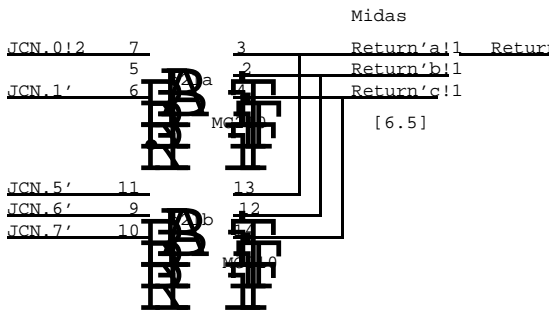
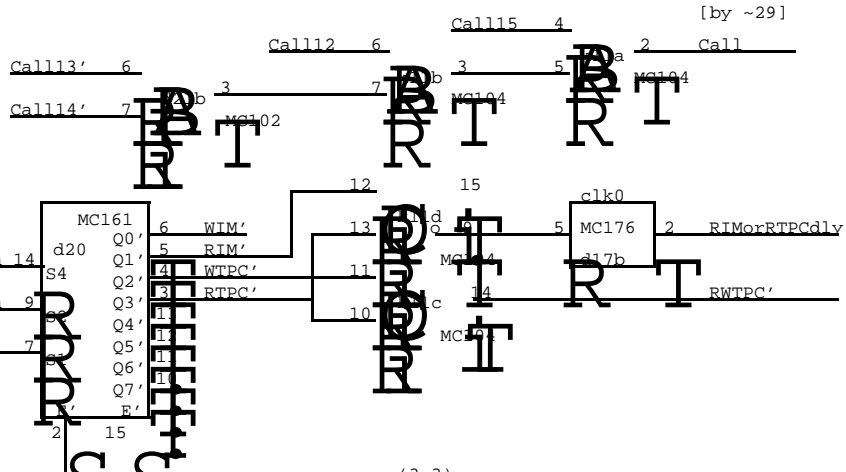
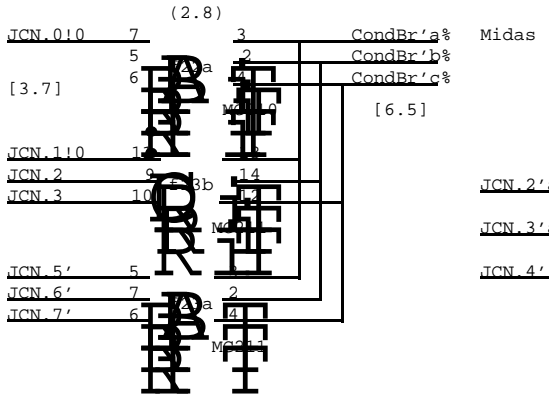
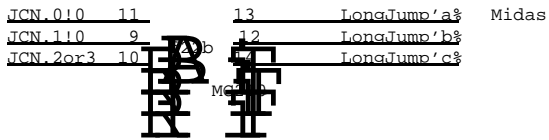
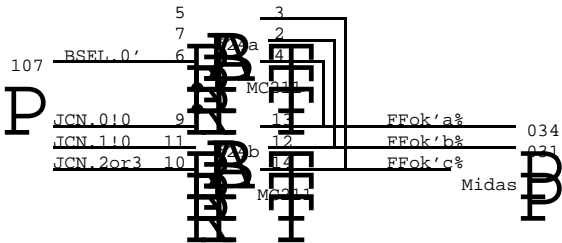
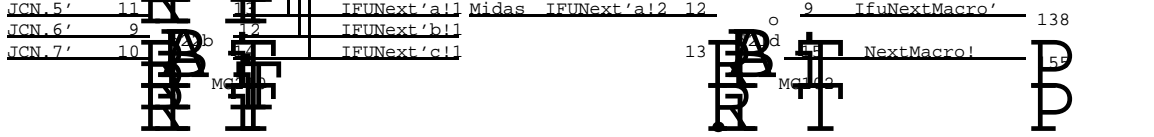
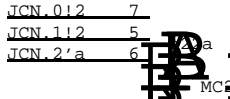
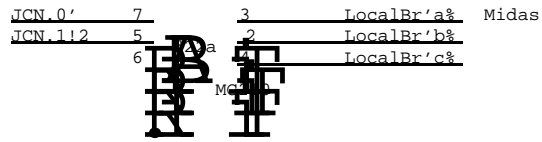
C o n t r o l   A

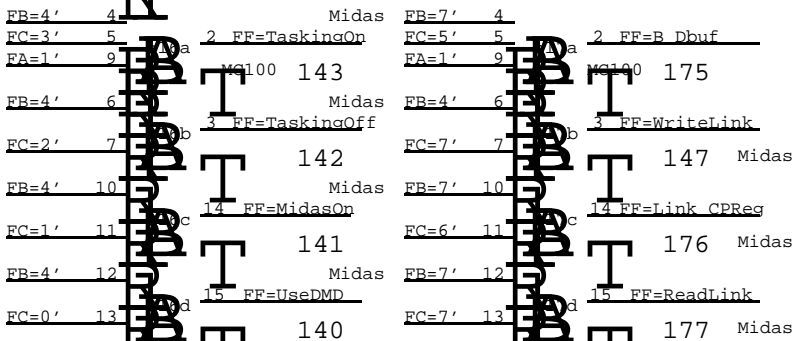
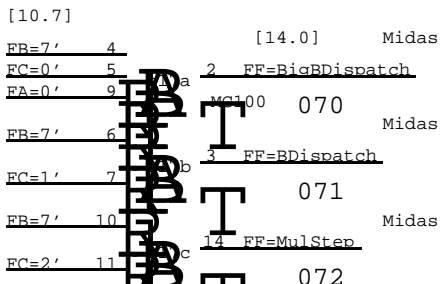
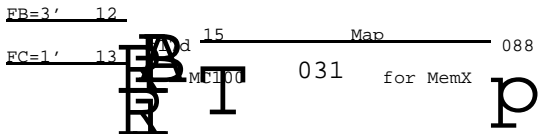
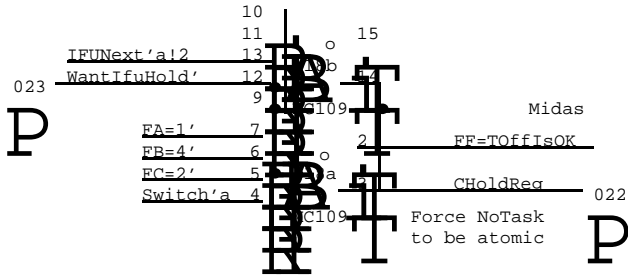
Table of contents

<u>TITLE</u>	<u>Page</u>
MIR- right half	01
CP Interface and Set MIR	02
JCN Decoding	03
FF Decoding	04
LinkX and Conditional Branch	05
Main Data Path, Bits 00 - 15	06 - 19
Control Slices for Data Path	20 - 21
Ready Logic 1	22
Ready Logic 2	23
Wakeup Priority Encoder	24
Task Switch logic	25
Task Registers:	
HTASK, BNT, CTASK, CTD, NEXT	26
Phase generator	27
Midas 1	28
Midas 2	29
Clocks	30
PreClock generator	31
Memory System Clock generator	32
Layout	33

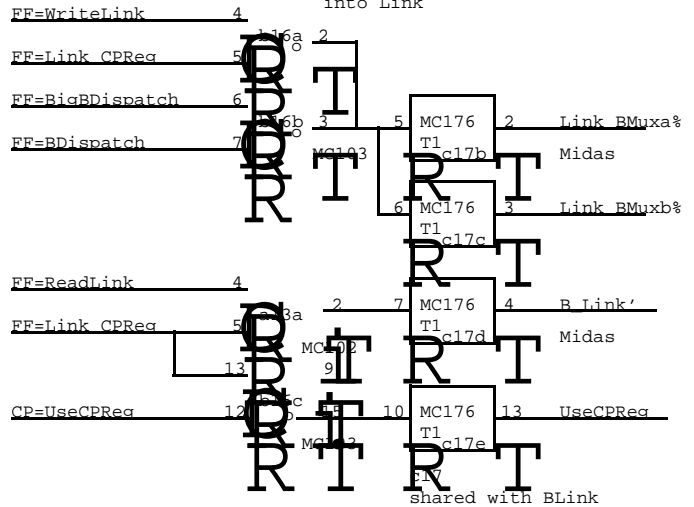
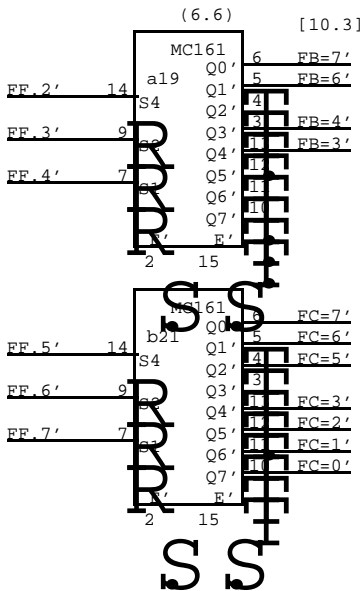
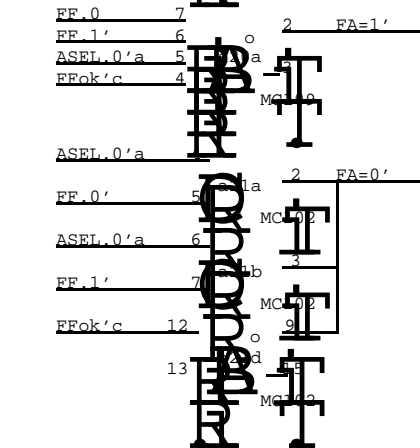
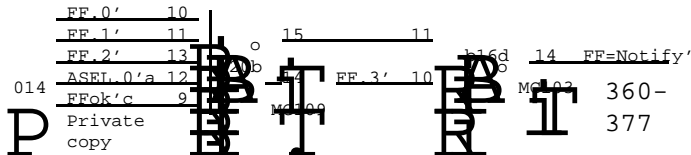




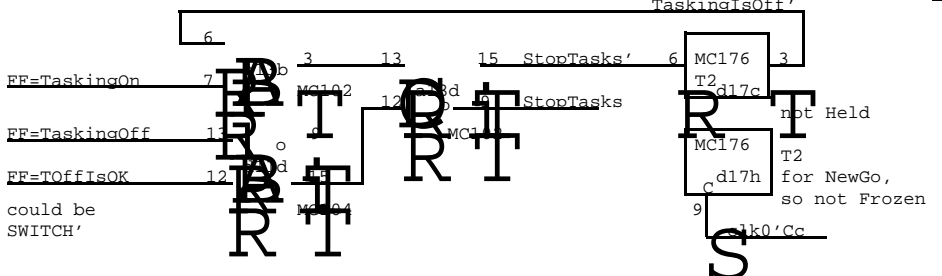
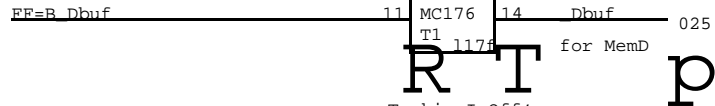




FF=Link\_CPREg loads  
compliment of CPReg  
into Link



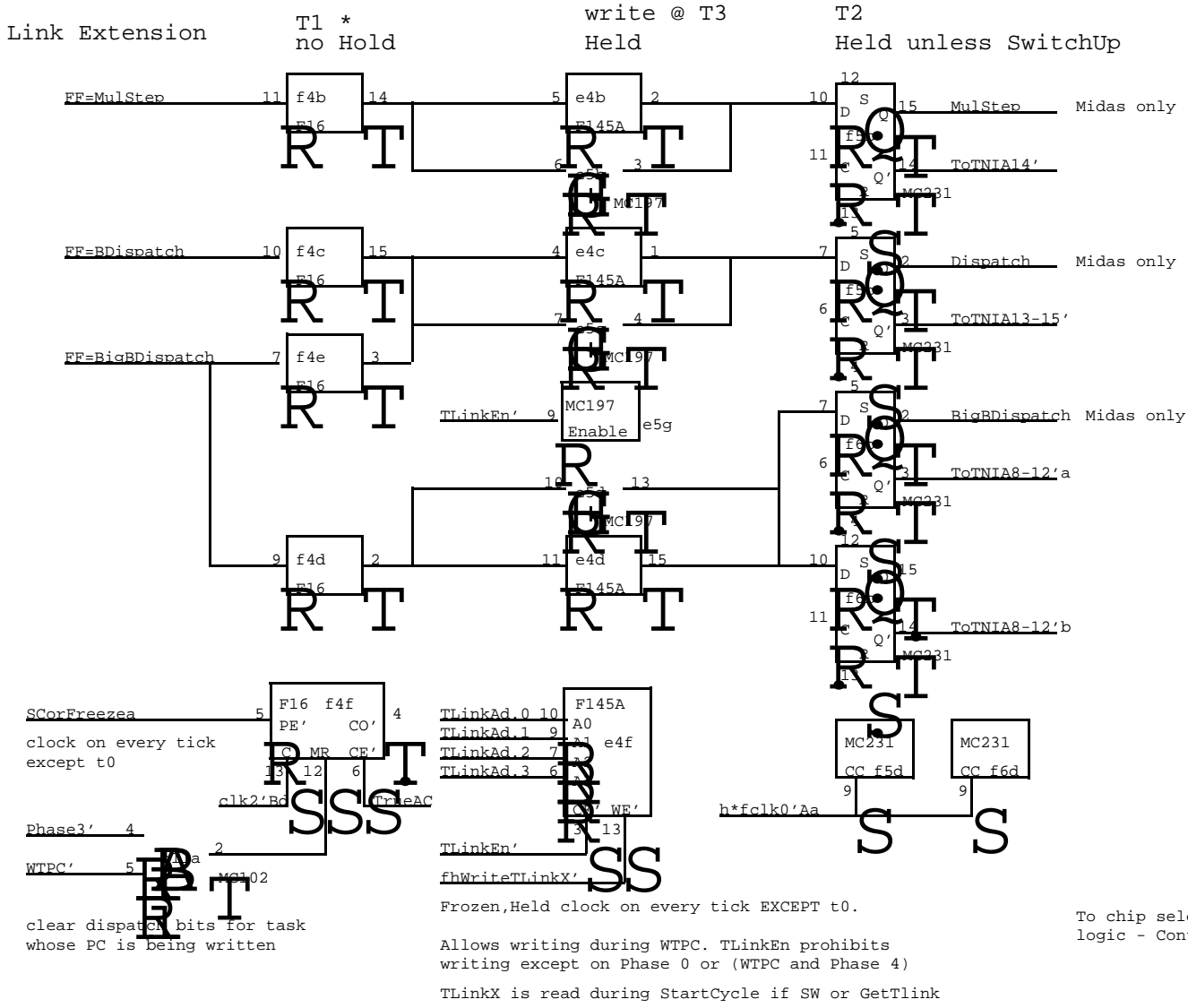
shared with Blink



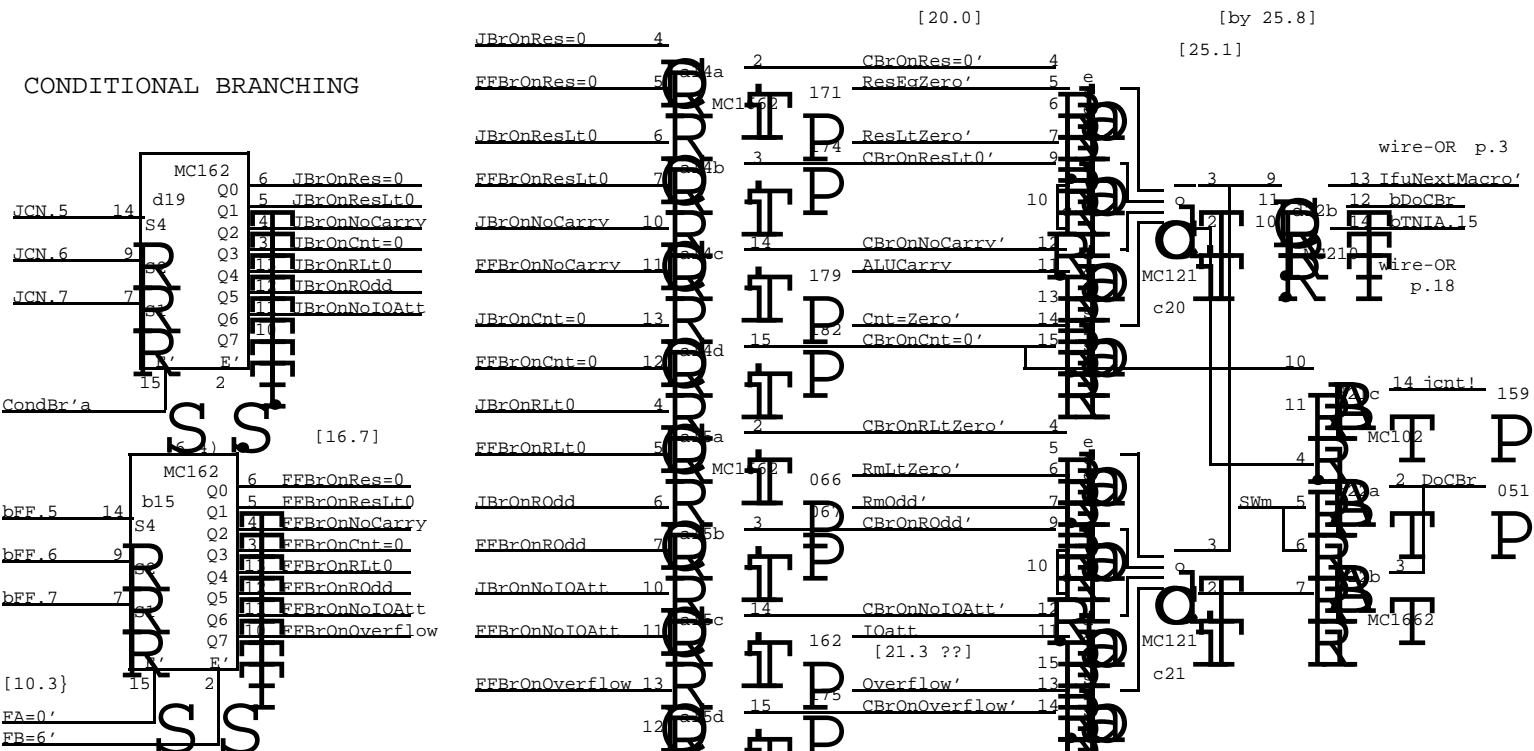
NOTE: TakingOff is aborted  
and HOLD is requested if  
Switch is pending when  
TaskingOff is executed

could be  
SWITCH'

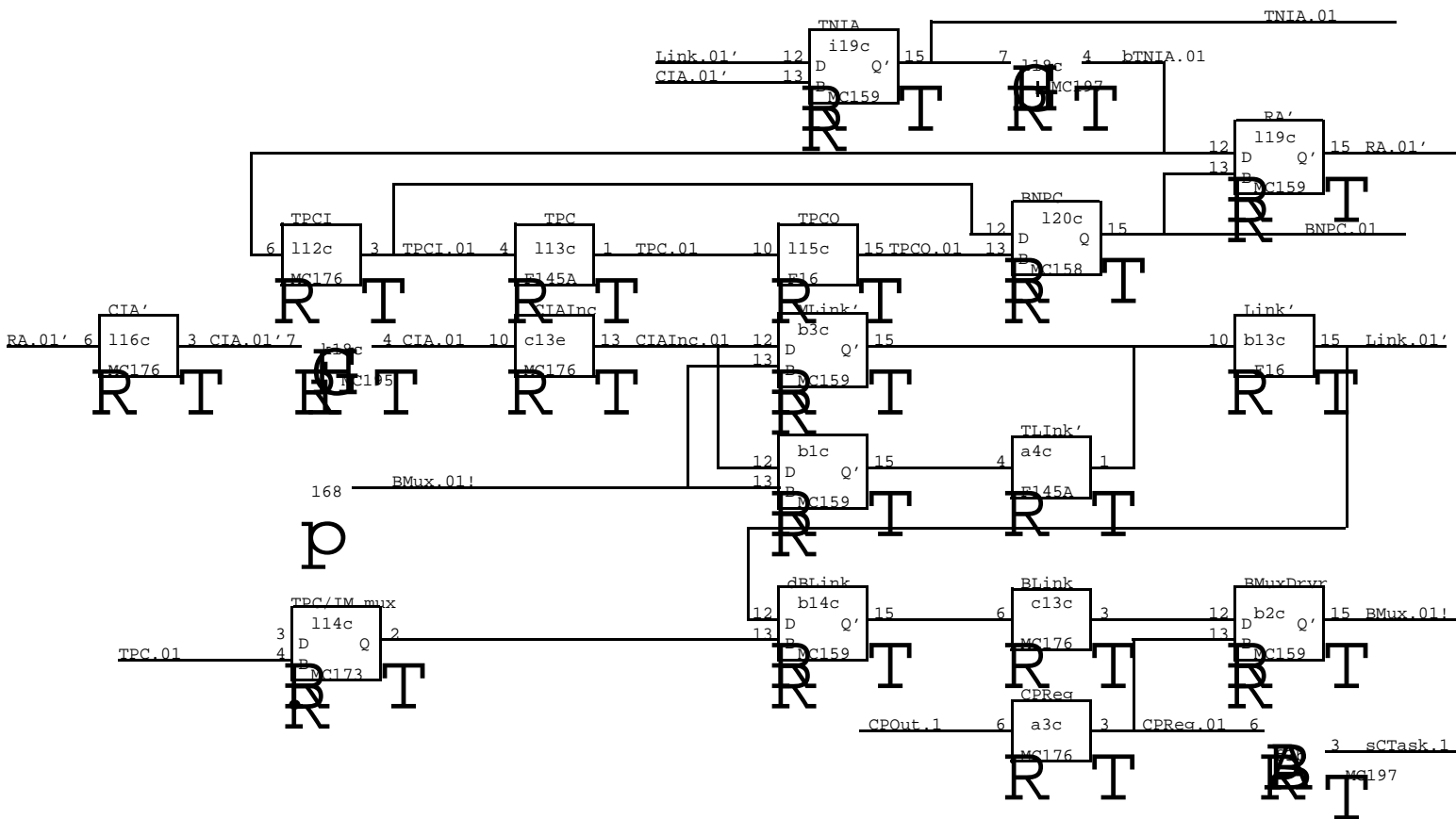
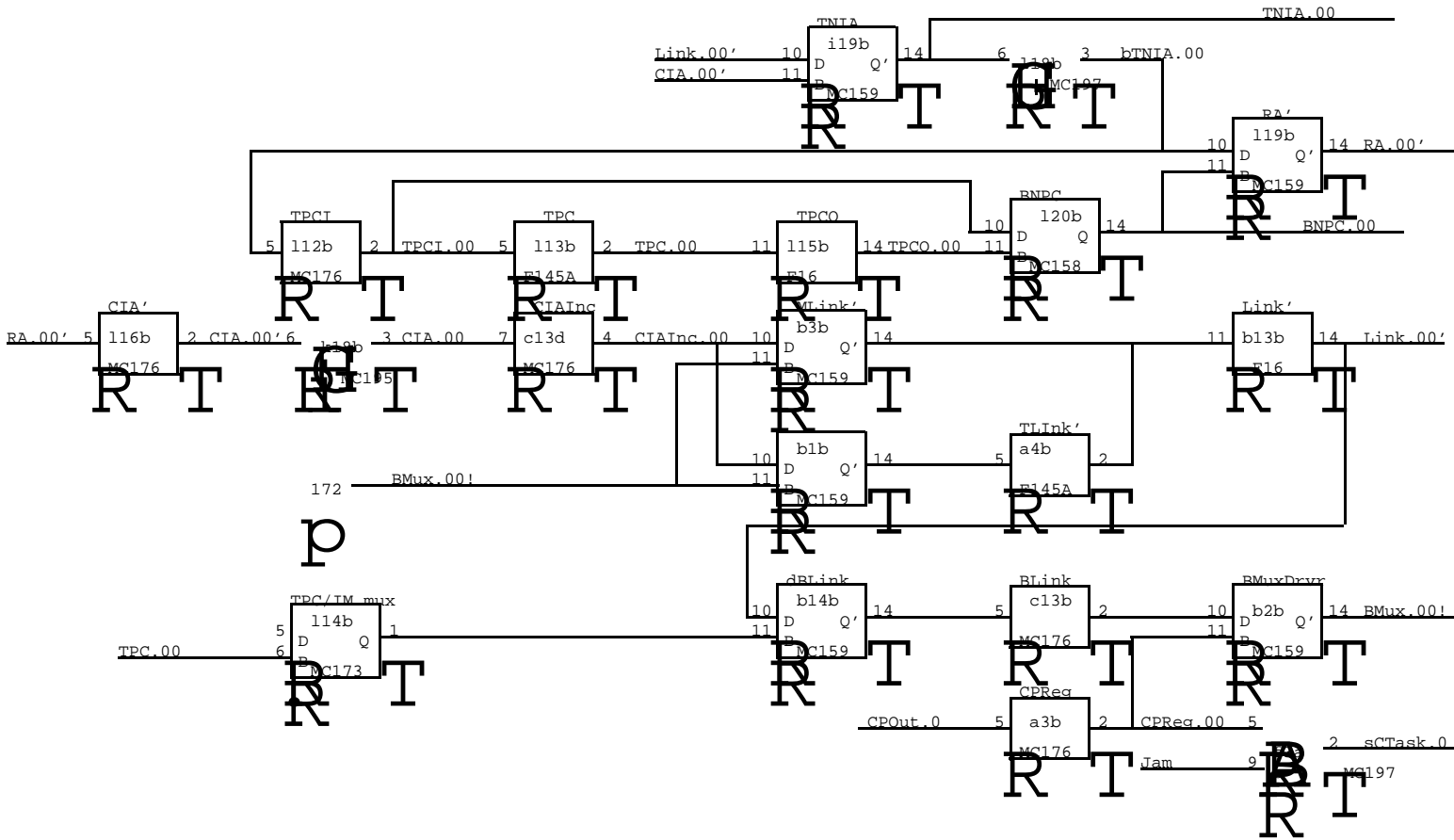
XEROX PARC	Project Dorado	Dorado Control FF DECODING LOGIC	File ContA04.sil	Designer Pier	Rev Da	Date 7/13/79	Page 04
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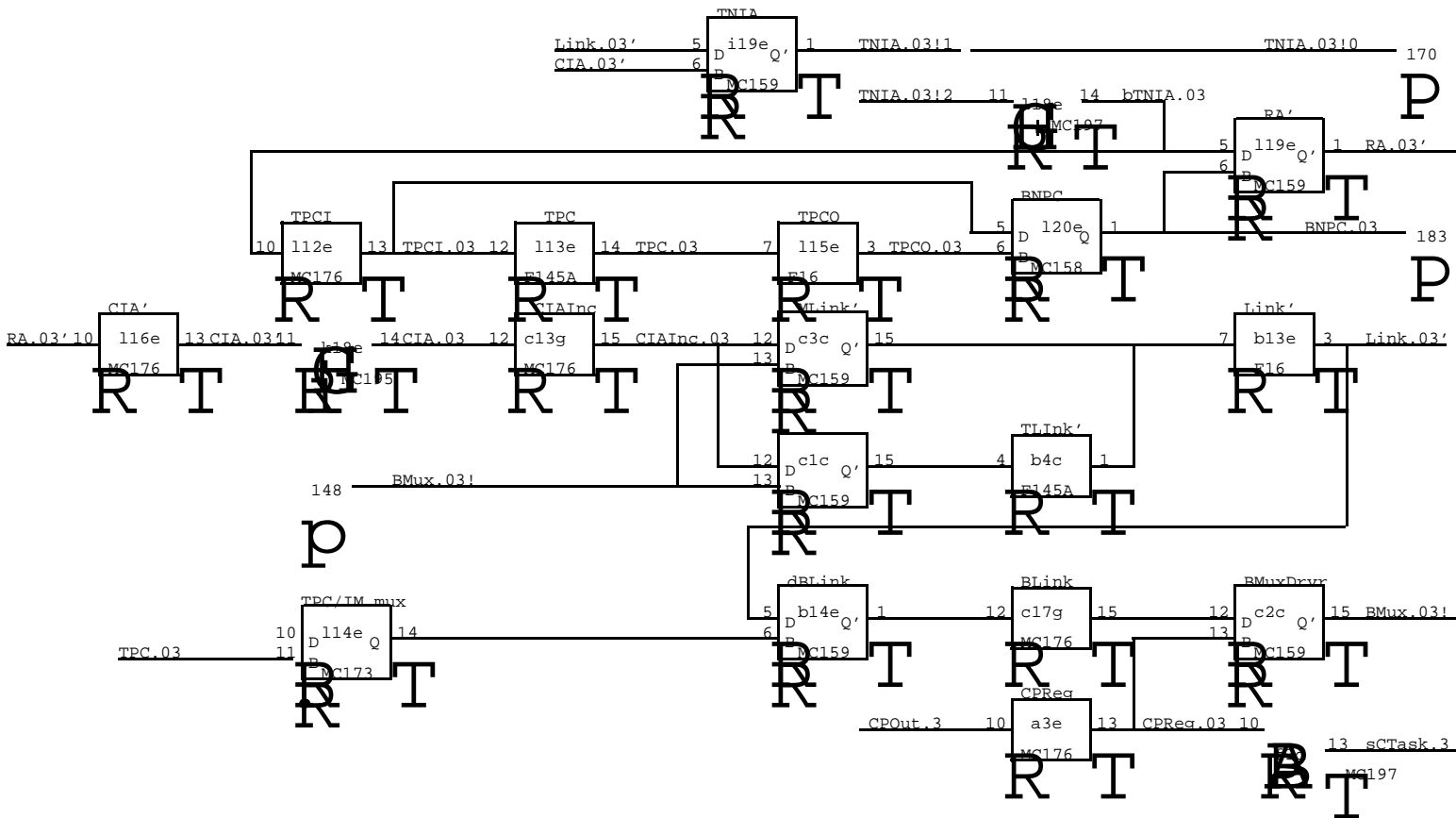
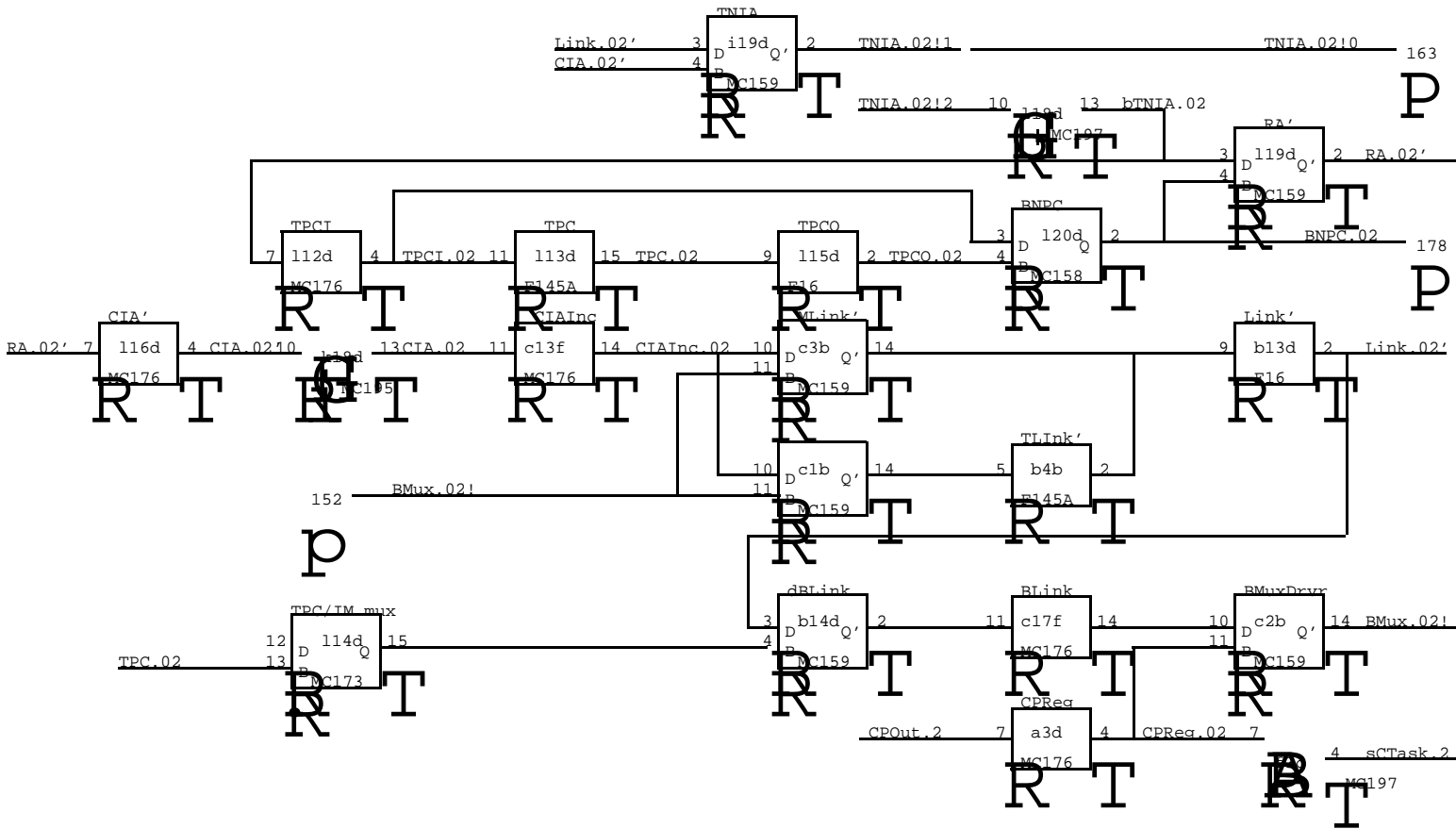
CONDITIONAL BRANCHING



XEROX PARC	Project Dorado	Link Extension Register Conditional Branch Logic	File ContA05.sil	Designer Pier	Rev Da	Date 7/13/79	Page 05
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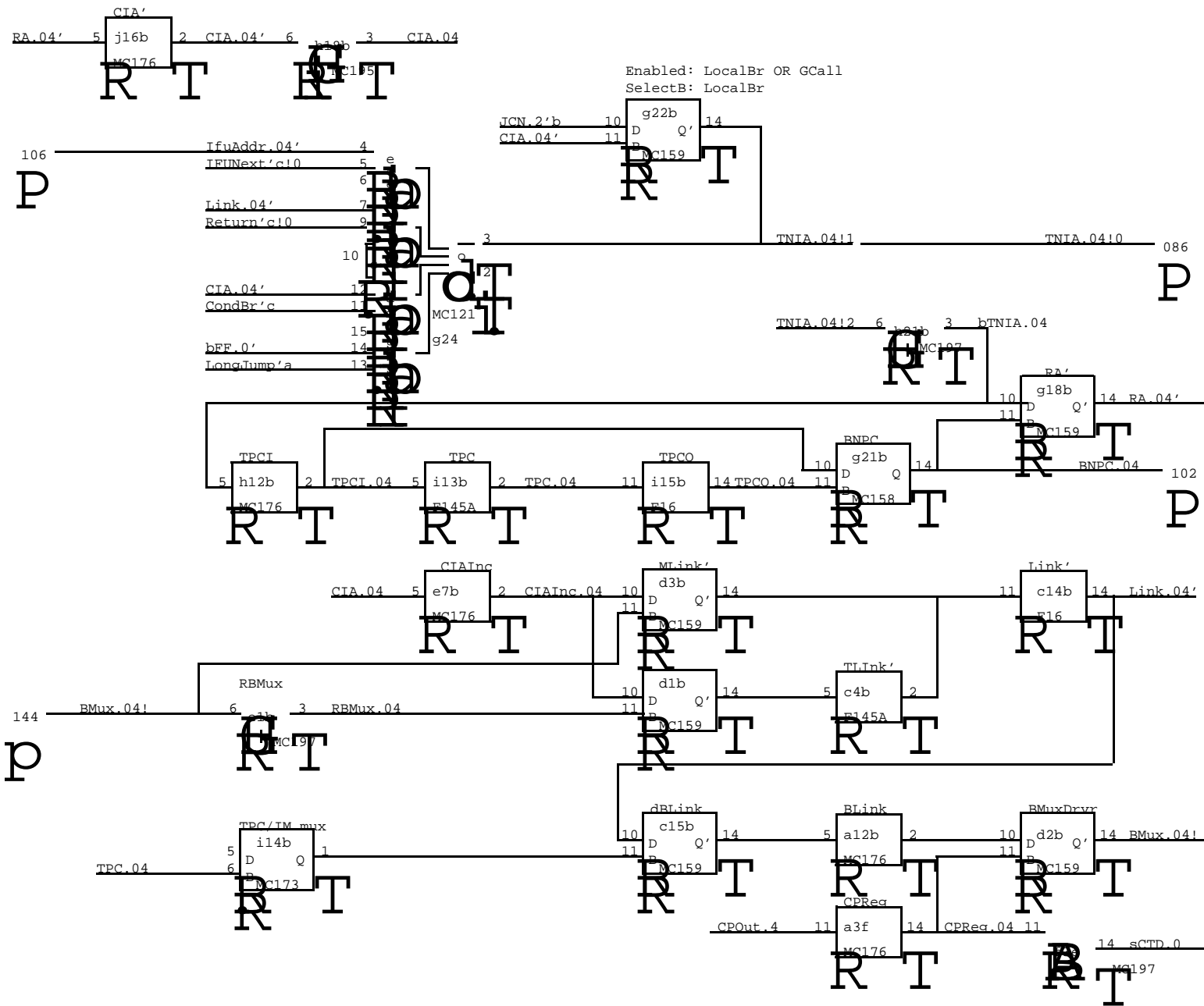


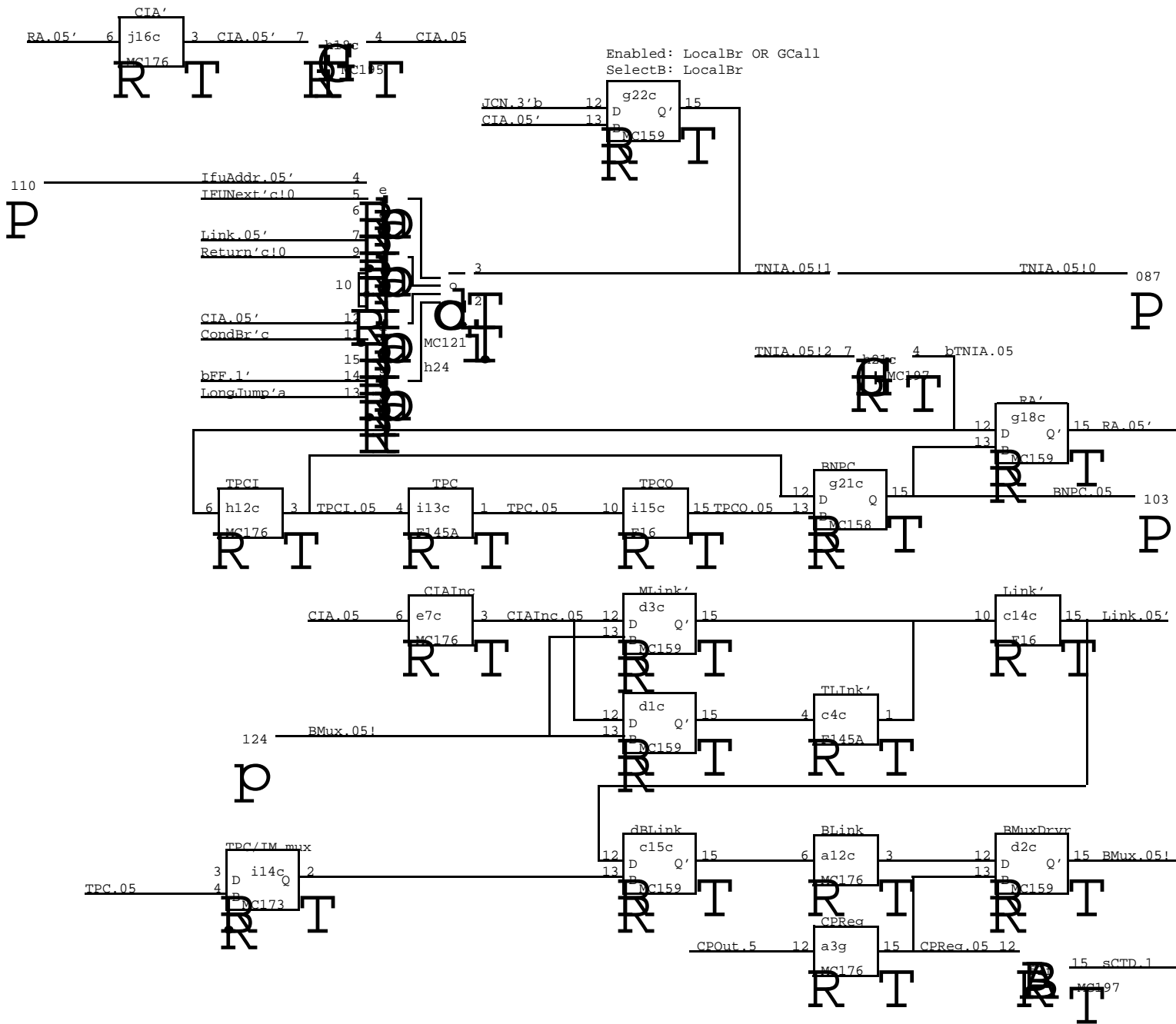
XEROX PARC	Project Dorado	Control Section Data Paths	File ContA06.sil	Designer Pier	Rev Da	Date 7/13/79	Page 06
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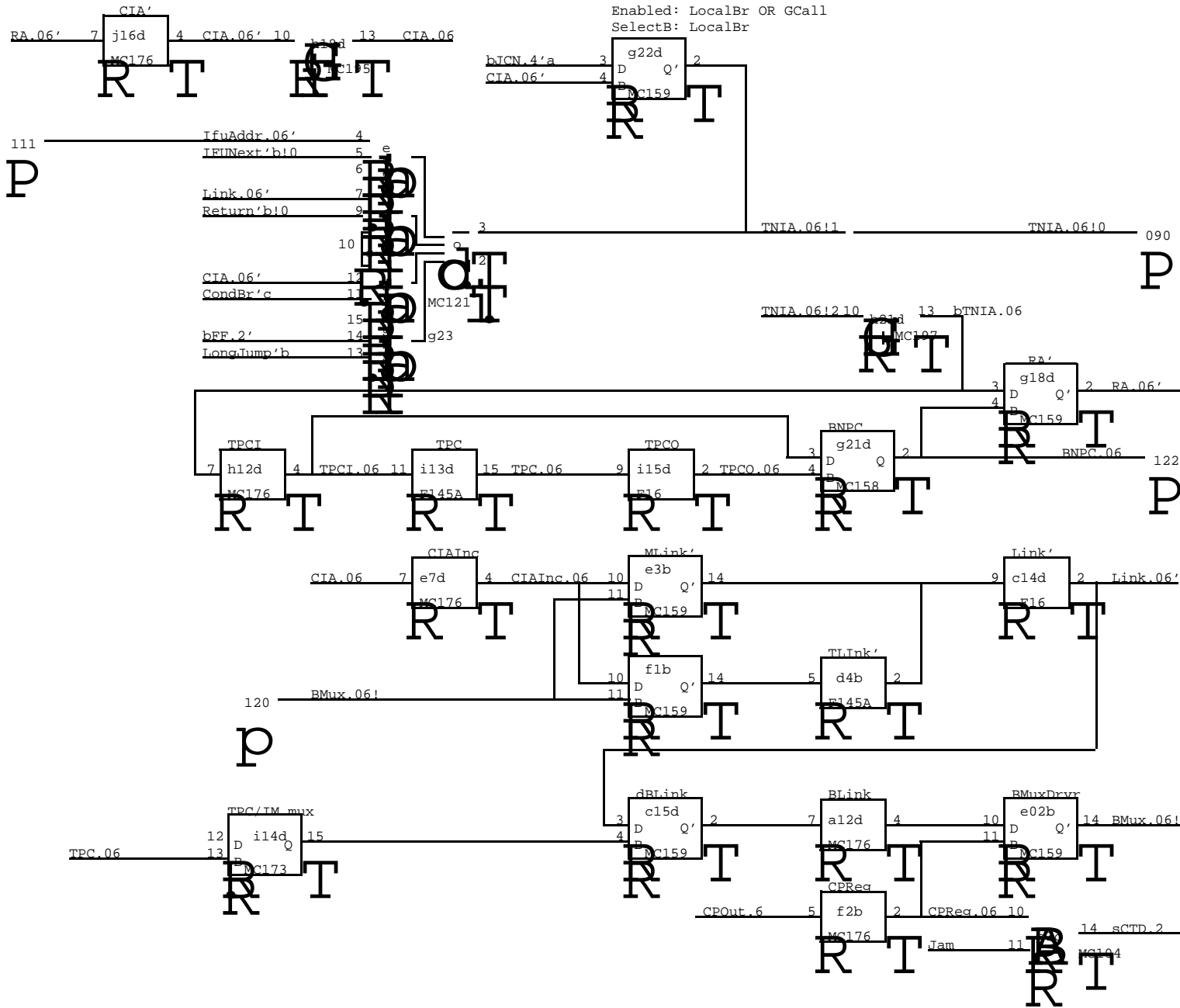


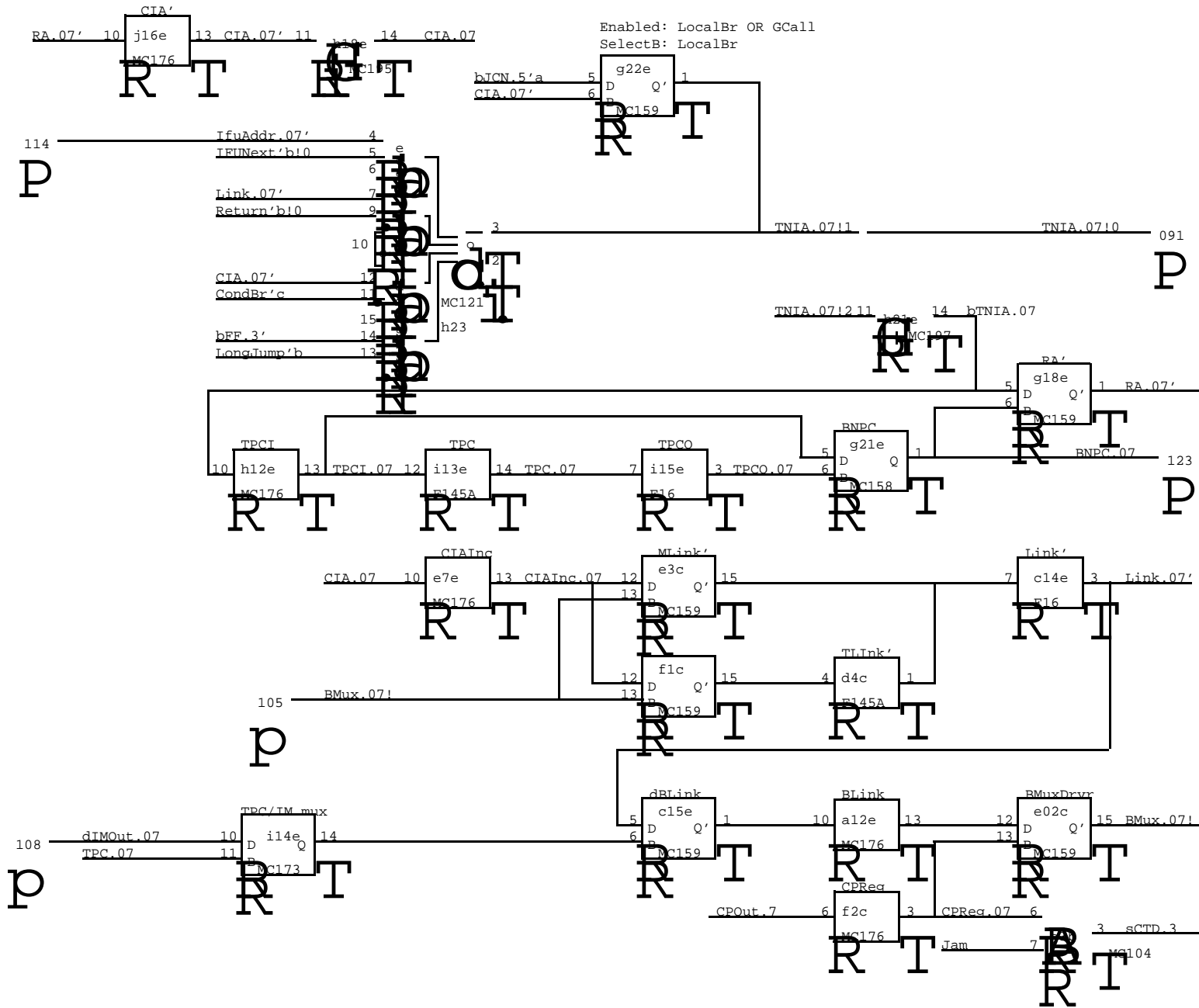
XEROX PARC	Project Dorado	Control Section Data Paths	File ContA07.sil	Designer Pier	Rev Da	Date 7/13/79	Page 07
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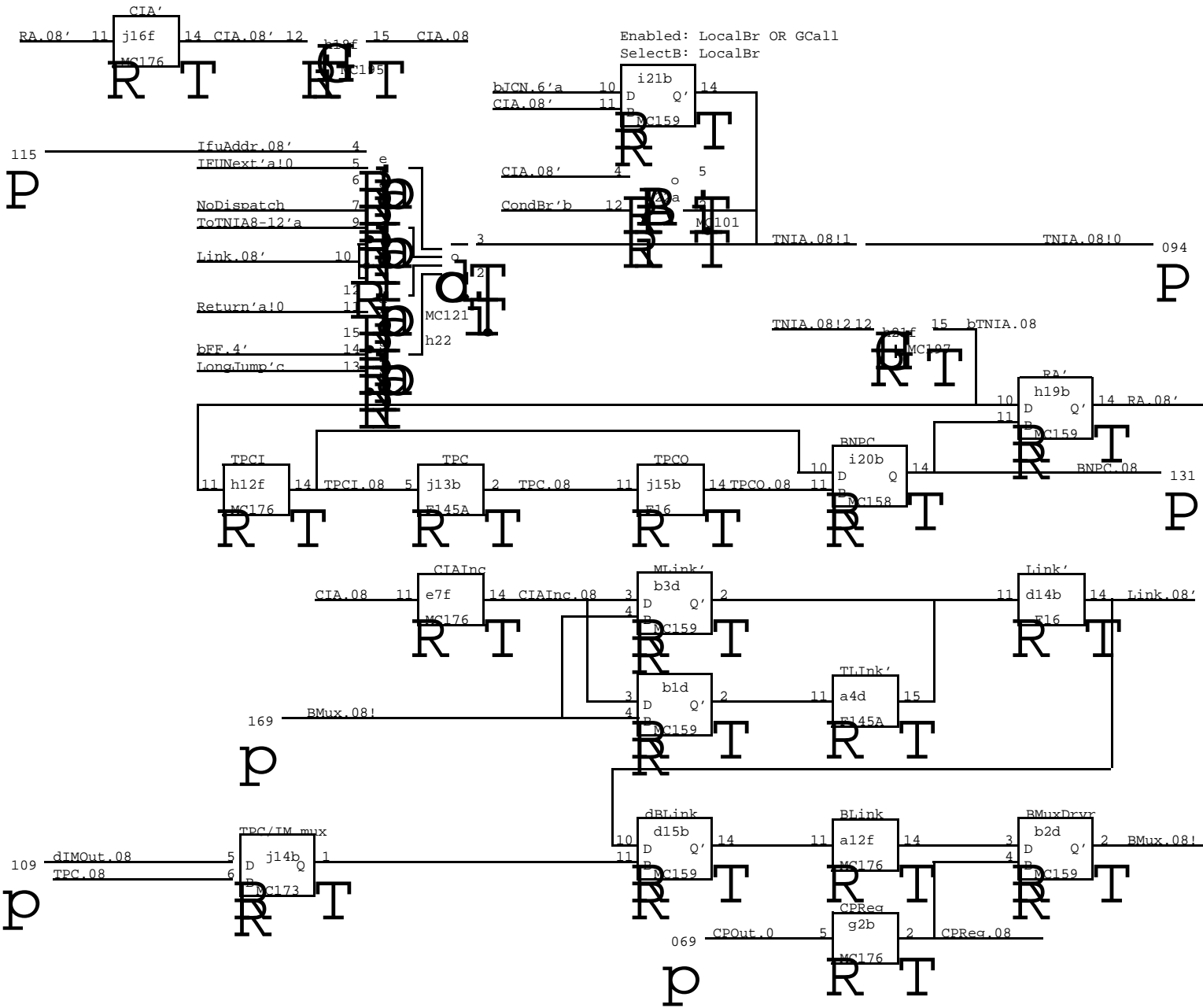


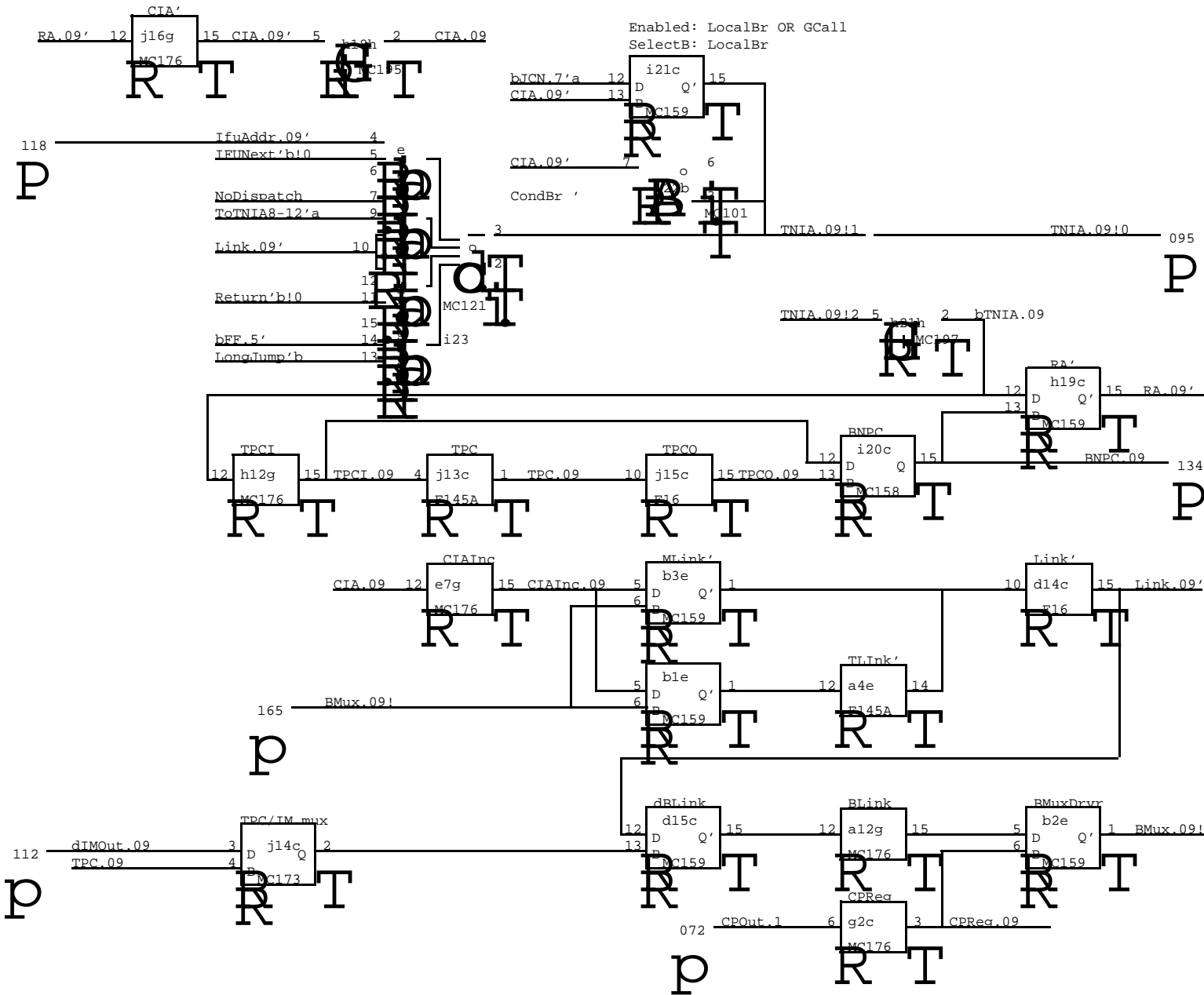


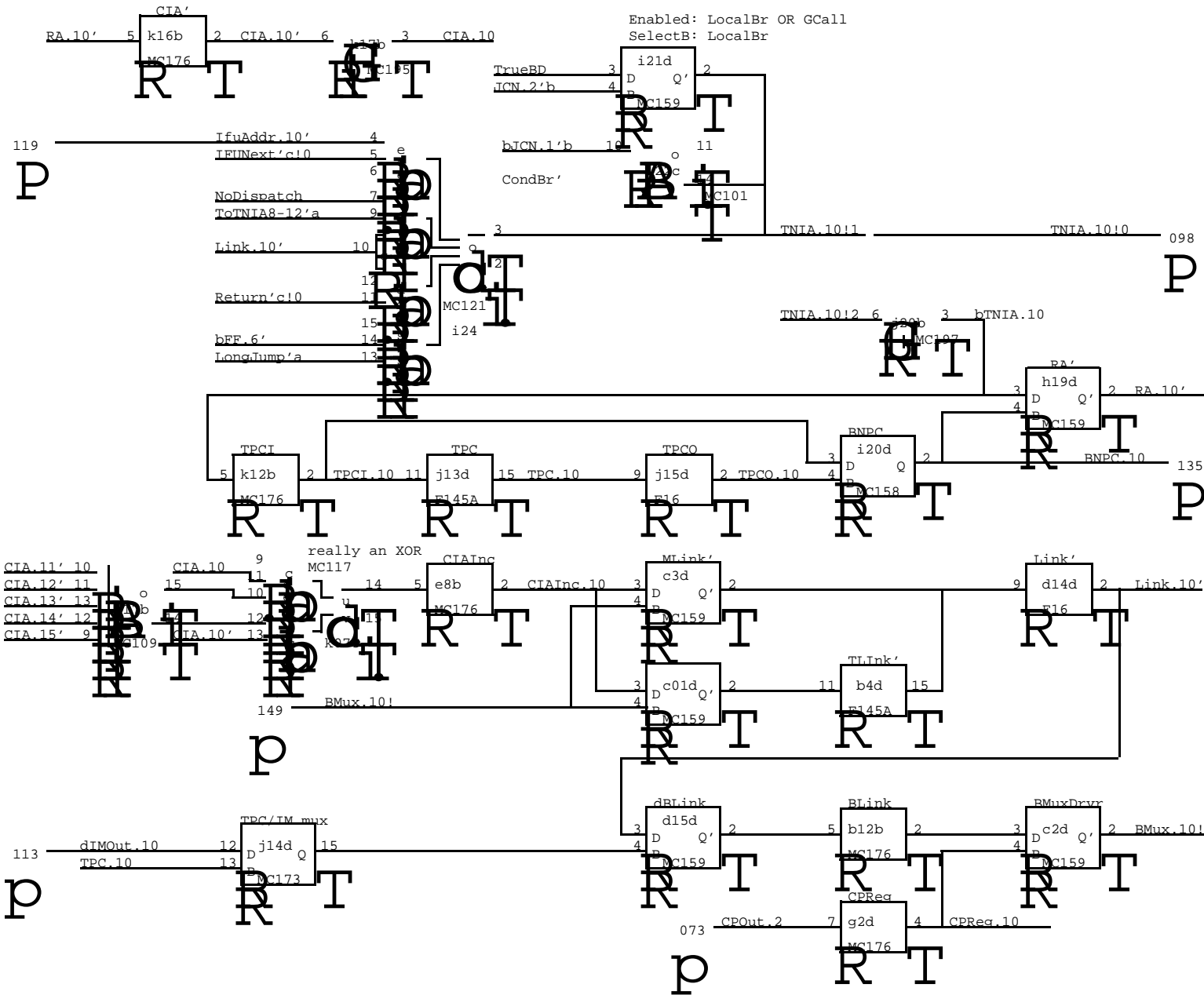


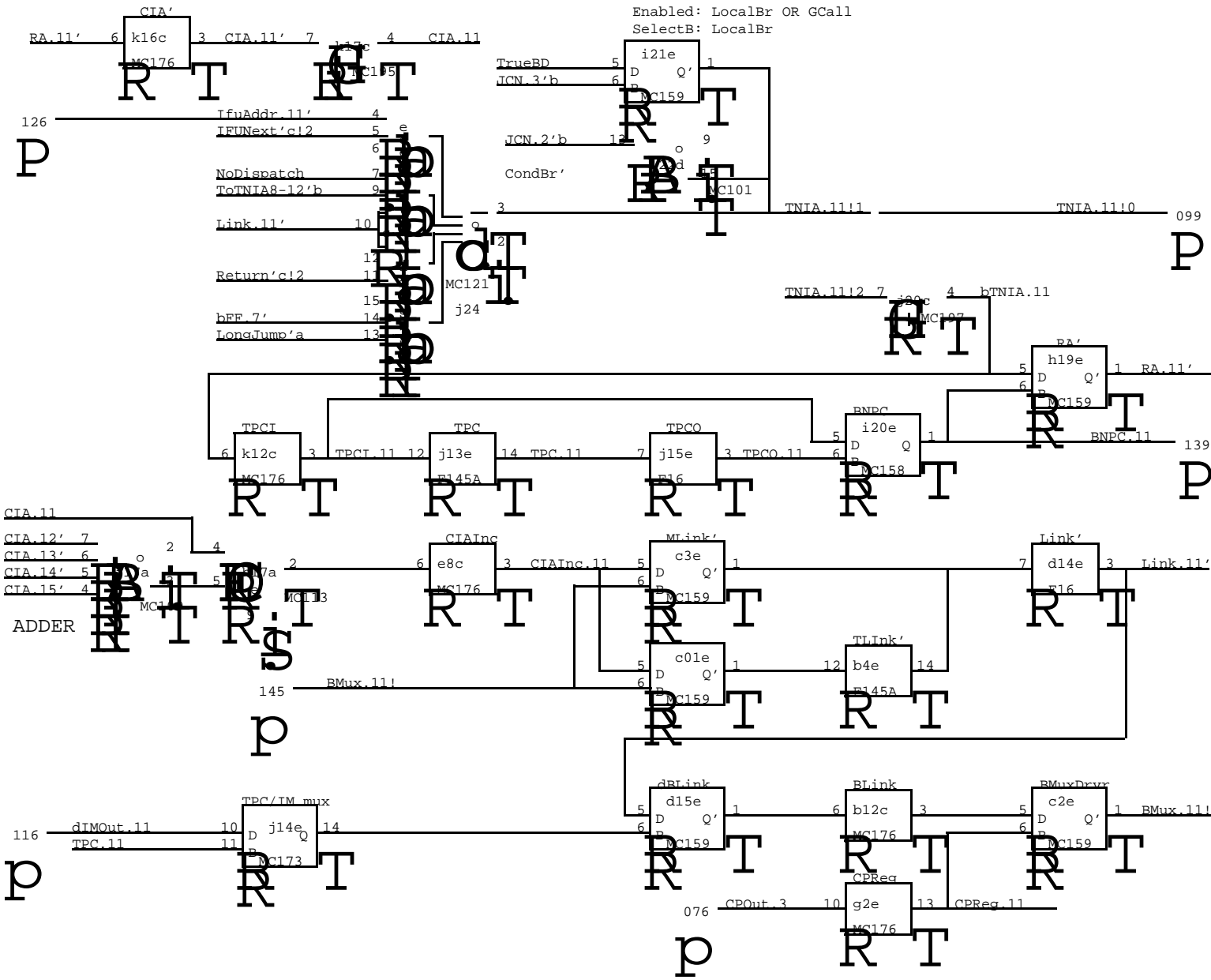




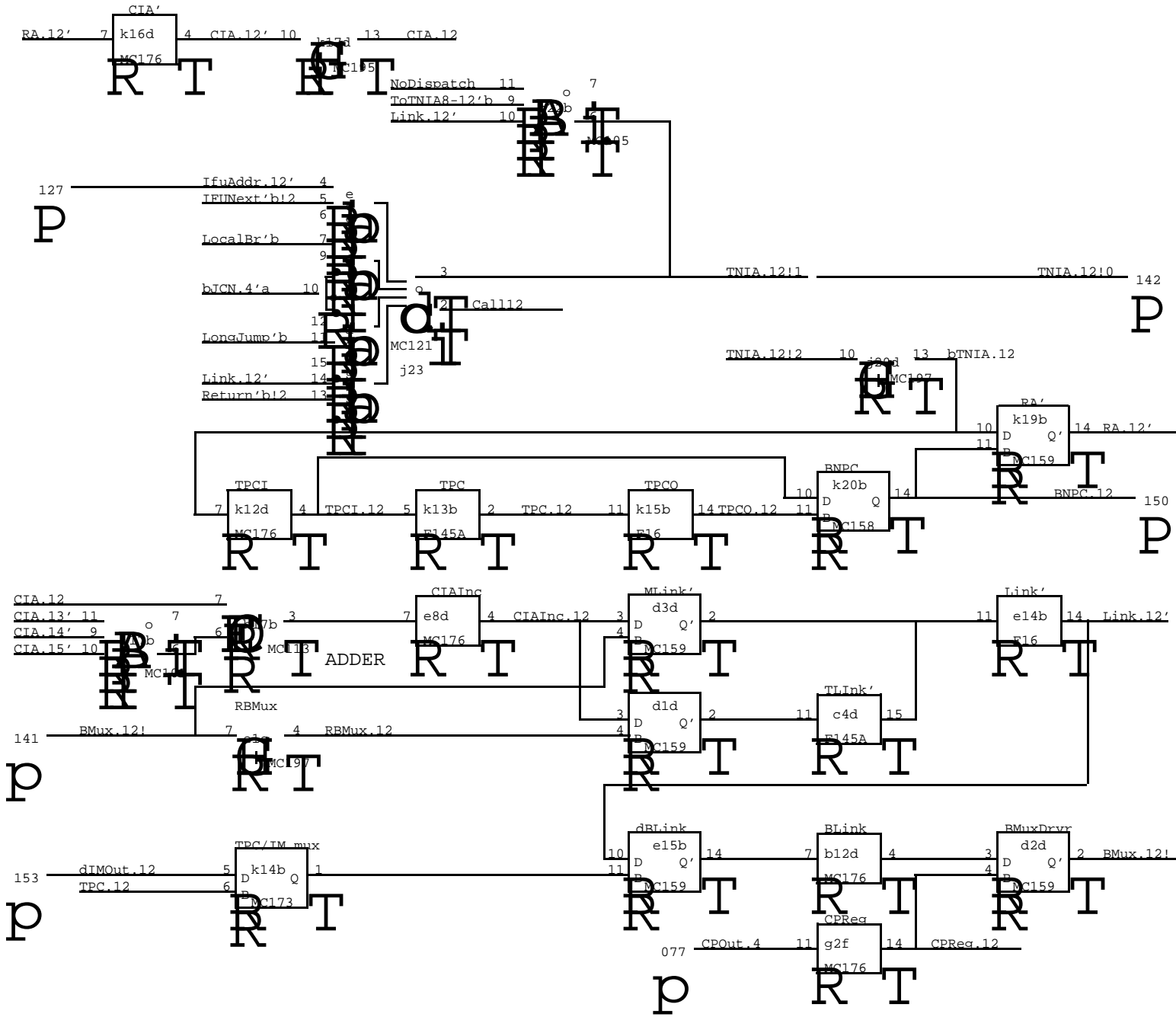


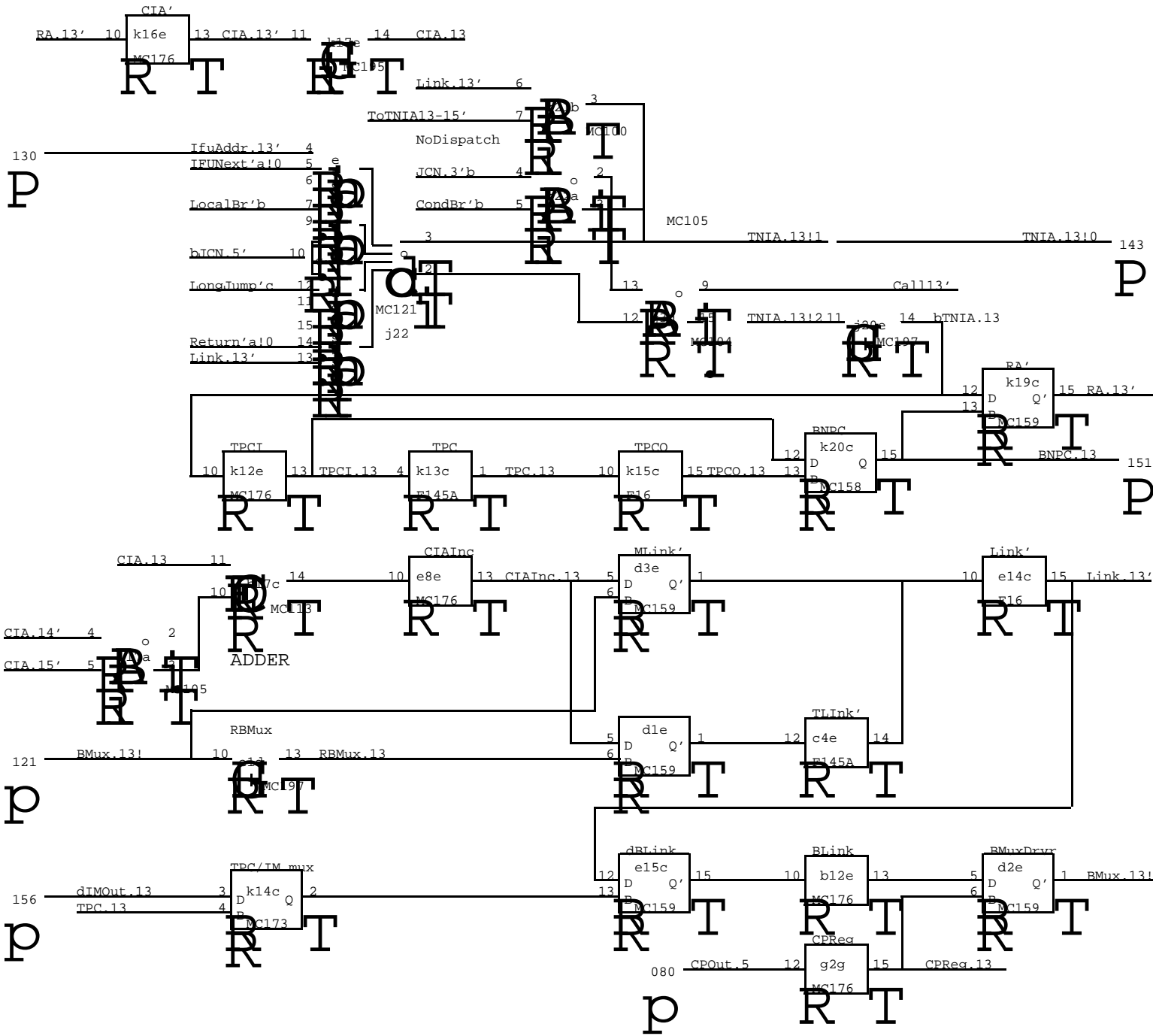


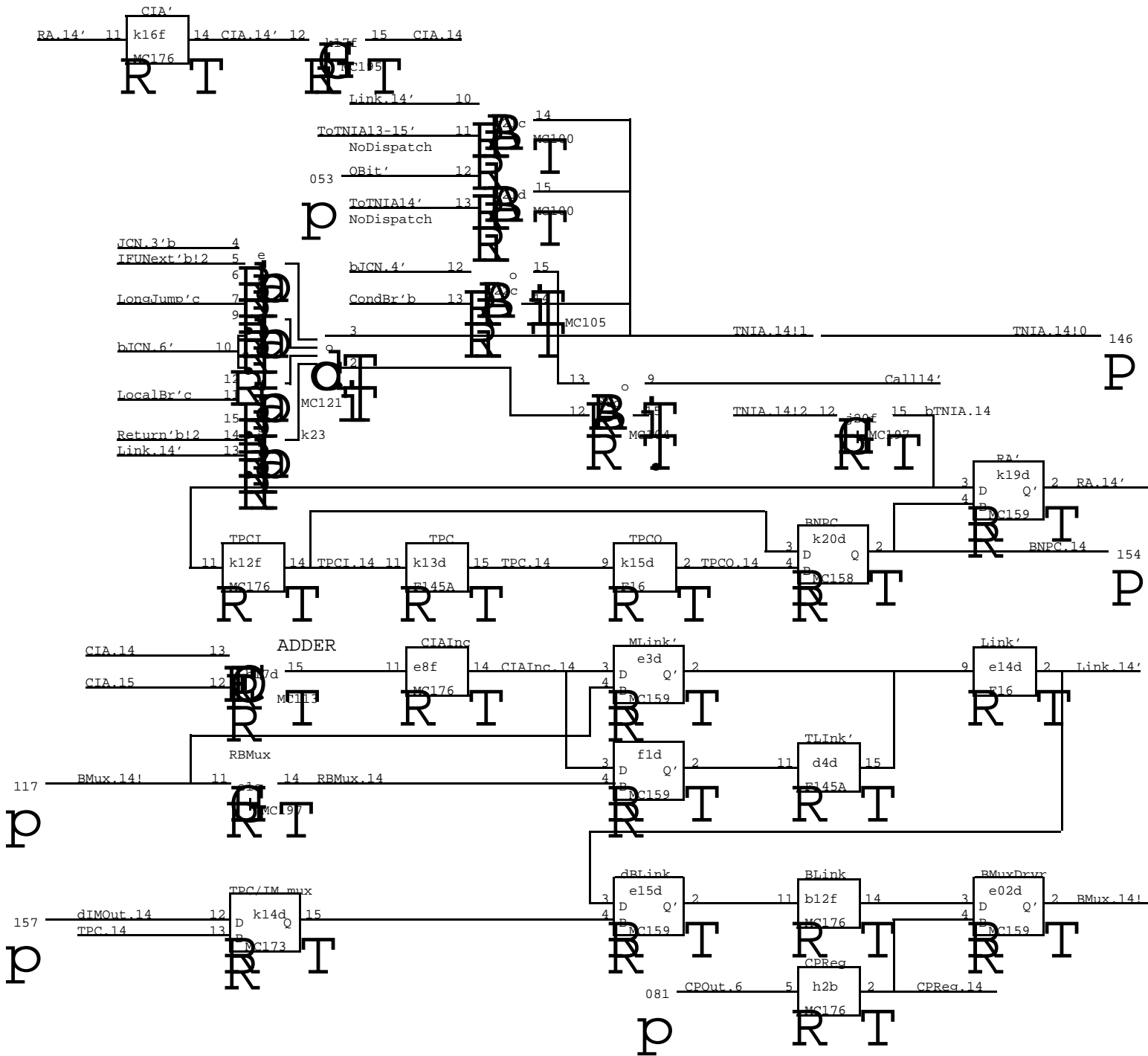


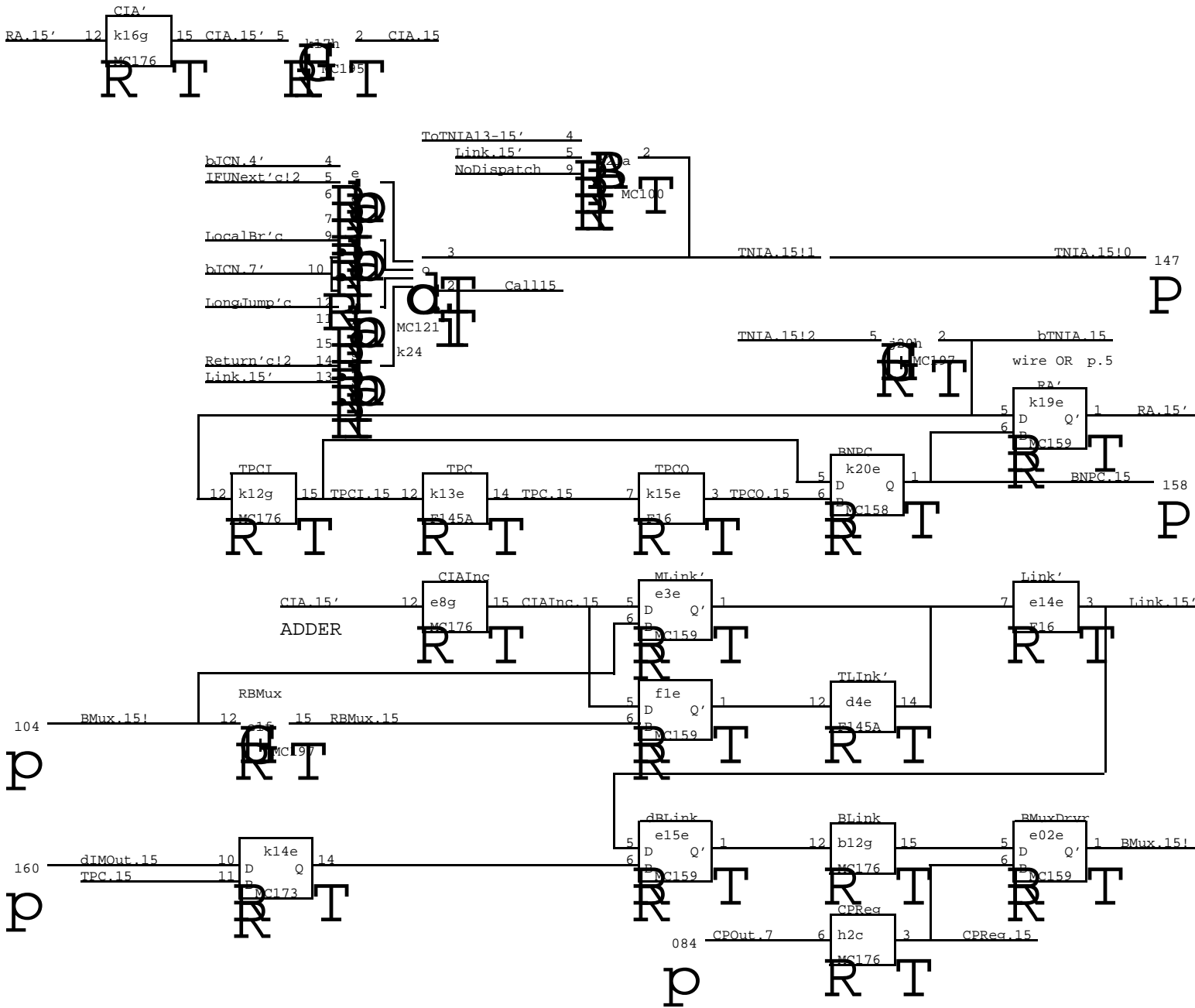


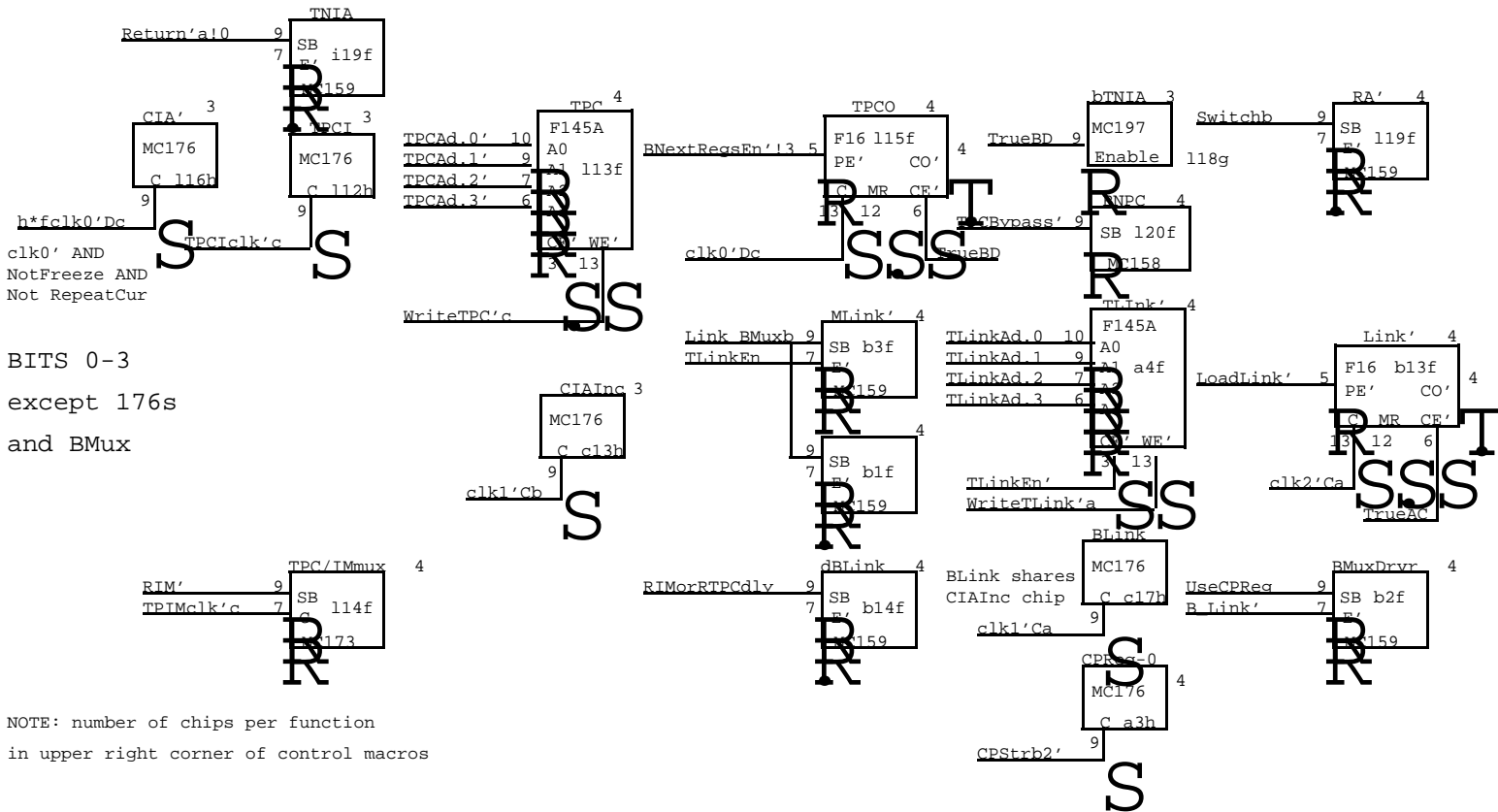






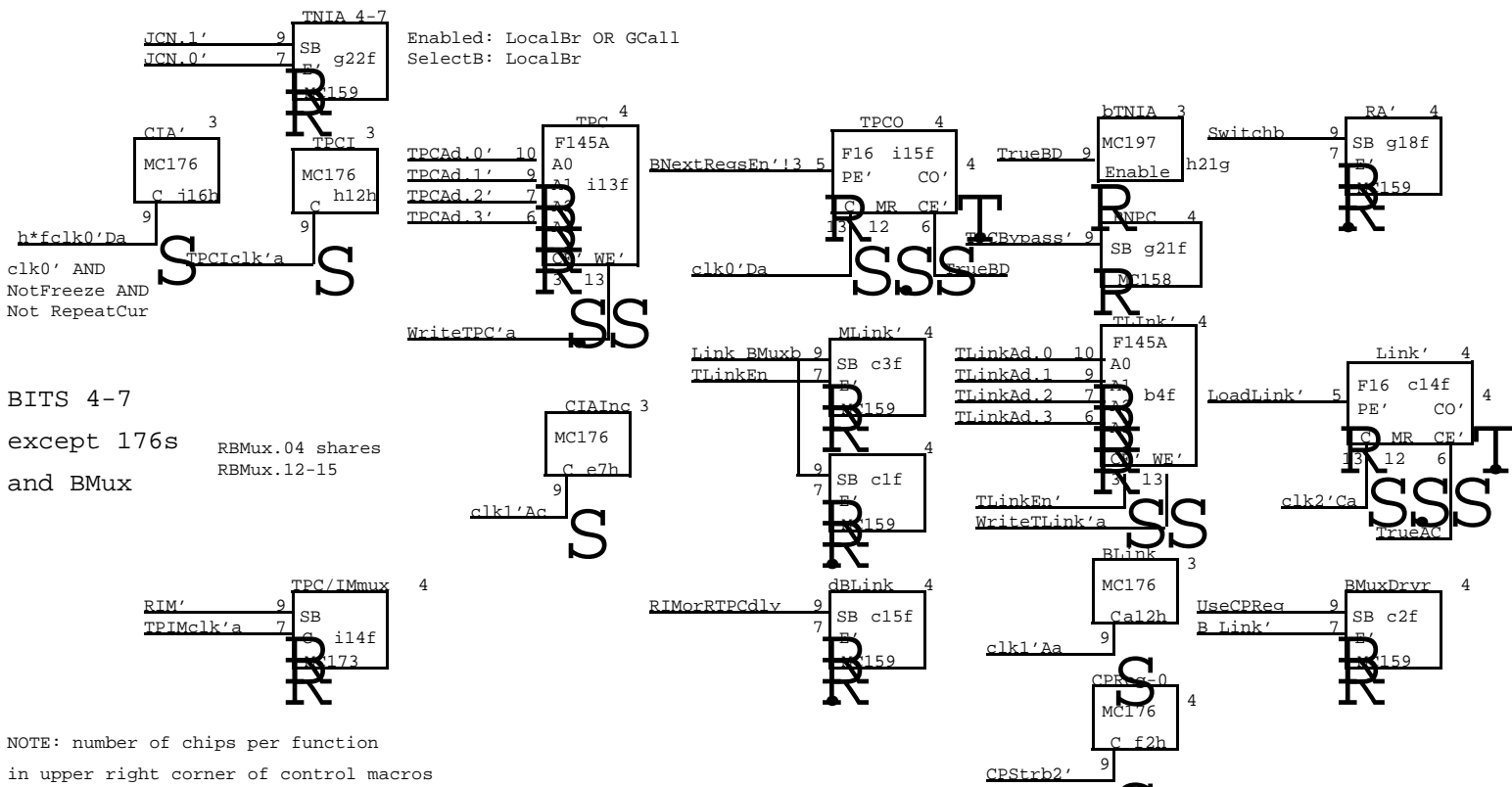






BITS 0-3  
except 176s  
and BMux

NOTE: number of chips per function  
in upper right corner of control macros

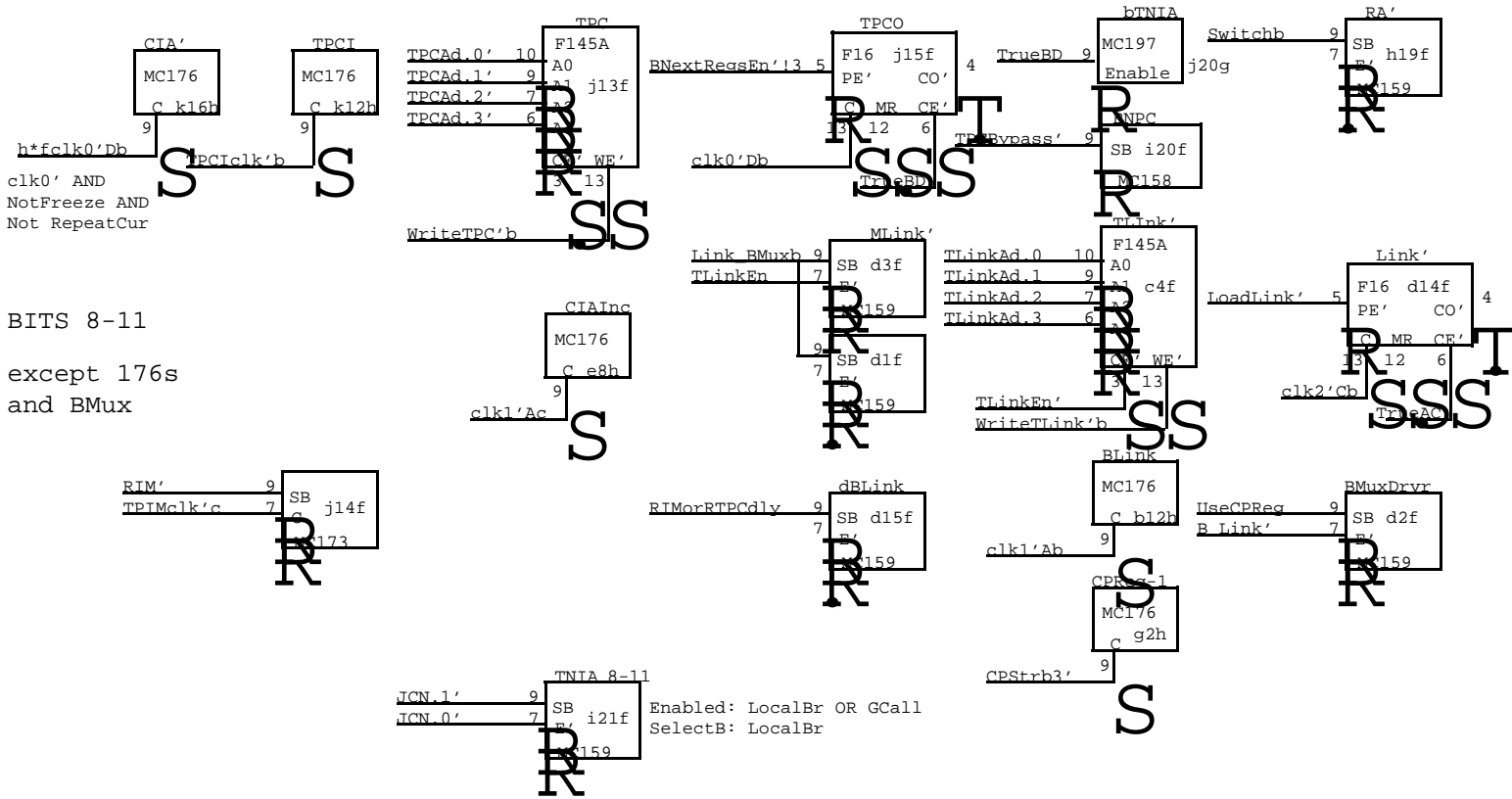


BITS 4-7  
except 176s  
and BMux

RBMux.04 shares  
RBMux.12-15

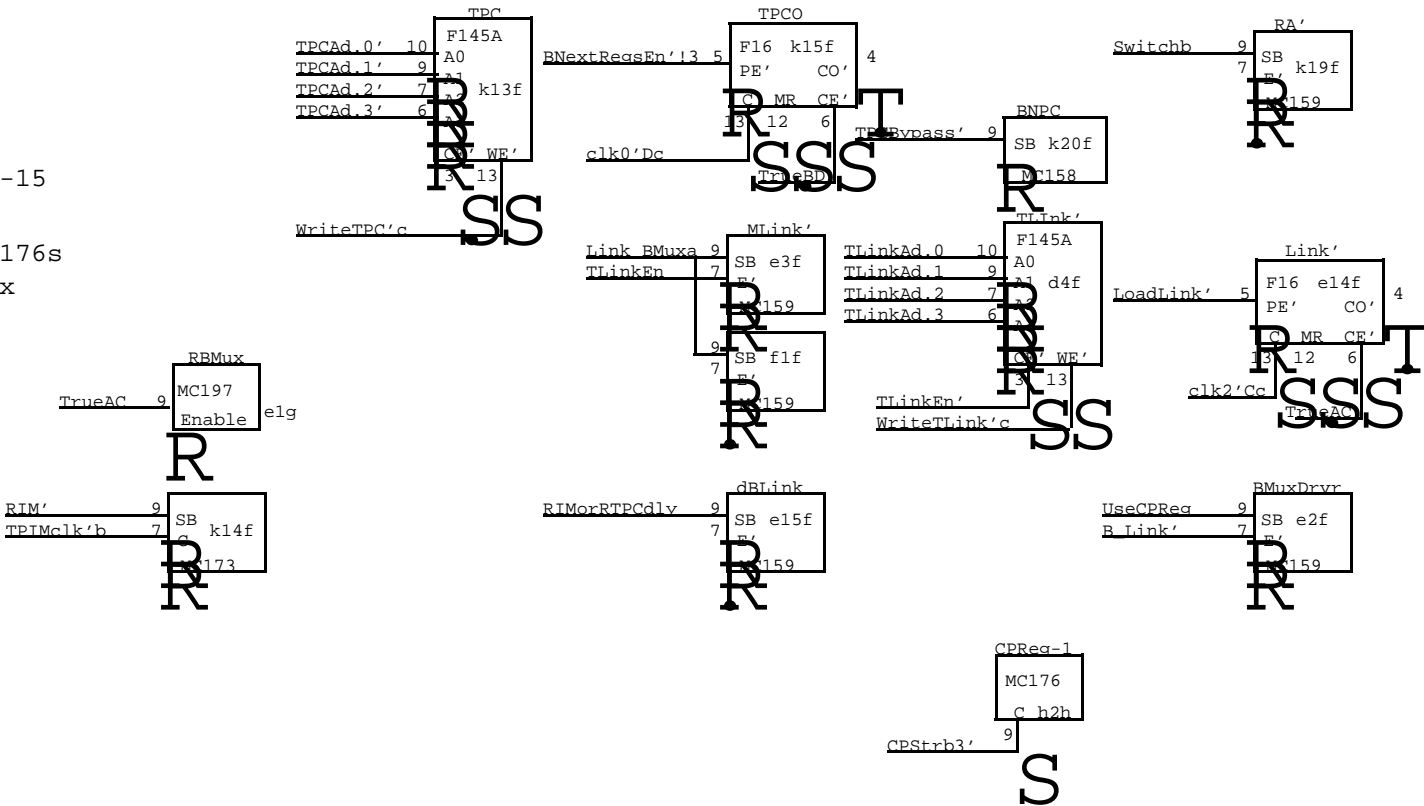
NOTE: number of chips per function  
in upper right corner of control macros

XEROX PARC	Project Dorado	Control Section Data Paths	File ContA20.sil	Designer Pier	Rev Da	Date 7/13/79	Page 20
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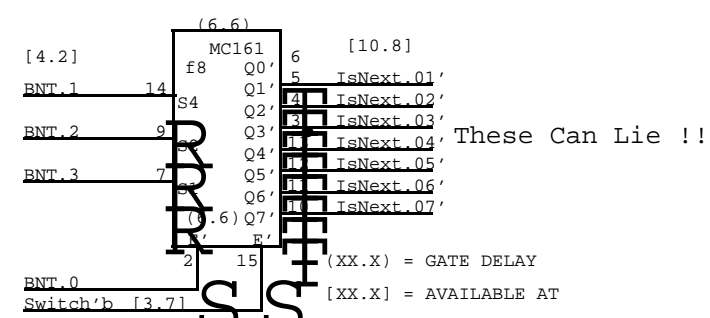
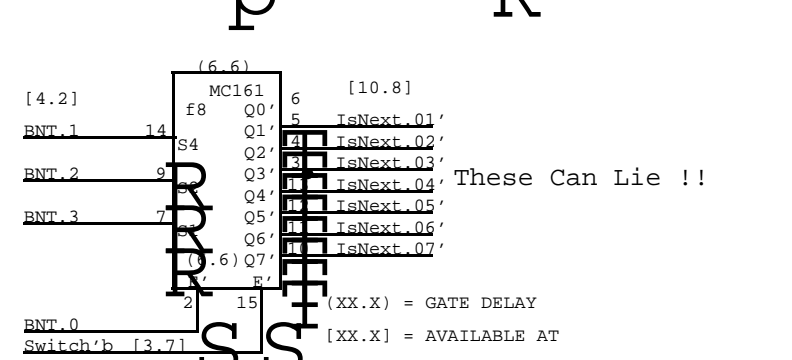
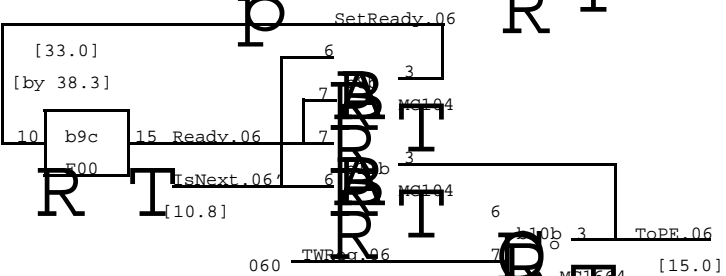
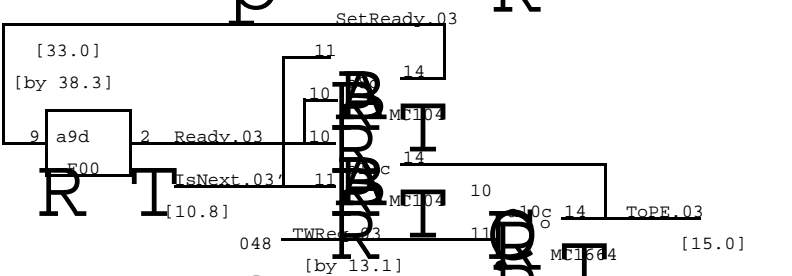
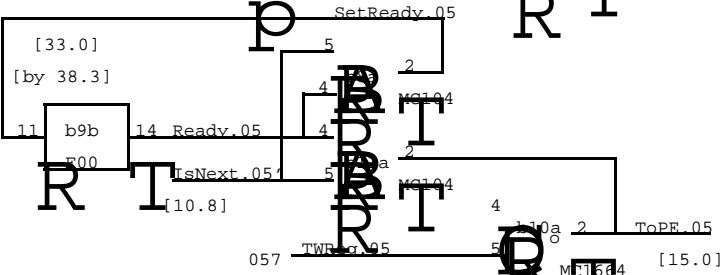
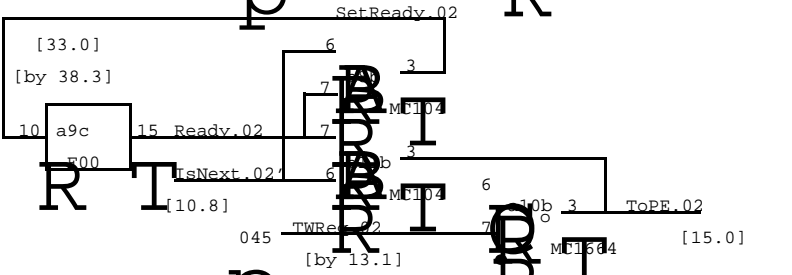
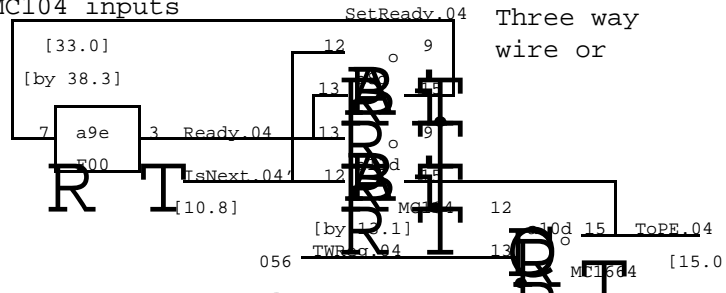
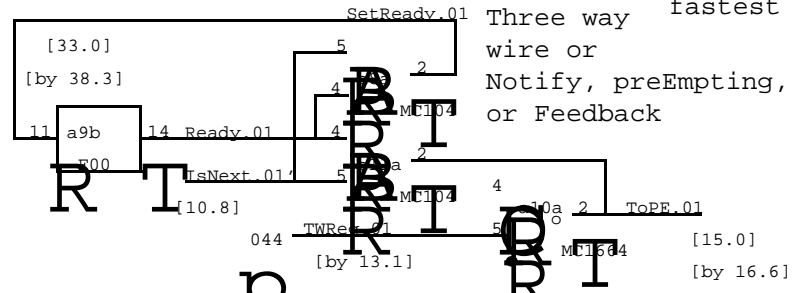
BITS 8-11  
 except 176s  
 and BMux

BITS 12-15  
 except 176s  
 and BMux

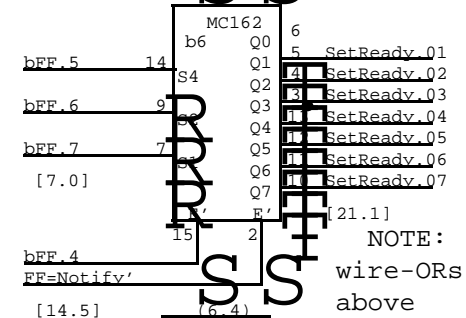


XEROX PARC	Project Dorado	Control Section Data Paths	File ContA21.sil	Designer Pier	Rev Da	Date 7/13/79	Page 21
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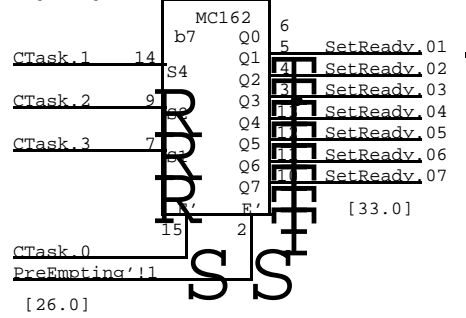
Note: choose IsNext' into fastest MC104 inputs



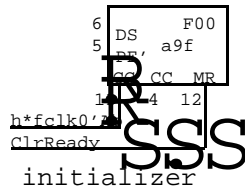
These Can Lie !!



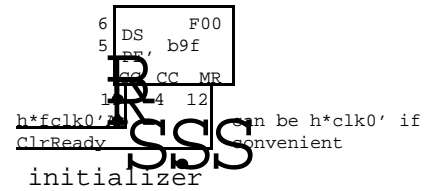
**NOTE !!!**  
Model0 Notify uses inverted FFs. These are uninverted; e.g. FF=361b is Notify[1]



Prevent loading when IsNext lies



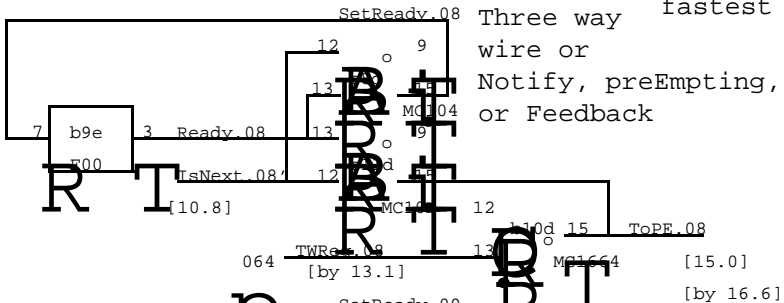
Prevent loading when IsNext lies



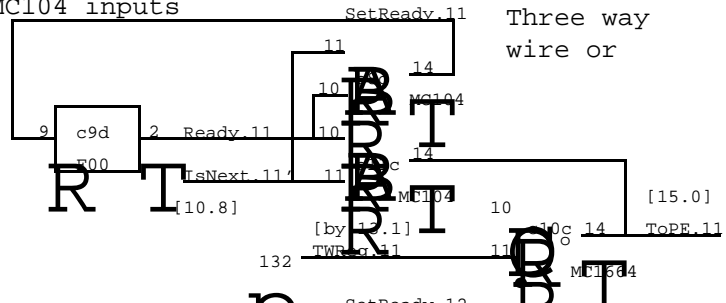
about 11 chips

XEROX PARC	Project Dorado	Ready Logic	File ContA22.sil	Designer Pier	Rev Da	Date 7/13/79	Page 22
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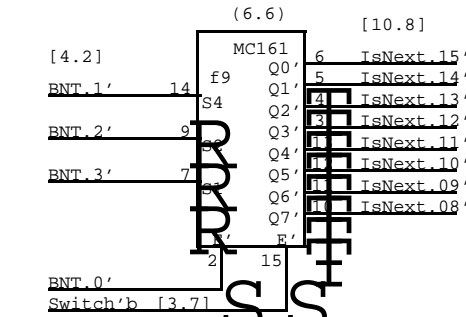
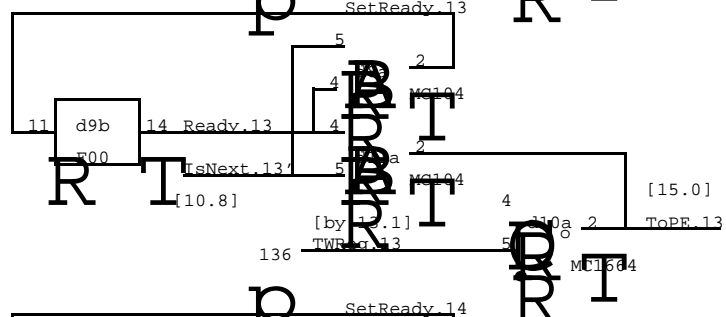
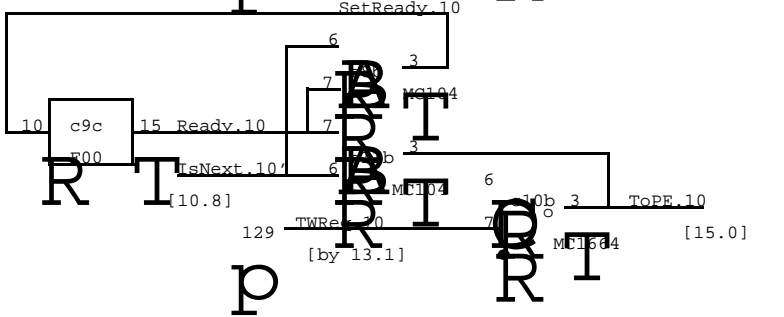
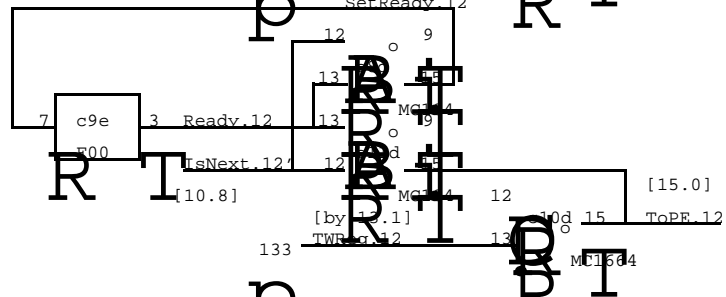
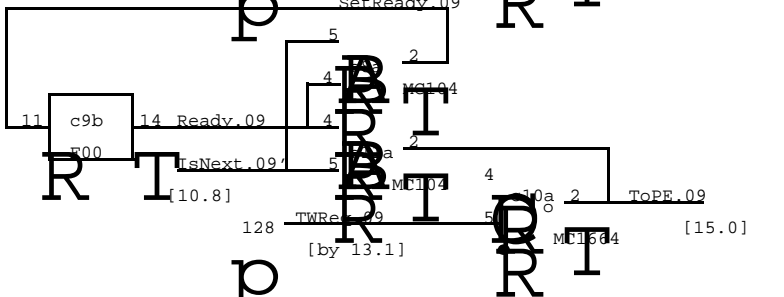
NOTE: choose IsNext' into fastest MC104 inputs



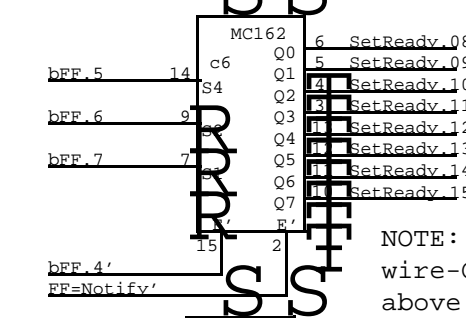
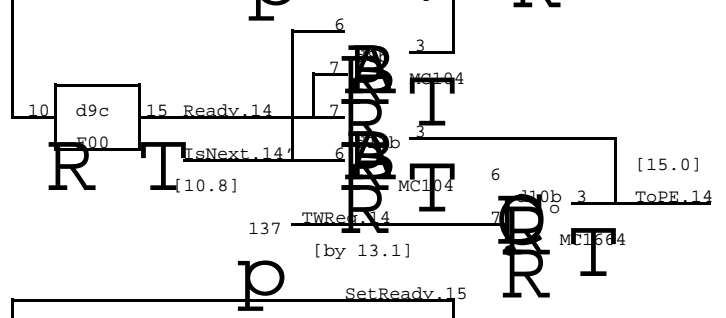
Three way wire or Notify, preEmpting, or Feedback



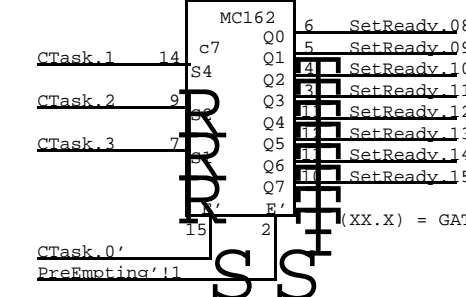
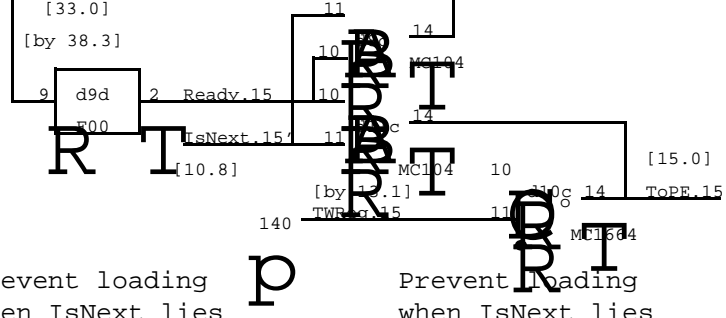
Three way wire or



These Can Lie !!



NOTE !!!  
Model0 Notify uses inverted FFs. These are uninverted, e.g FF=371b is Notify[9]



NOTE: wire-ORs above

Prevent loading when IsNext lies

Prevent loading when IsNext lies



can be h\*clk0' if convenient

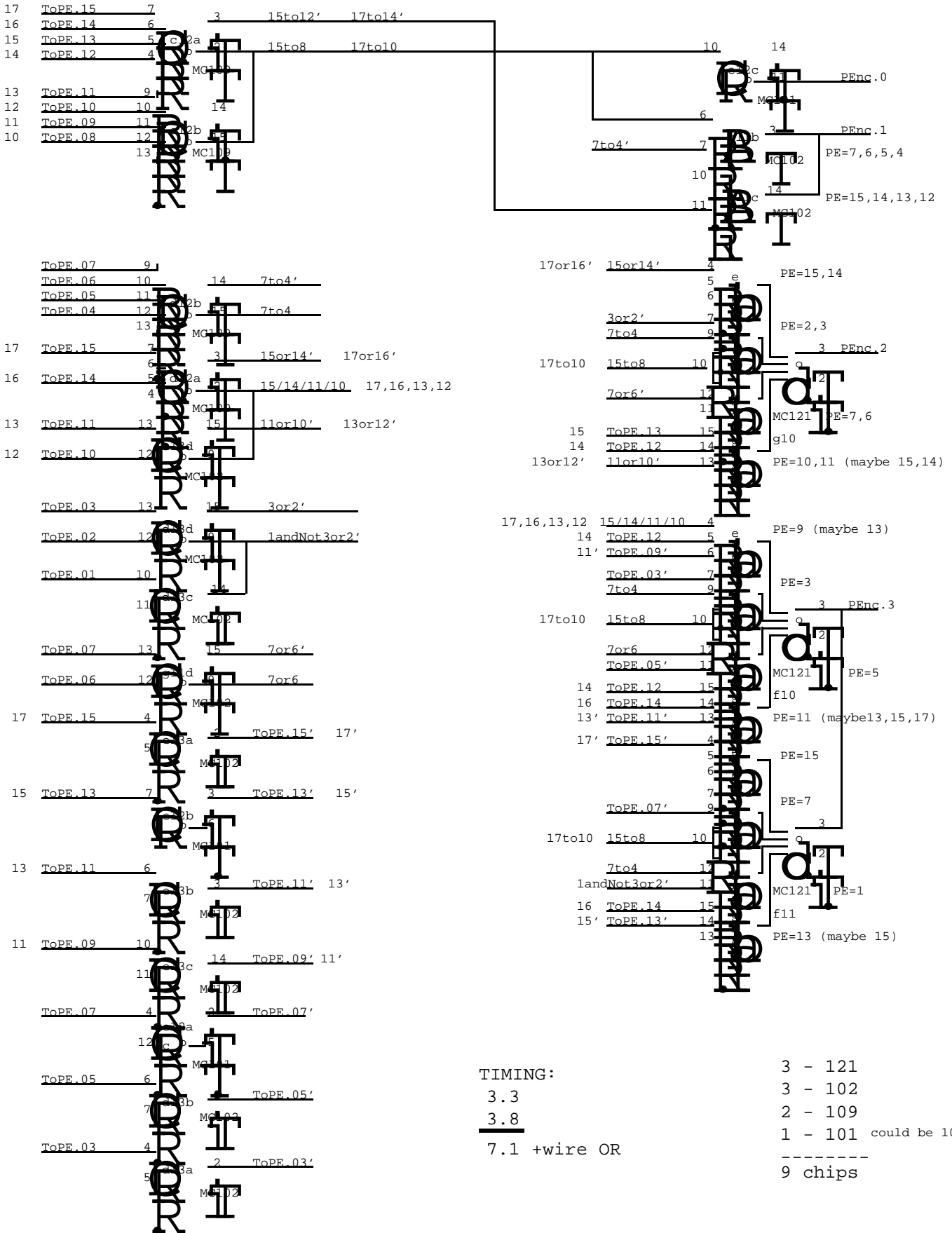
can be h\*clk0' if convenient

about 11 chips

XEROX PARC	Project Dorado	Ready Logic	File ContA23.sil	Designer Pier	Rev Da	Date 7/13/79	Page 23
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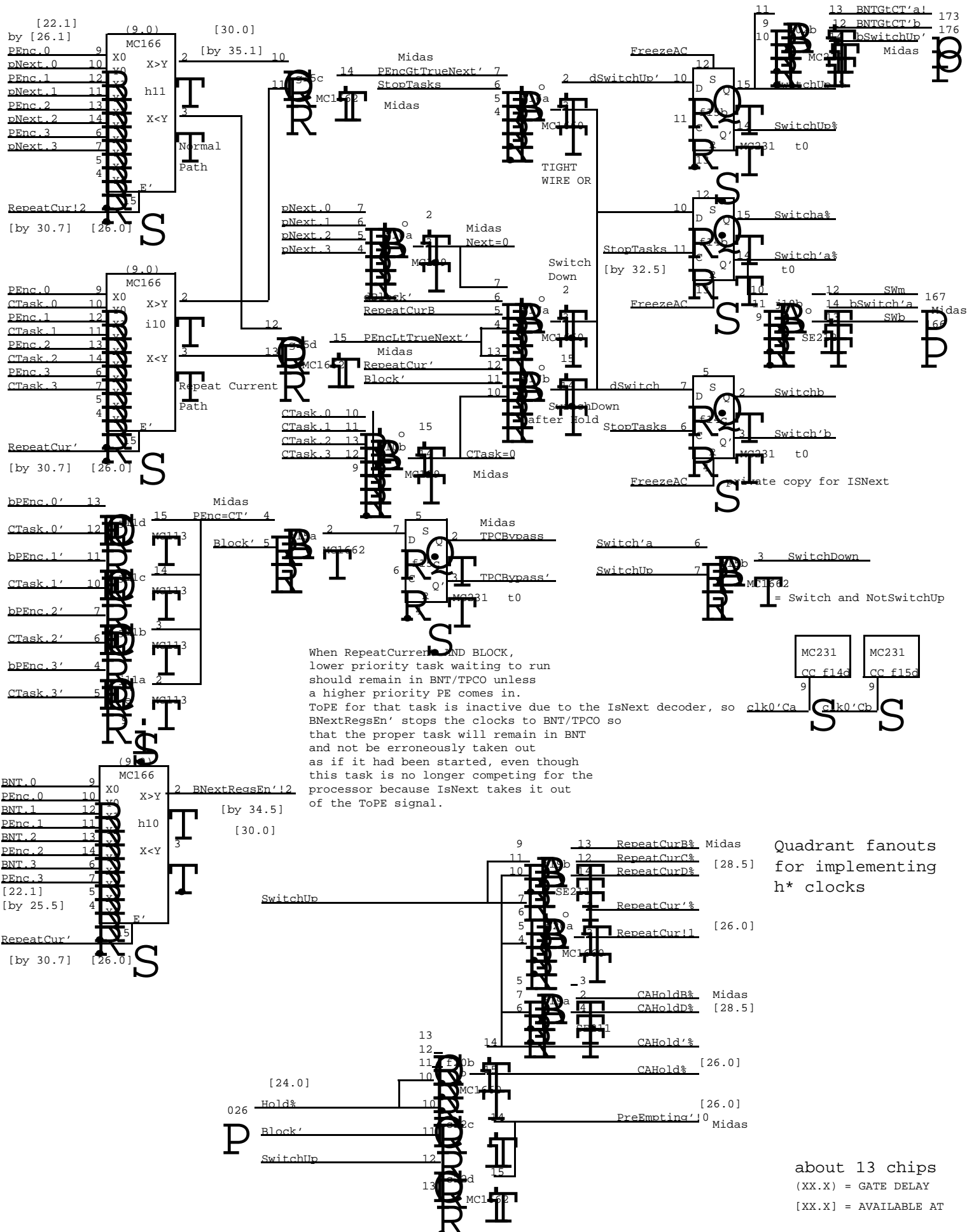
REQUEST NUMBERS  
IN FONT 2 ARE OCTAL



TIMING:

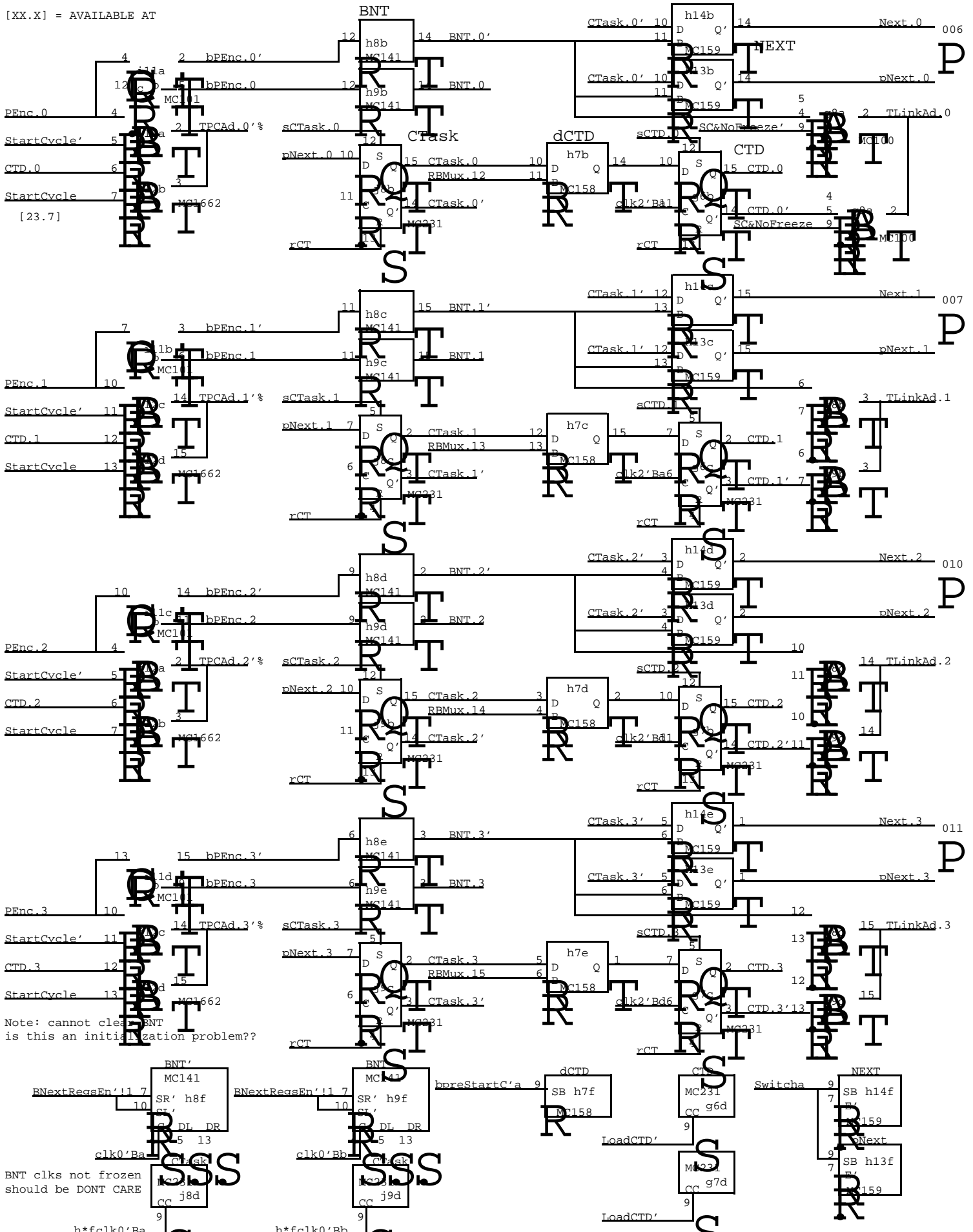
3.3  
3.8  
7.1 +wire OR

3 - 121  
3 - 102  
2 - 109  
1 - 101 could be 102  
-----  
9 chips

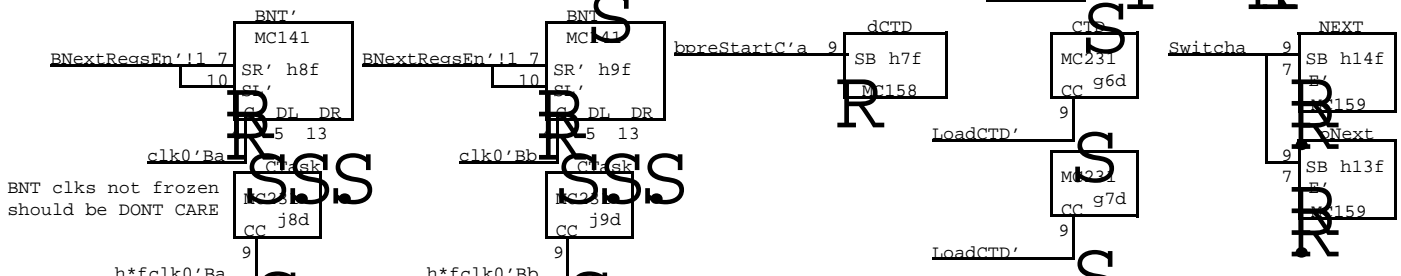


XEROX PARC	Project Dorado	Task Switch Generator	File ContA25.sil	Designer Pier	Rev Da	Date 7/13/79	Page 25
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(XX.X) = GATE DELAY  
 [XX.X] = AVAILABLE AT



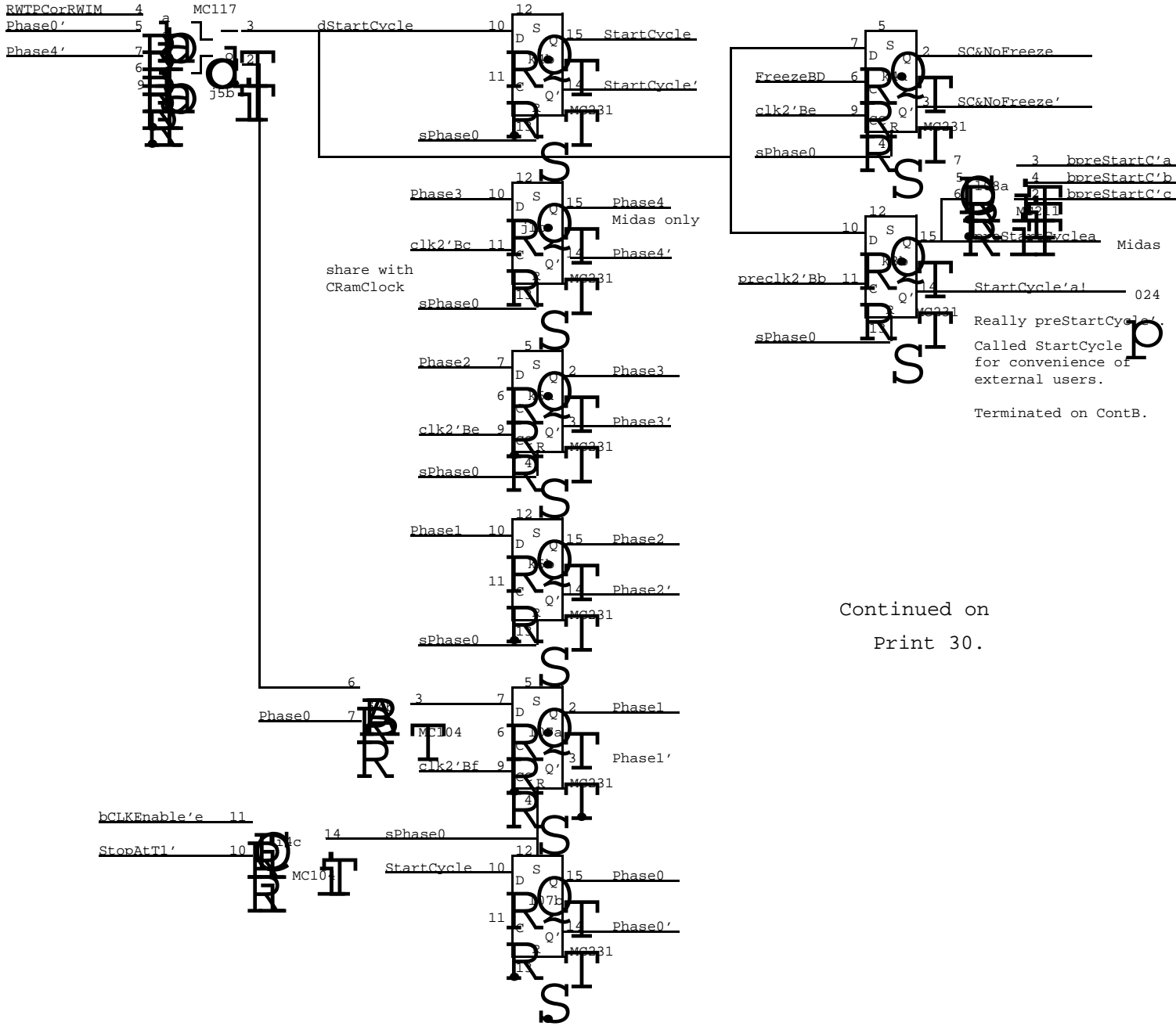
Note: cannot clear BNT  
 is this an initialization problem??



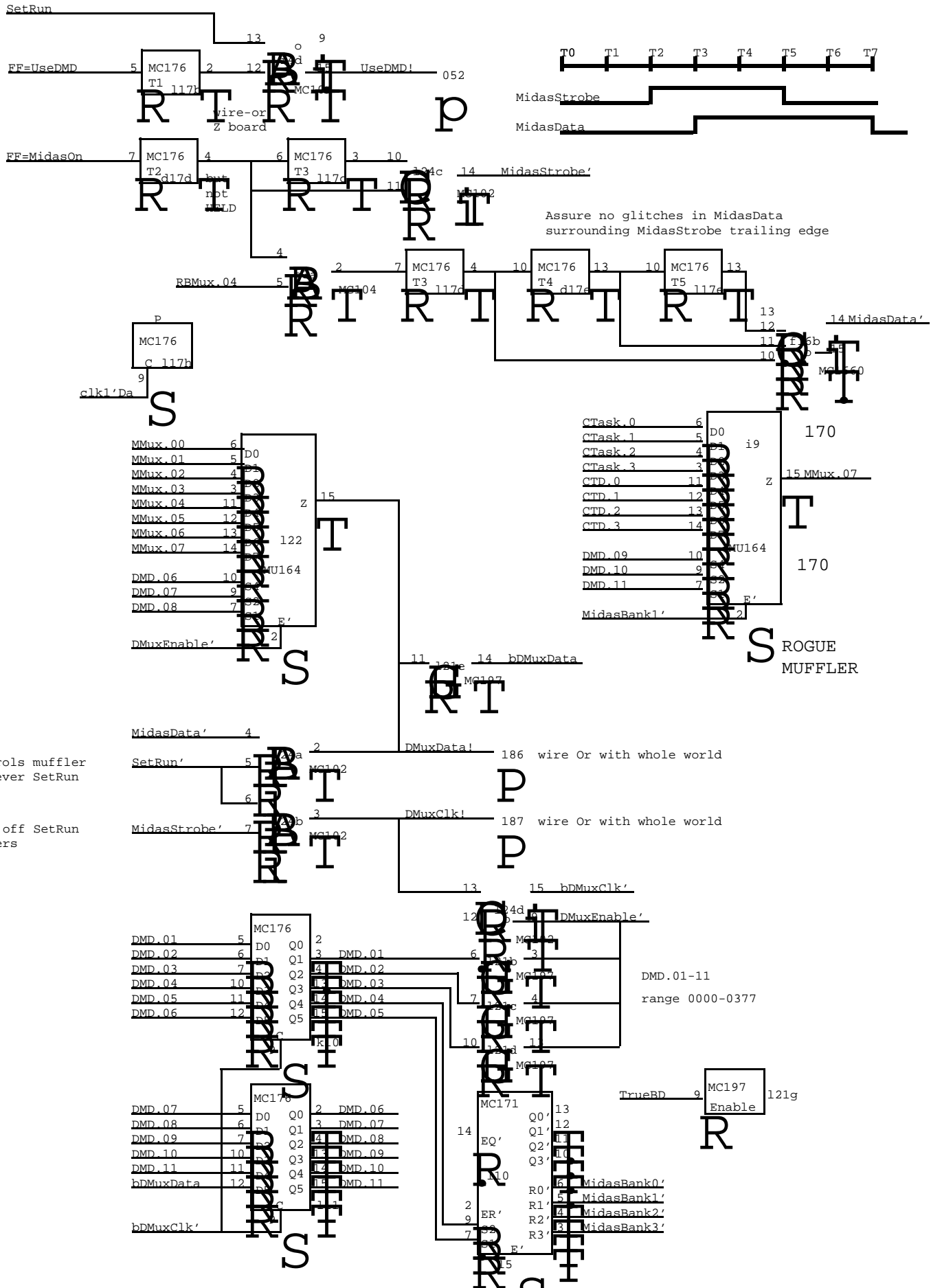
XEROX PARC	Project Dorado	Task Registers: HTask, BNT,CTask,CTD,Next	File ContA26.sil	Designer Pier	Rev Da	Date 7/13/79	Page 26
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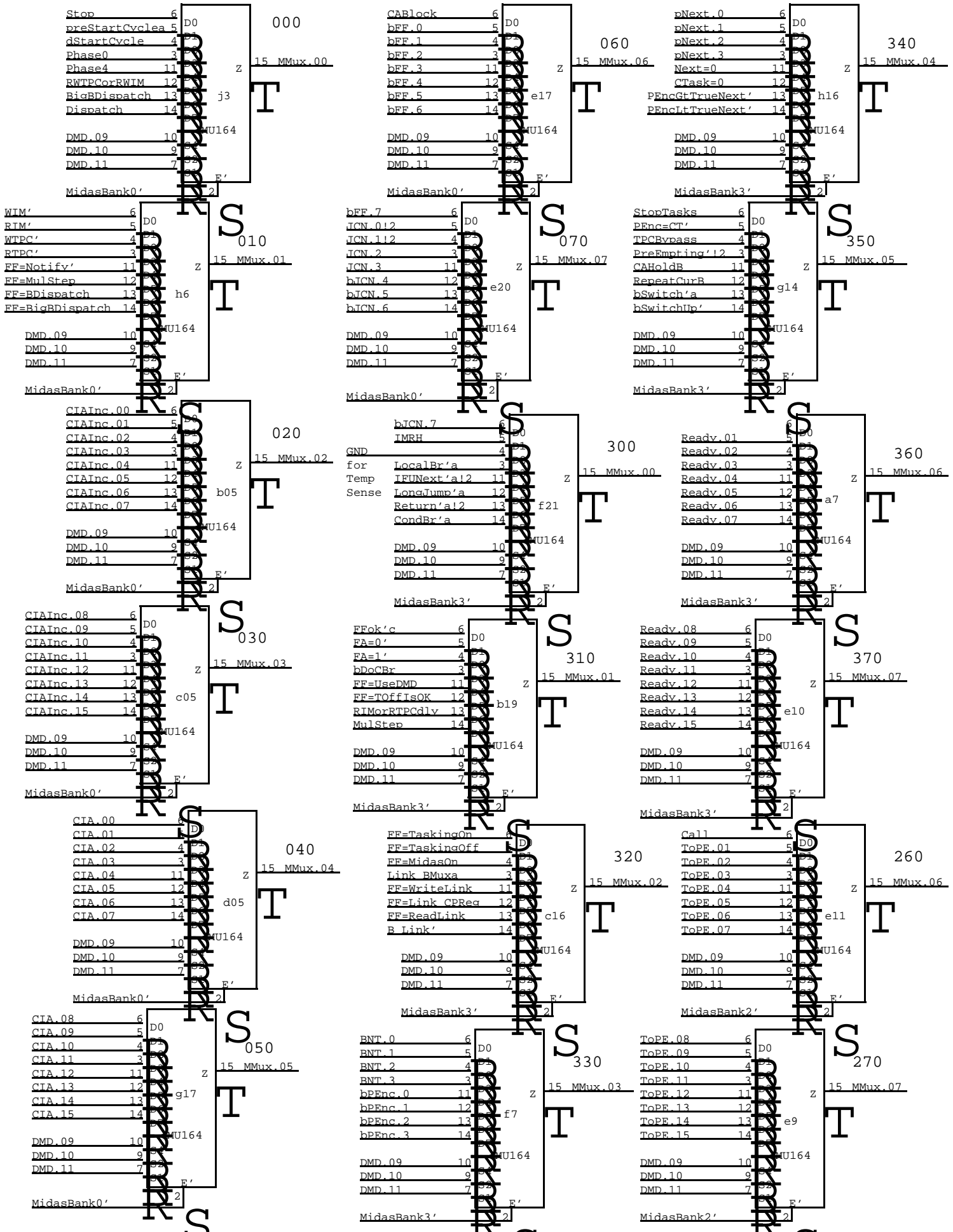
[9.8]

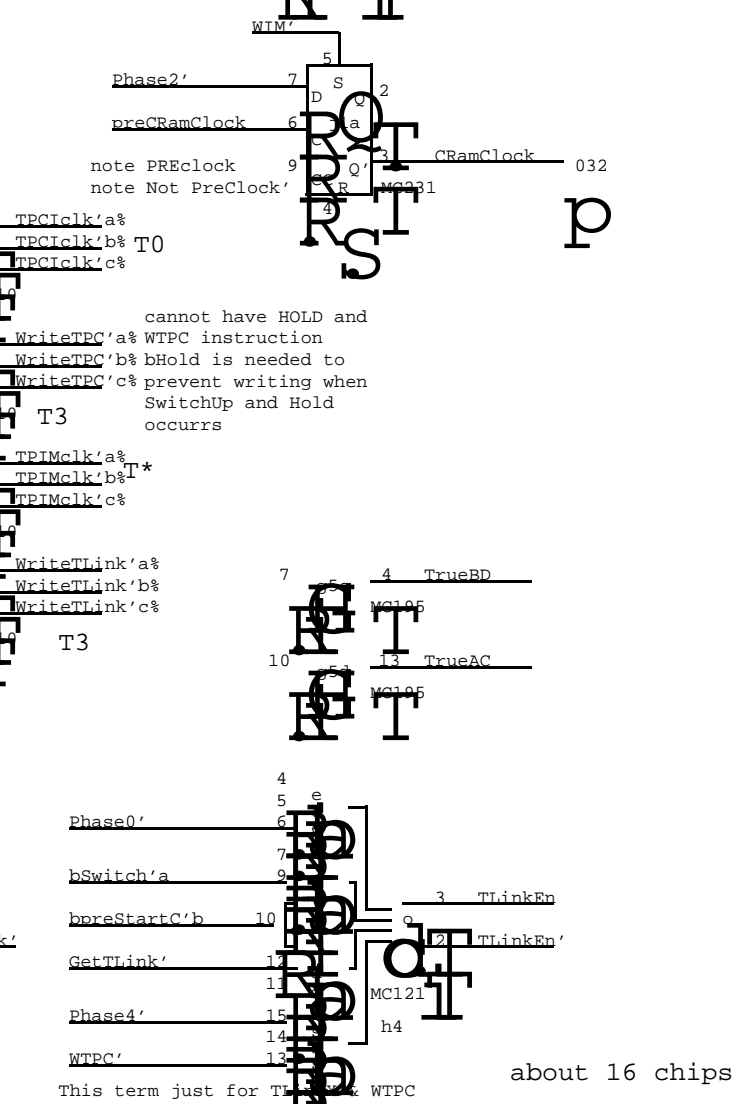
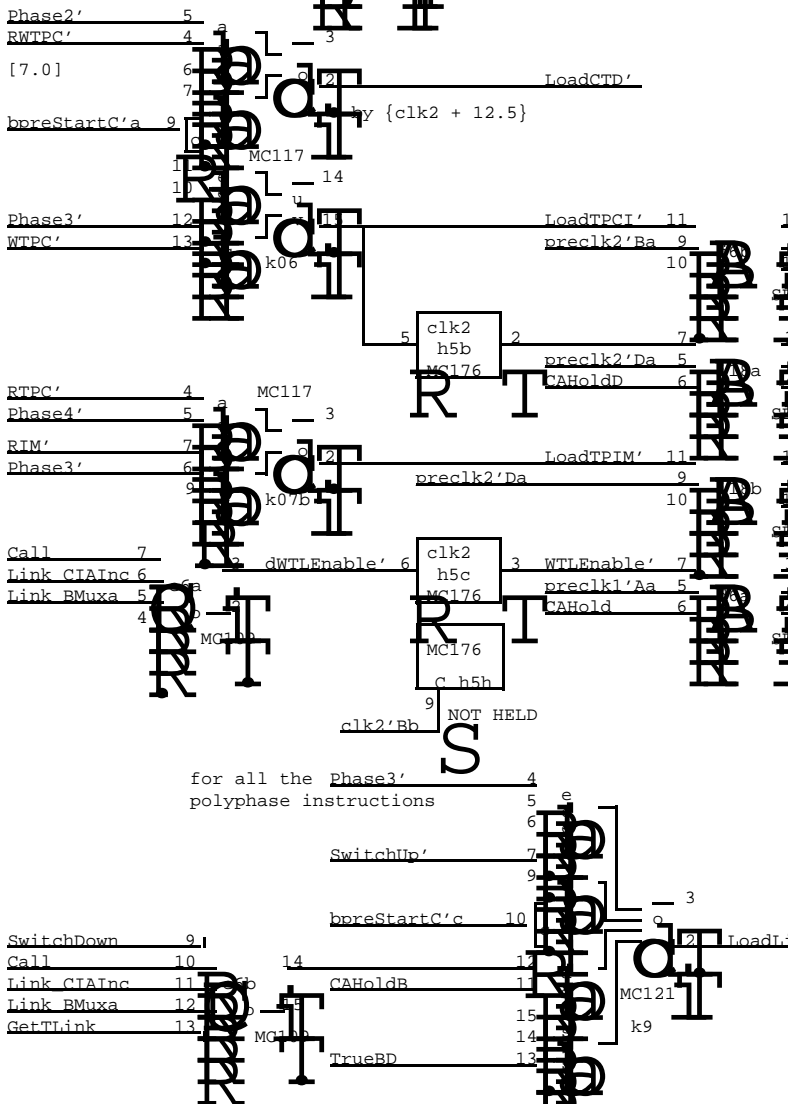
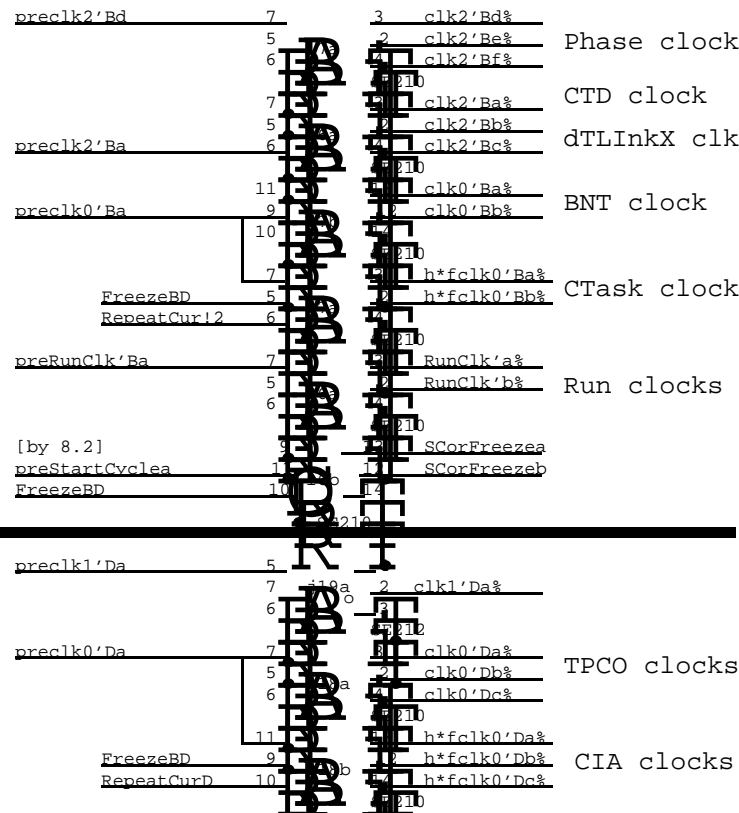
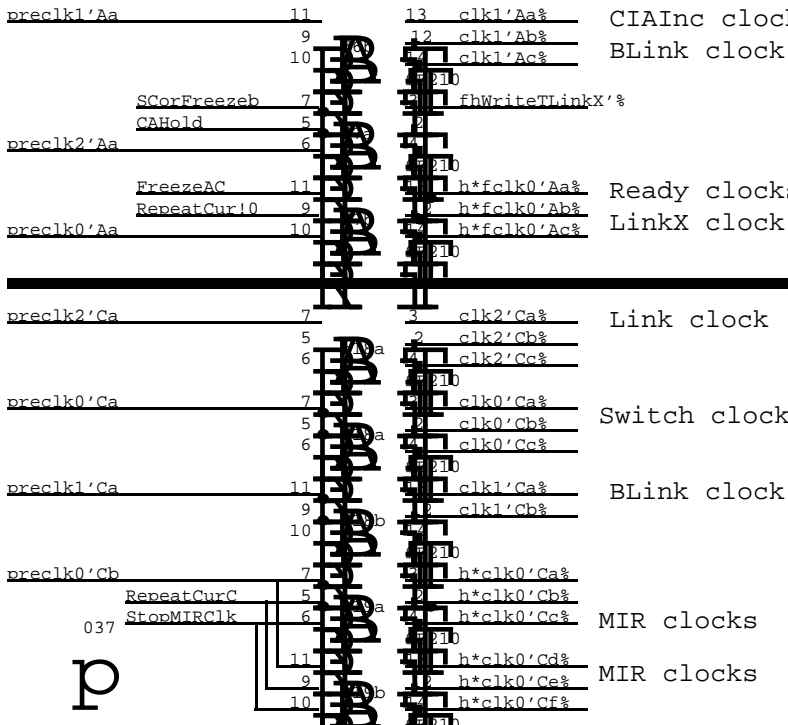
[by 10.9]

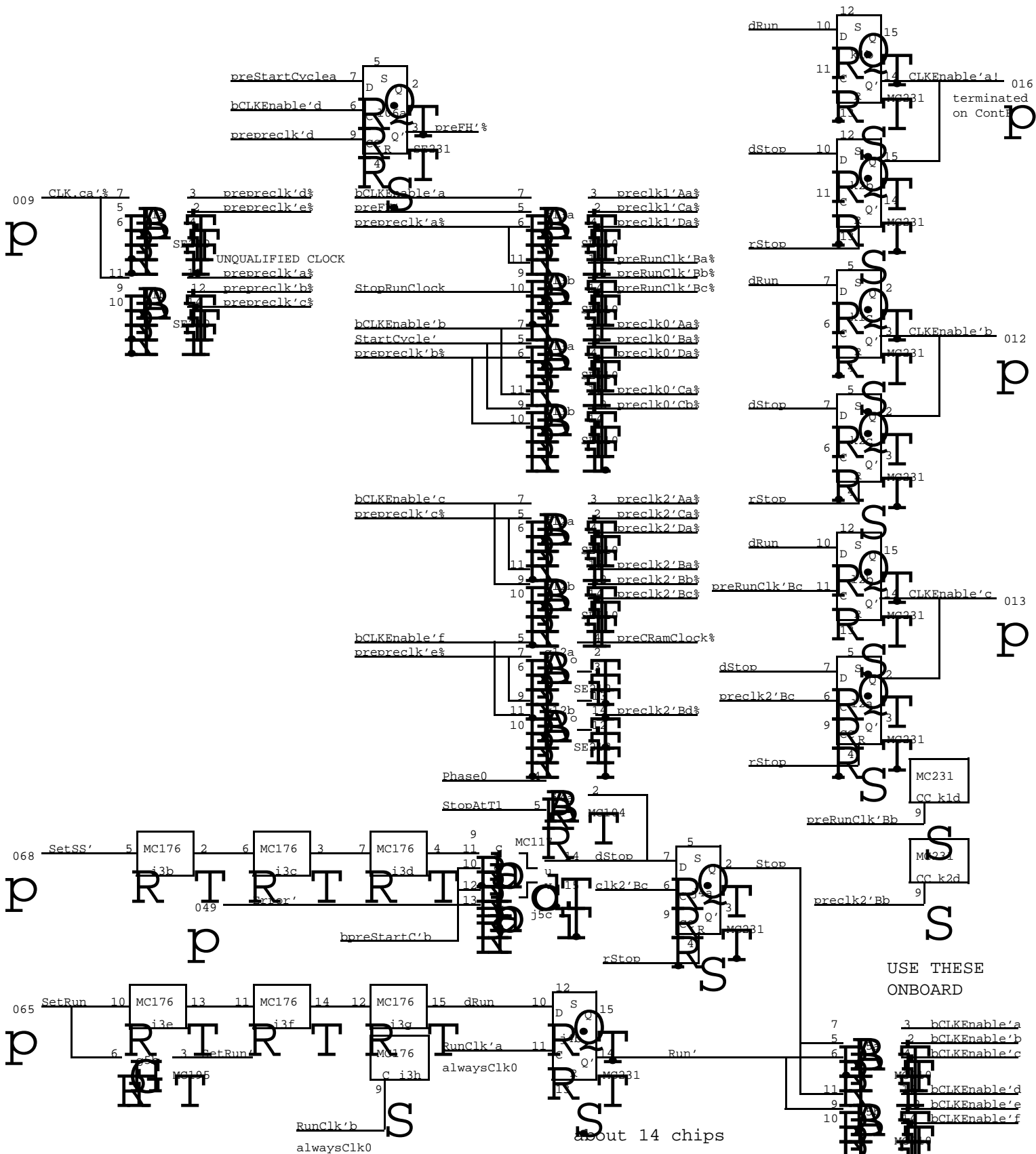


Continued on  
Print 30.



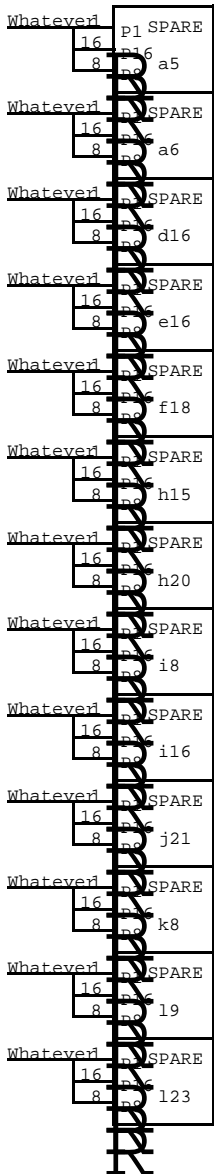
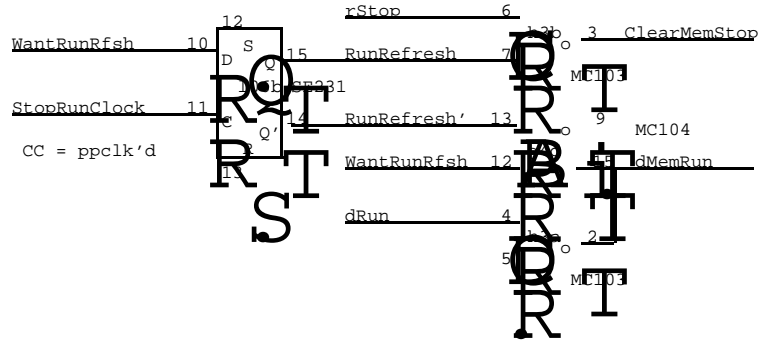
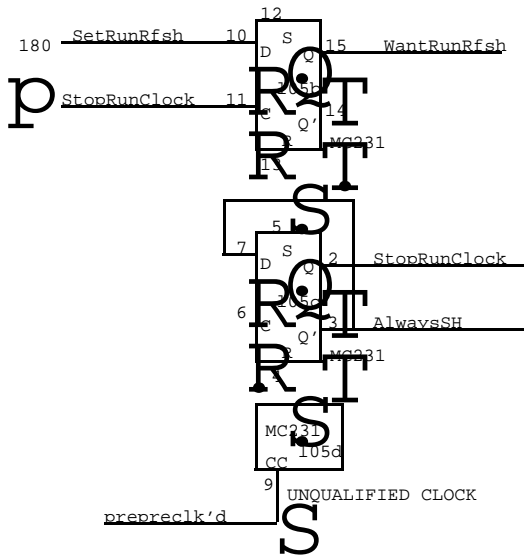




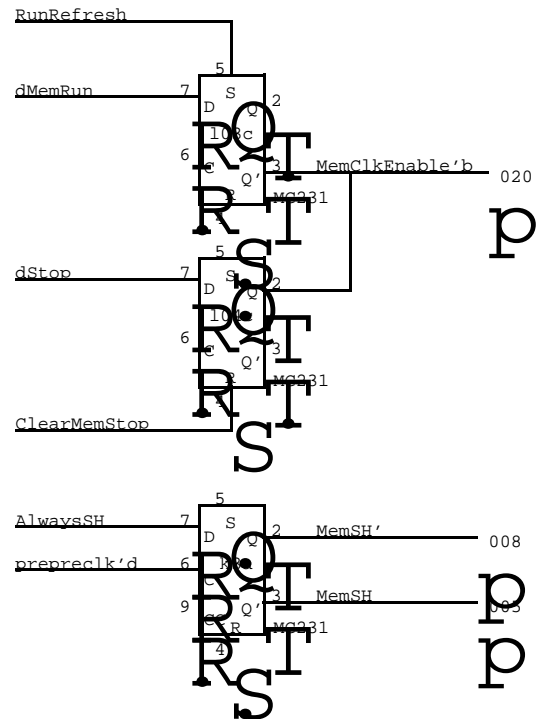
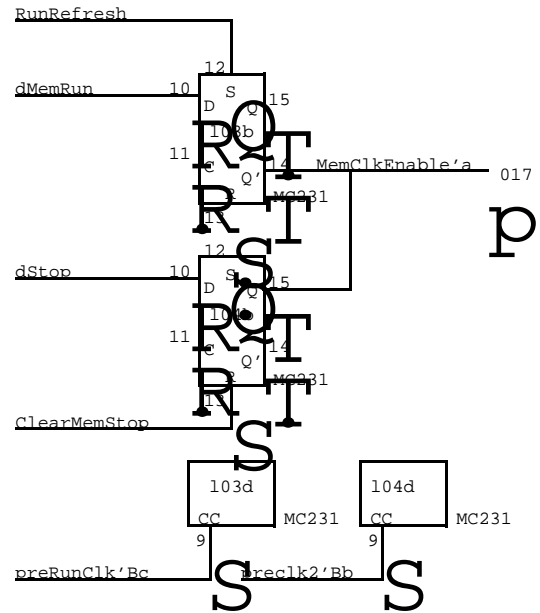


XEROX PARC	Project Dorado	PreClock generator	File ContA31.sil	Designer Pier	Rev Da	Date 7/13/79	Page 31
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MultiWire  
spares



C	IMRHP	BNTGtCT	dCSOut	TWReq9-15	dCSOut	CP INTERFACE	TWReq1-8	RSTK	CLOCK	B													
a	181	b	168	c	153	d	137	e	124	f	109	93	g	80	h	64	i	48	j	33	k	20	l
1	CPStrobe 161 2	dTLINK	dTLINK	dTLINK	RBMux .4, .12-15	dTLINK	SetMIR	SetMIR	SetMIR	CramClk Phase4	CLKEN	RAWClk	1										
2	MIR/BGtCT 2,25	PrMux	PrMux	PrMux	PrMux	CPREG-0	CPREG-1	CPREG-1	CLOCK	CONTROL	CLKEN	CLKEN	2										
3	CPREG-0	TLINK	TLINK	TLINK	TLINK	CPREG-0	CPREG-1	CPREG-1	dStpRun	MU	SCycle 27 MemSH' 30	MEMCLKEN	3										
4	TLINK 145	TLINK	TLINK	TLINK	TLINK	TLINK	TLINK	TLINK	sPh0,d. 31,27,27,28	Stp/run	SC(NF)	MEMCLKEN	4										
5	MU 020	MU 030	MU 040	TLINKX bypass 197 5	LINKX	inverter	CLK2 30,30,,,, 176	bClkEn	Err/dSC	2,3 231 25	RunRfsh	5											
6	NOTIFY 162	CLK	CLK	dWTL 109	LINKX	CTD	MU 010	CLK	CLK	TPCI/CTD	FH	6											
7	MU 360	PREEMPT 162	CLK	CIAInc 76	MU 330	dCTD	clk/Freez 210	CLK	TPCclk CIA 117	0,1 231	7												
8	SETREADY 104	IS	TLINK	BNT	CTASK	bSC 27,B 211	8																
9	READY F00	3*23,D F00	MU 270	NEXT	Addr	MU 170	LoadLink	9															
10	TWREQ 1664	3*23,D 1664	MU 370	PE	BNxtEn	PE>TN	CT=NX=0	DMD 176	MIDAS 171	10													
11	ToPE drivers 104	3*23,4 104	MU 260	PE>TN	bPE	PE=CT	CALL	DMD 176	11														
12	BLINK 176	ToPE rcvrs 109	3*24, d101	PRECLK 210	PRECLK 212	TPCI	TPCAD 1662	TPCI	TPCI	12													
13	4,4,c,4 102	LINK F16	BLINK CIAInc 176	PRECLK 210	PRECLK 210	pNext	TPC	TPC	TPC	13													
14	dBLINK 159	LINK F16	LINK F16	LINK F16	SWUp	MU 350	NEXT	TPIM	TPIM	TPIM	14												
15	5,5,5,4 102	FFBR 162 5	dBLINK 159	dBLINK 159	dSwup	STKSEL 231 1,C	MU 340	CIA'	CIA'	CIA'	15												
16	4,4,5,4 100 4	MU 320	dSwdwn 1660	MU 050	CIA ADDER 105	109	CIA	clk1 4*28,4,g 176	16														
17	bFF 212 1	CLK	CLK	IMRH	RA	CIA	CLK	CLK	CIA	bTNIA	17												
18	FB= 161 4	MU 310	CLK	JBr	IMRH	Hold	bJCN	RA	TNIA 0-3	CLK/SW	RA	18											
19	bFF 109 4	DoCBr 121 5	RW... 161 3	MU 070	RptCur 1660	bJCN	BNPC	bTNIA	BNPC	BNPC	20												
20	FC= 102 4	DoCBr 121 5	3,3,5,3 102	RETURN 210 3	MU 300	BNPC	bTNIA	bTNIA	Midas 4*28 fh 197	21													
21	bFF 212 1	bFF 212 1	DoCBr 5 PreEmp 1662	LocalBr 210 3,5	IFUNext 210 3	CBR/LJ 210 3	TNIA	8	TNIA	13	Midas 164	22											
22	FF2,3 231 1	FF6,7 231 1	JCN0,1 231 1	JCN2or3 231 1	IMRH, BLK 231 1	CBR	6	7	9 TNIA	12	14	23											
23	FF0,1 231 1	FF4,5 231 1	JCN4,5 231 1	JCN2,3 231 1	JCN6,7 231 1	FFok 211 3	4	5	10	11	15	Midas 102	24										

C a 11 b 26 c 39 d 55 e 70 f 86 g 99 h 114 i 129 j 143 k 159 l 174 D  
E NEXT BLOCK HOLD/ FFOK dMIR FF0-3 dMIR BrCond FF4-7 TNIA0-7 BNPC0-2 IFADR TNIA/BNPC BrCond SW DMUX