D O R A D O S C H E M A T I C S

C o n t r o l A

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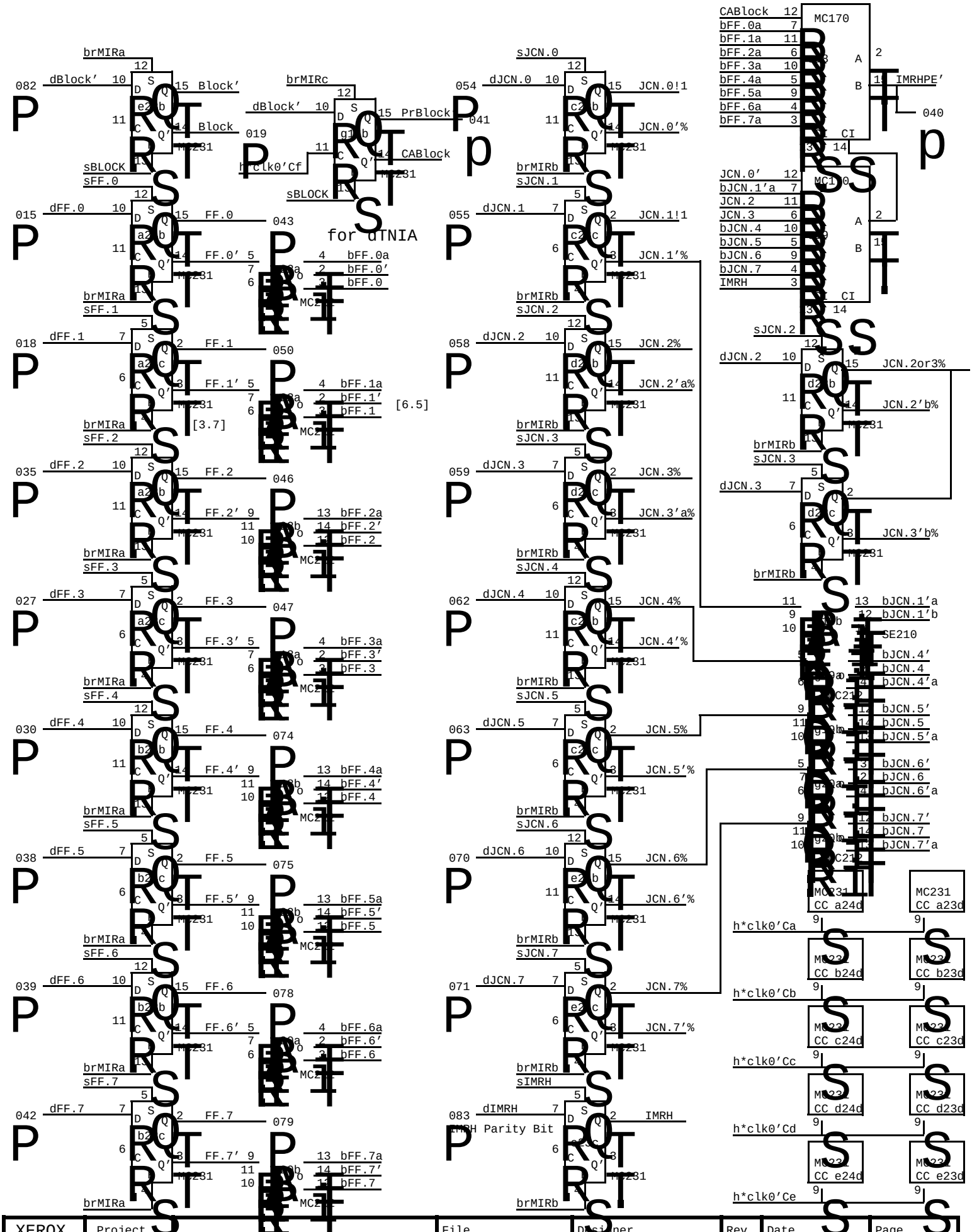
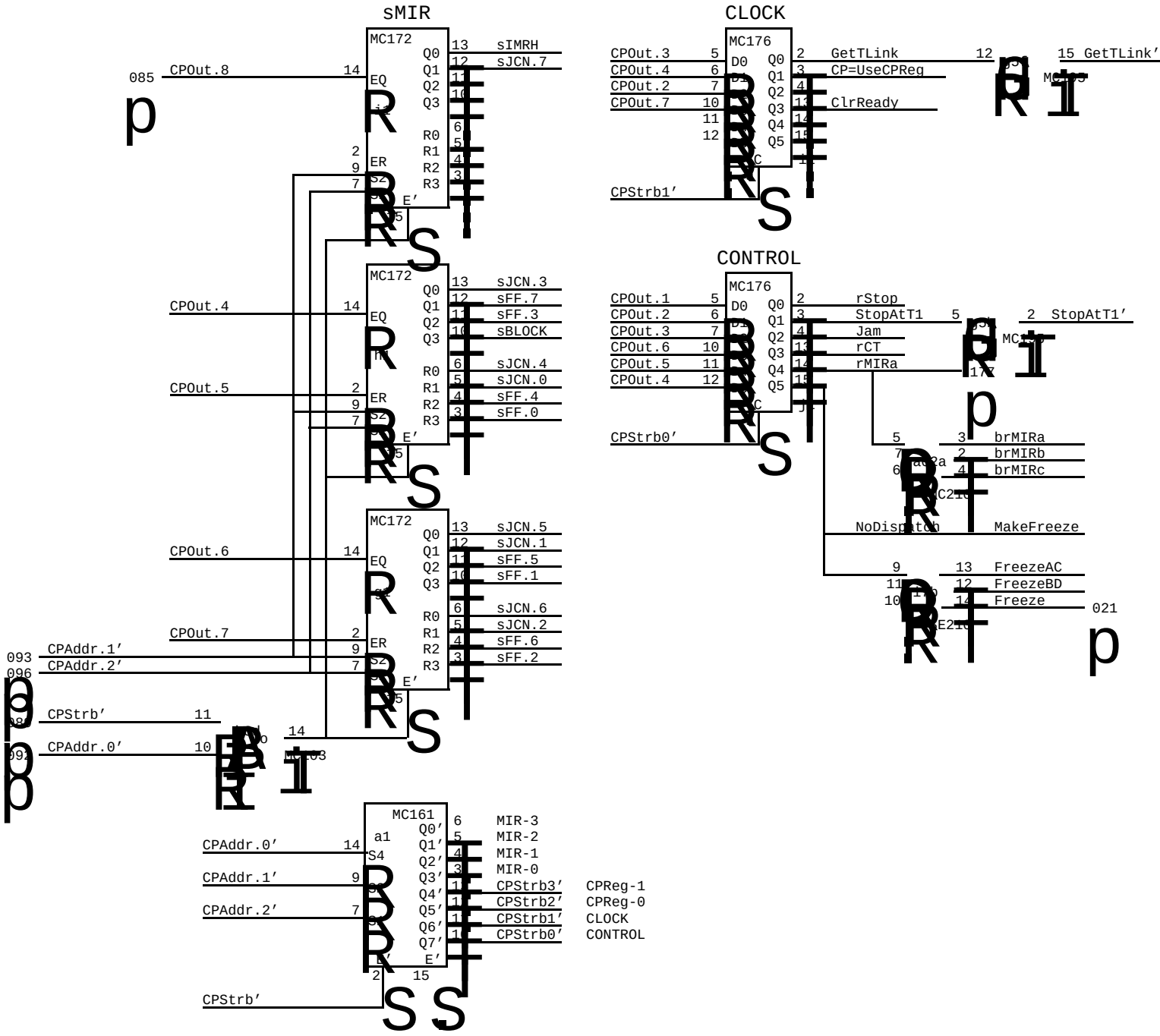
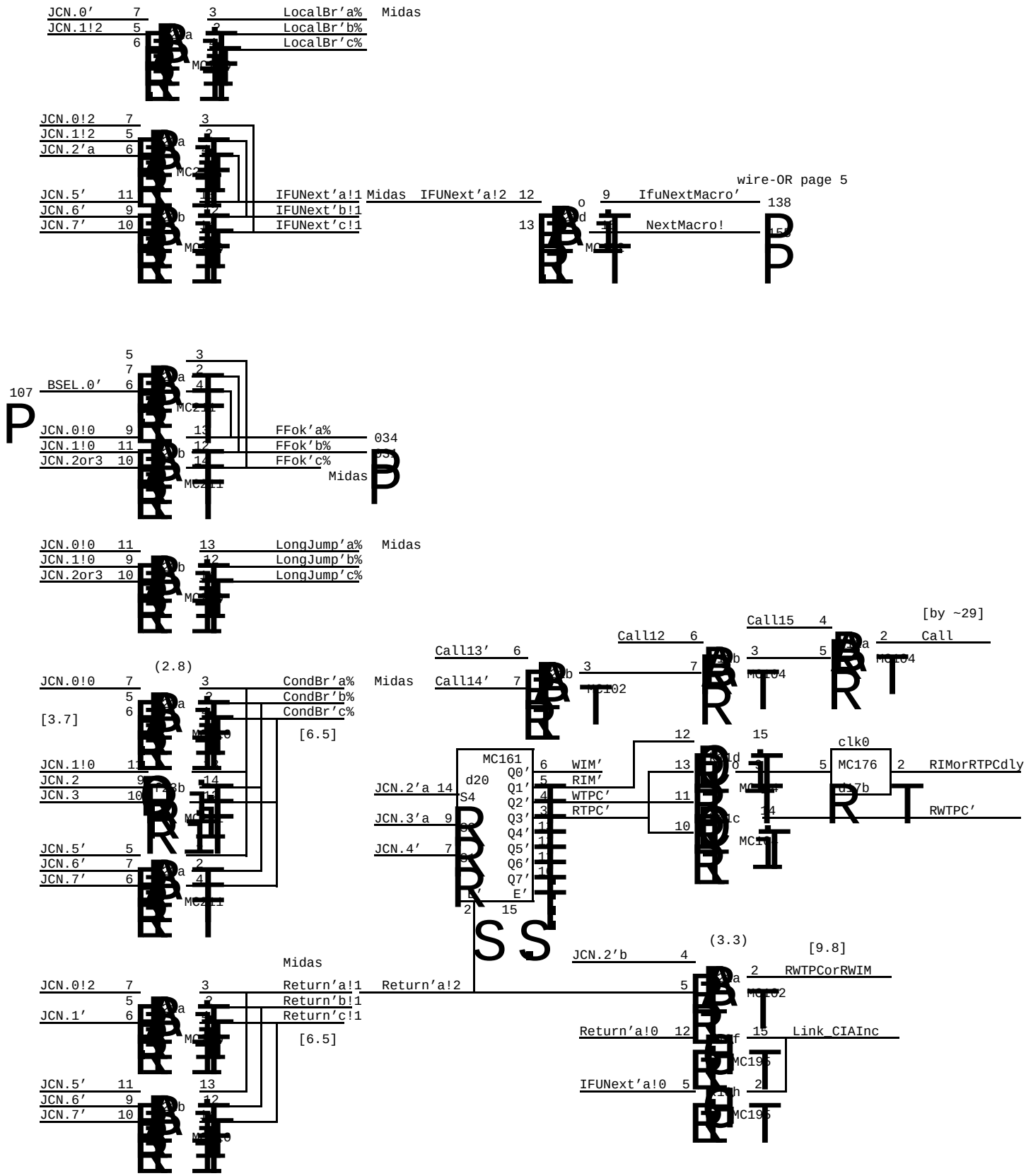


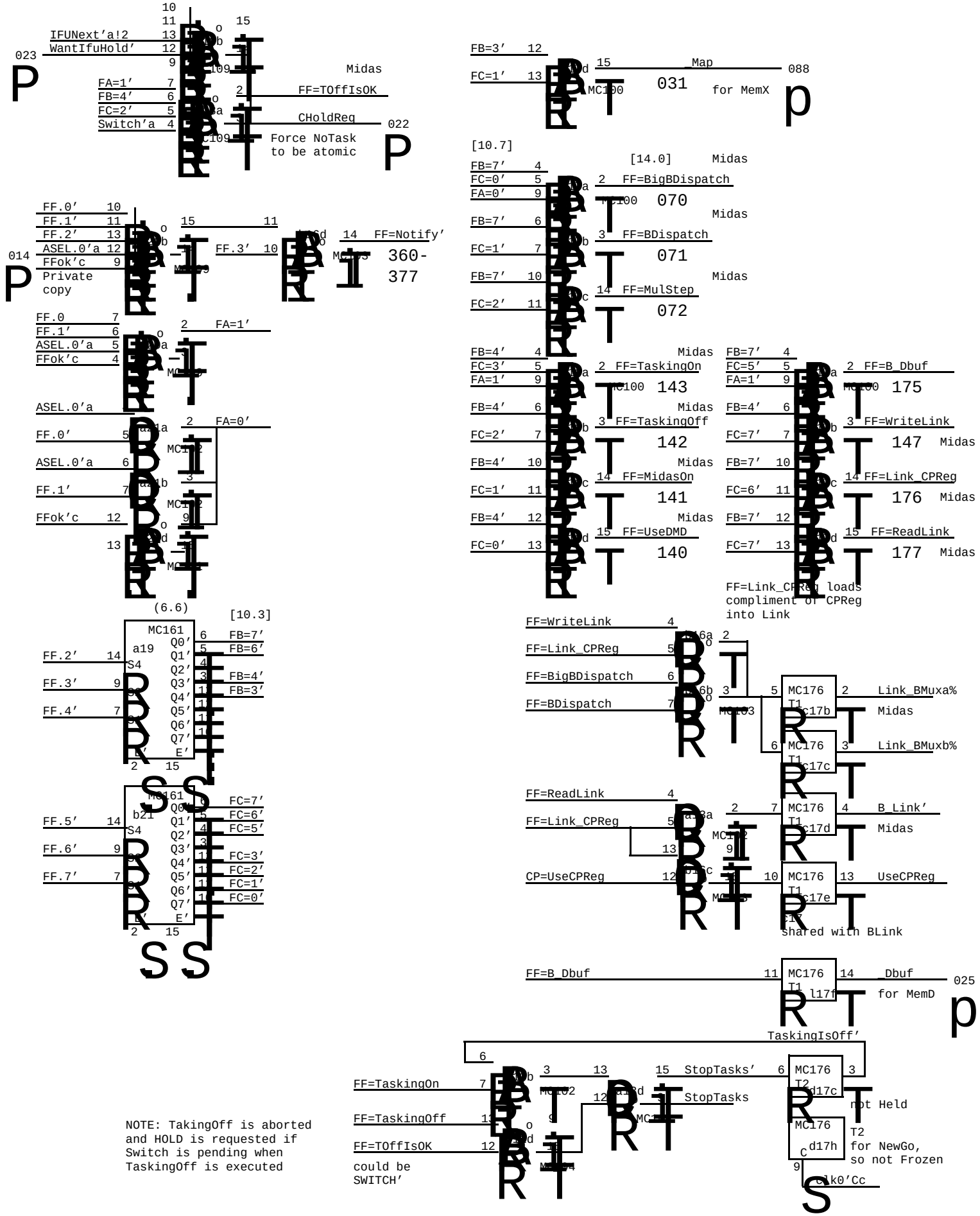
XEROX PARC	Project Dorado	MIR - Right Half	File ContA01.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 01



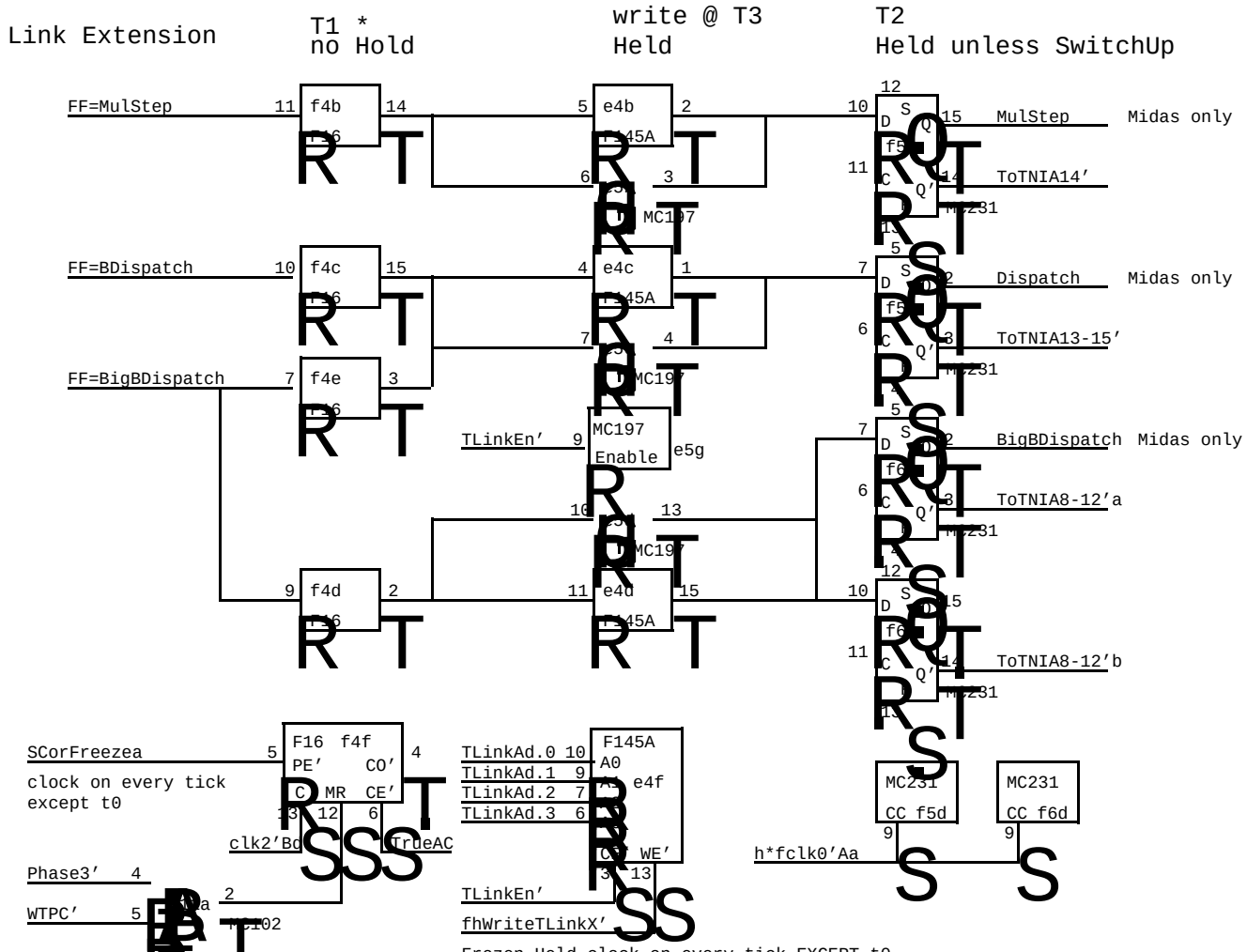
XEROX PARC	Project: Dorado	CP Interface and Set MIR	File: ContA02.sil	Designer: Pier	Rev: Cd	Date: 7/13/79	Page: 02

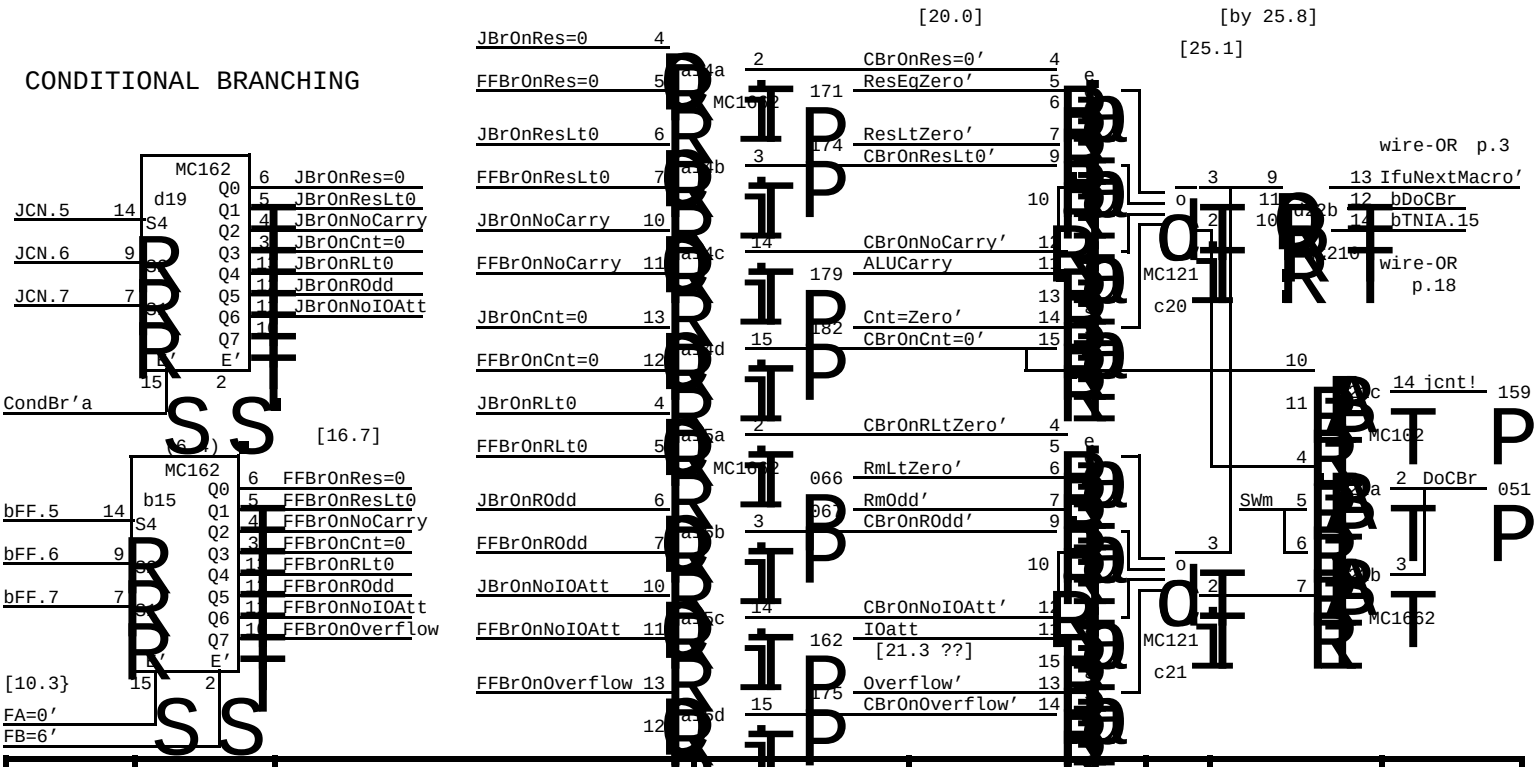


XEROX PARC	Project Dorado	JCN Decoding	File ContA03.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 03

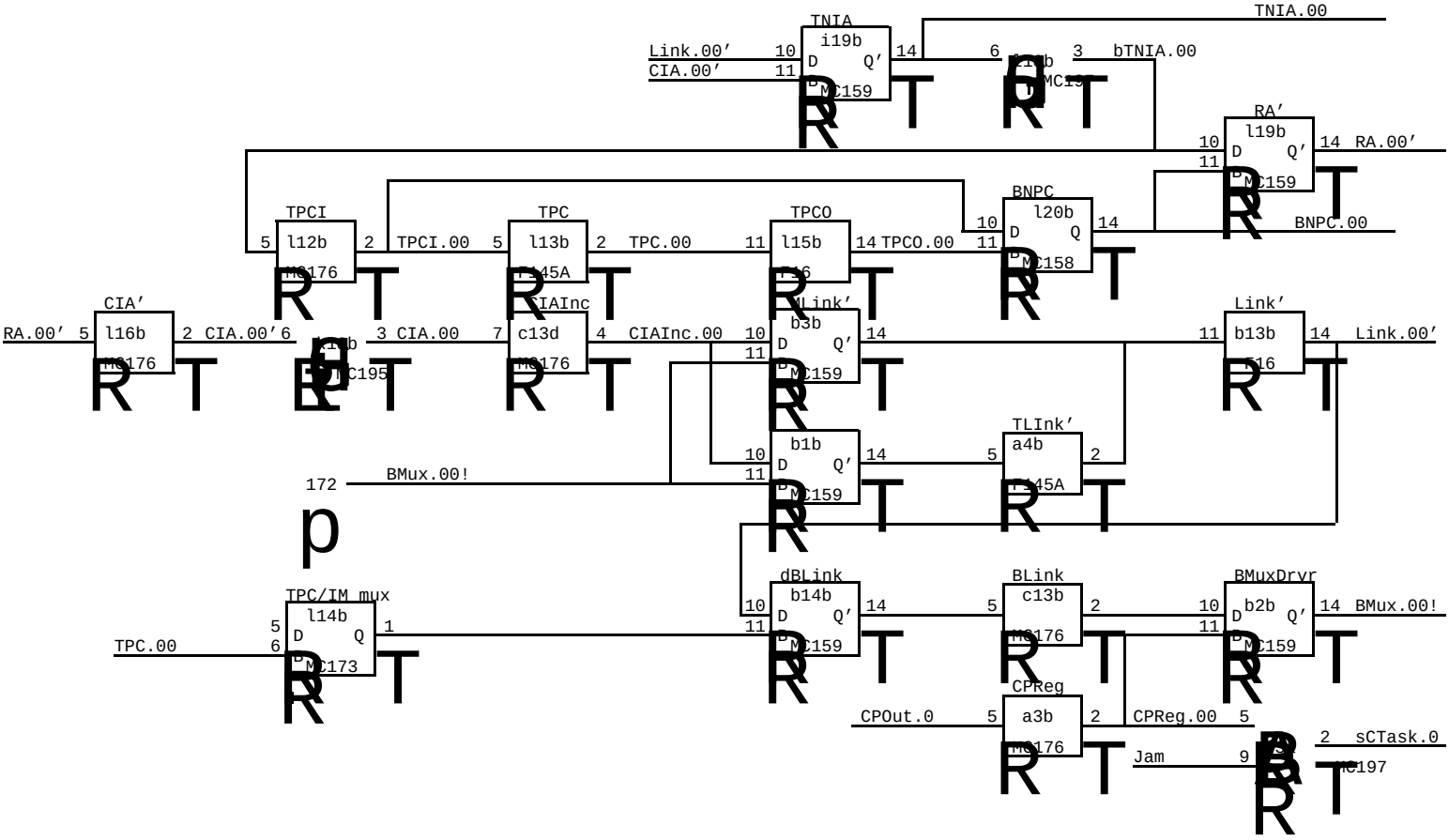


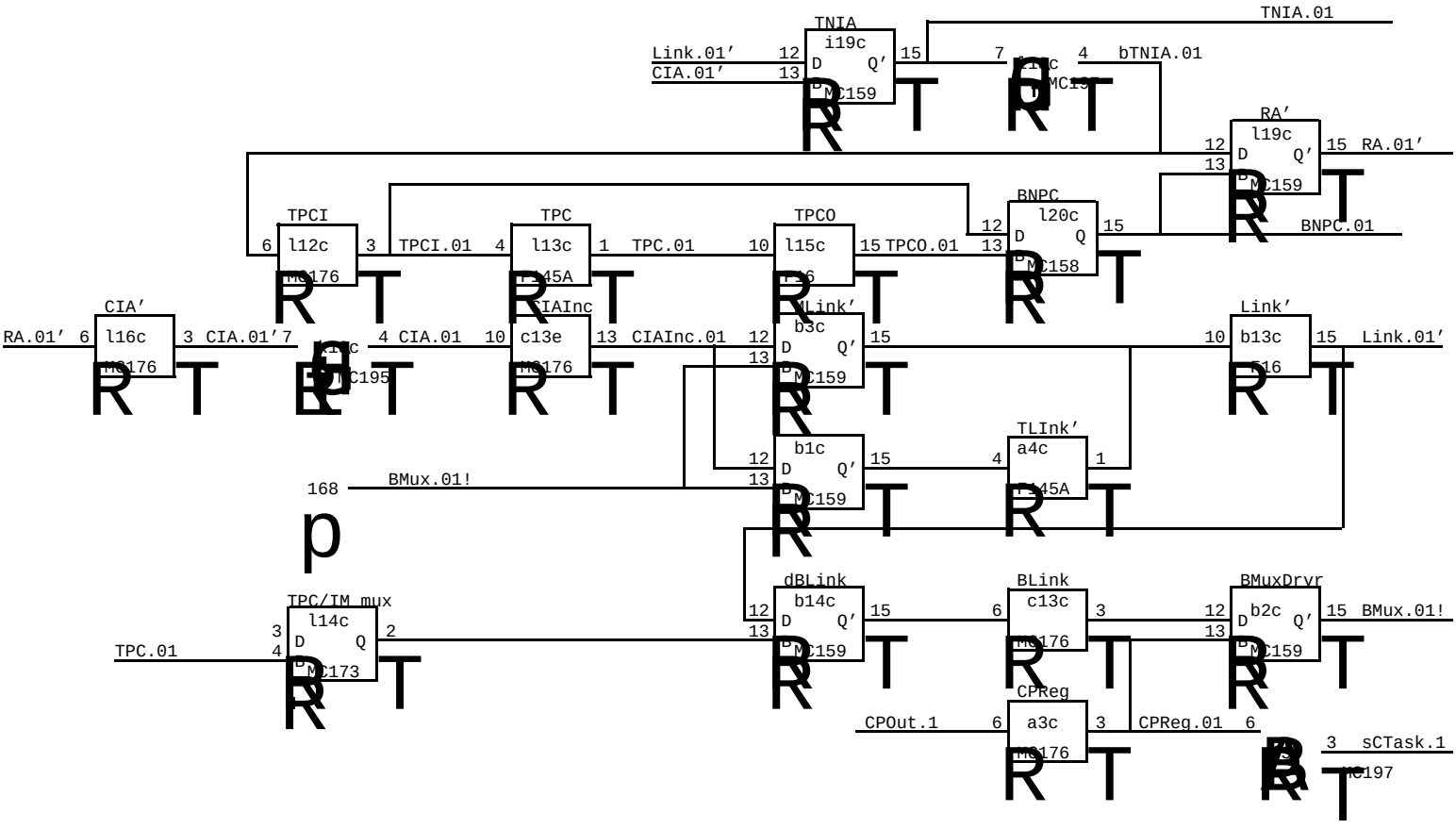
XEROX PARC	Project Dorado	Dorado Control FF DECODING LOGIC	File ContA04.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 04





XEROX PARC	Project Dorado	Link Extension Register Conditional Branch Logic	File ContA05.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 05





XEROX PARC	Project	Control Section Data Paths	File	Designer	Rev	Date	Page
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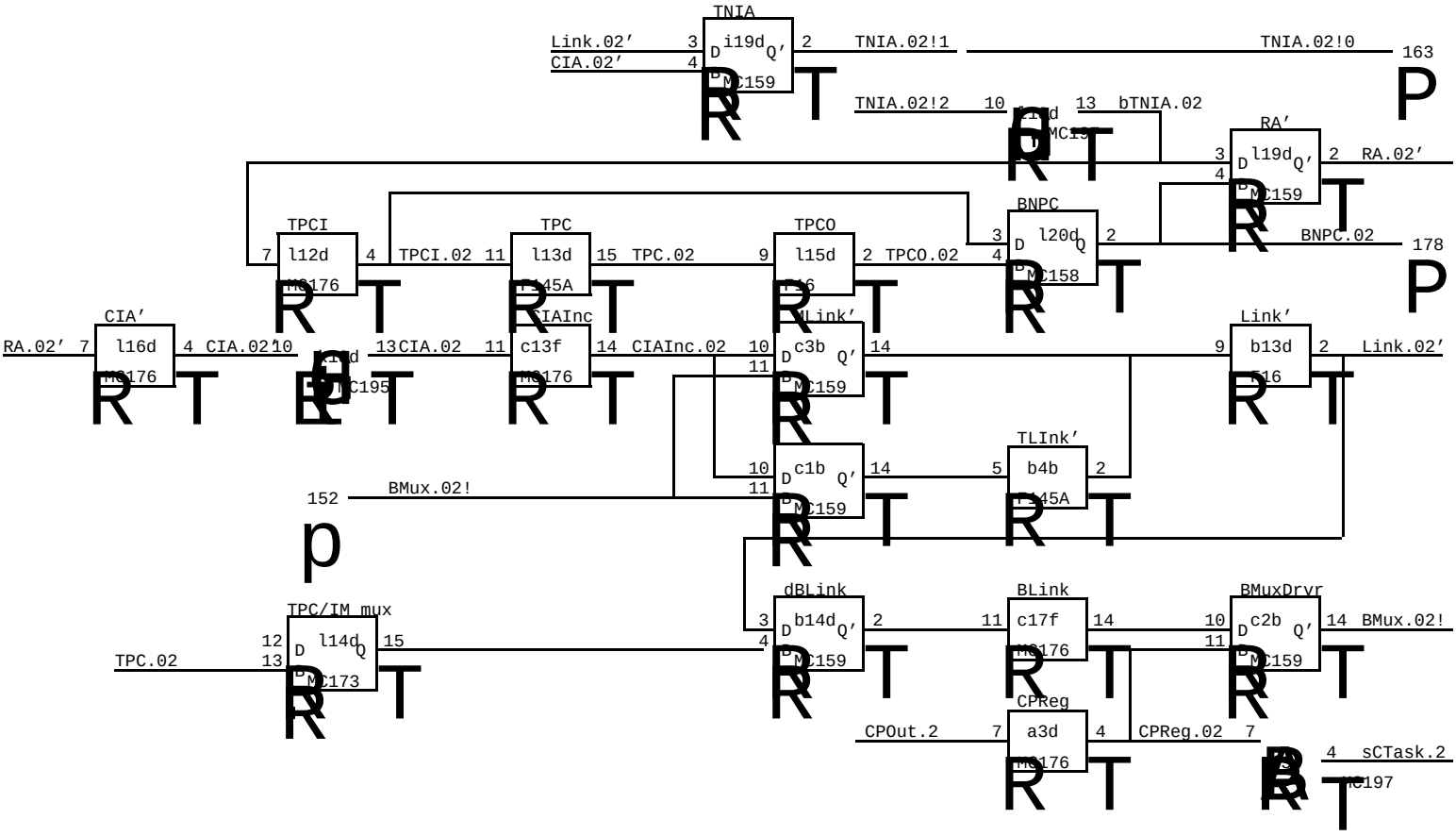
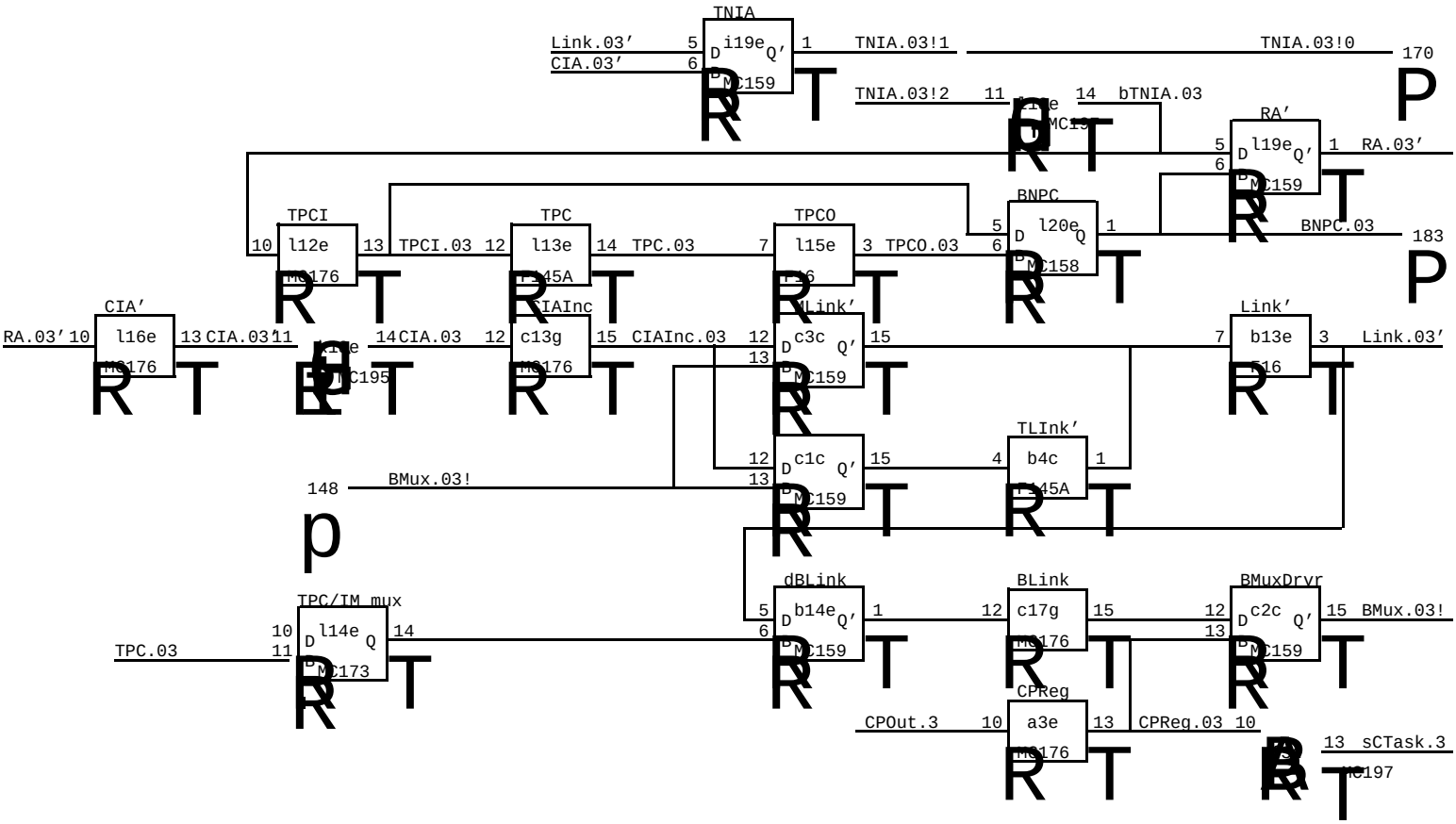
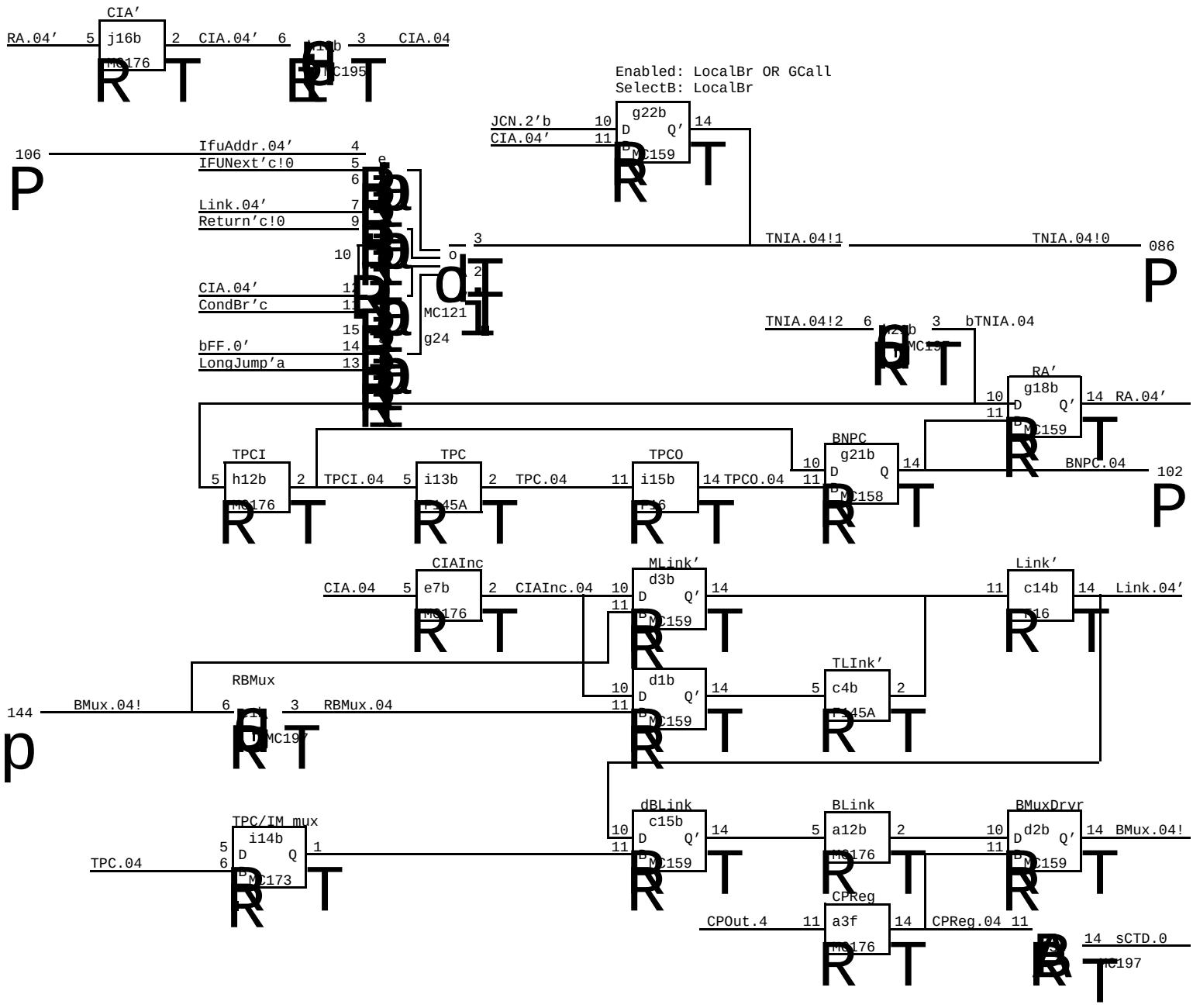
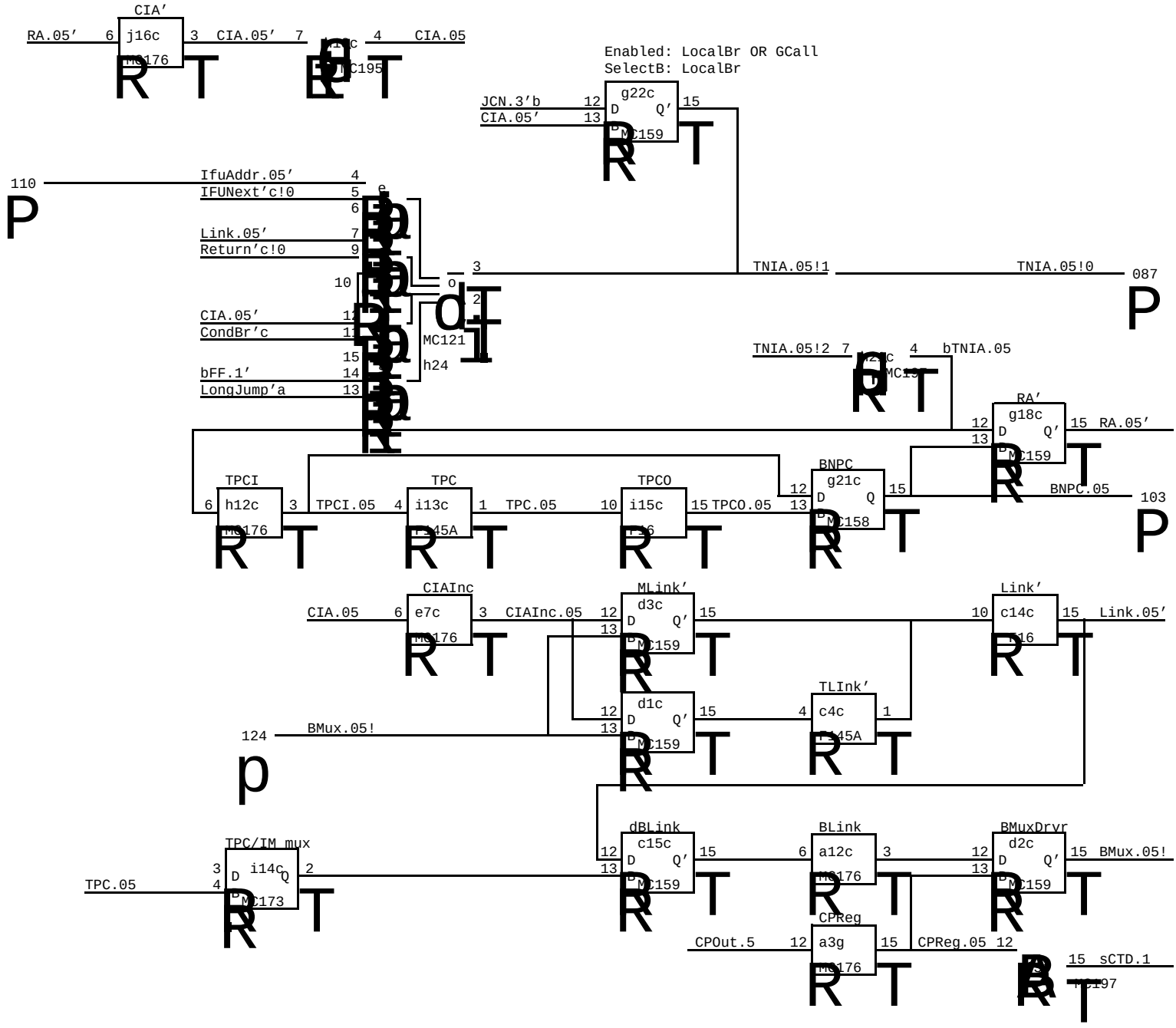




XEROX PARC	Project Dorado	Control Section Data Paths	File ContA07.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 07



XEROX PARC	Project Dorado	Control Section Data Paths	File ContA08.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 08



XEROX PARC	Project	Control Section Data Paths	File	Designer	Rev	Date	Page
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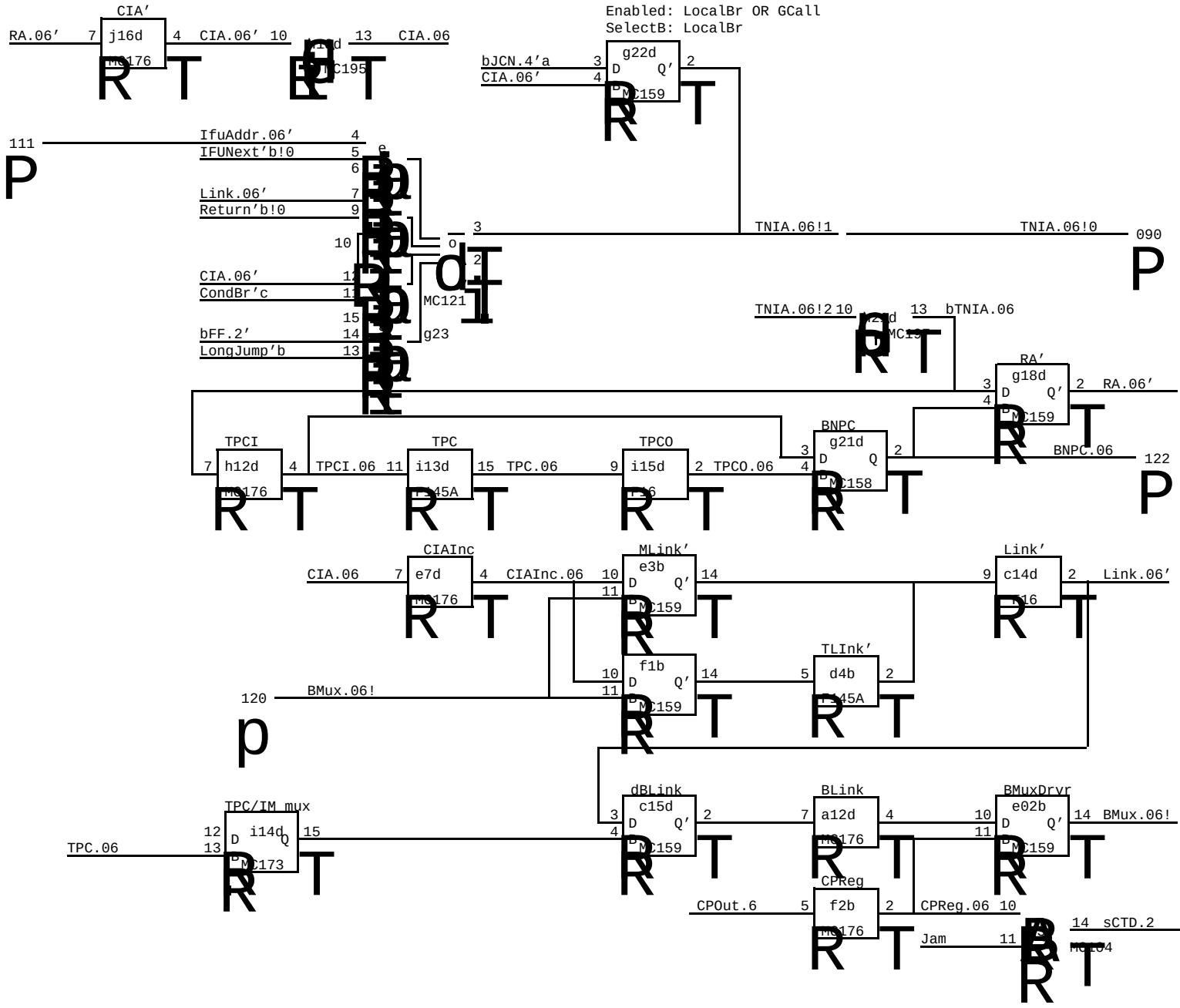
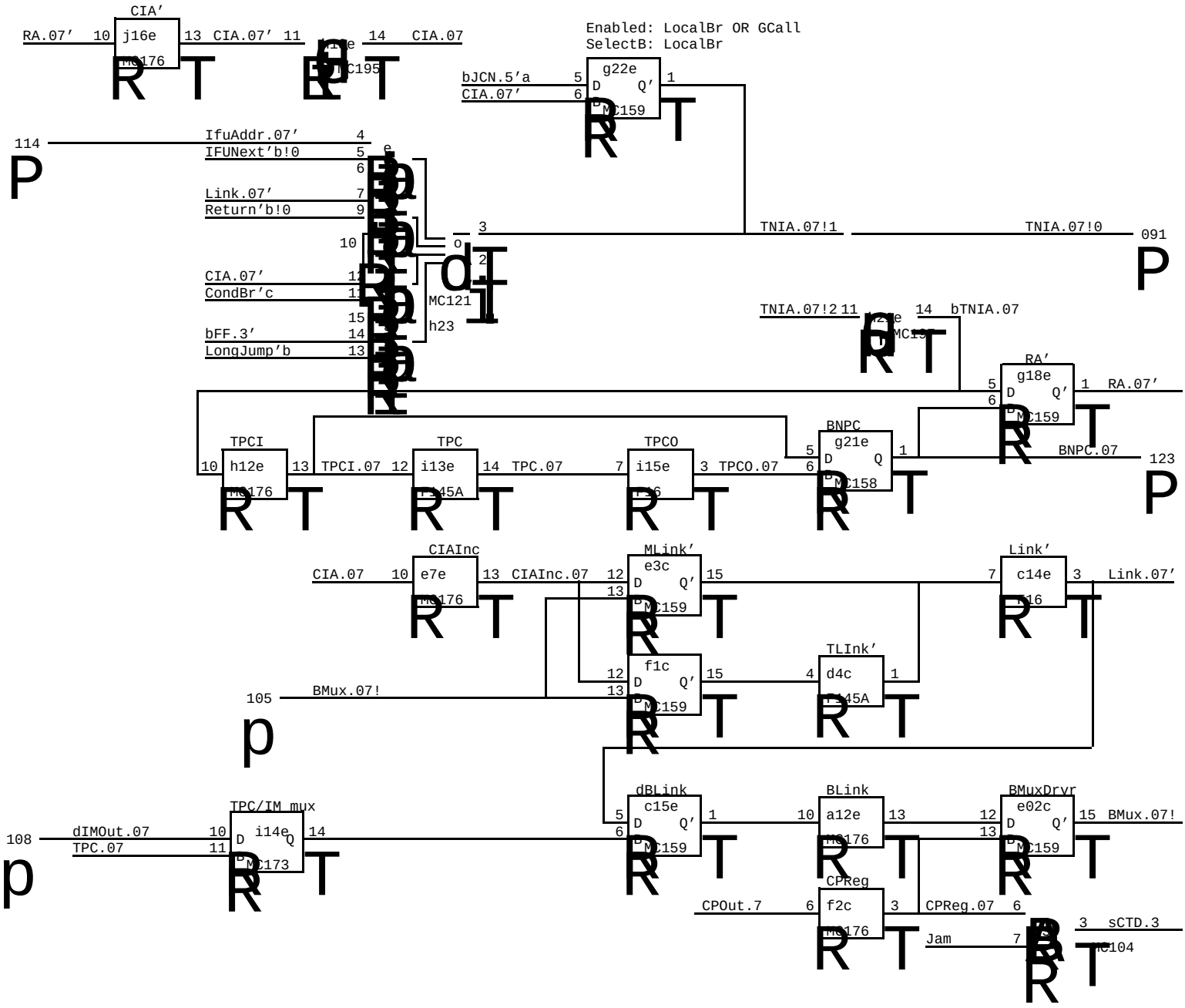
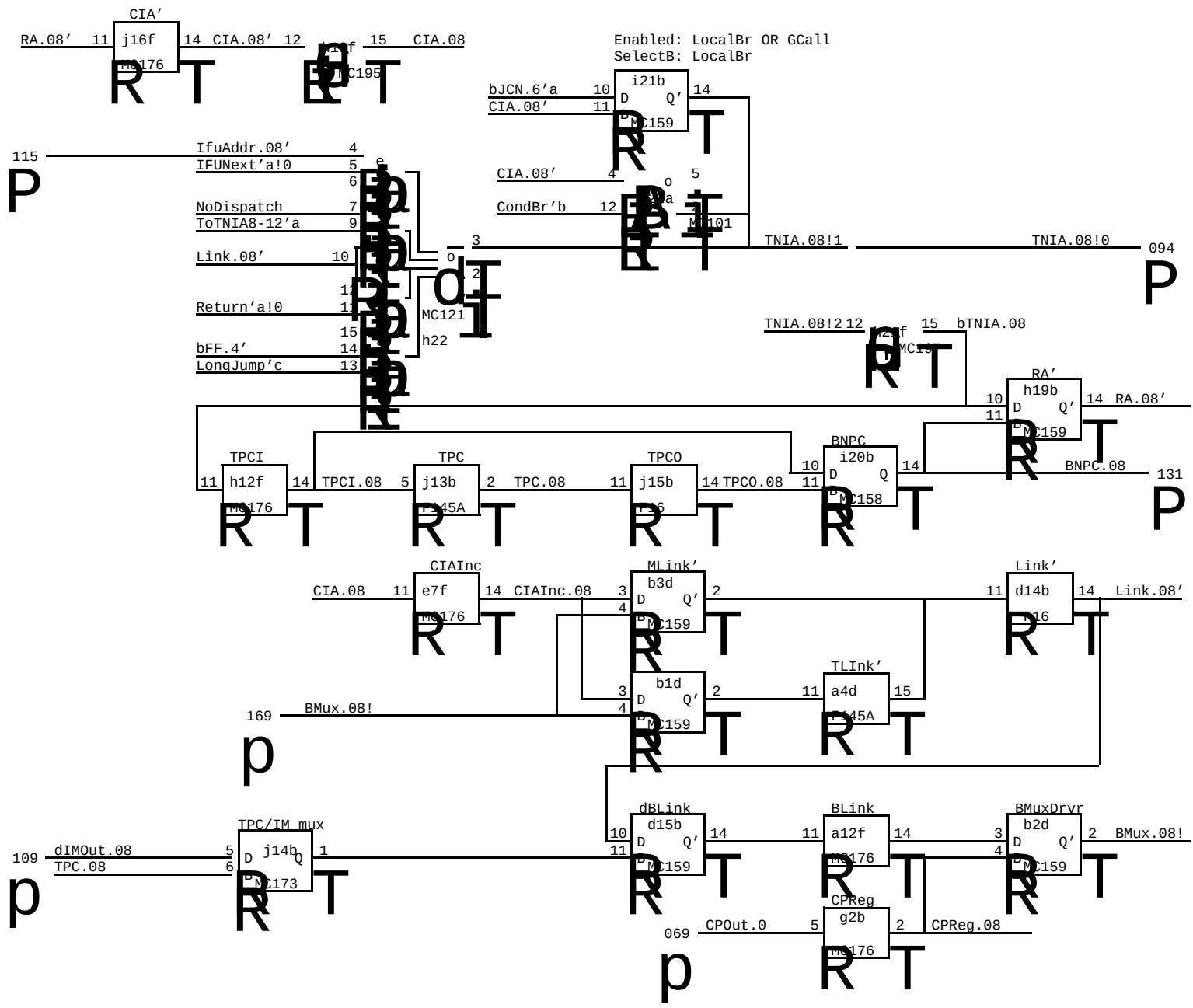


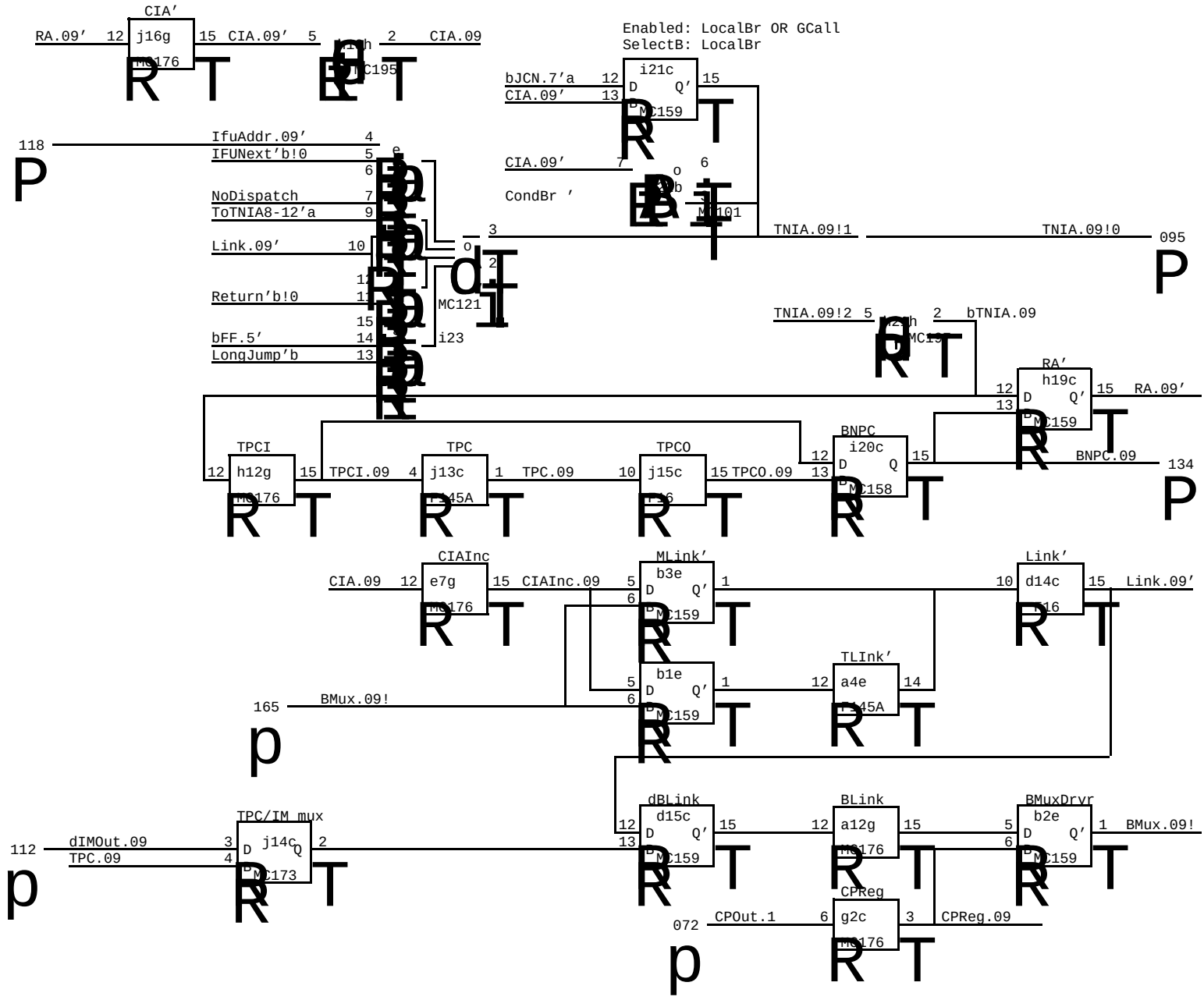
XEROX PARC	Project	Control Section Data Paths	File	Designer	Rev	Date	Page
	Dorado		ContA10.sil	Pier	Cd	7/13/79	10



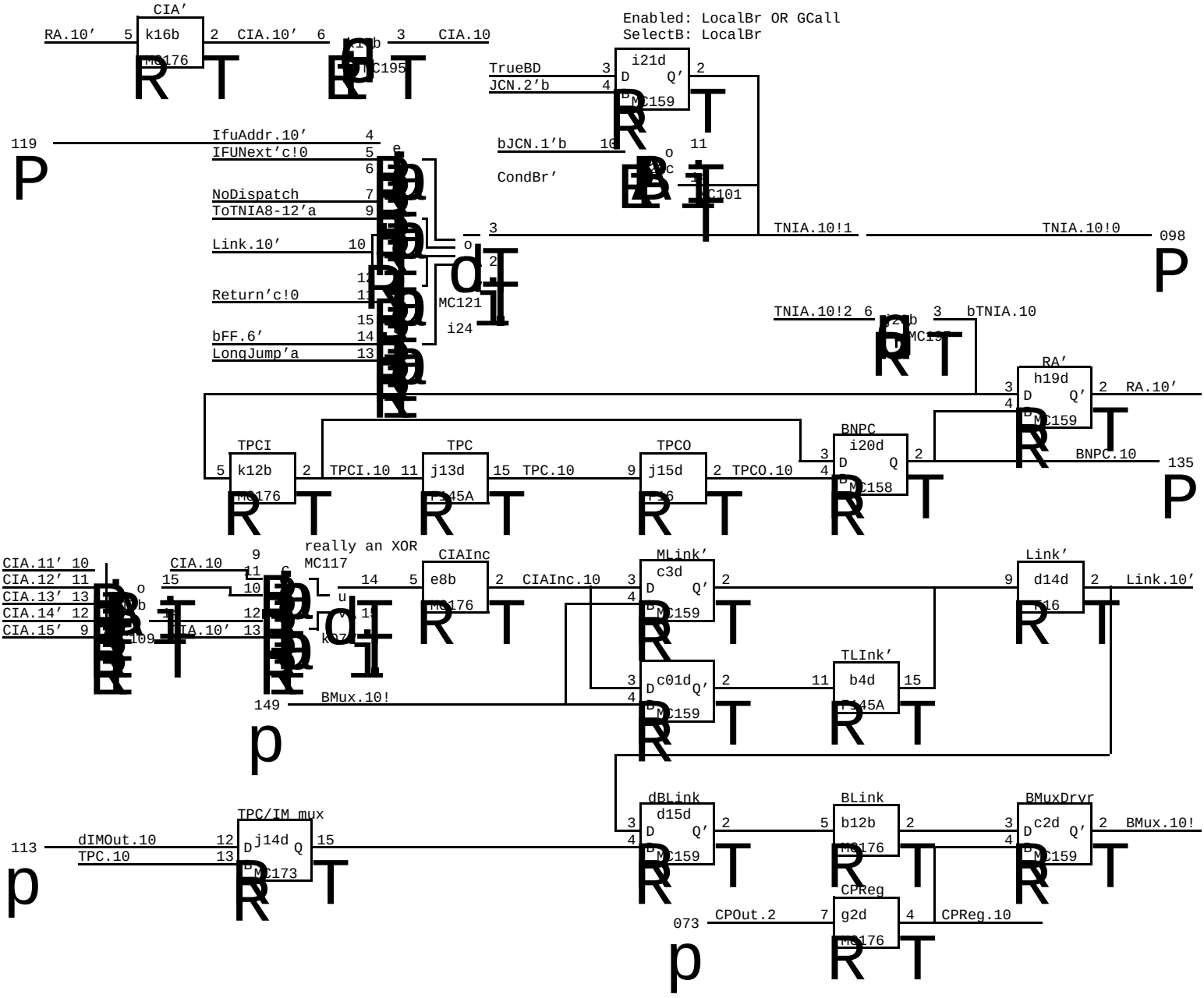
XEROX PARC	Project Dorado	Control Section Data Paths	File ContA11.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 11



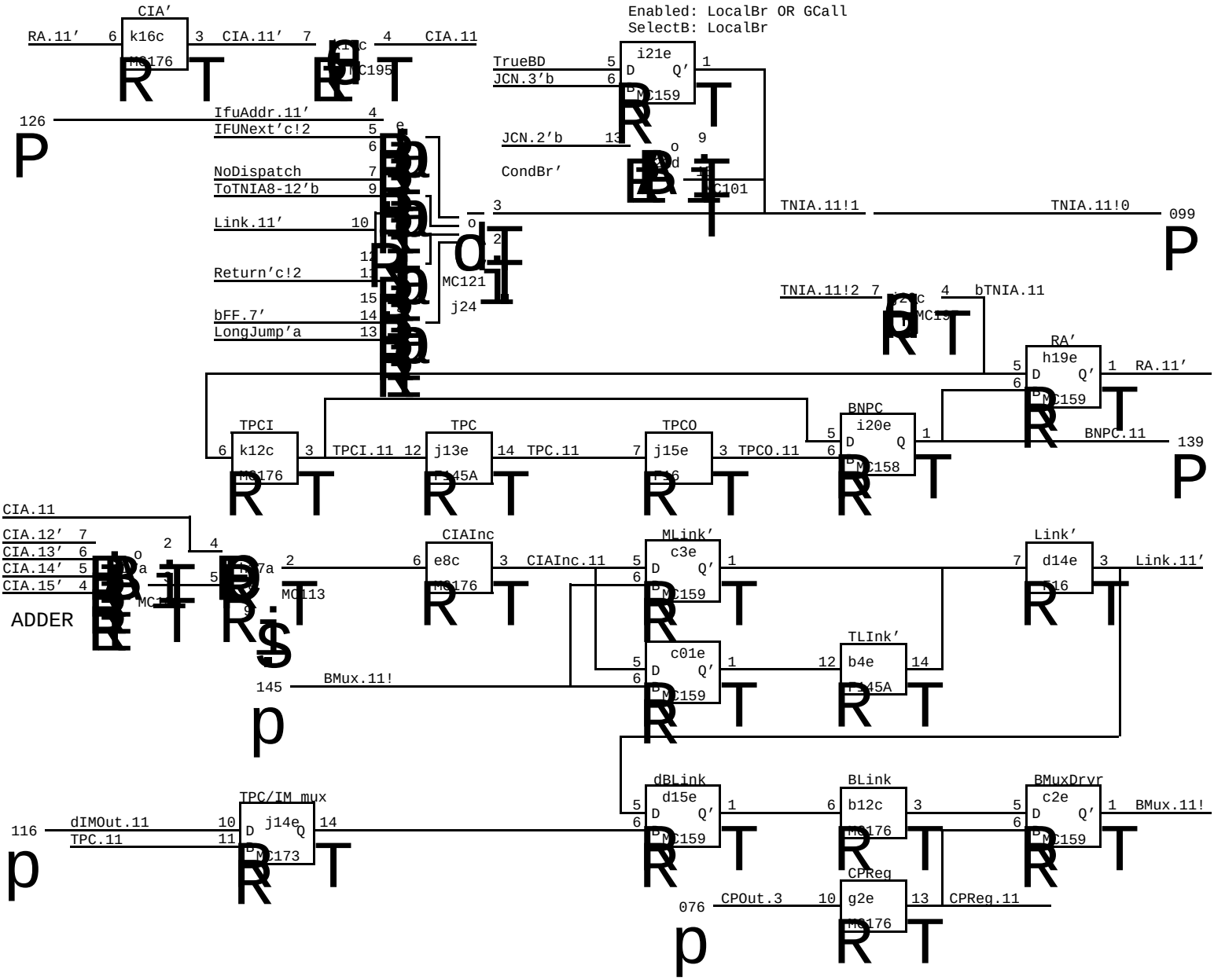
XEROX PARC	Project Dorado	Control Section Data Paths	File ContA12.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 12



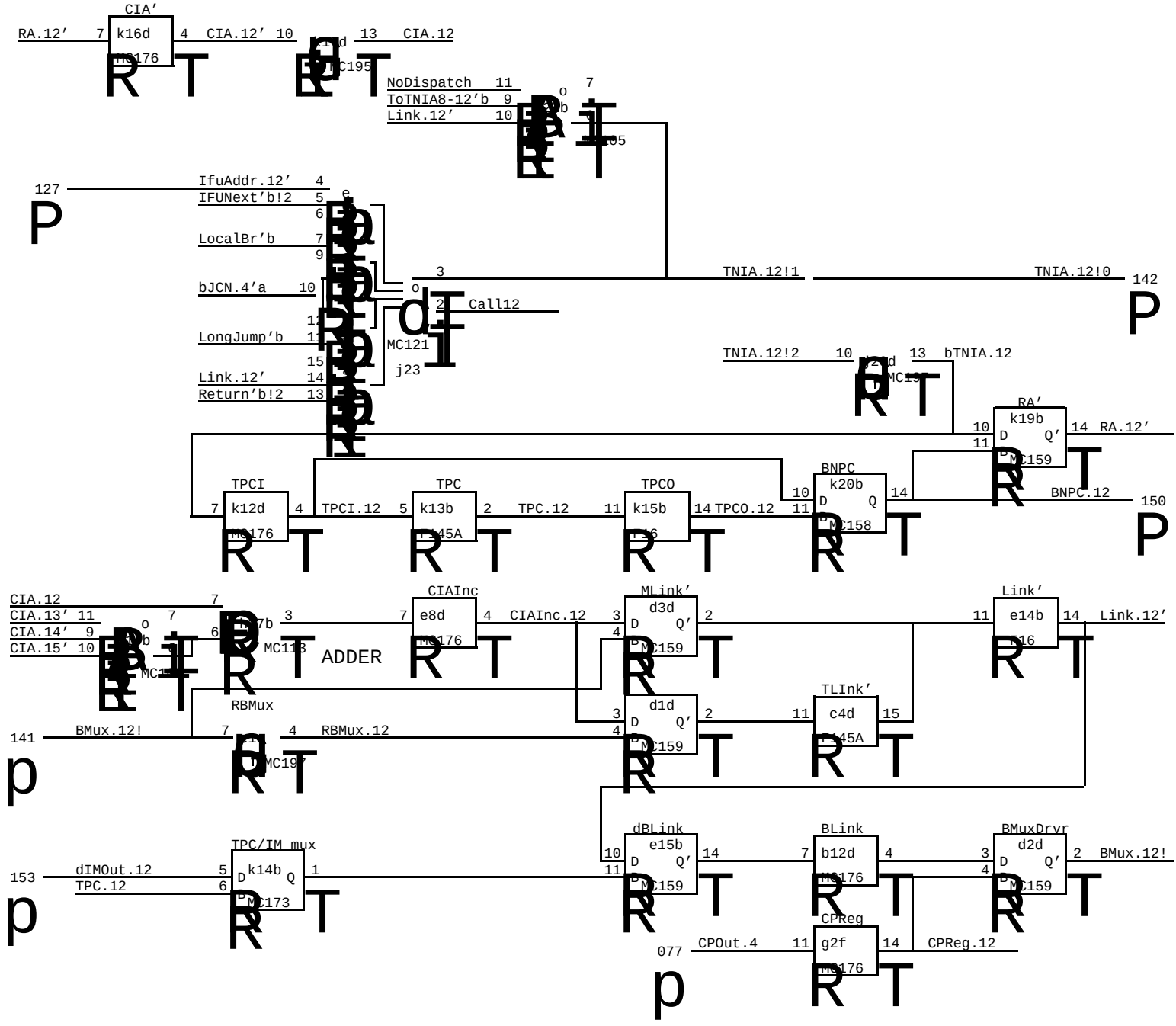
XEROX PARC	Project	Control Section Data Paths	File	Designer	Rev	Date	Page
	Dorado		ContA13.sil	Pier	Cd	7/13/79	13



XEROX PARC	Project Dorado	Control Section Data Paths	File ContA14.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 14



XEROX PARC	Project	Control Section Data Paths	File	Designer	Rev	Date	Page
	Dorado		ContA15.sil	Pier	Cd	7/13/79	15



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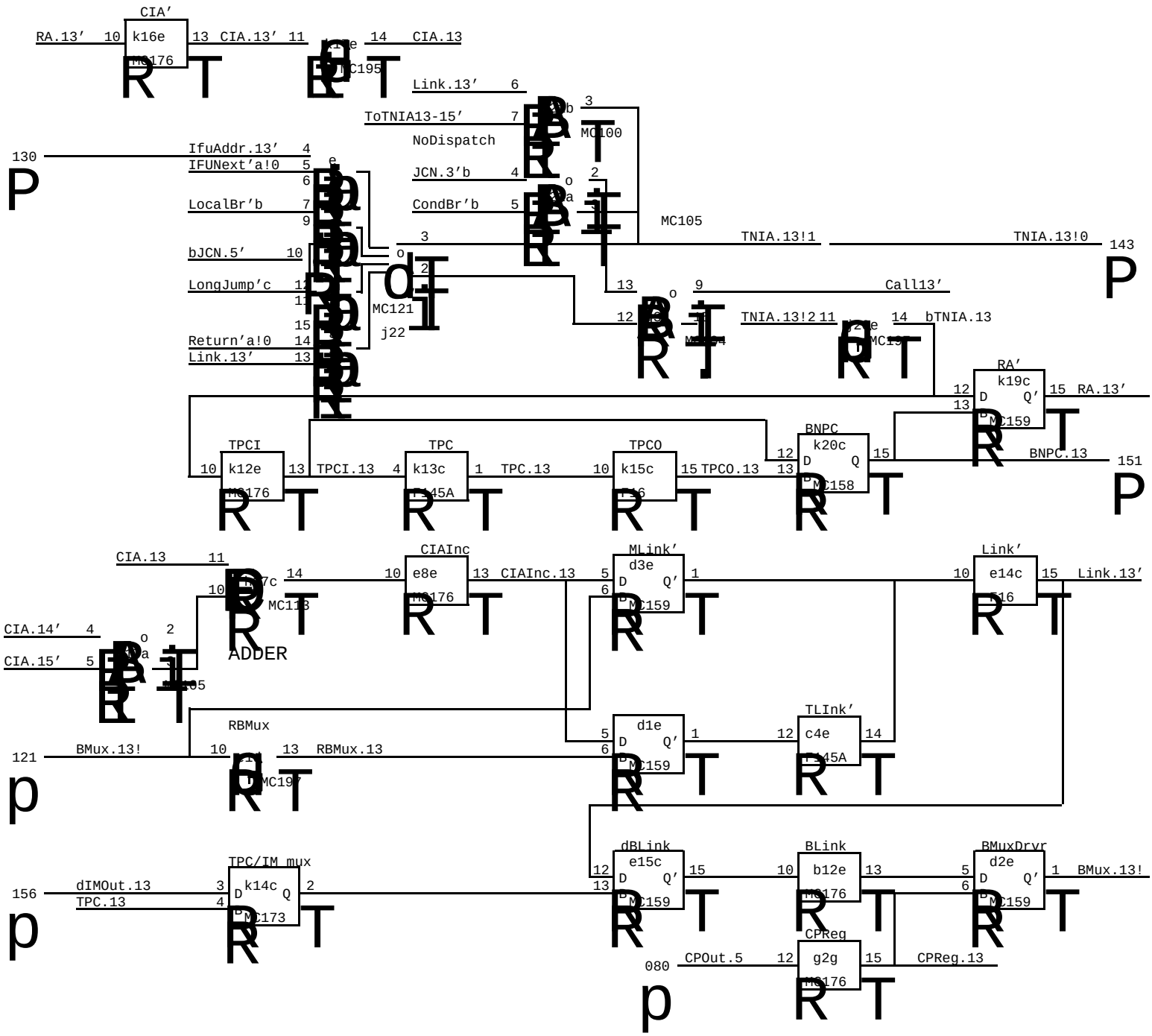
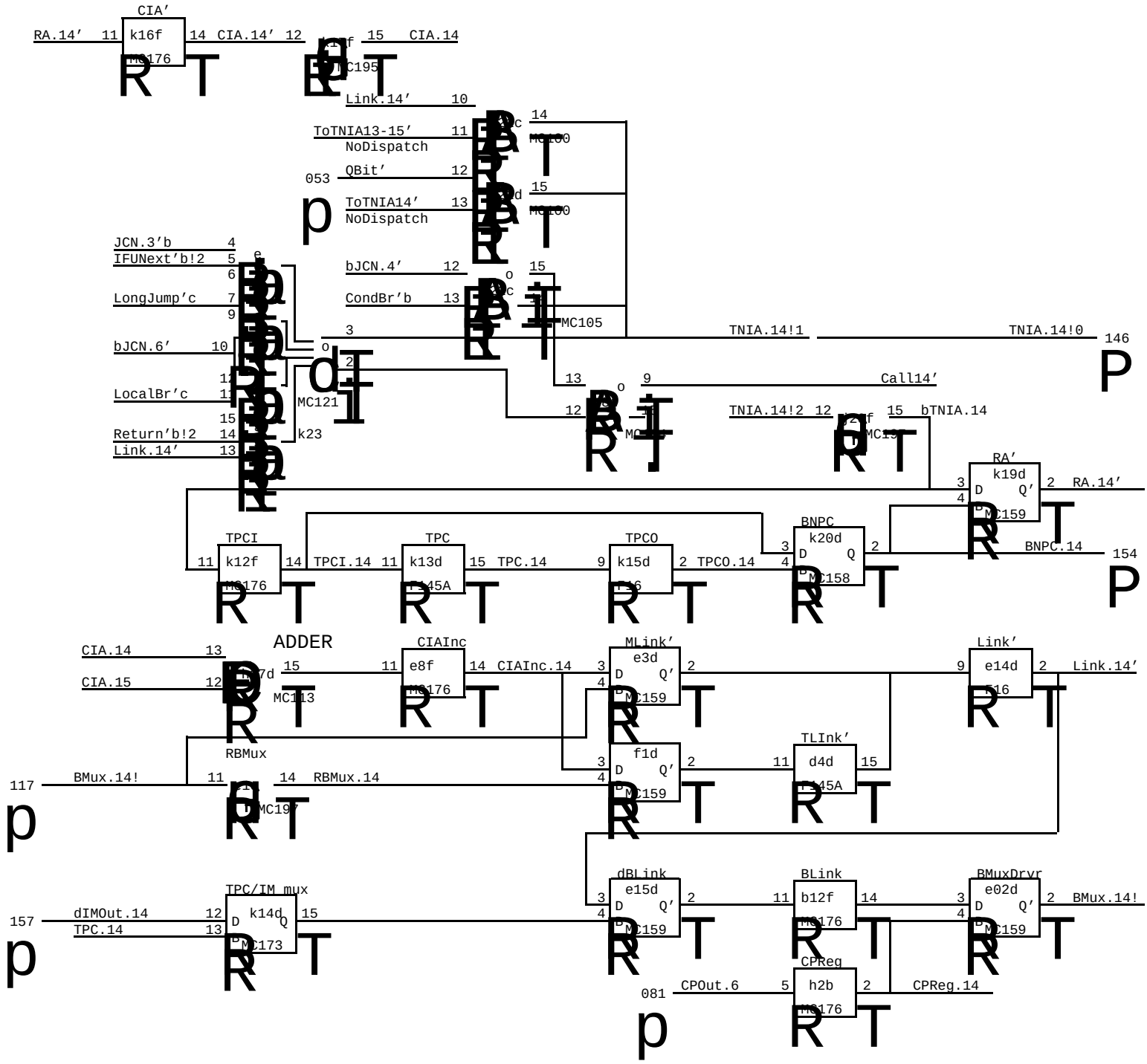
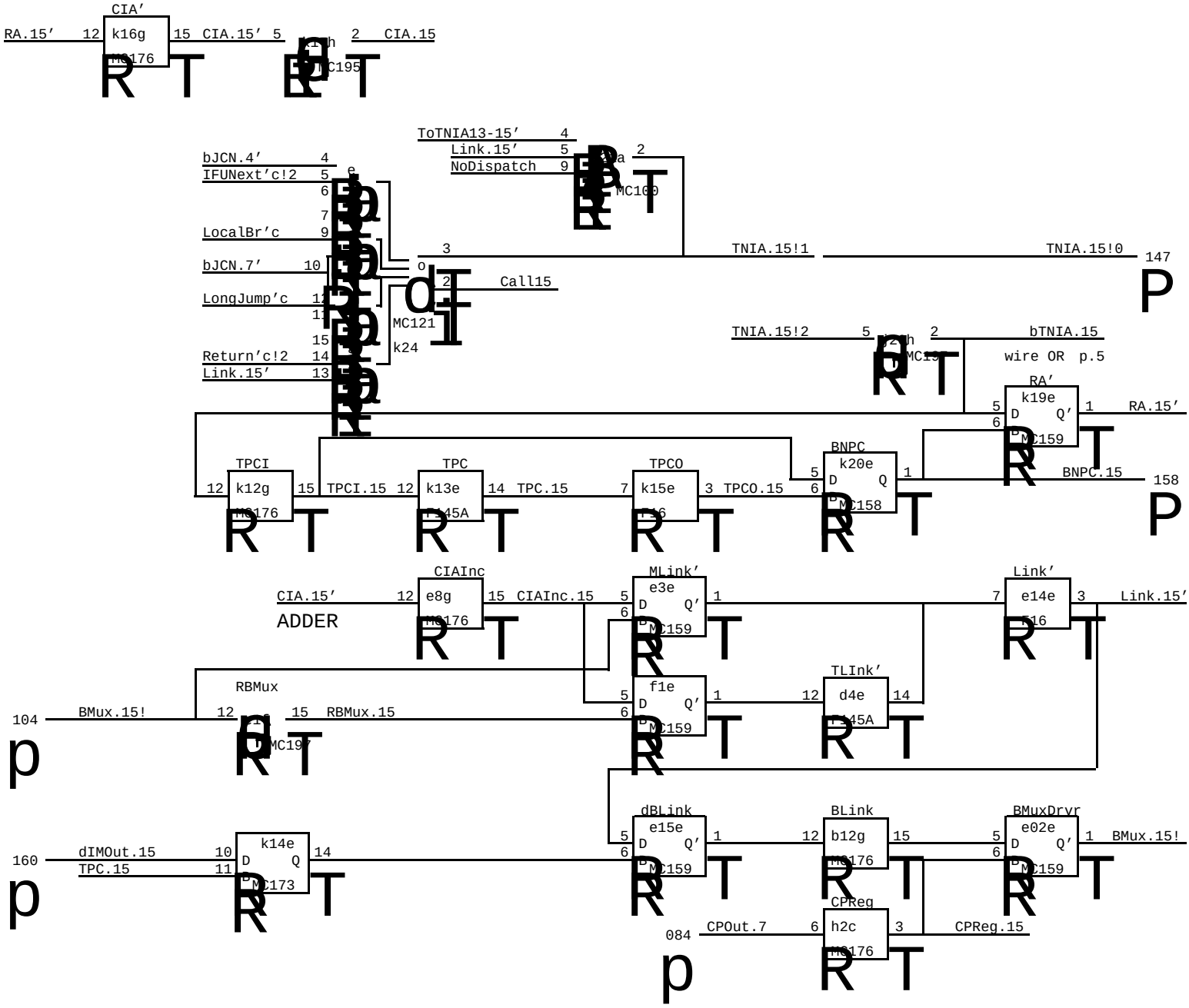


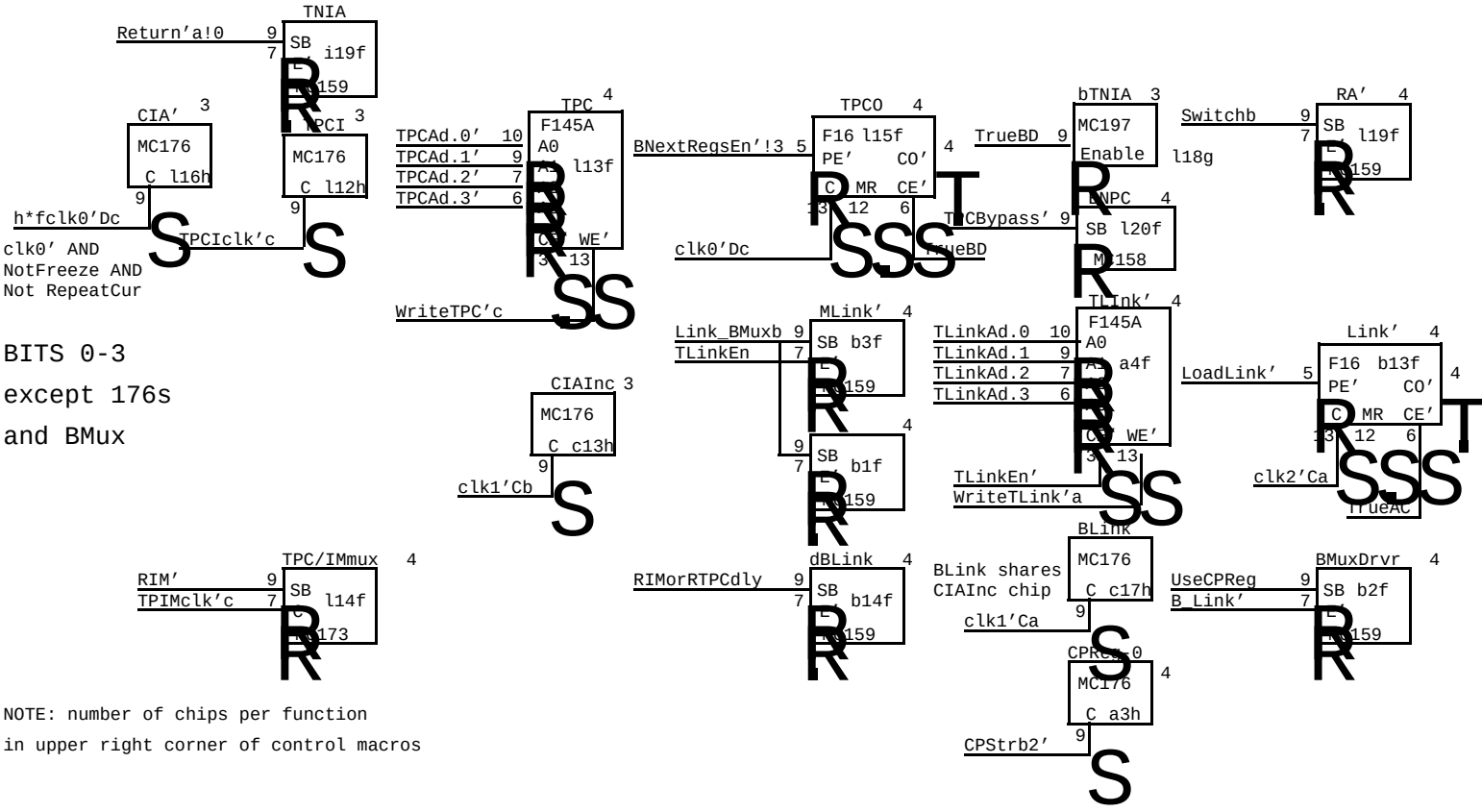
XEROX PARC	Project Dorado	Control Section Data Paths	File ContA17.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 17



XEROX PARC	Project Dorado	Control Section Data Paths	File ContA18.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 18

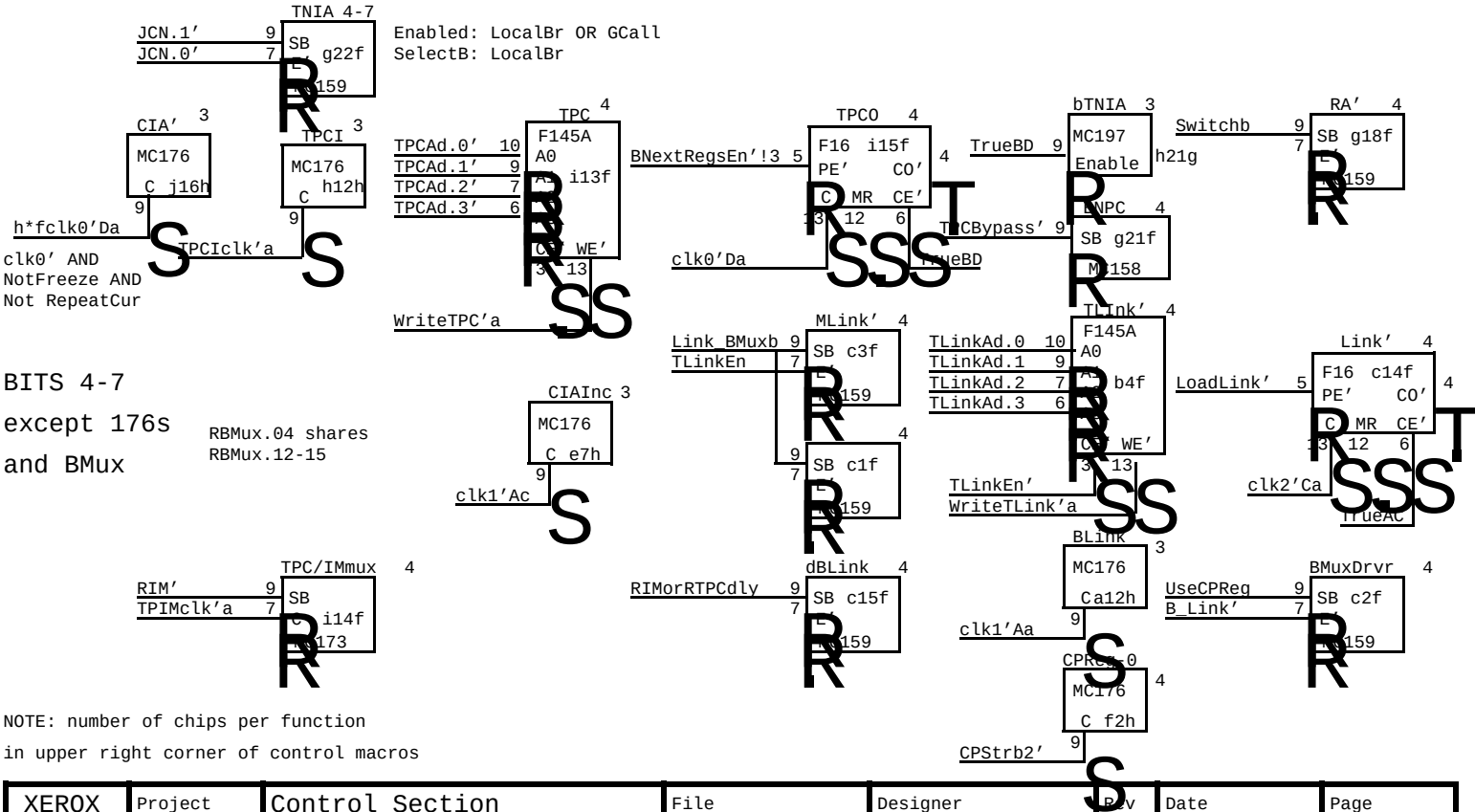


XEROX PARC	Project Dorado	Control Section Data Paths	File ContA19.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 19



BITS 0-3
except 176s
and BMux

NOTE: number of chips per function
in upper right corner of control macros

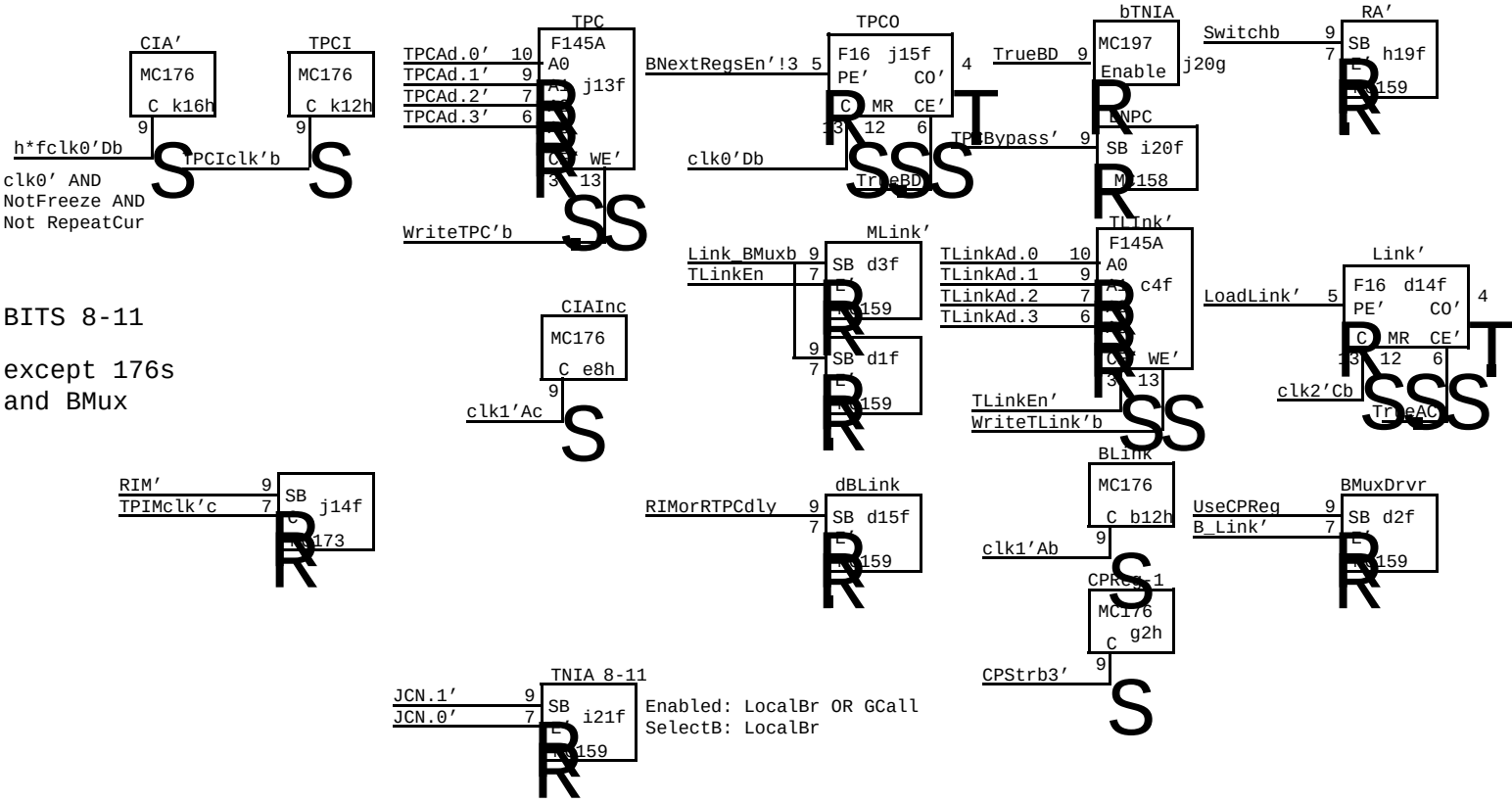


BITS 4-7
except 176s
and BMux

RBMux.04 shares
RBMux.12-15

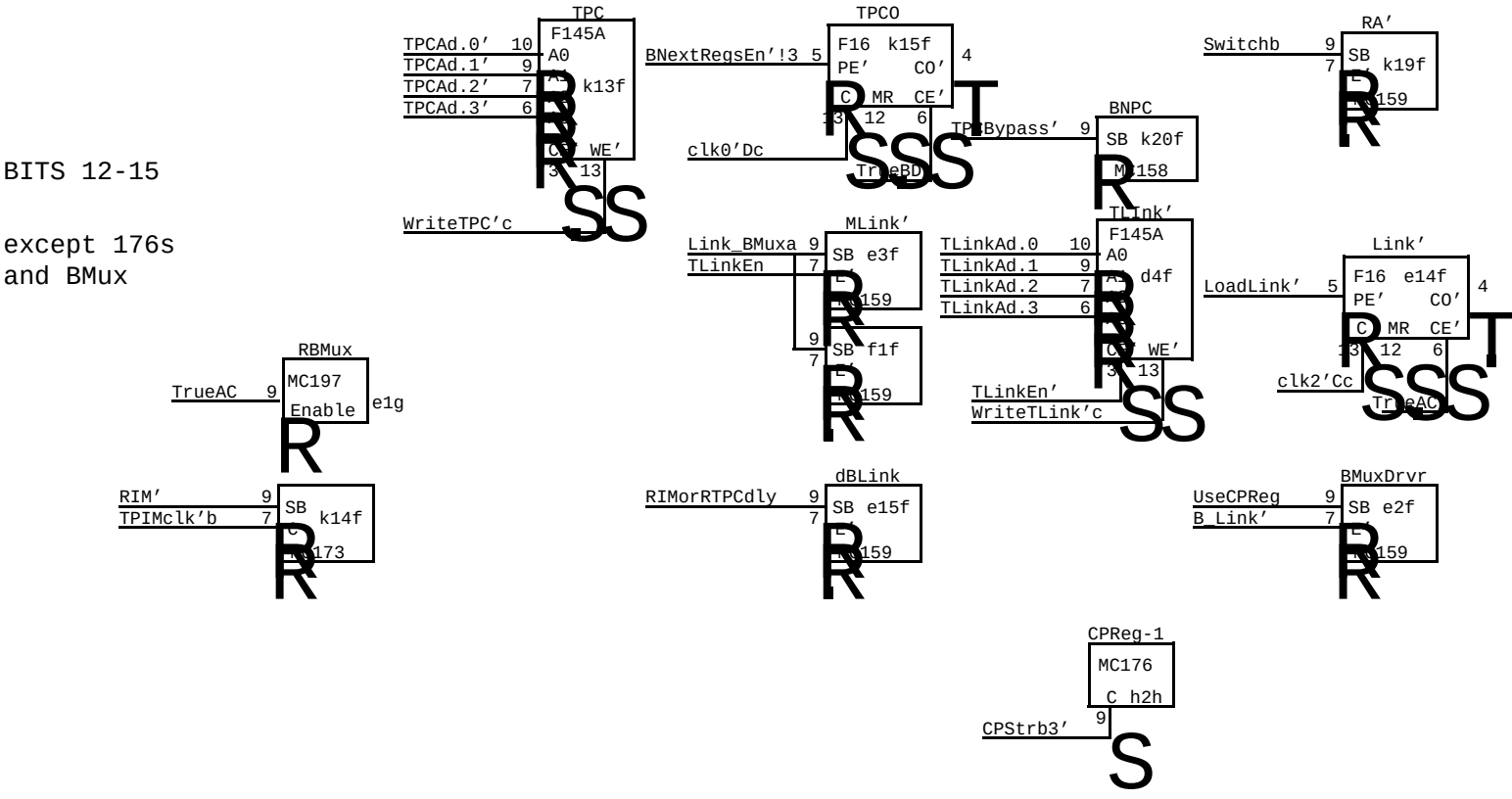
NOTE: number of chips per function
in upper right corner of control macros

XEROX PARC	Project Dorado	Control Section Data Paths	File ContA20.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 20



BITS 8-11

except 176s
and BMux

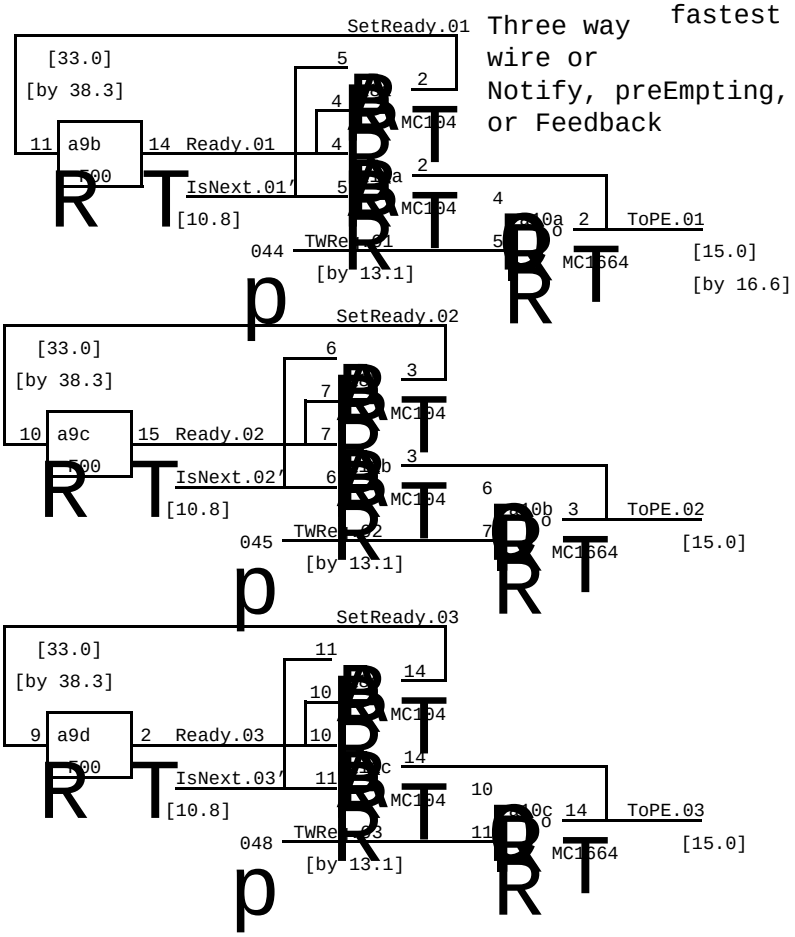


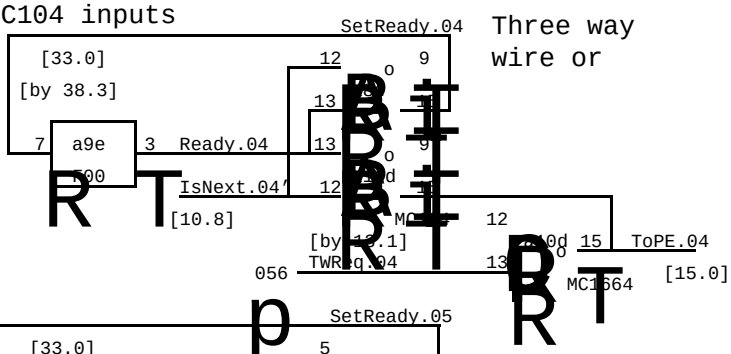
BITS 12-15

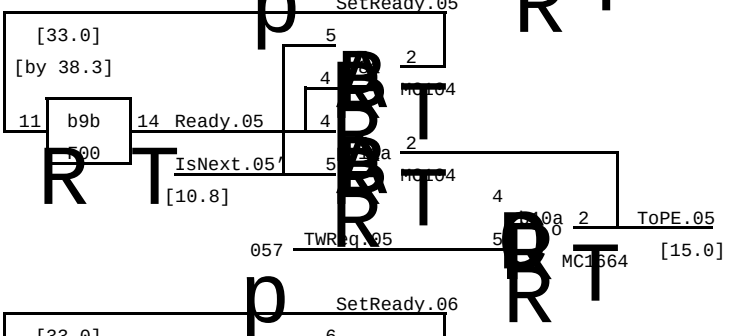
except 176s
and BMux

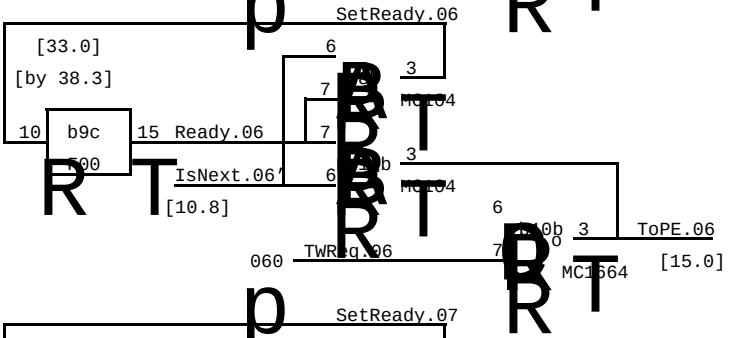
XEROX PARC	Project Dorado	Control Section Data Paths	File ContA21.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 21

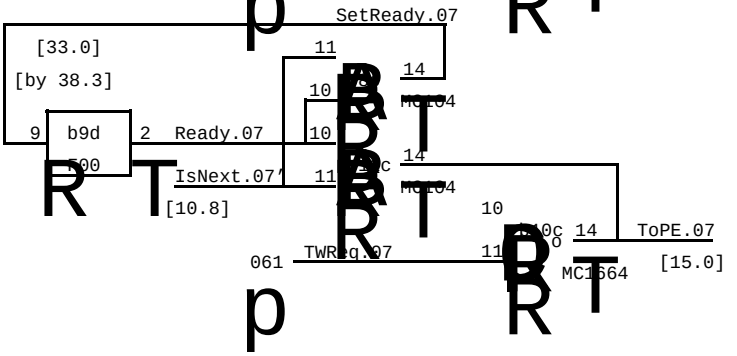
Note: choose IsNext' into fastest MC104 inputs

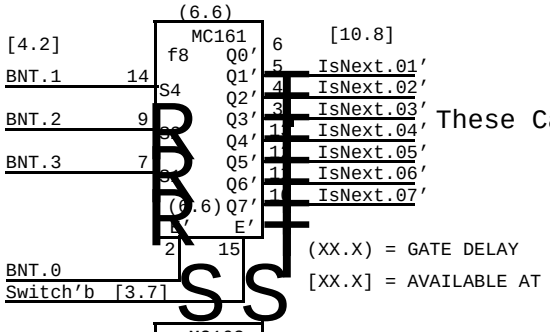


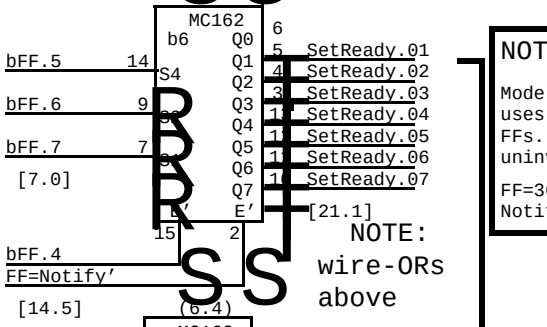








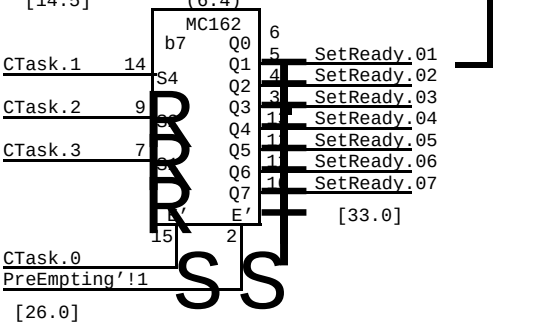


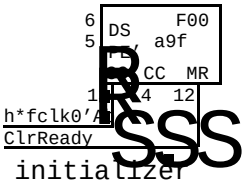


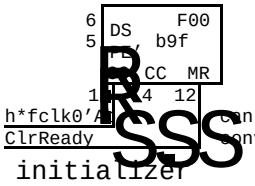
NOTE !!!

Model0 Notify uses inverted FFs. These are uninverted;e.g.

FF=361b is Notify[1]



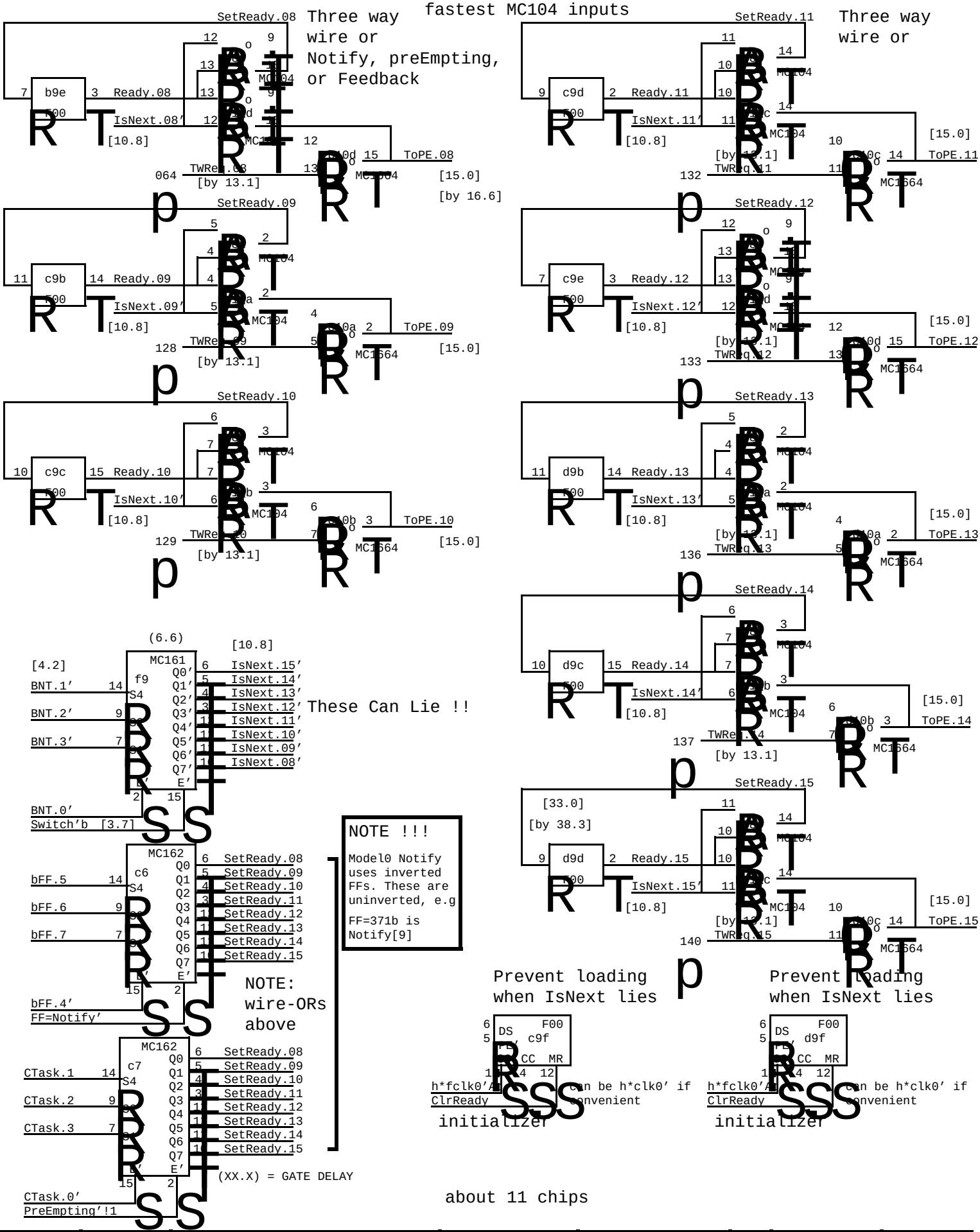




about 11 chips

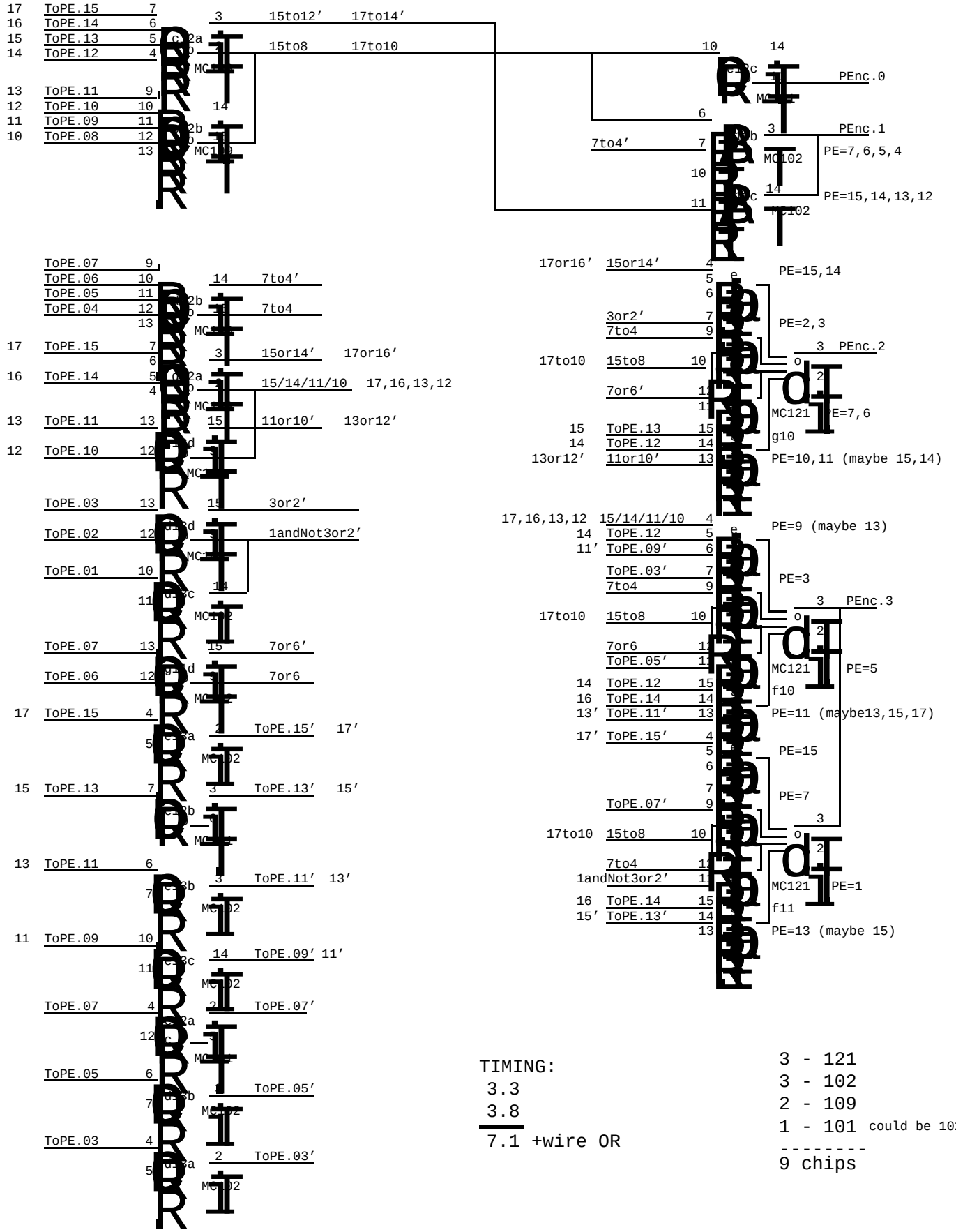
XEROX PARC	Project Dorado	Ready Logic	File ContA22.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 22

NOTE: choose IsNext′ into fastest MC104 inputs



XEROX PARC	Project: Dorado	Ready Logic	File: ContA23.sil	Designer: Pier	Rev: Cd	Date: 7/13/79	Page: 23

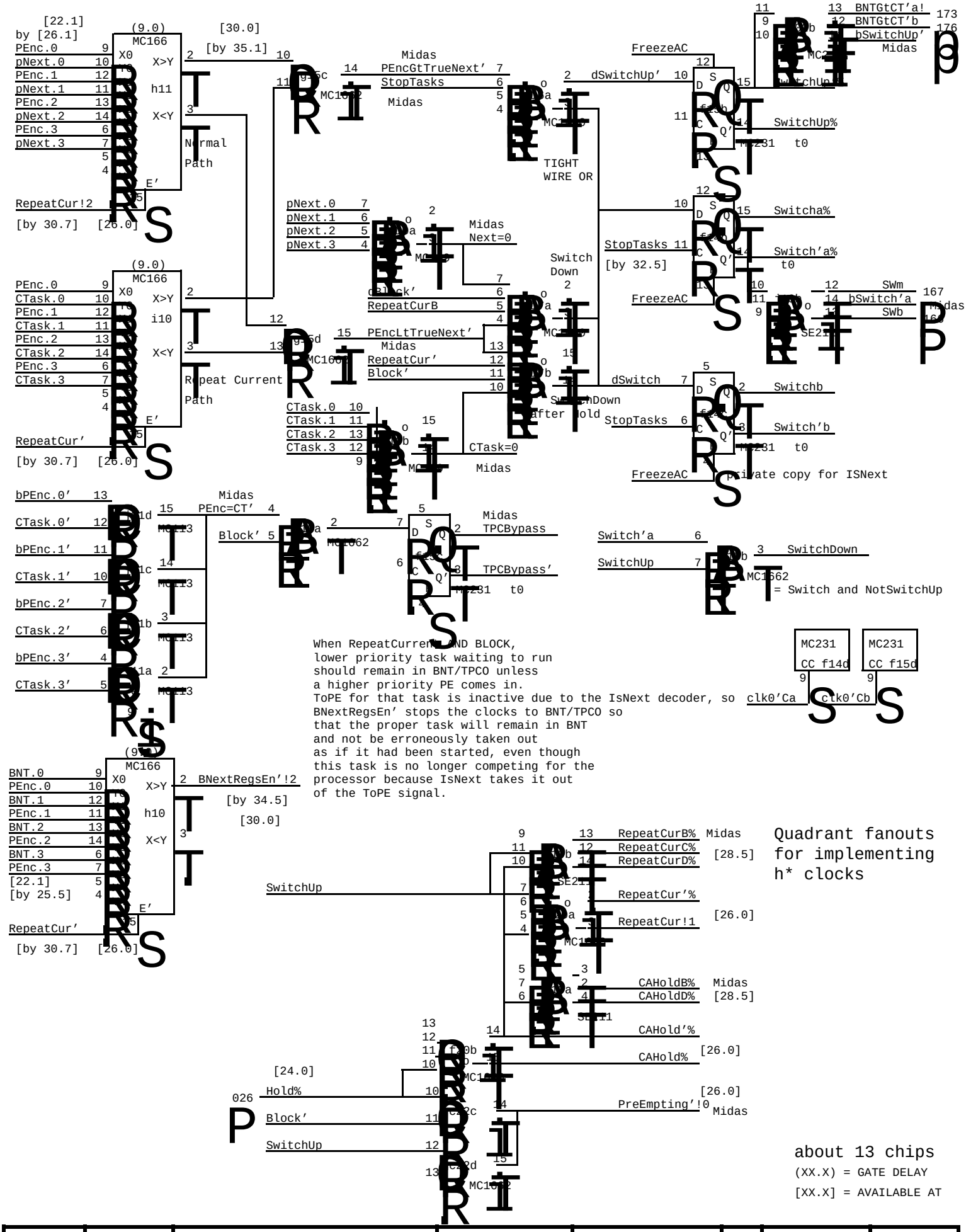
REQUEST NUMBERS
IN FONT 2 ARE OCTAL



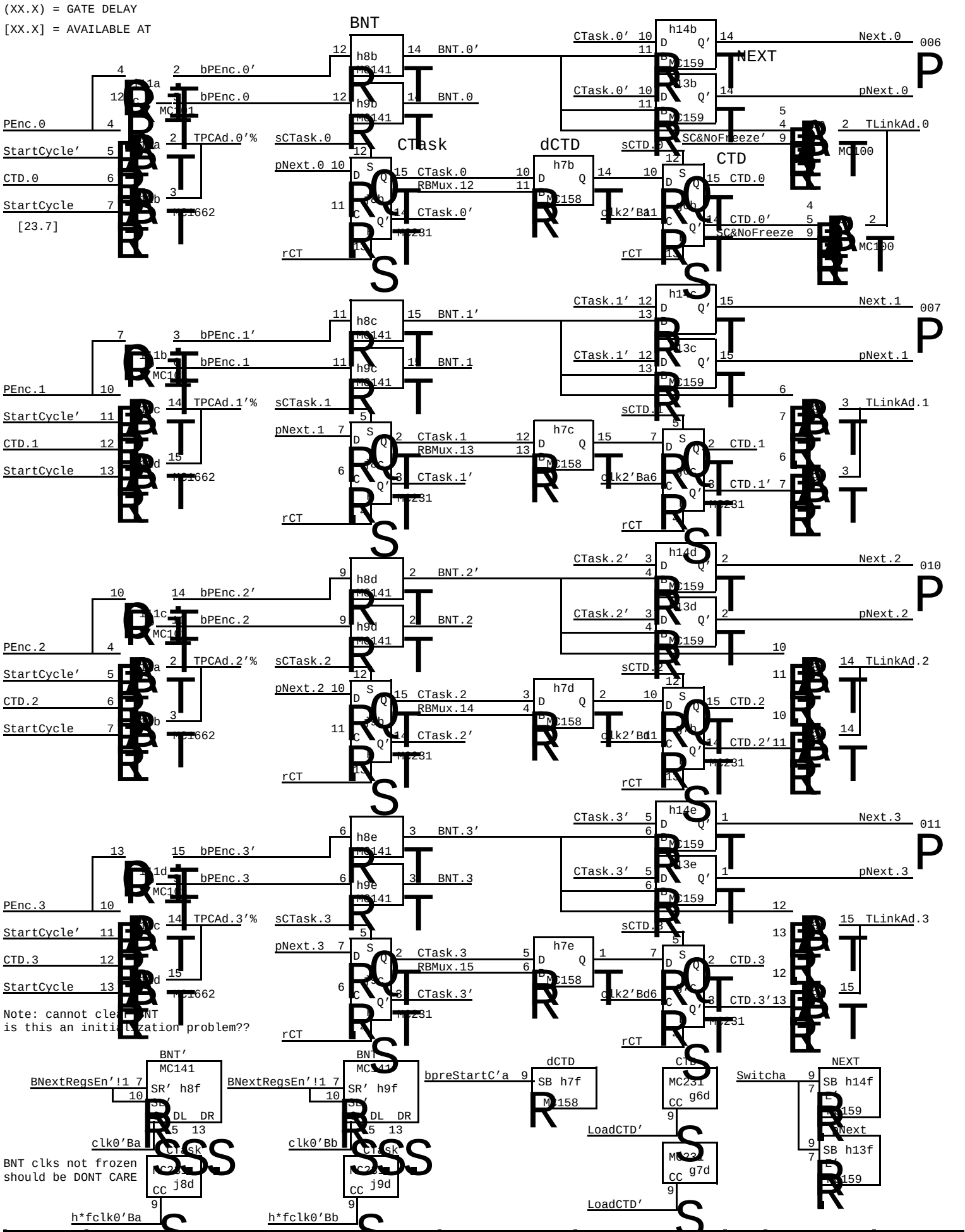
TIMING:
3.3
3.8
7.1 +wire OR

3 - 121
3 - 102
2 - 109
1 - 101 could be 102
---
9 chips

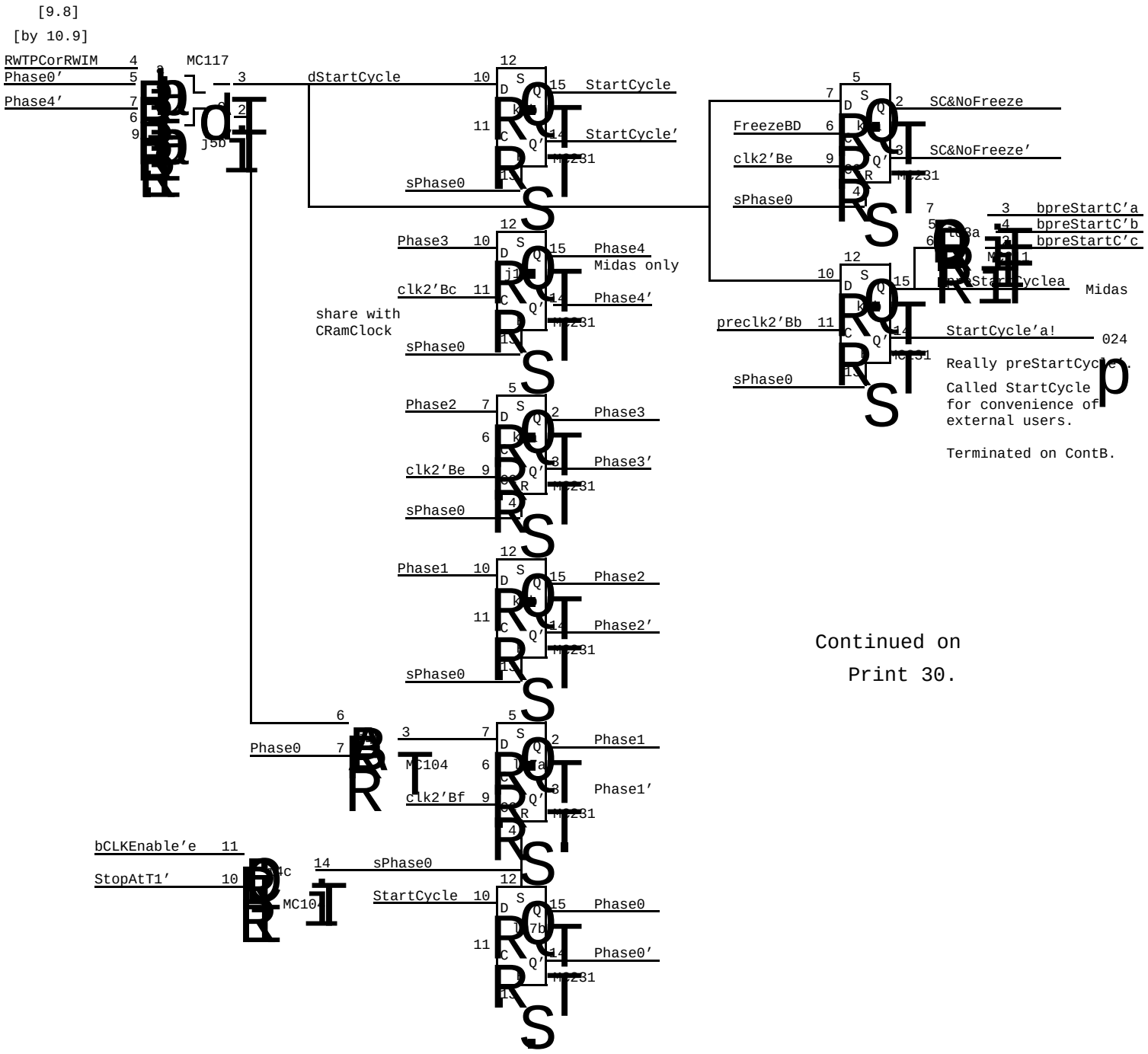
XEROX PARC	Project Dorado	Wakeup Priority Encoder	File ContA24.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 24



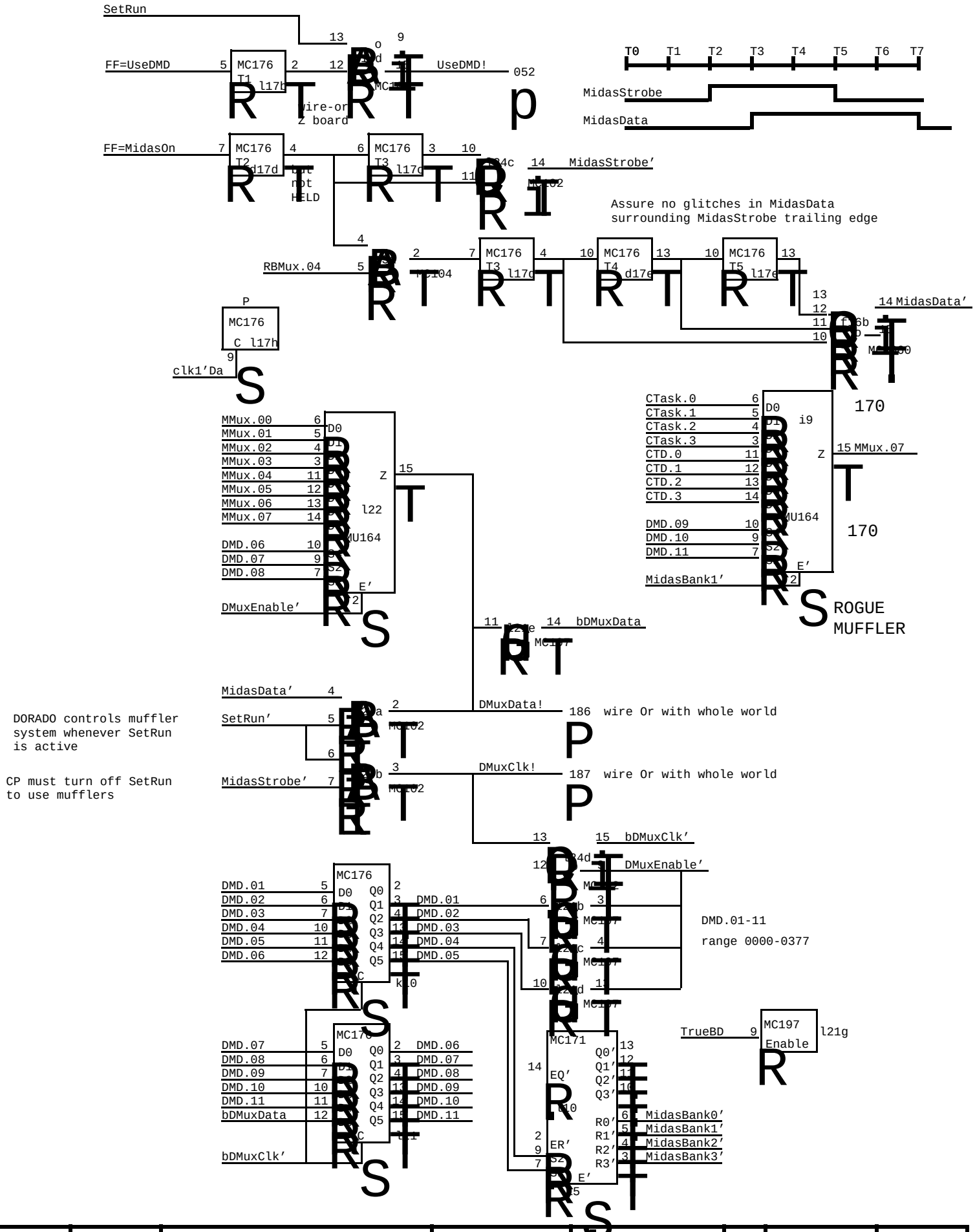
XEROX PARC	Project		File	Designer	Rev	Date	Page
	Dorado	Task Switch Generator	ContA25.sil	Pier	Cd	7/13/79	25



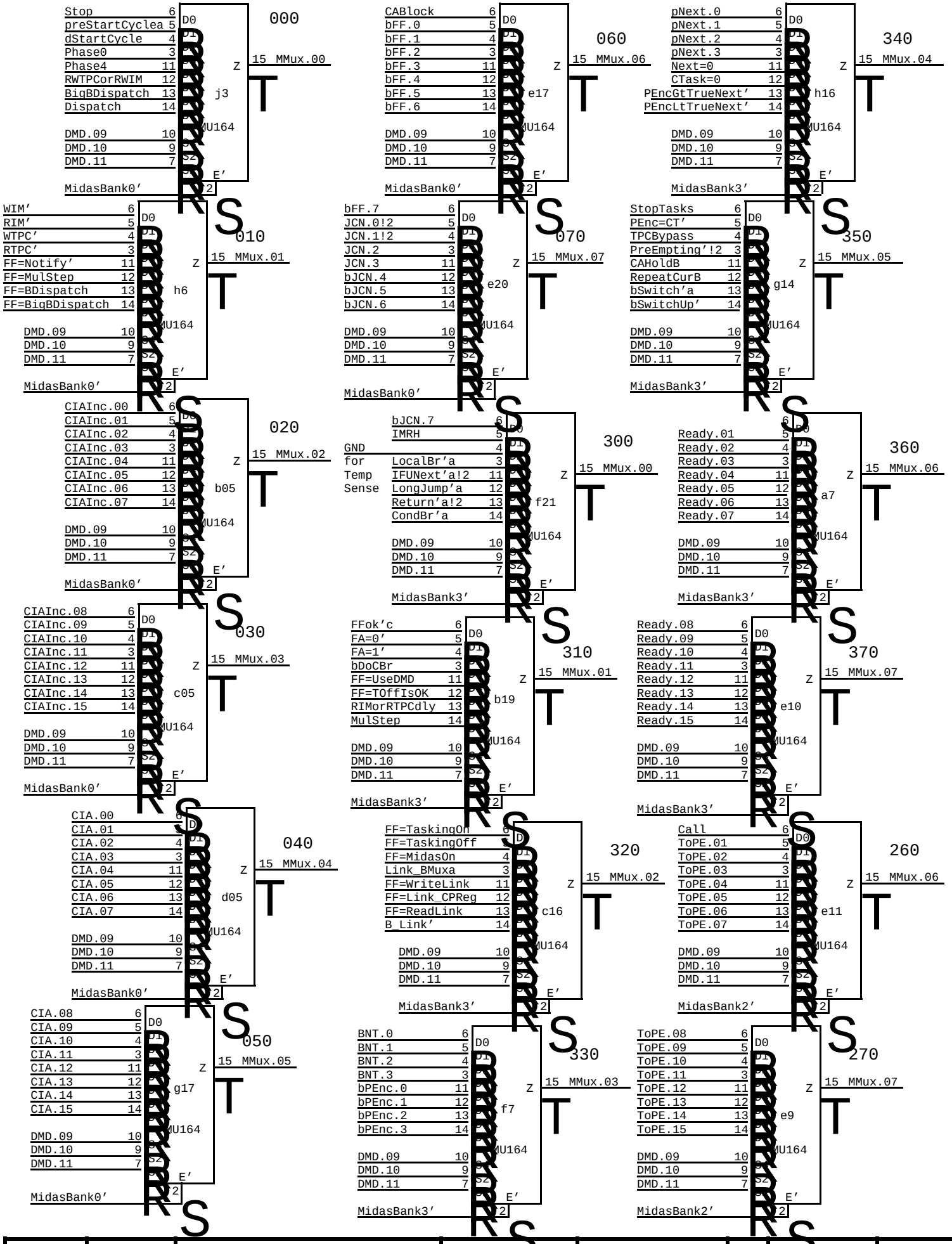
XEROX PARC	Project Dorado	Task Registers: HTask, BNT,CTask,CTD,Next	File ContA26.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 26



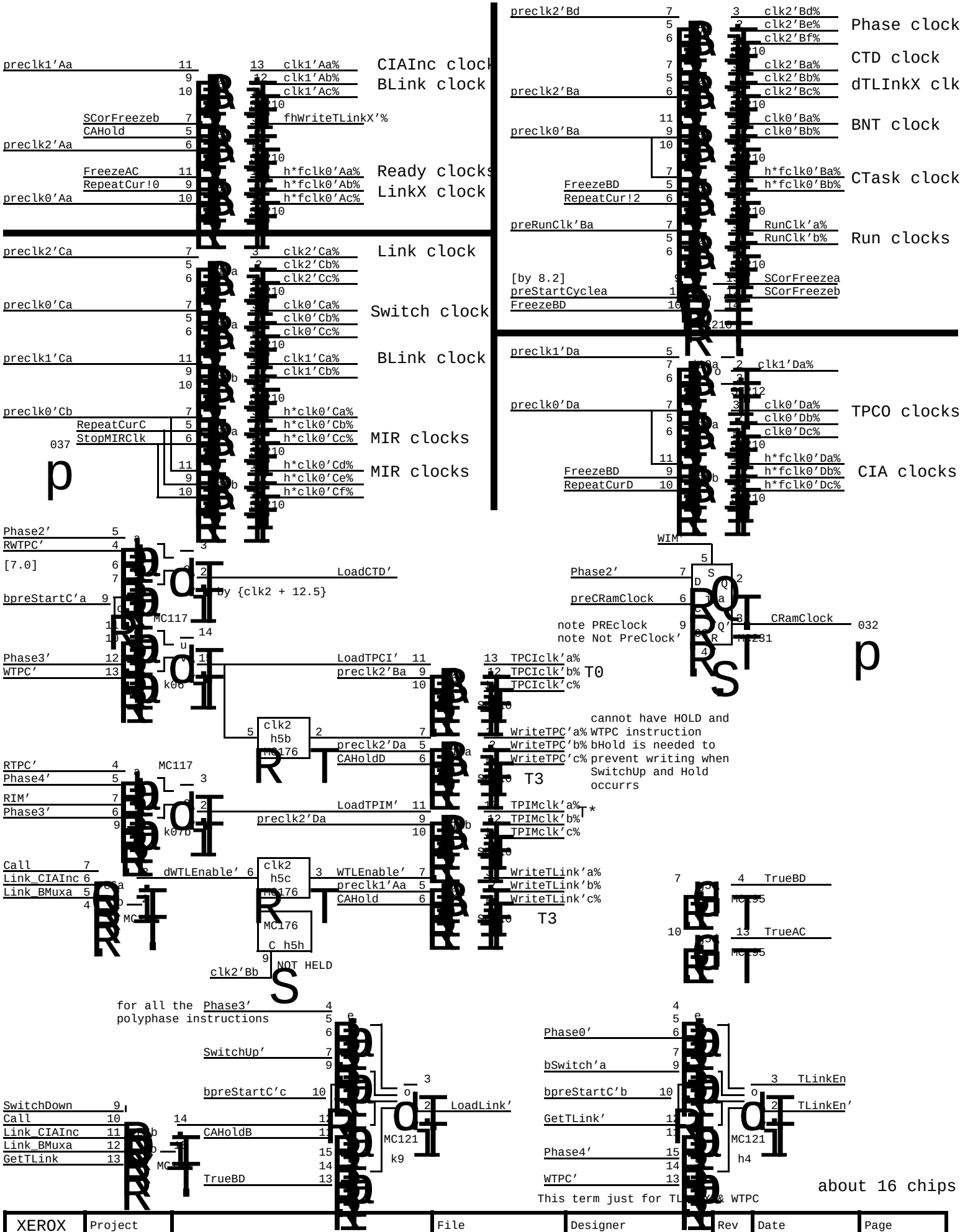
XEROX PARC	Project Dorado	Phase Generator	File ContA27.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 27



XEROX PARC	Project Dorado	Midas Interface	File ContA28.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 28

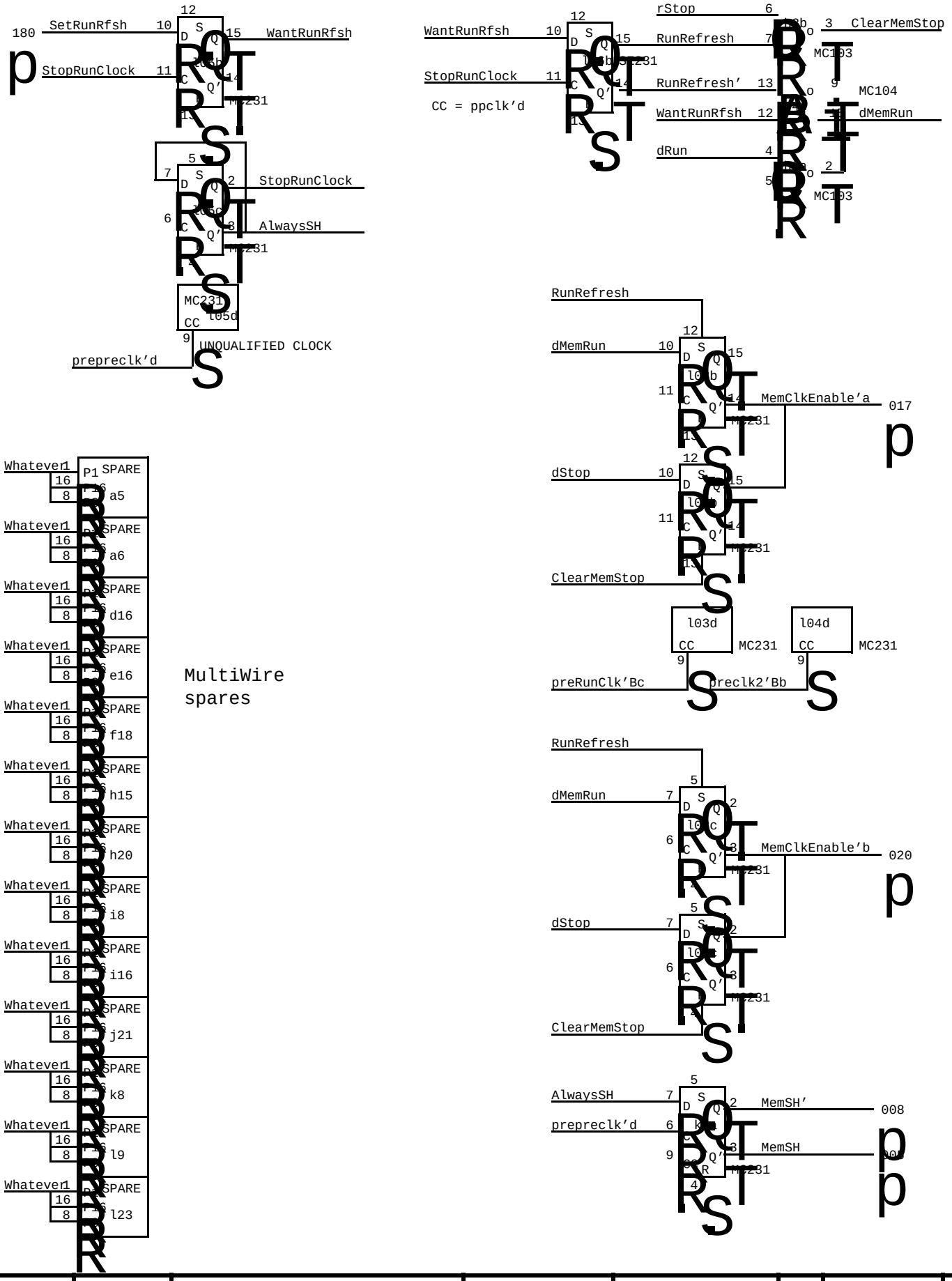


XEROX PARC/CSL	Project Dorado	Midas Interface	File ContA29.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 29



XEROX PARC	Project Dorado	Clock Control	File ContA30.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 30

XEROX PARC	Project Dorado	PreClock generator	File ContA31.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 31



XEROX PARC	Project Dorado	Memory Clock Generator	File ContA32.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 32

	a 181	b 168	c 153	d 137	e 124	f 109	93 g	80 h	64 i	48 j	33 k	20 l	
	IMRHPE BNTGtCT		dCSOut	TWReq9-15		dCSOut		CP INTERFACE	TWReq1-8	RSTK		CLOCK	
1	CPStrobe 161 2	dTLINK	dTLINK	dTLINK	RBMux .4,.12-15	dTLINK	SetMIR	SetMIR	SetMIR	CramClk Phase4 231	CLKEN 231	RAWClk 210	1
2	MIR/BGtCT 2,25 210	DTBMux	DTBMux	DTBMux	DTBMux	CPREG-1	CPREG-1	CLOCK	CONTROL	CLKEN 231	CLKEN 231		2
3	CPREG-0 176	TLINK	TLINK	TLINK	TLINK	TLINK 197		dNCE,OP 32,32C,2	dStpRun 176	MU 000	SCycle 27 MemSH' 30 231	MEMCLKEN 231	3
4	TLINK 145	TLINK 145	TLINK 145	TLINK 145	TLINKX 145 5	TLINK F16 5	MemMap 104	TLinkEn 121	sPh0,d.. 31,27,27,28 104	Stp/run 231	SC(NF) 231	MEMCLKEN 231	4
5		MU 020	MU 030	MU 040	TLINKX bypass 197 5	LINKX 231 5	inverter 195	CLK2 30,30,,,,, 176	bClkEn 210	Err/dSC 117	2,3 231 25	RunRfsh 231	5
6		NOTIFY 162 162		CLK 210	dWTL 109	LINKX 231 5	CTD 231	MU 010	CLK 210	CLK 210	TPCI/CTD 117	FH 231	6
7	MU 360	PREEMPT 162 162		CLK 210	CIAInc 176	MU 330	231	dCTD 158	clk/Freez 210	CLK 210	TPCSclk CIA 117	0,1 231	7
8	SETREADY 104	104	104	104	176	IS 161	TLink 100	BNT 141		CTASK 231		bSC 27,B 211	8
9	READY F00	F00	F00	3*23,D F00	MU 270	NEXT 161	Addr 100	141	MU 170	231	LoadLink 121		9
10	TWREQ 1664	1664	1664	3*23,D 1664	MU 370	PE 121	121	BNxtEn 166	PE>TN 166	CT=NX=0 109	DMD 176	MIDAS 171	10
11	ToPE drivers 104	104	104	3*23,4 104	MU 260	121	102	PE>TN 166	bPE 101	PE=CT 113	CALL 104	DMD 176	11
12	BLINK 176	176	ToPE rcvrs 109	109	3*24, d101	PRECLK 210	PRECLK 212	TPCI 176	TPCAd 1662	1662	TPCI 176	TPCI 176	12
13	4,4,c,4 102	LINK F16	BLINK CIAInc 176	102	102	PRECLK 210	PRECLK 210	pNext 159	TPC 145	TPC 145	TPC 145	TPC 145	13
14	102 5	dBLINK 159	LINK F16	LINK F16	LINK F16	SWITCH 231	MU 350	NEXT 159	TPIM 173	TPIM 173	TPIM 173	TPIM 173	14
15	5,5,5,4 102	FFBR 162 5	dBLINK 159	dBLINK 159	dBLINK 159	SWUp 231	1662		TPCO F16	TPCO F16	TPCO F16	TPCO F16	15
16	100 4	4,4,5,4 103	MU 320			dSWup 1660	STKSEL 231 1,C	MU 340		CIA' 176	CIA' 176	CIA' 176	16
17	100 4	100 4	clk1 4*4 BLINK 176 6,8	T2 3,4, 26,26 176 fg	MU 060	dSWdwn 1660	MU 050	113	CIA ADDER 105	109	CIA 195	clk1 4*28,4,g 176	17
18	bFF 212 1	109 4	CLK 210	CLK 210	IMRH 170 1		RA 159	CIA 195	CLK 210	CLK 210	CIA 195	bTNIA 197	18
19	FB= 161 4	MU 310	CLK 210	JBr 162 5	IMRH 170 1	Hold 211	bJCN 212 1	RA 159	TNIA 0-3 159	CLK/SW 212	RA 159	RA 159	19
20	109 4	bFF 212 1	DoCBr 121 5	RW... 161 3	MU 070	RptCur 1660	bJCN 212 1		BNPC 158	bTNIA 197	BNPC 158	BNPC 158	20
21	102 4	FC= 161 4	DoCBr 121 5 d	3,3,5,3 102	RETURN 210 3	MU 300	BNPC 158	bTNIA 197	bTNIA 159		100	Midas 4*28 197 fh	21
22	bFF 212 1	bFF 212 1	DoCBr 5 PreEmp 1662	LocalBr 3,5 210	IFUNext 210 3	CBr/LJ 210 3	TNIA 159	8 121	TNIA 101	13 121	105	Midas 164	22
23	FF2,3 231 1	FF6,7 231 1	JCN0,1 231 1	JCN2or3 231 1	IMRH,BLK 231 1	CBr 211 3	6 121	7 121	9 TNIA 121	12 121	14 121		23
24	FF0,1 231 1	FF4,5 231 1	JCN4,5 231 1	JCN2,3 231 1	JCN6,7 231 1	FFok 211 3	4 121	5 121	10 121	11 121	15 121	Midas 102	24
	a 11	b 26	c 39	d 55	e 70	f 86	99 g	114 h	129 i	143 j	159 k	174 l	
	NEXT BLOCK	HOLD'	FFOK	dMIR	FF0-3 dMIR	BrCond	FF4-7	TNIA0-7	BNPC0-2	IFADR	TNIA/BNPC	BrCond	SW DMUX

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