

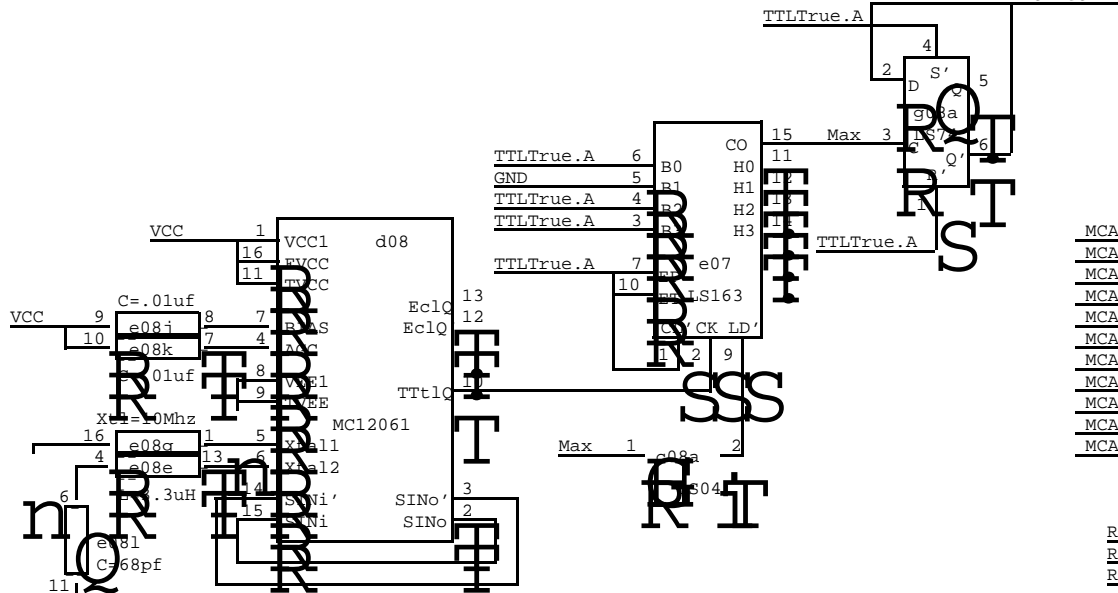
D O R A D O S C H E M A T I C S

B a s e B o a r d

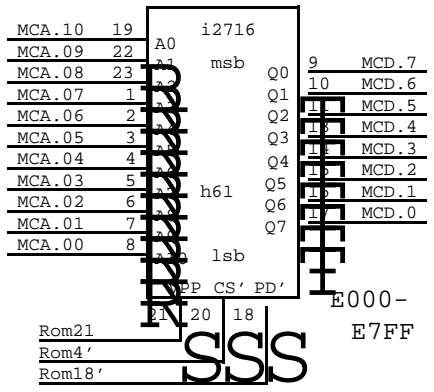
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(1 MHz 50% duty)
MCPreClk



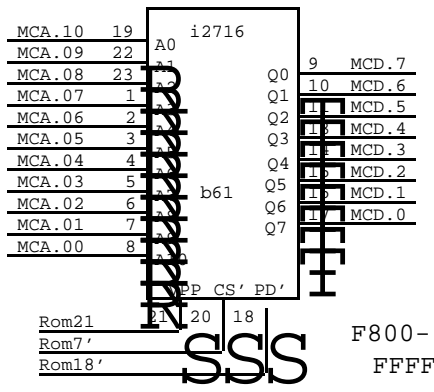
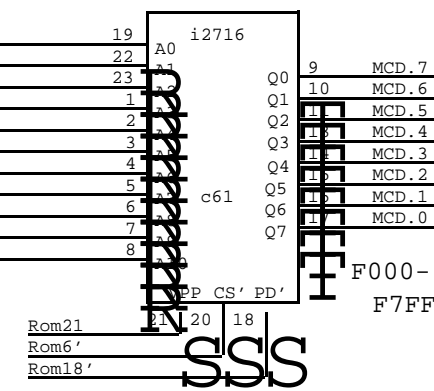
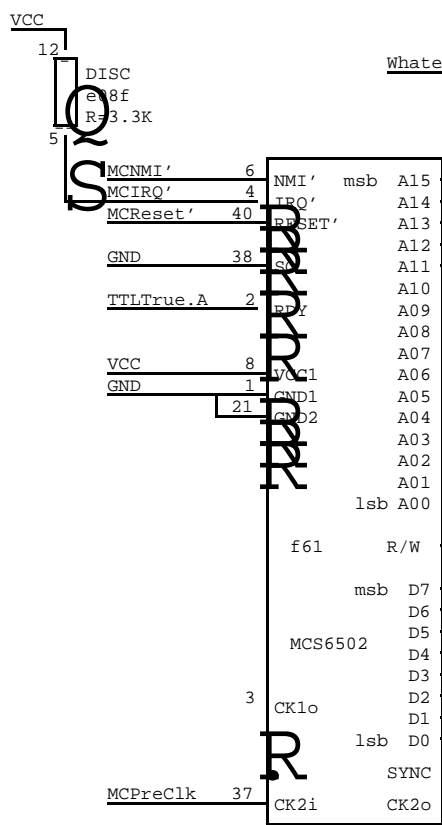
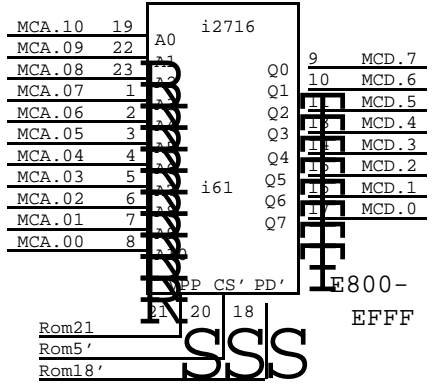
Other EPROMS
C000 to DFFF
on Page 19.

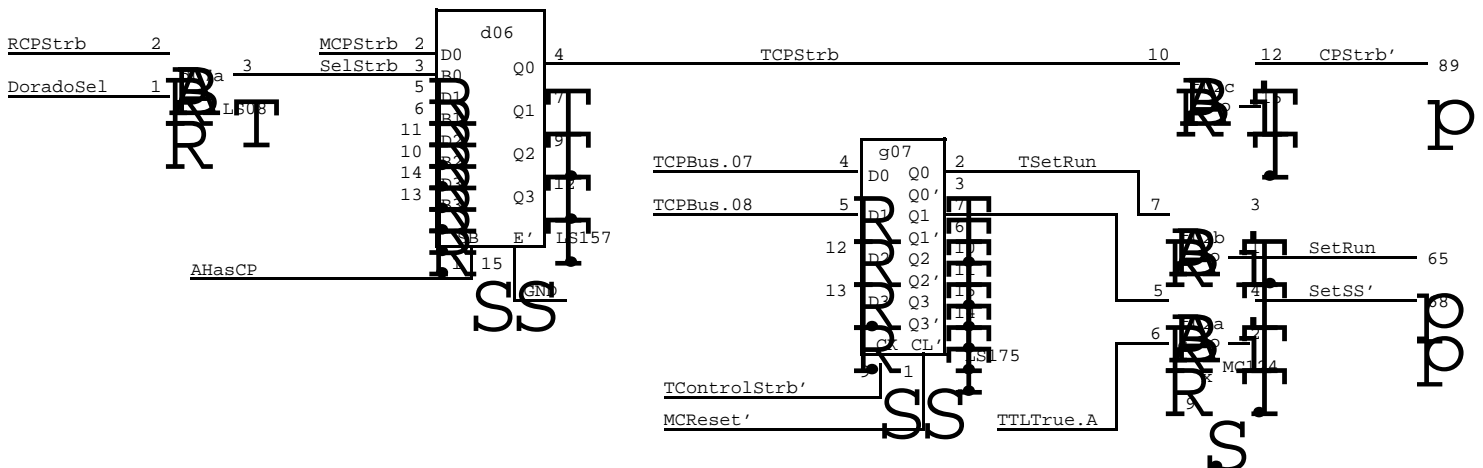
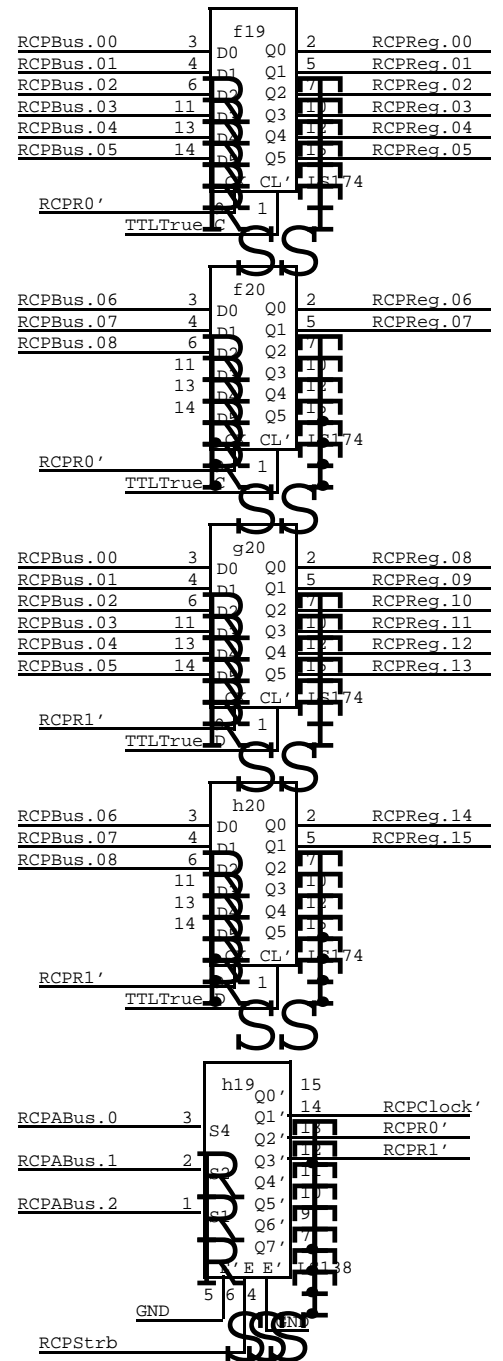
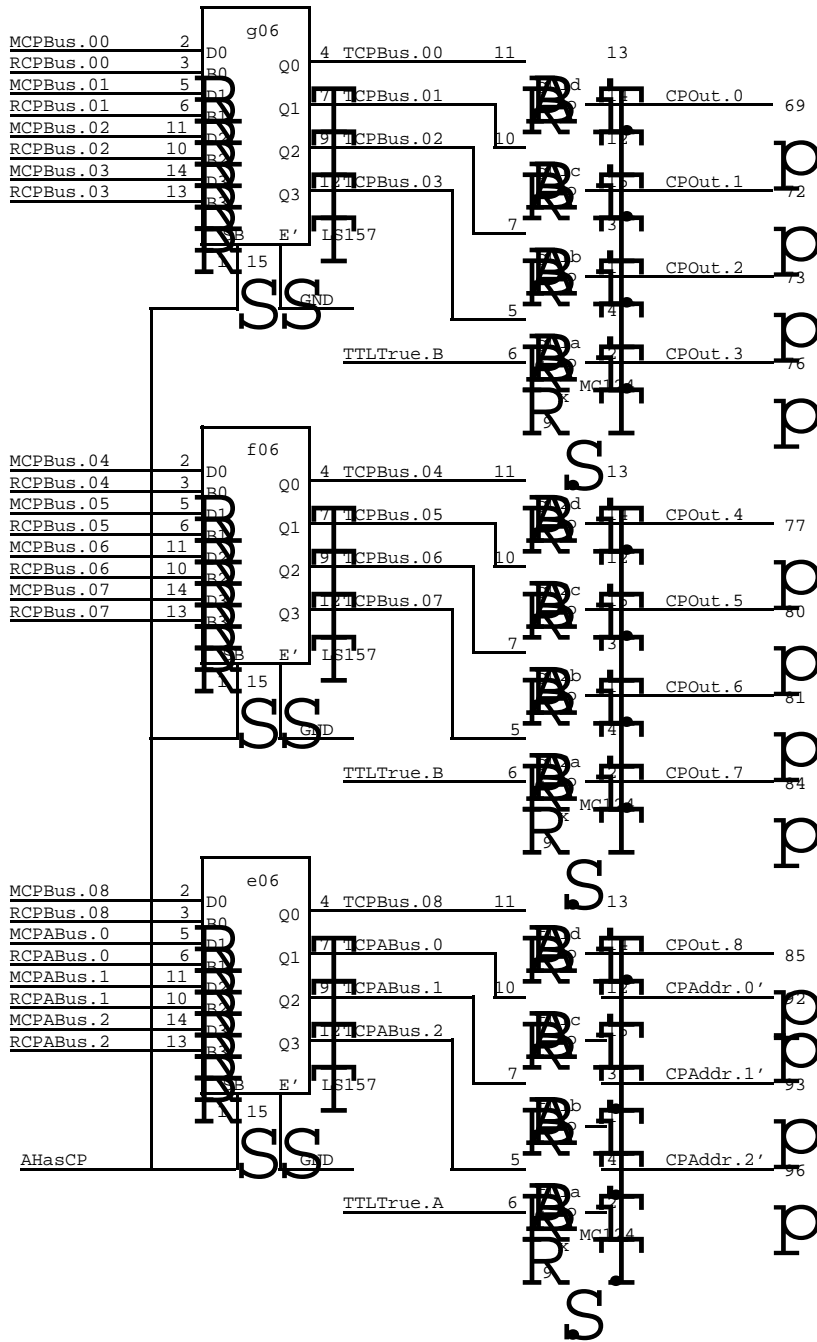


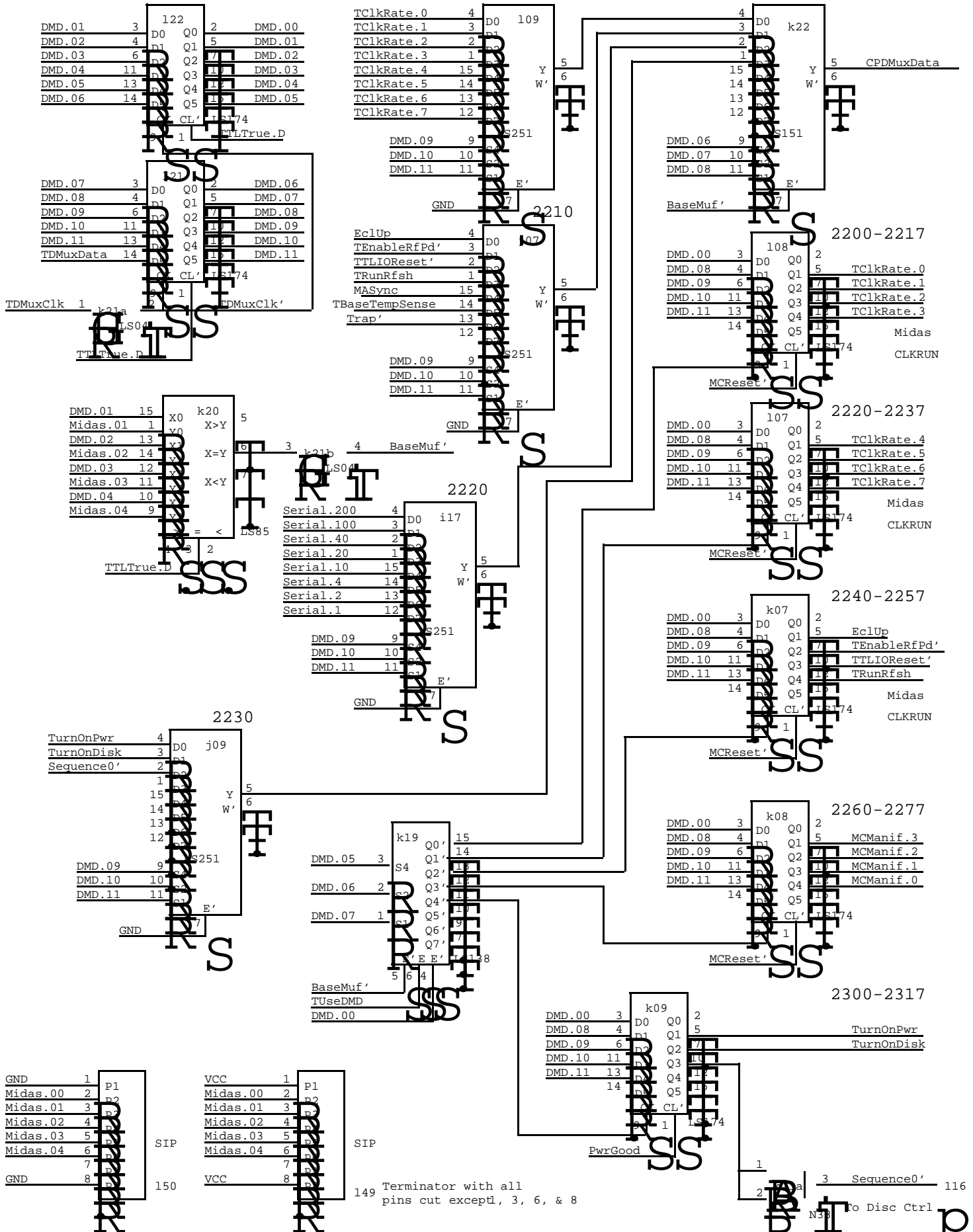
EPROM JUMPERS

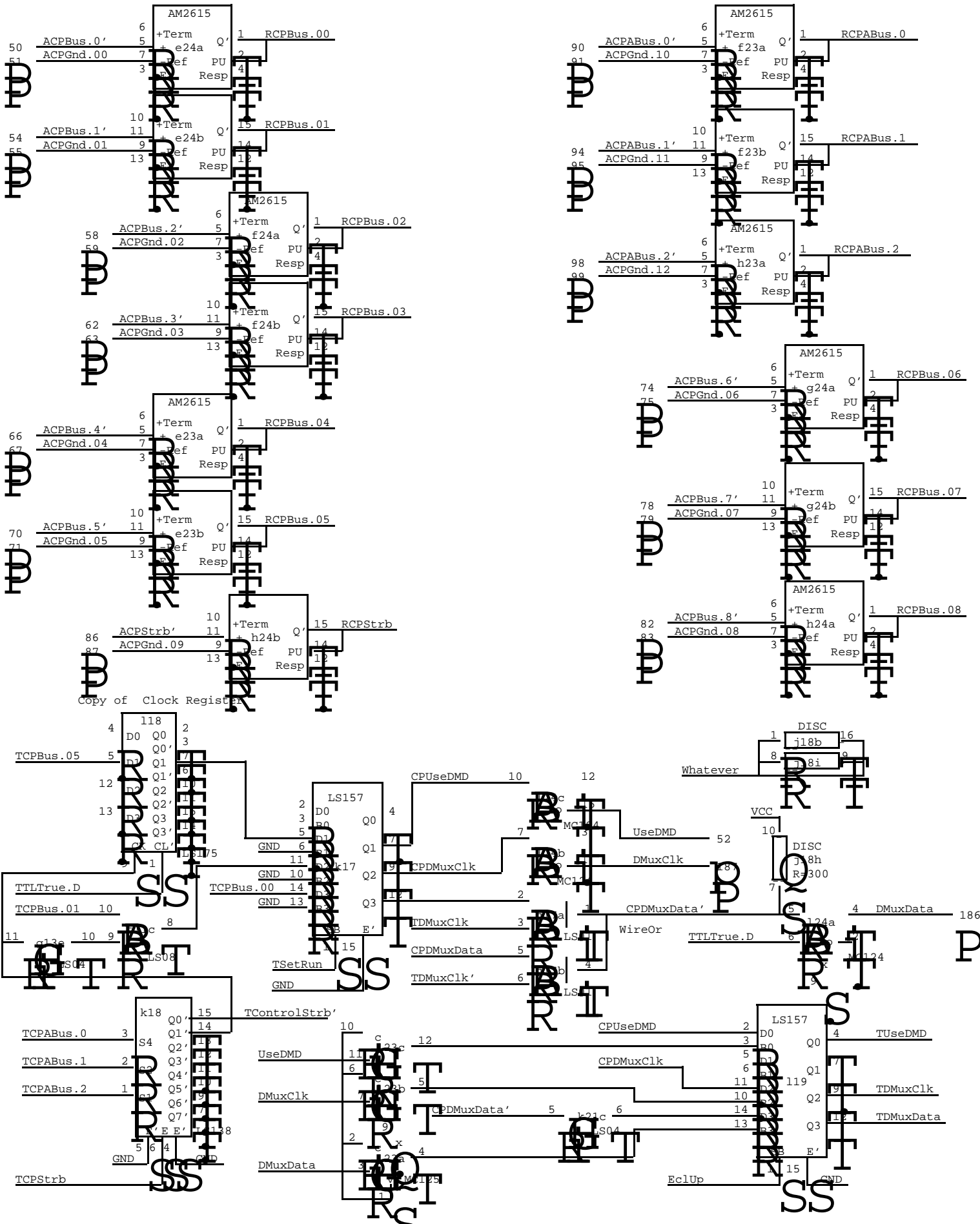
RSA.3 for expansion EPROMS

MCA.14	1	P1	P16	16	RSA.3
MCA.13	2	P2	JMP P15	15	RSA.2
MCA.12	3	P3	JMP P14	14	RSA.1
MCA.11	4	P4	JMP P13	13	RSA.0
VCC	5	P5	JMP P12	12	Rom21
GND	6	P6	JMP P11	11	Rom18'
Whatever	8	P8	JMP P9	9	



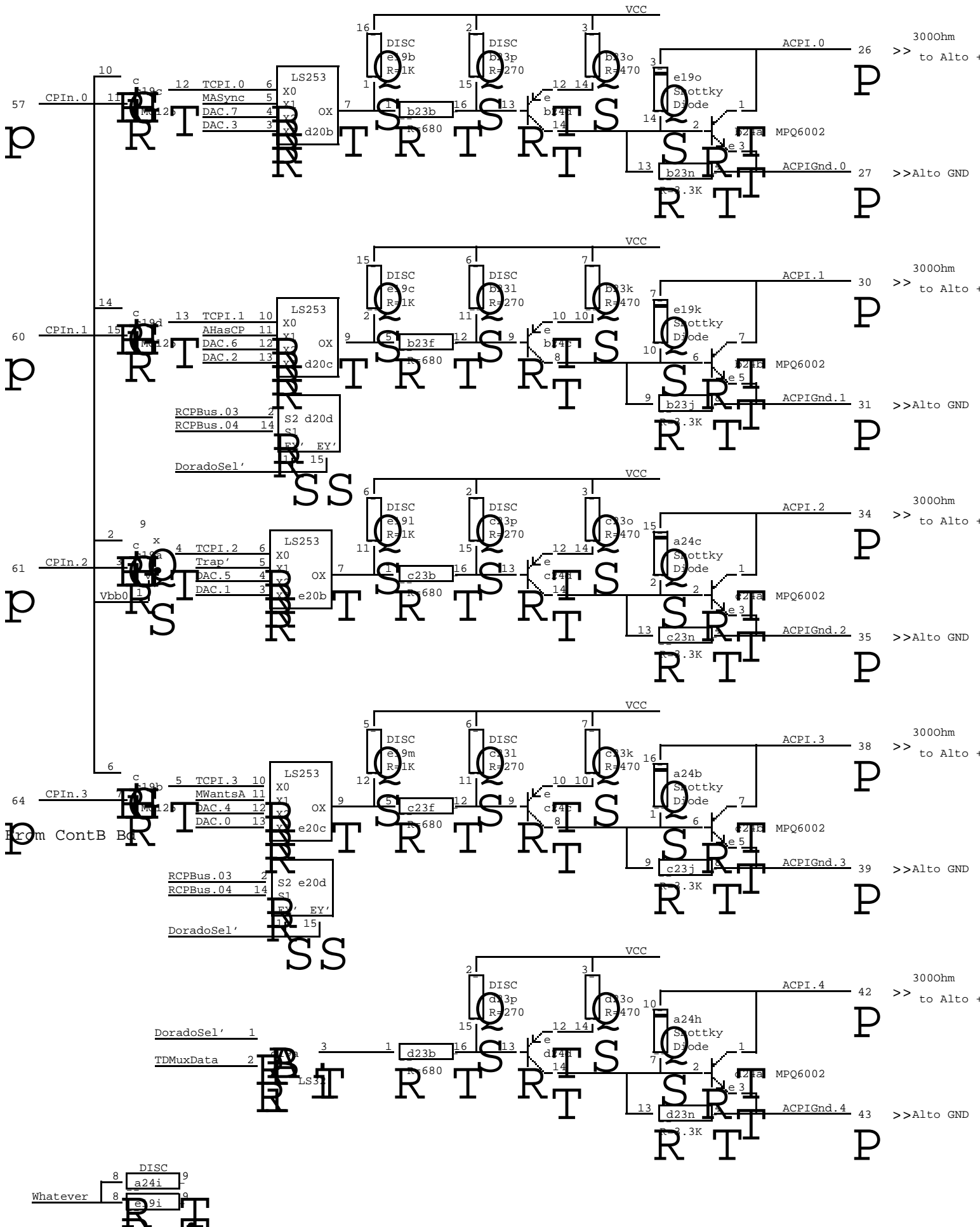




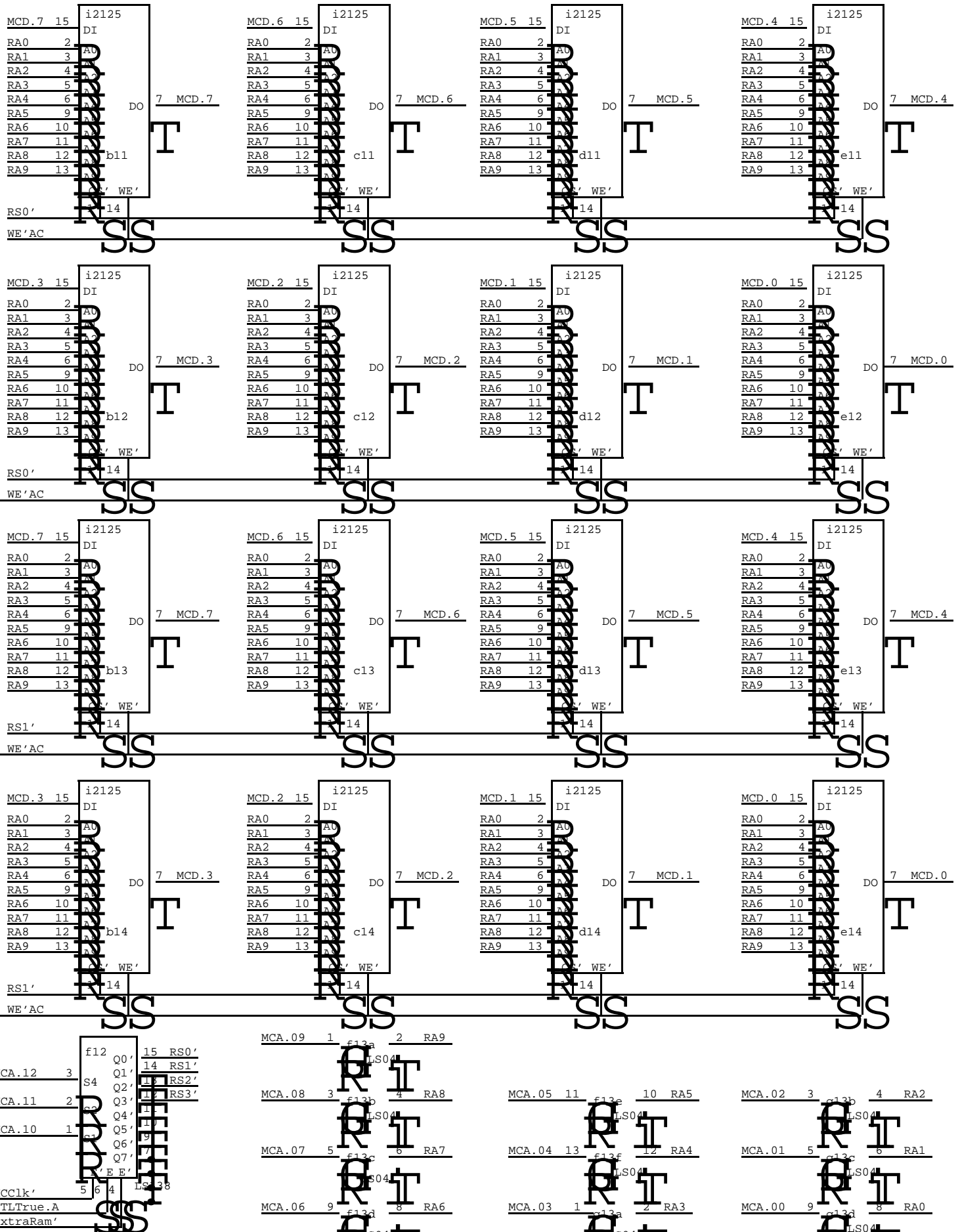


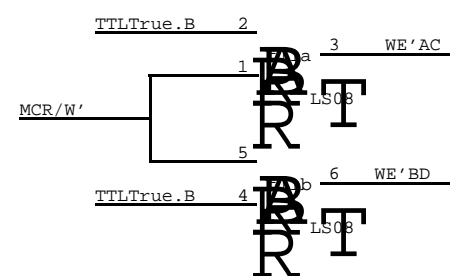
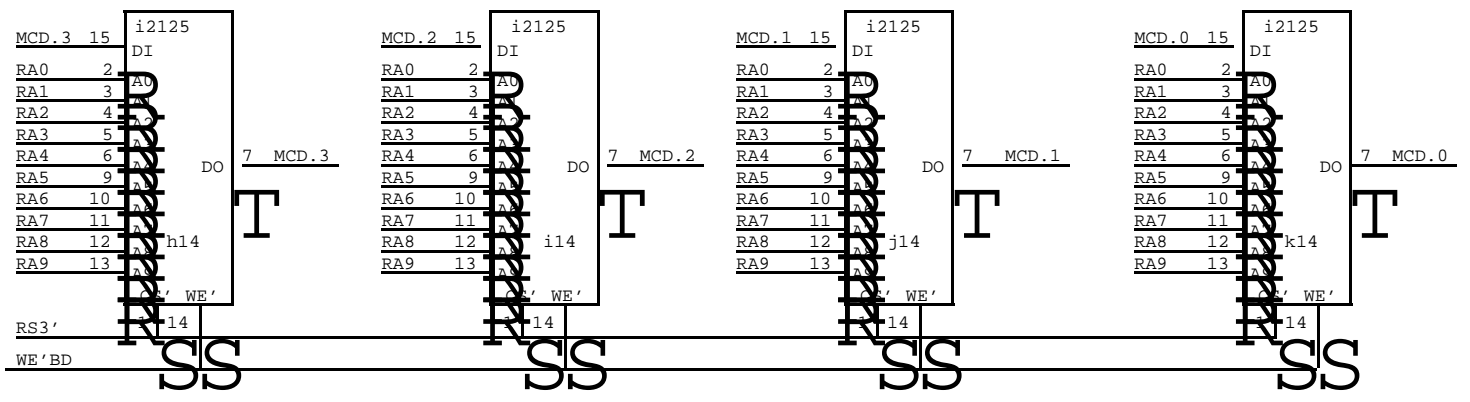
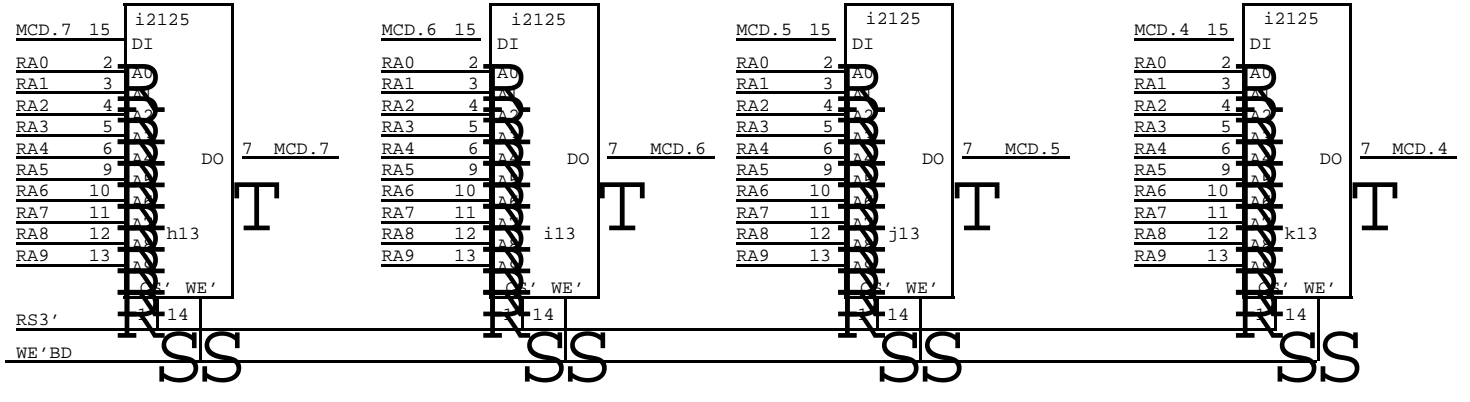
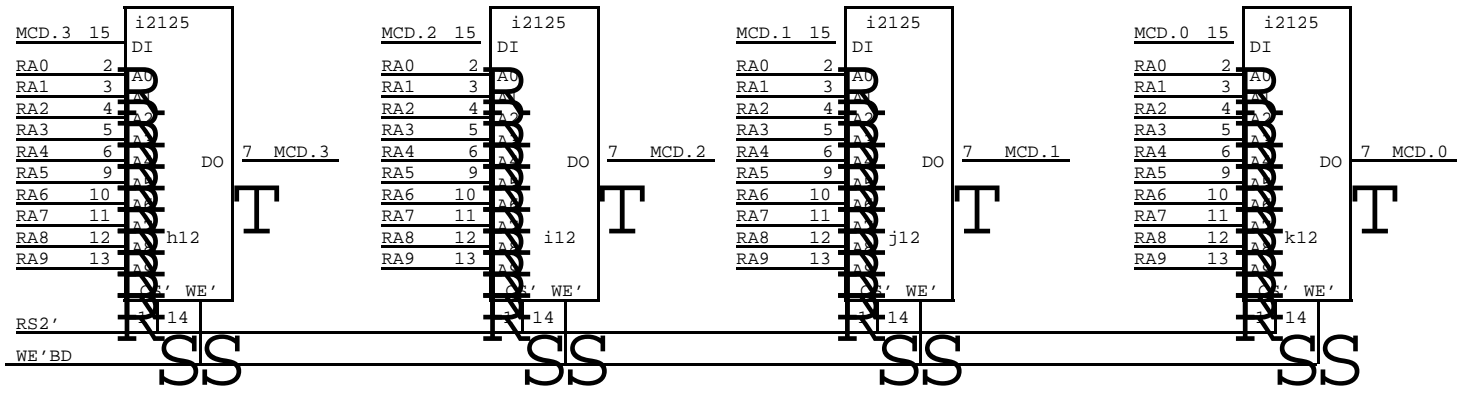
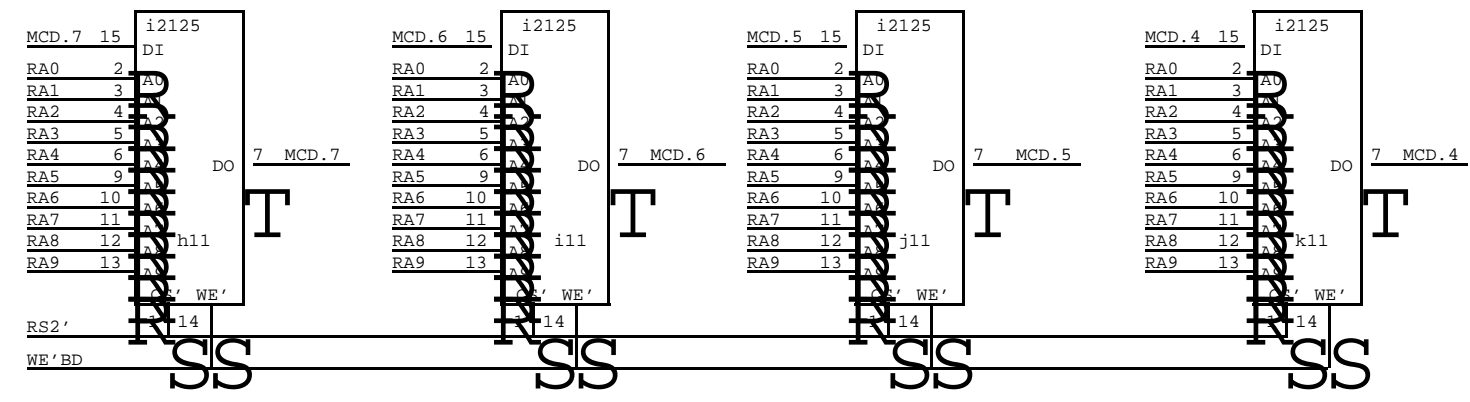
Copy of Clock Register

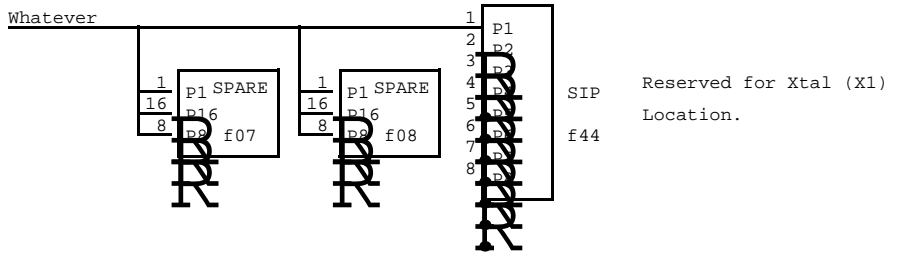
XEROX CSL	Project Dorado	Dorado Base Board Alto Control Bus Receivers	File Basebd05.sil	Designer McCreight	Rev Am	Date 7/25/79	Page 05
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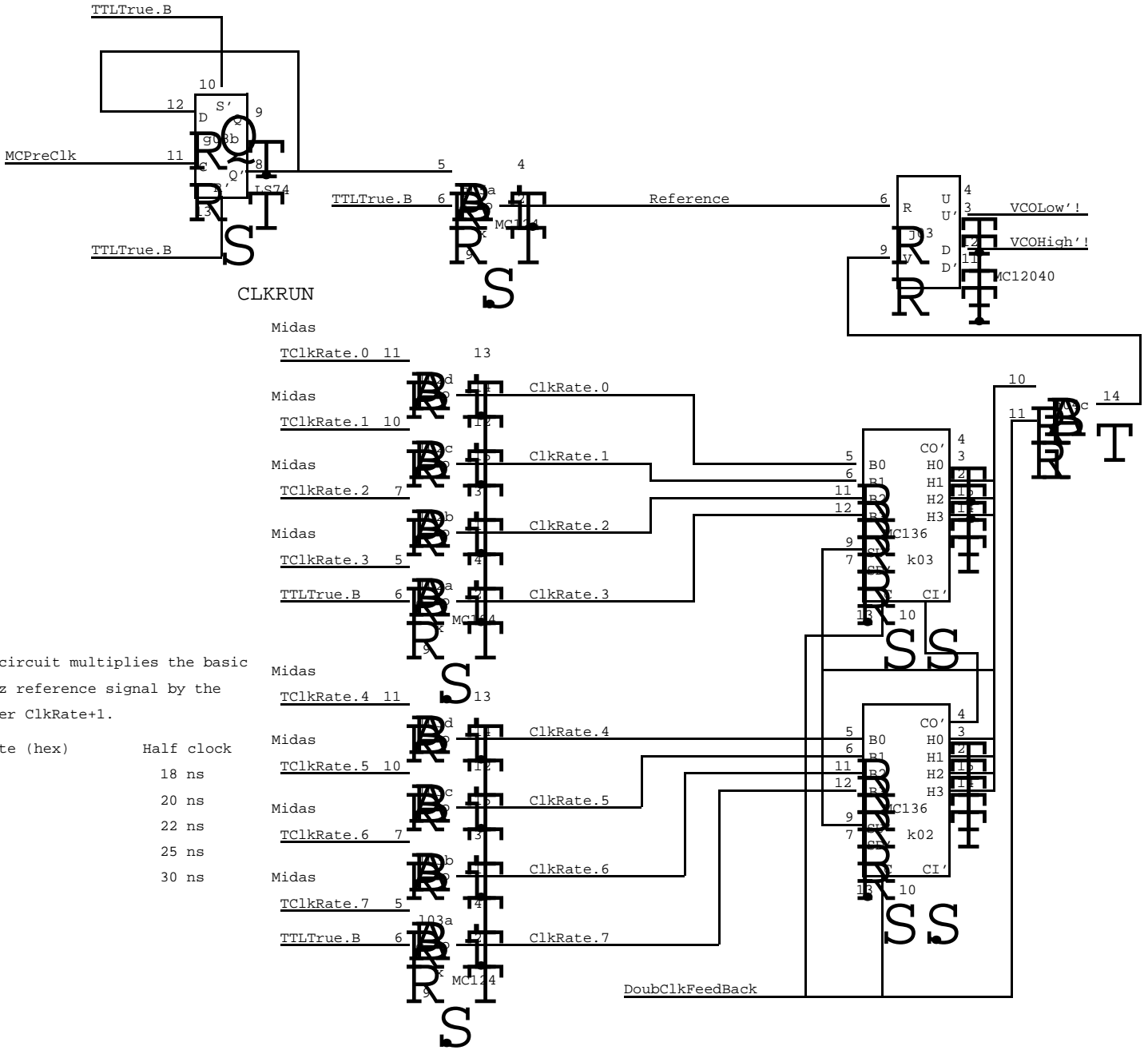
RAMS ARE OPTIONAL







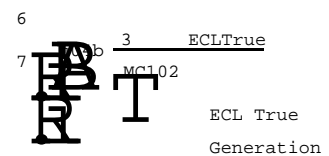
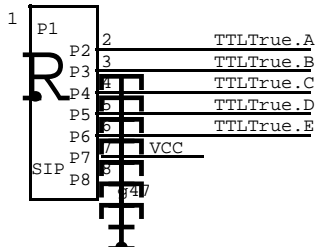
SIP Reserved for Xtal (X1) Location.

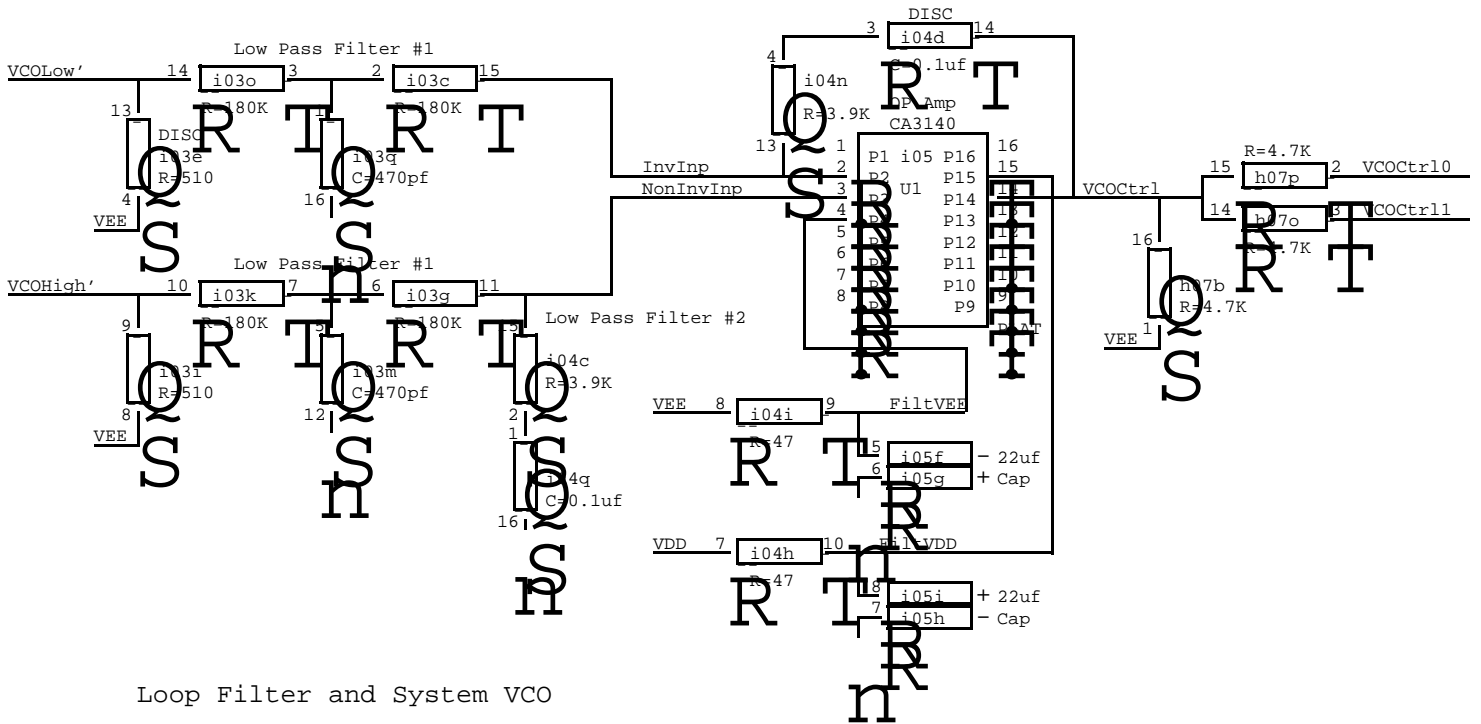
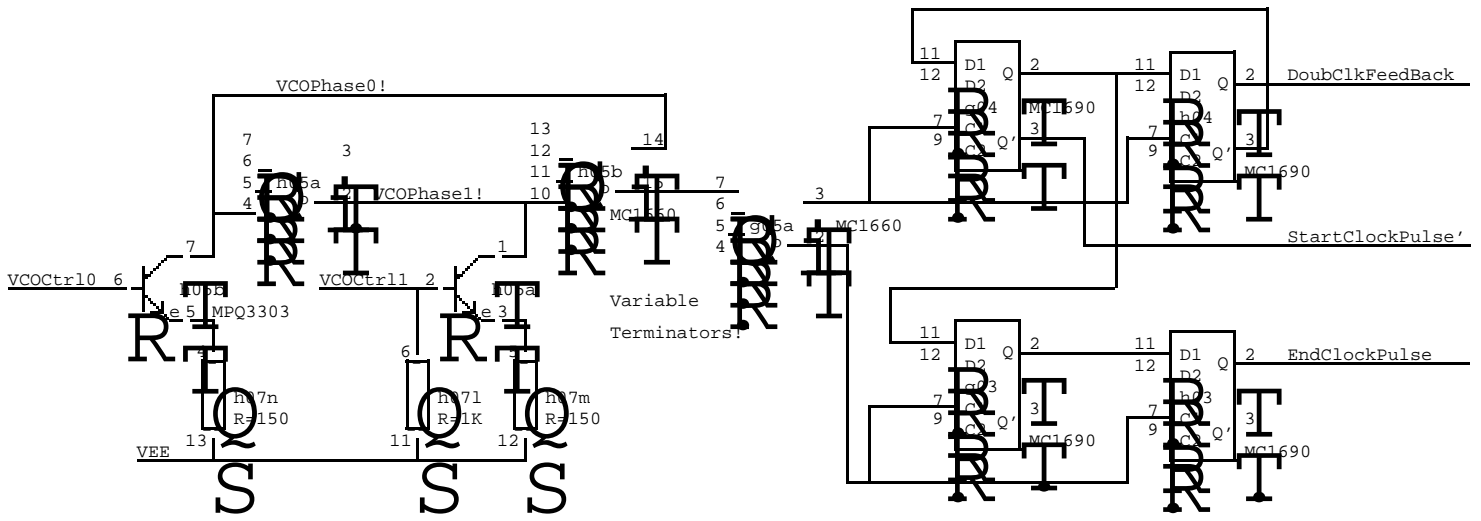


This circuit multiplies the basic 490kHz reference signal by the integer ClkRate+1.

ClkRate (hex)	Half clock
70	18 ns
66	20 ns
5D	22 ns
52	25 ns
44	30 ns

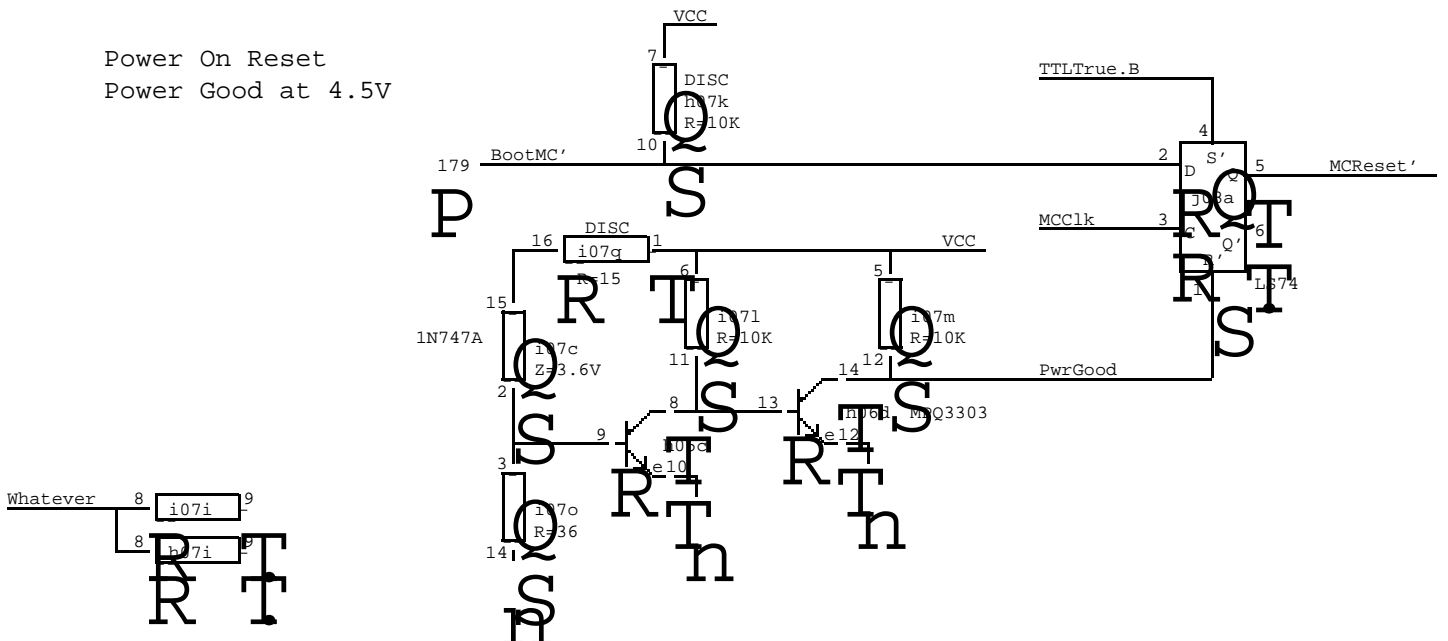
TTL True Generation

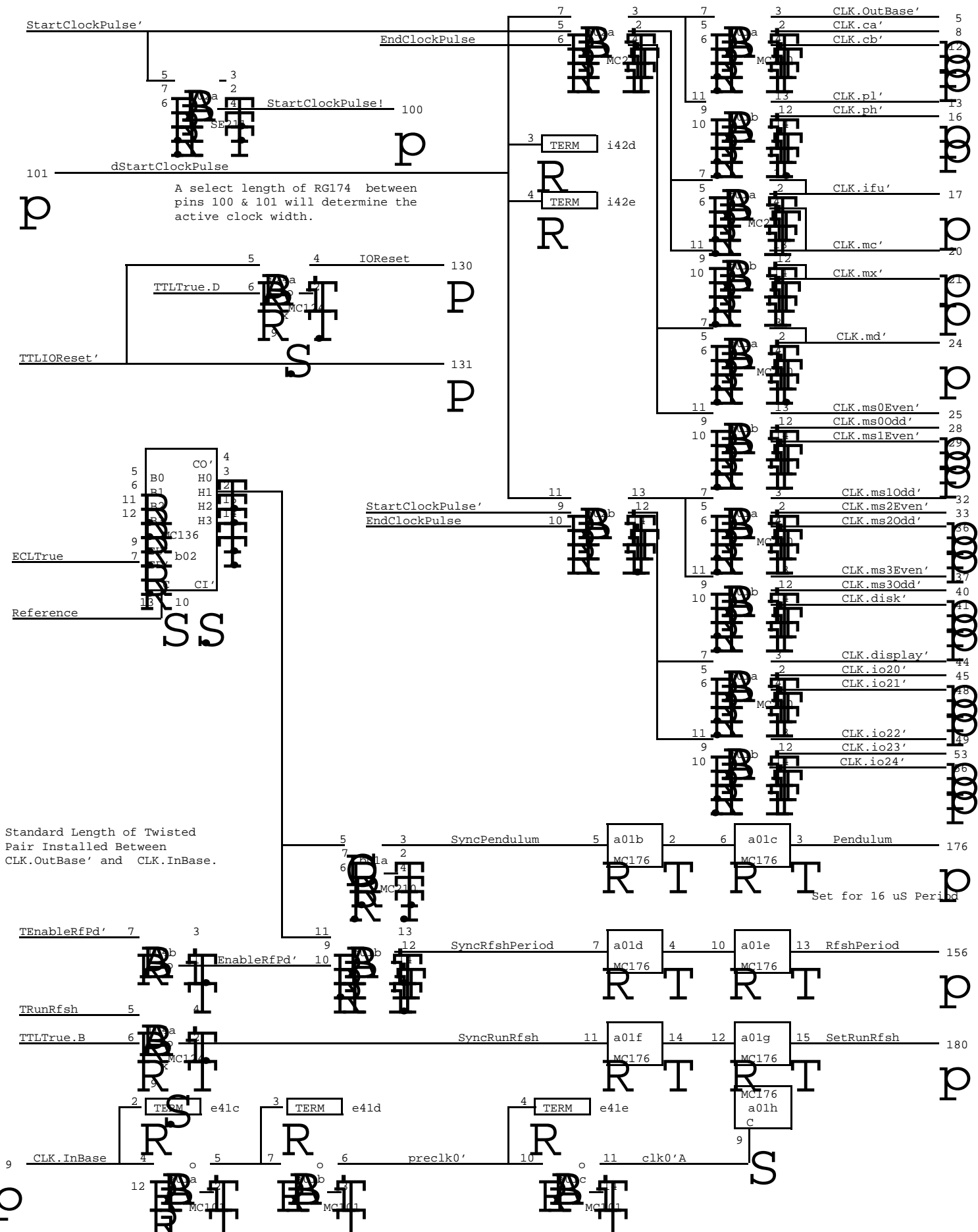




Loop Filter and System VCO

Power On Reset
Power Good at 4.5V





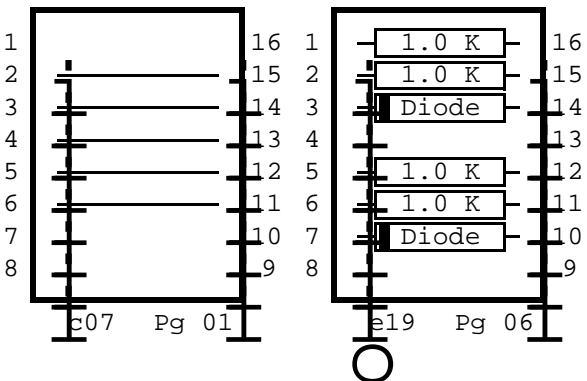
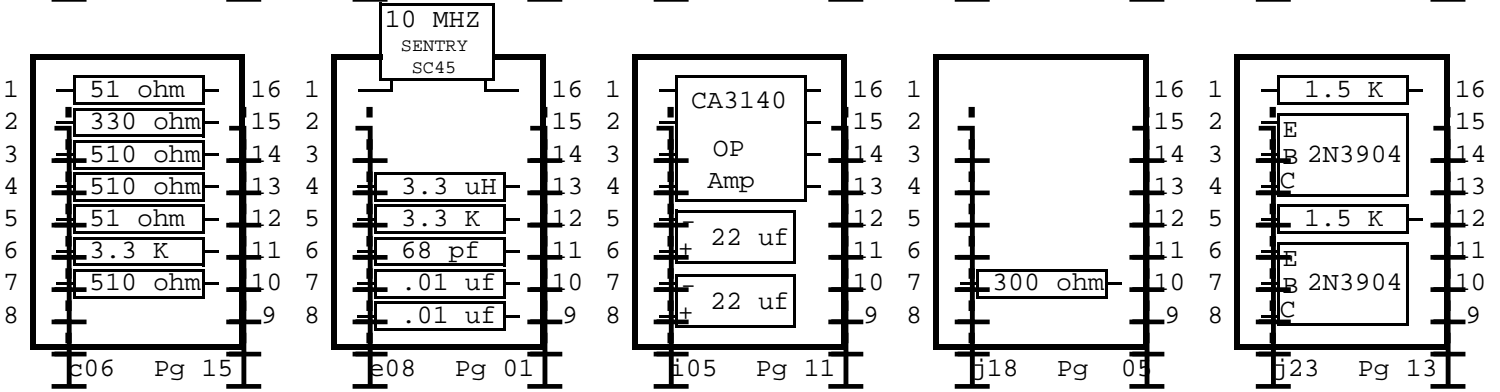
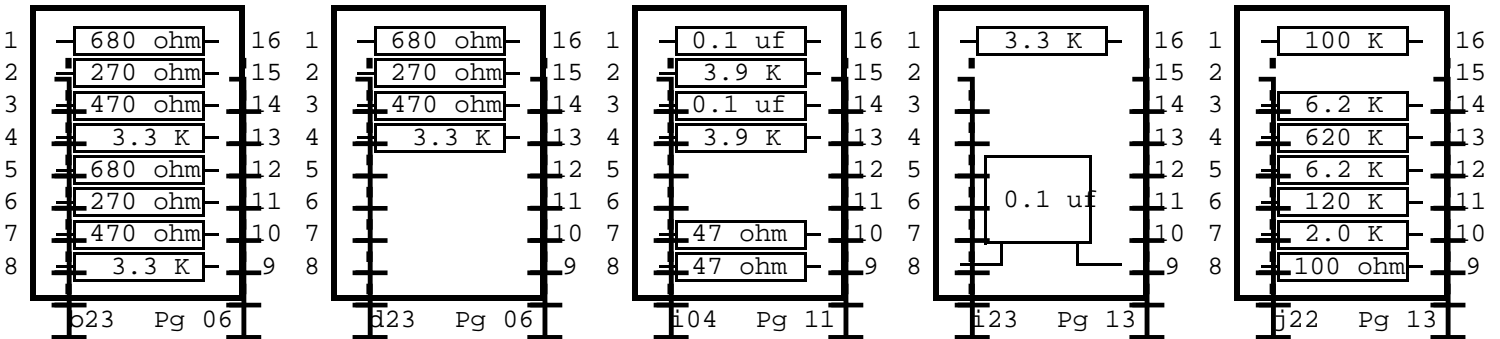
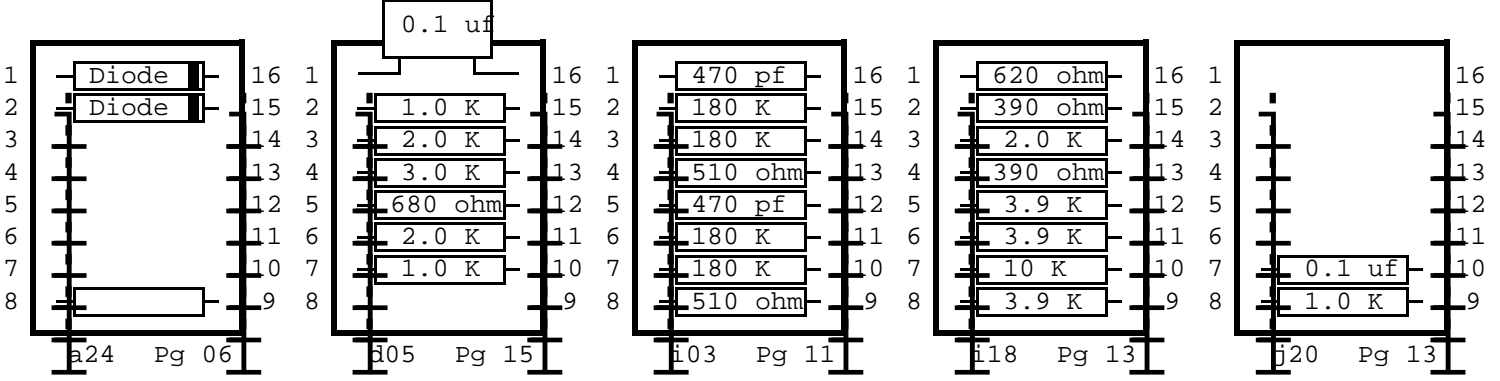
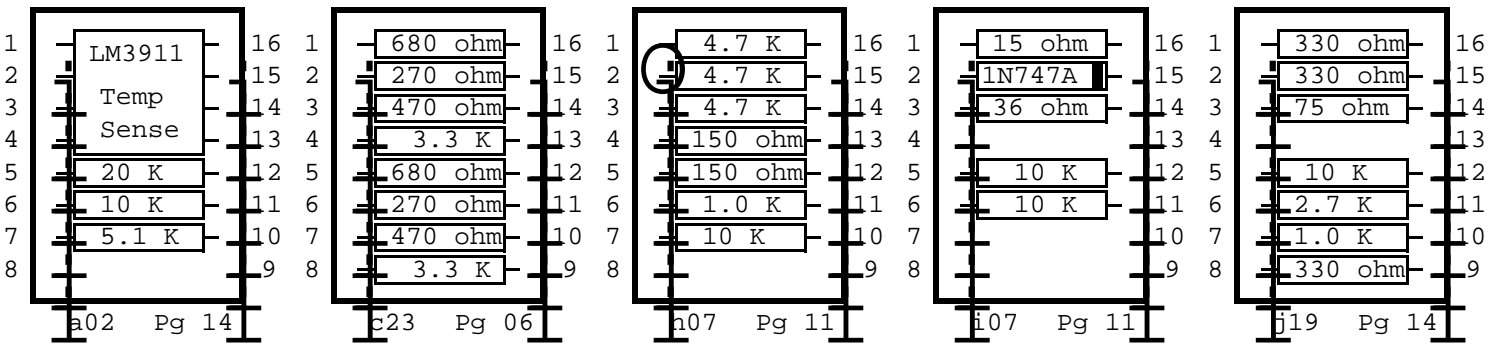
A select length of RG174 between pins 100 & 101 will determine the active clock width.

Standard Length of Twisted Pair Installed Between CLK.OutBase' and CLK.InBase.

Set for 16 uS Period

XEROX CSL	Project Dorado	Clock Generator Backpanel distributor	File BaseBd12.sil	Designer McCreight	Rev Am	Date 7/25/79	Page 12
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	a 181	b 168	c 153	d 137	e 124	f 109	g 93	h 80	i 64	j 48	k 33	l 20	
1	RunRfsh Pendulum 176 14	Pendulum RfshPeriod 210 14	BootNO 19,b,c,d Ls01 19		CLK.INBase 14,14,14,c 101	CPBus 124 3	CPBus 124 3	CLK.xx 210 14	CLK.xx 210 14	CLK.xx 210 14	CLK.xx 210 14	CLK.xx 210 14	1
2	BaseTemp Sense plat 17	Pendulum 136 14				CPBus 3,3,3,19 124	CPBus 124 3		StClkPulse 14,b SE211	Clk delay 210 14	ClkRate 136 11	ClkRate.0 to .3 124 11	2
3		b60 D800-D8FF	c60 D000-D7FF		e60 C800-C8FF	f60 C000-C7FF		EndClockPulse 1690 12	Low pass filter 1 12	VCO Contr 12040 11	ClkRate 136 11	ClkRate.4 to .7 124 11	3
4	24 Pins i2716	24 Pins i2716	24 Pins i2716	24 Pins i2716	24 Pins i2716	24 Pins i2716	24 Pins i2716	StartClock Pulse' 1690 12	DoubClk FeedBack 1690 12	Low pass filter 2 12	ECL True a,11,11,d 102	RunRfsh 14,14,c,d 124	4
5			KbData MPQ6002 PLAT 19	KbData discretes PLAT 19				VCO 12,b 1660 12	Op-amp CA3140 12	Reference 11,b,c,d 124			5
6			KbData discretes PLAT 19		TCP LS157 3	BUS LS157 3			PwrGood' array 12				6
7			EPROMS Jmps Plat 1	SelStrb 3,b,c,d LS08 3	Max LS163 1	Reserve For Xtal Location 1	TsetRun TsetSS LS175 3	Transistor discretes 12	PwrGood' Discretes 12	Muffler 2210- 2217 LS251 4	manifold 2240- 2257 LS174 4	manifold 2220- 2237 LS174 4	7
8			1,1,1,19,e LS04	uProc Clk 12061 1	Clk Discretes 1	Reserve For Xtal Location 1	MCPrecClk 1,11 LS74	TBaseTemp 17,17,19,d 125		MCRreset' 12,b LS74	manifold 2260- 2277 LS174 4	manifold 2200- 2217 LS174 4	8
9	EPROM b61 F800-FFFF	EPROM c61 F000-F7FF	MicroComputer f61 40 pins			EPROM h61 E000-E7FF	EPROM i61 E800-EFFF			Muffler 2230- 2237 LS251 4	manifold 2300- 2317 LS174 4	Muffler 2200- 2207 LS251 4	9
10	24 Pins i2716	24 Pins i2716		6502			24 Pins i2716	24 Pins i2716					10
11		Bit 7	6	5	4	WE'AC,BD 9,9,5,17 LS08	ROM0'-7' LS138 1	Bit 7	6	5	4		11
12		3	2 ^{1st}	2K ¹	0	RS0'-3' LS138 8		3	2	1 2 nd	2K	0	12
13		7 i2125	RAMS 6	RAMS 5	4 i2125	RA9-4 LS04 8	RA3-0 8,8,8,8,5,5 LS04	7 i2125	RAMS 6	RAMS 5	4 i2125		13
14		3	2	1	0	ExtraRam LS139 2	RAM0'-3' LS138 2	3	2	1	0		14
15		500 16	c62		400 16			580 16	i62		480 16	162	15
16		6532 40 pins	2		6532 40 pins	2		6532 40 pins	2		6532 40 pins	2	16
17									Muffler 2220- 2227 LS251 2	CPDMuxData 5,5,c,d LS01	Midas LS157 5		17
18		BaseAttn' 10,b,c,d LS00						TempRef CA3140 17	CV Discretes 15	Pullups Plat	Stuff LS138 4 LS175 5		18
19	DoradoSel LS251 10	BaseAttn 10,10,c,d LS04	TCPI.x 125 6	TDMuxData 6,b,c,d LS32	Pullups PLAT 6	LS174 3	RCPClock' LS138 3	CVDD CVTT CA3140	Discretes TurnOnPwr LED 17		LS138 4 LS157 5		19
20		Dorado Sel	DoradoSel	TACPI.x LS253 6	TACPI.x LS253 6	CAB LS174 3	MUX LS174 3	CVEE VrefBuf CA3140 15	CI Low Pass PLAT 15		LS85 4 17	TurnOff2v MPQ6002	20
21					600 16	f63	Watchdog Timer 14521 9	Serial# LS85 10	DACOUT CVCC A3140	CI op-amp CA3140 15	4,4,5,d 14,f LS04	DMD Gen LS174 4	21
22					6532 40 pins	9	Watchdog Timer LS74 9	0-377 LS85 10	DAC 8BC 15	Discretes 15	MUF MUX 74151 4	LS174 4	22
23		ACPI0 & 1 Discretes 6	ACPI2 & 3 Discretes 6	ACPI4 Discretes 6	RCPBus04 RCPBus05 AM2615 5	RCPBus.1 RCPBus.0 AM2615 5	Watchdog Timer 7486 9	RCPBus.2 AM2615 5	Discretes 15	PwrRef 2N3904 PLAT 15	LED,Seq0, Relay Dvr N38 17	5,5,5,d 125	23
24	Schottky Diodes Plat	ACPI0 & 1 MPQ6002 Kistor 6	ACPI2 & 3 MPQ6002 Kistor 6	ACPI4 MPQ6002 Kistor 6	RCBus00 RCPBus01 AM2615 5	RCPBus02 RCPBus03 AM2615 5	RCPBus06 RCPBus07 AM2615 5	RCPBus08 RCPStrb AM2615 5	IOreset 4.b.c.d 124	CITT CIEE CD4051 15	CIDD CICC CD4051 15	5,5,5,d 24	24



NOTES:

All diodes are HP 5082-2835 unless otherwise noted
 Locations b60, c60, e60, f60, b61, c61, h61, and i61 are EPROMS and must be programmed
 Location k22 can use a 74151 instead of a 741S151
 Location l49 must be loaded with a SIP having pins 2, 4