L A R K

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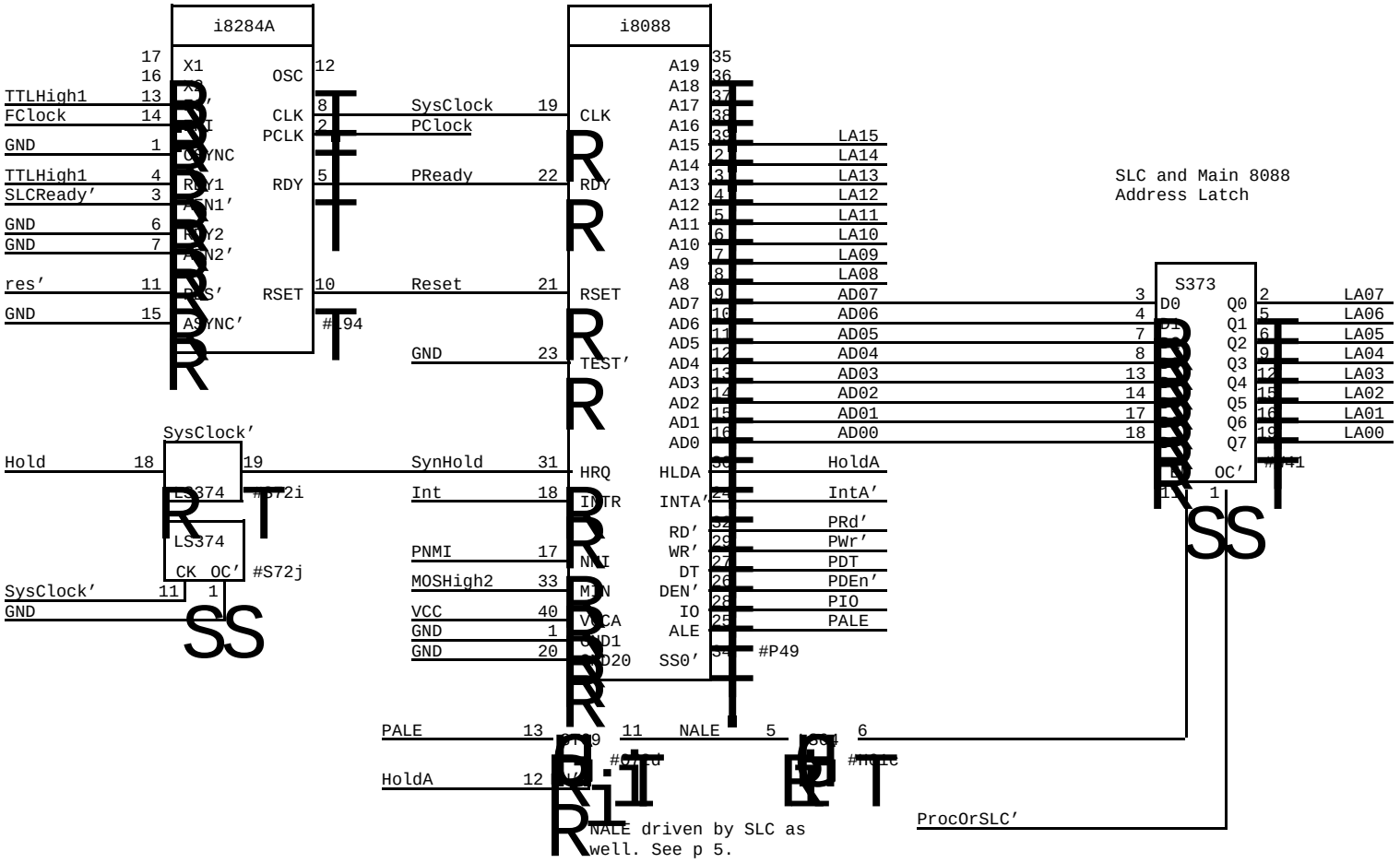
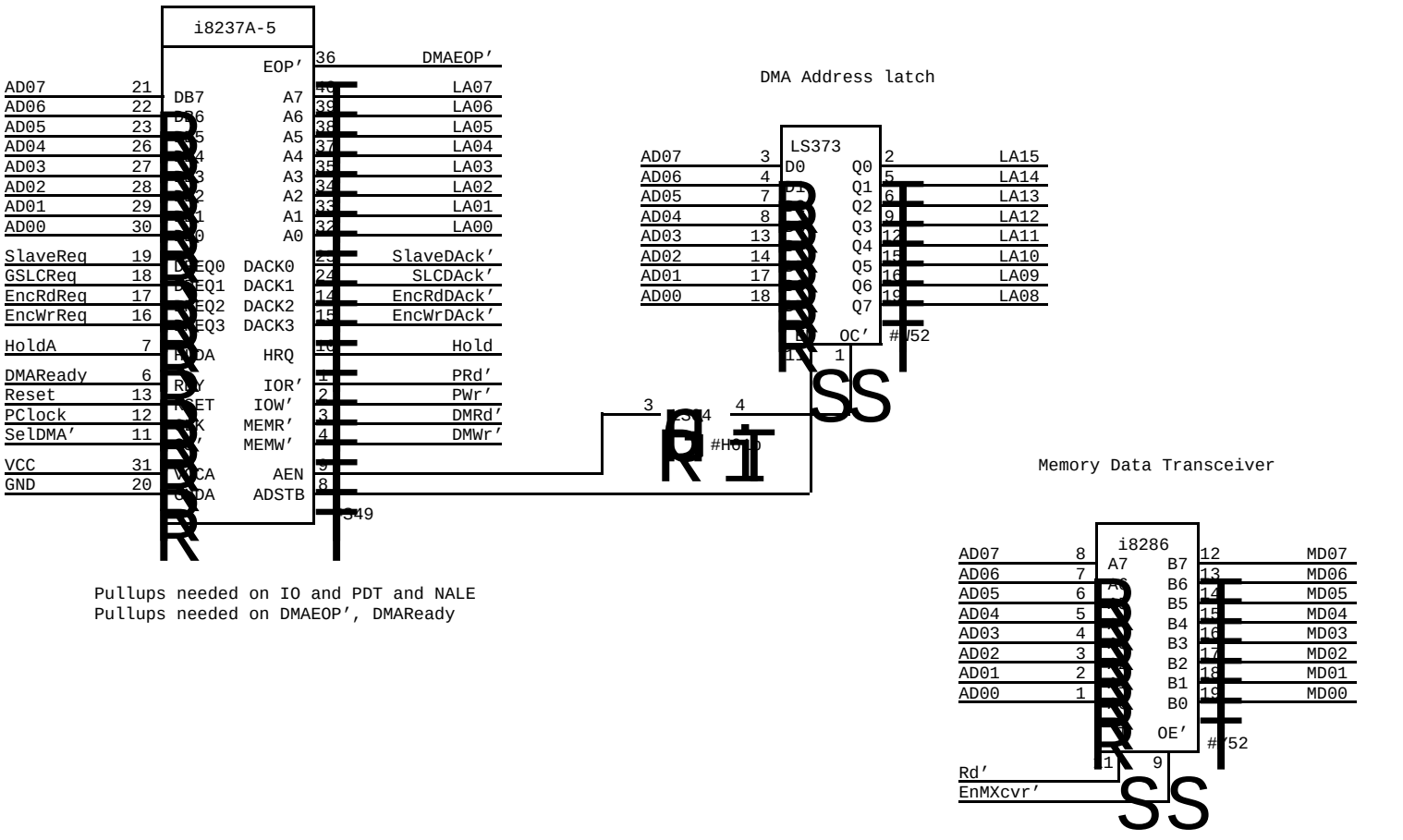
REFERENCE FIGS

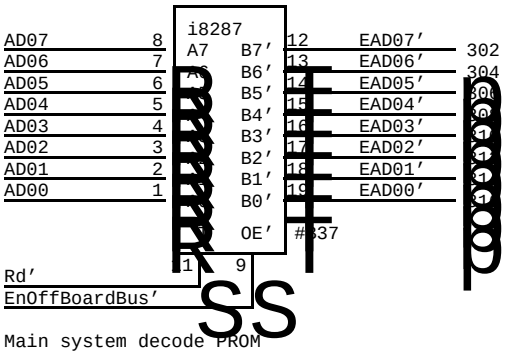
See Page 20



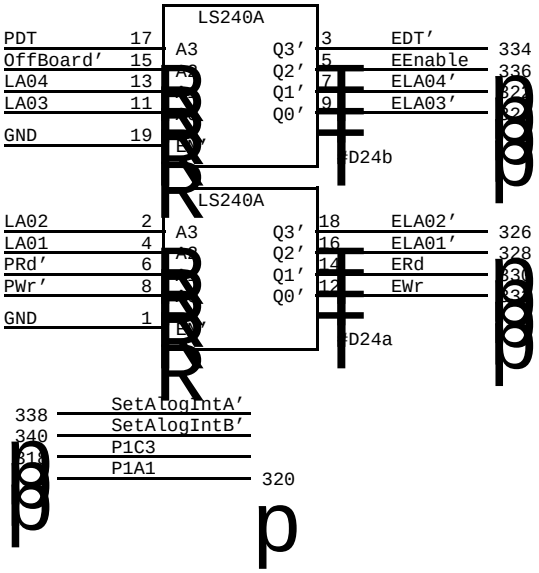


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	Main 8088	ETT01.sil	S. Ornstein L. Stewart	Ai	6/01/82	01

Off board data bus transceiver

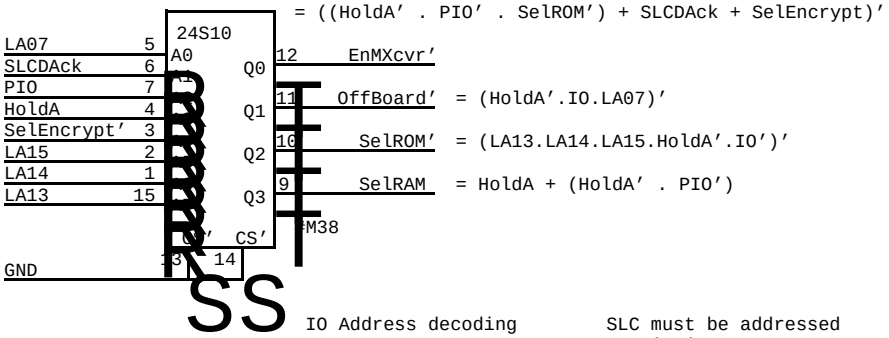


Off board control signal drivers



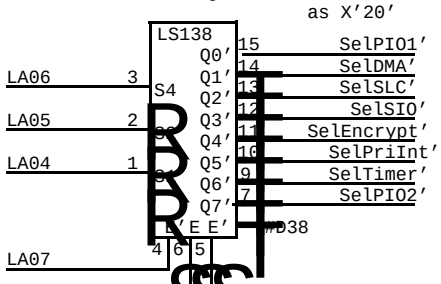
Main system decode PROM

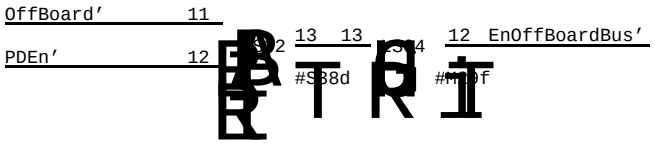
= ((HoldA′ . PIO′ . SelROM′) + SLCDAck + SelEncrypt)′

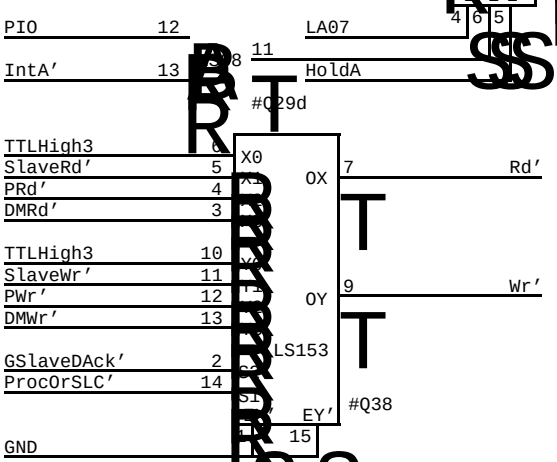


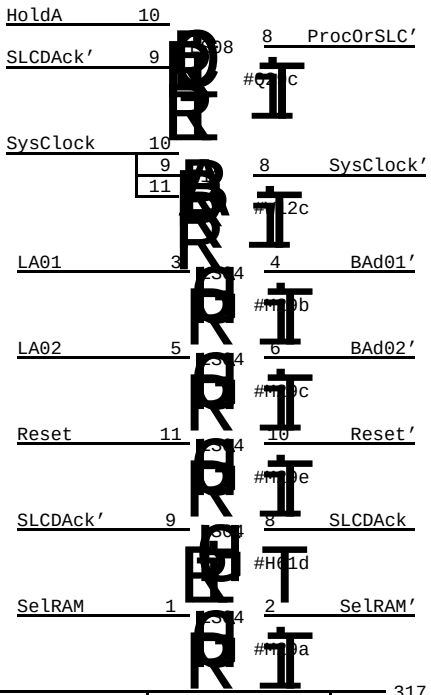
IO Address decoding

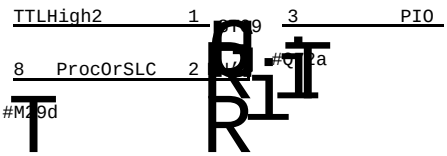
SLC must be addressed as X′20′



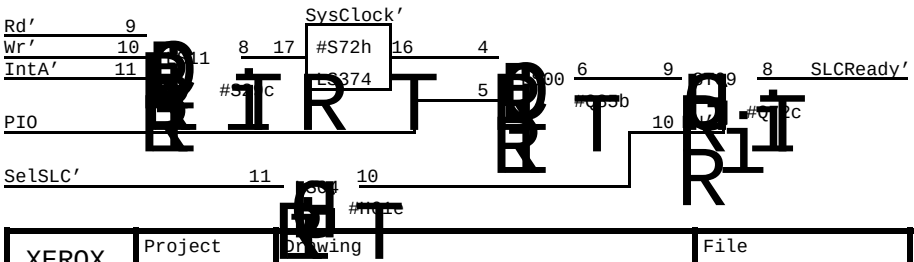


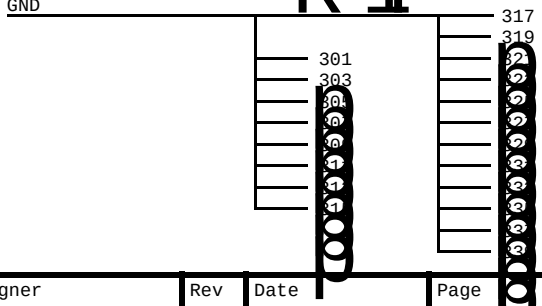






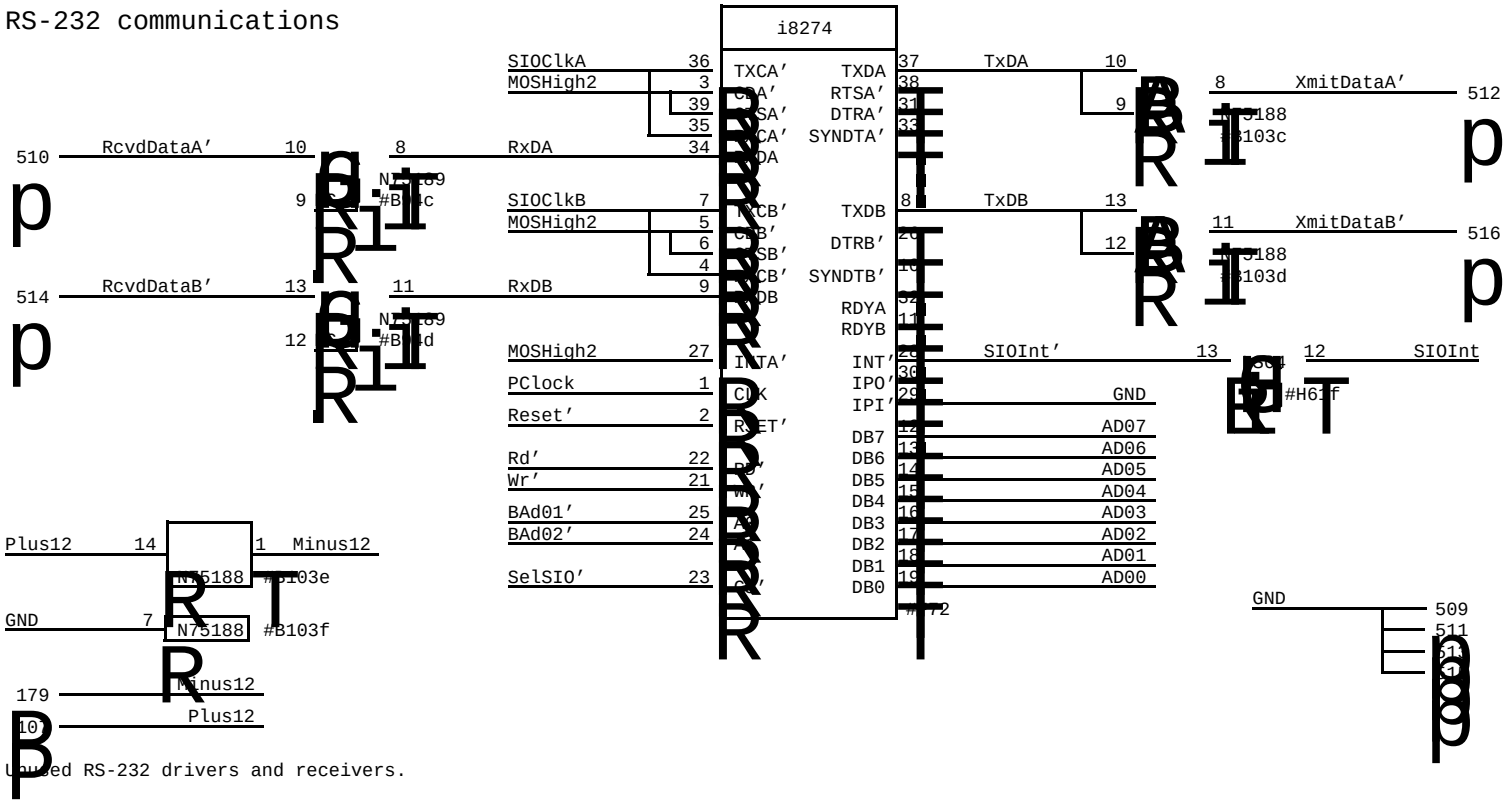
Wait state generator for Main CPU IO references



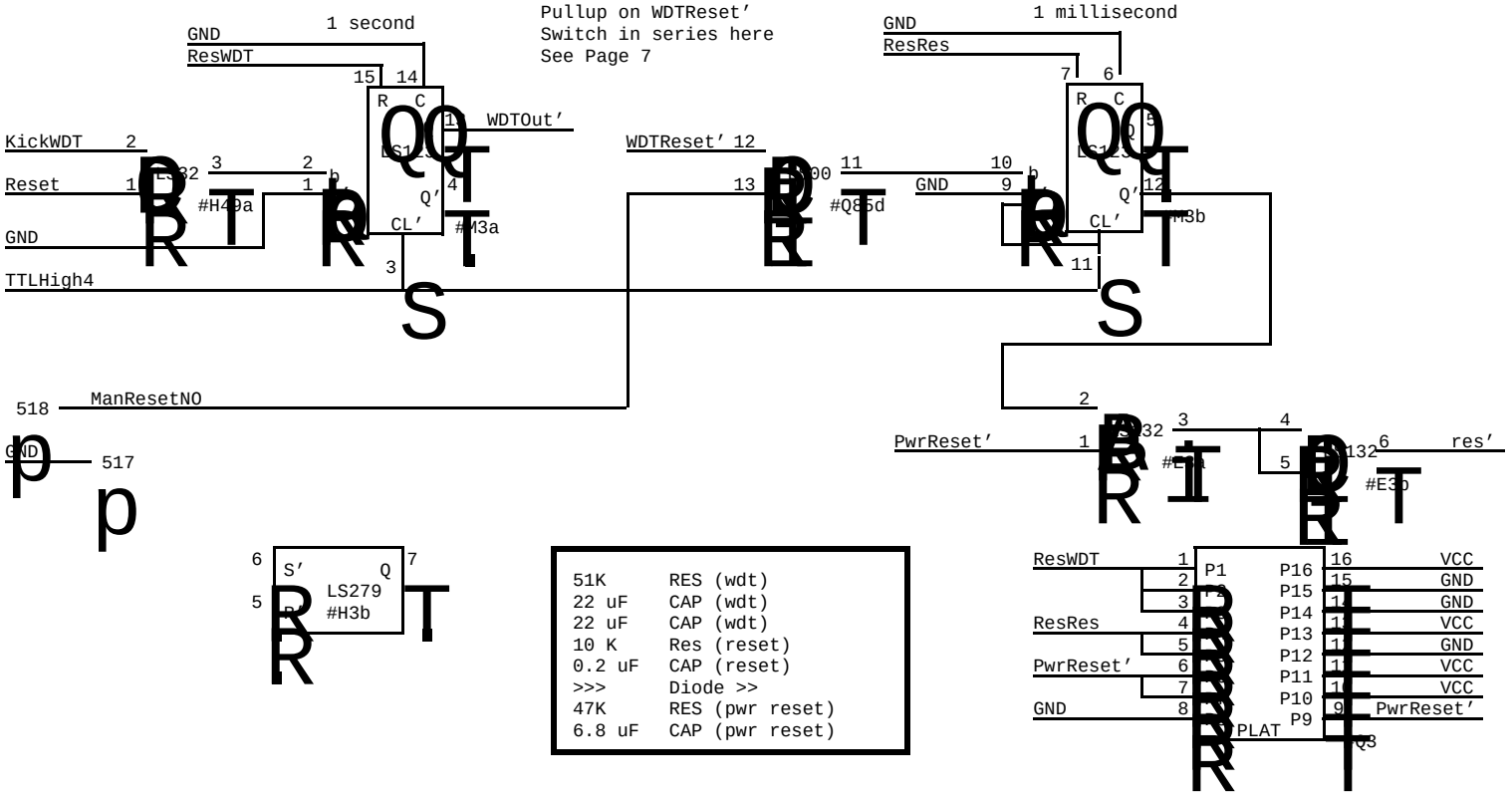


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	Main CPU Data Paths	ETT02.sil	S. Ornstein L. Stewart	Ai	8/31/82	02

RS-232 communications

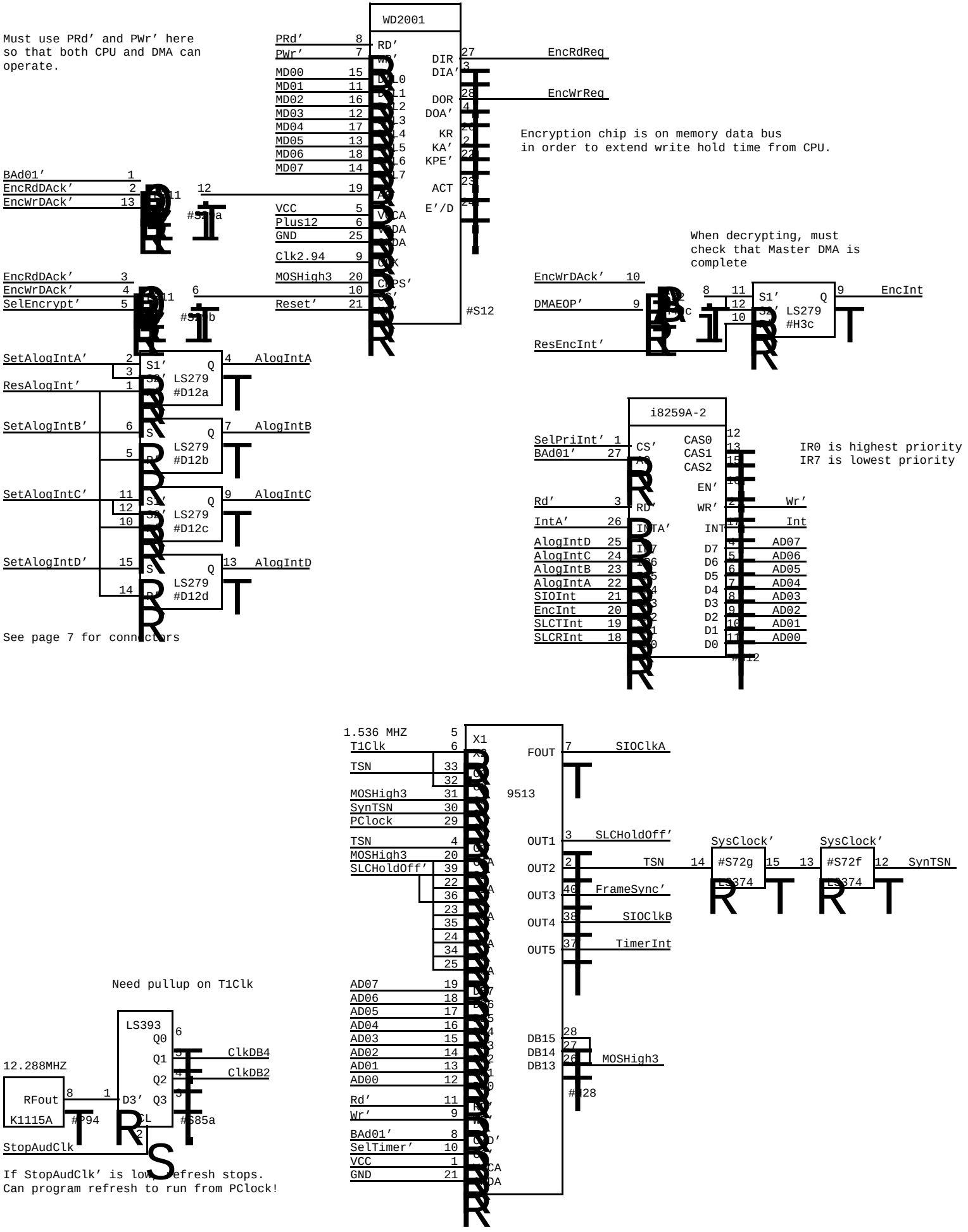


Watchdog timer and Reset circuit



51K	RES (wdt)
22 uF	CAP (wdt)
22 uF	CAP (wdt)
10 K	Res (reset)
0.2 uF	CAP (reset)
>>>	Diode >>
47K	RES (pwr reset)
6.8 uF	CAP (pwr reset)

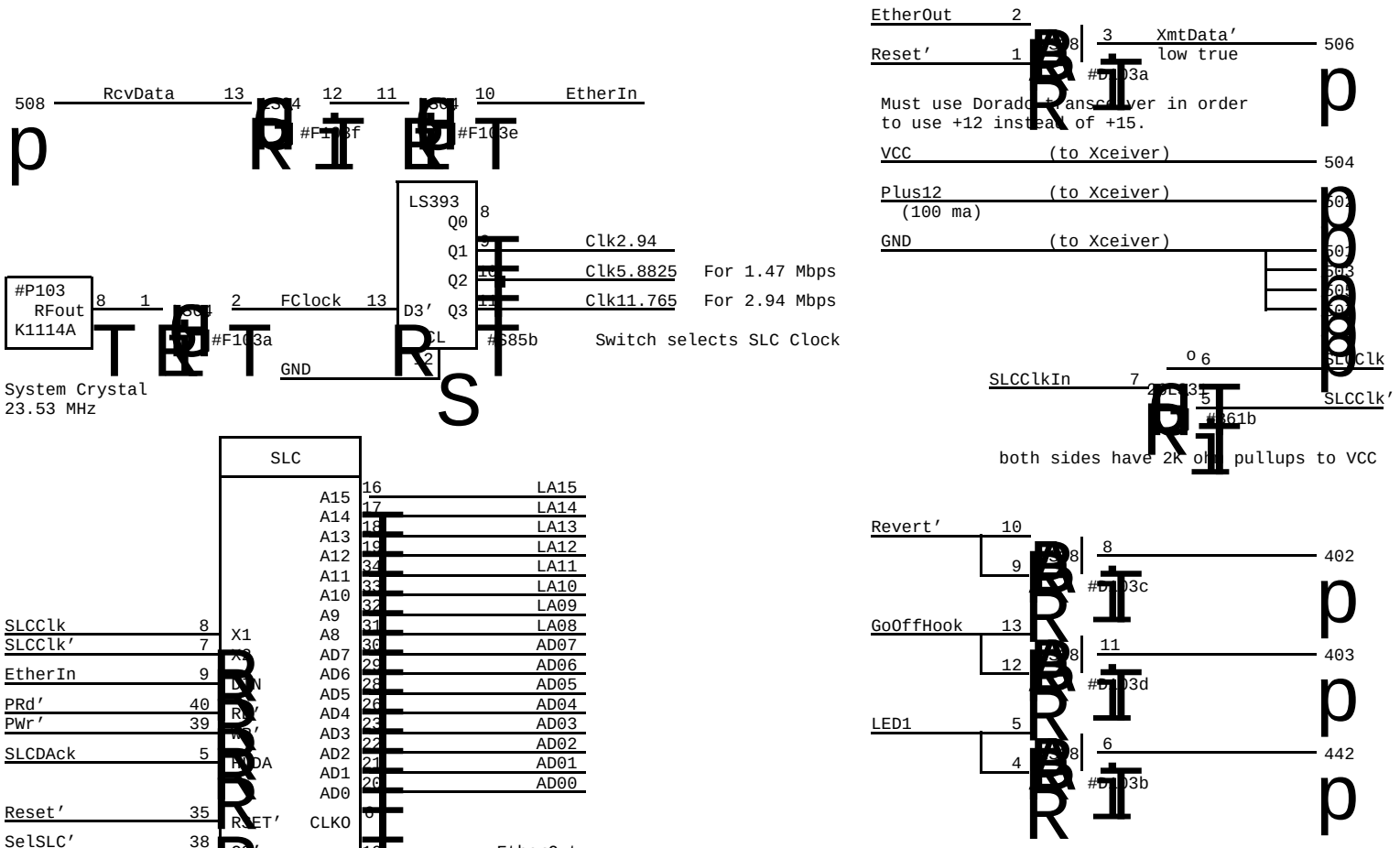
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	RS-232. Reset	ETT03.sil	S. Ornstein L. Stewart	Ai	10/01/82	03



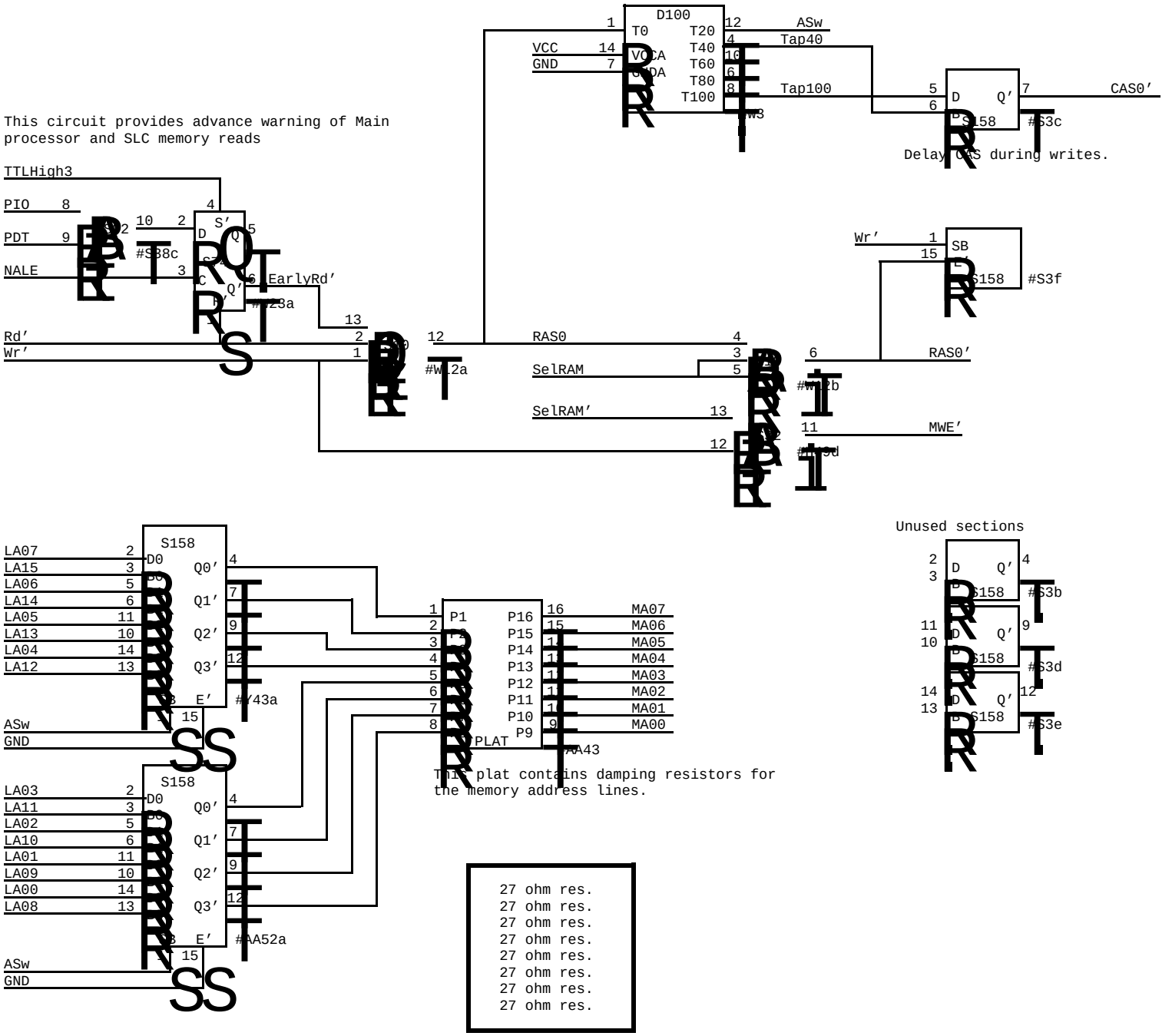
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	Timer, Interrupts, Encryption	ETT04.sil	S. Ornstein L. Stewart	Ai	7/29/82	04

ETHERNET DRIVE/RECEIVE

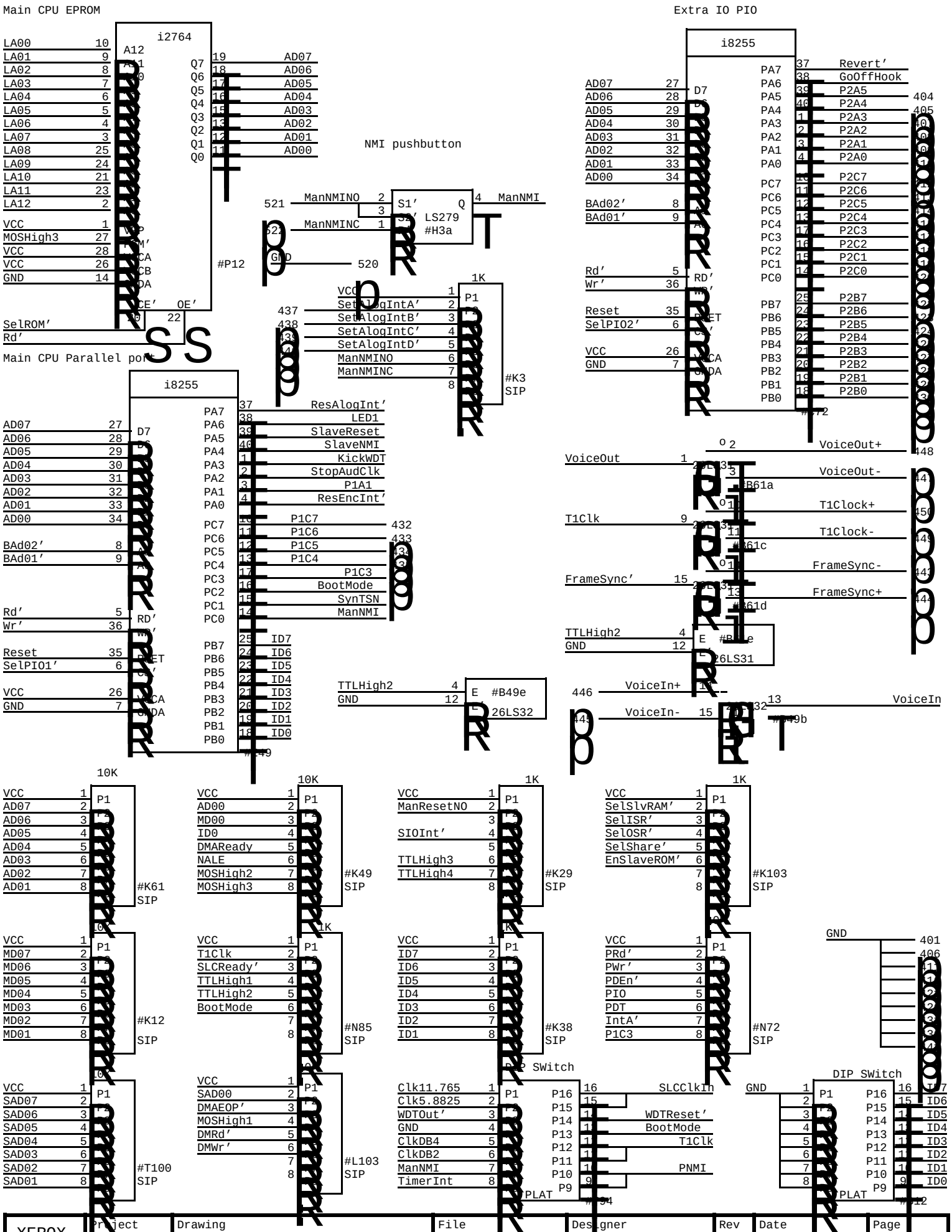
SLC floats EtherOut during and after Reset!



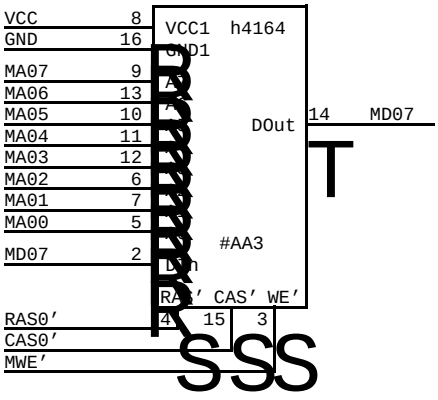
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	Ethernet	ETT05.sil	S. Ornstein L. Stewart	Ai	8/31/82	05

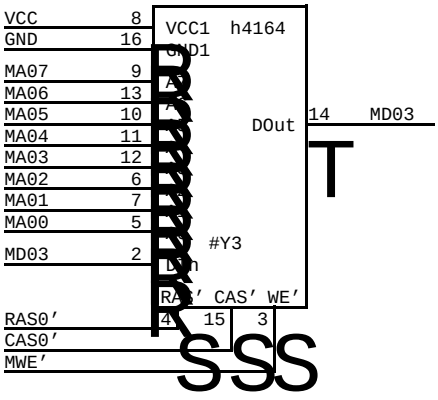


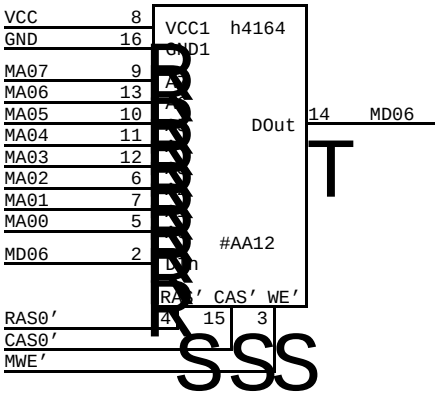
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	DRAM Memory Control	ETT06.sil	S. Ornstein L. Stewart	Ai	3/25/82	06

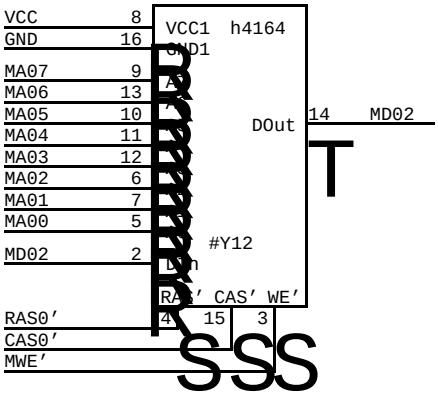


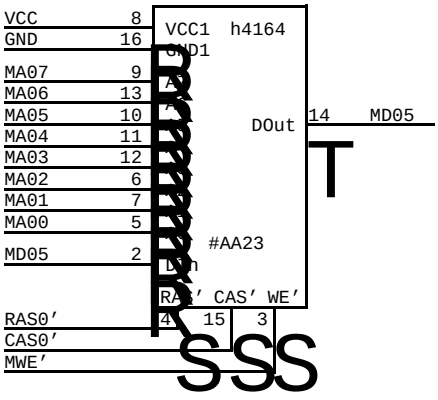
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	Main CPU ROM & PIO	ETT07.sil	S. Ornstein L. Stewart	Ai	10/01/82	07

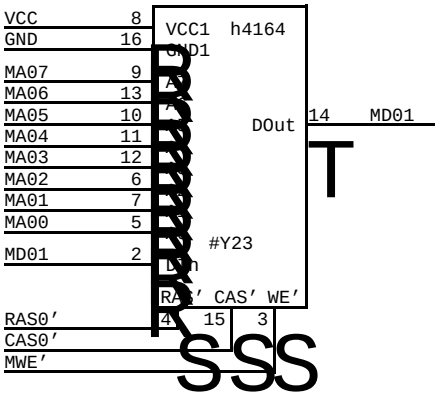


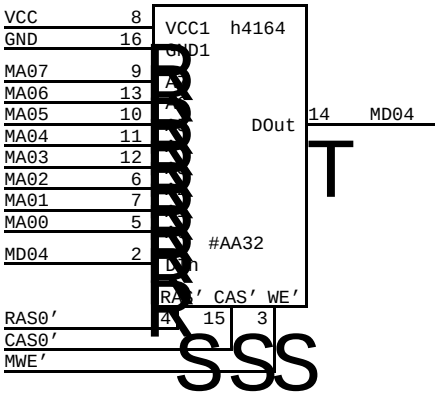


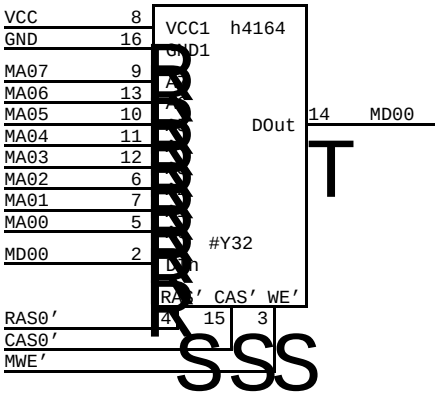




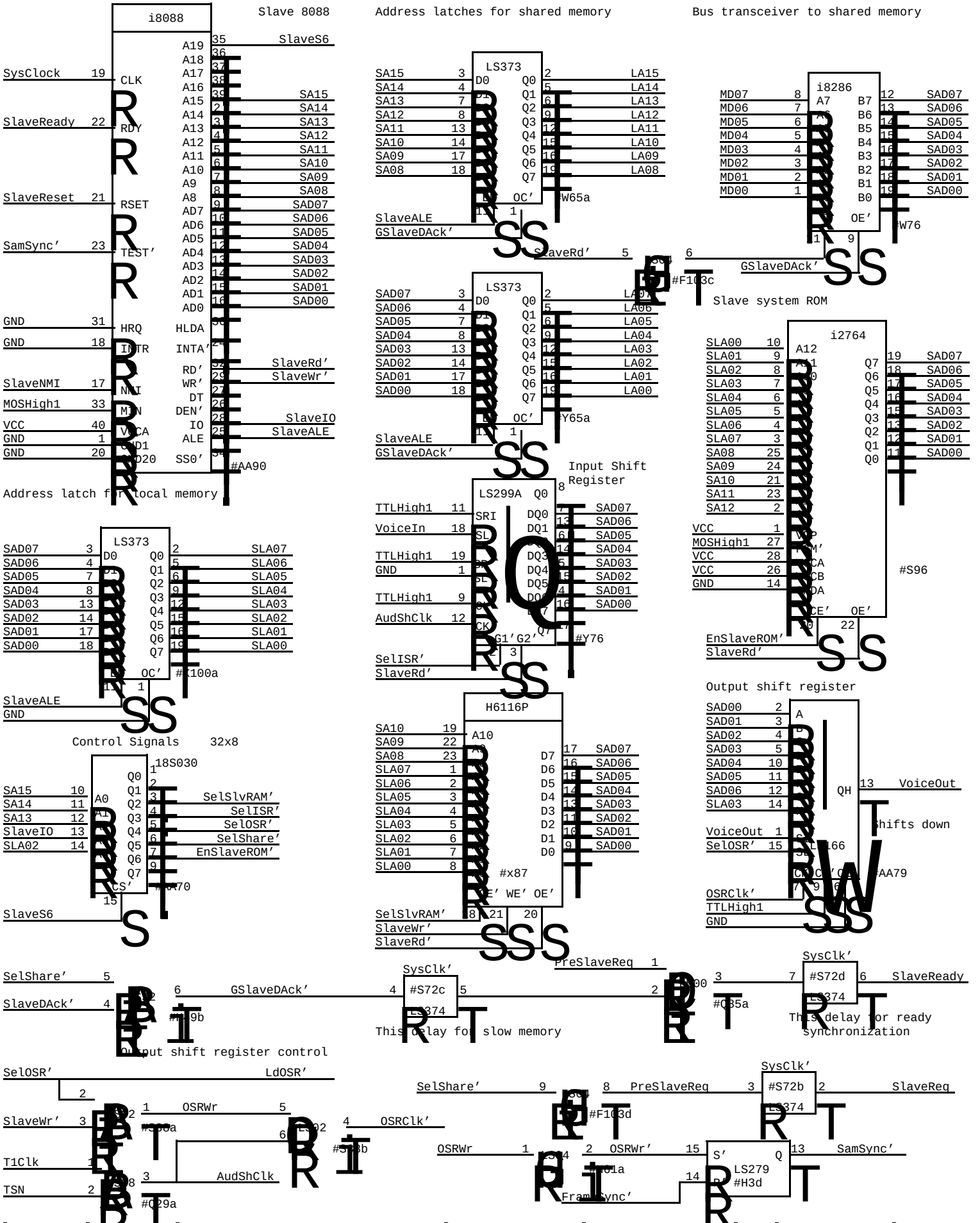




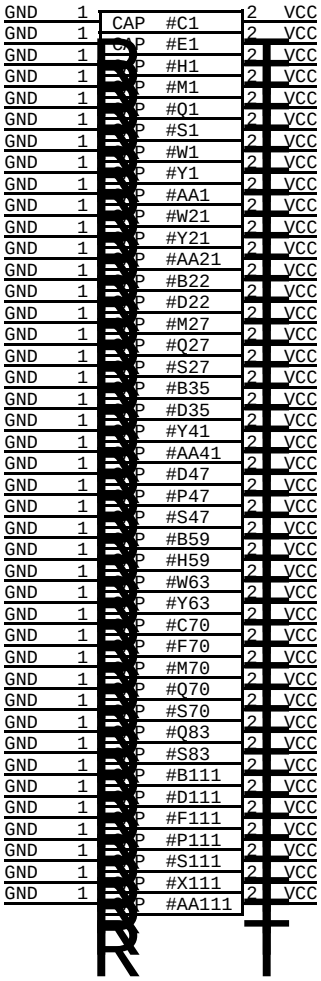




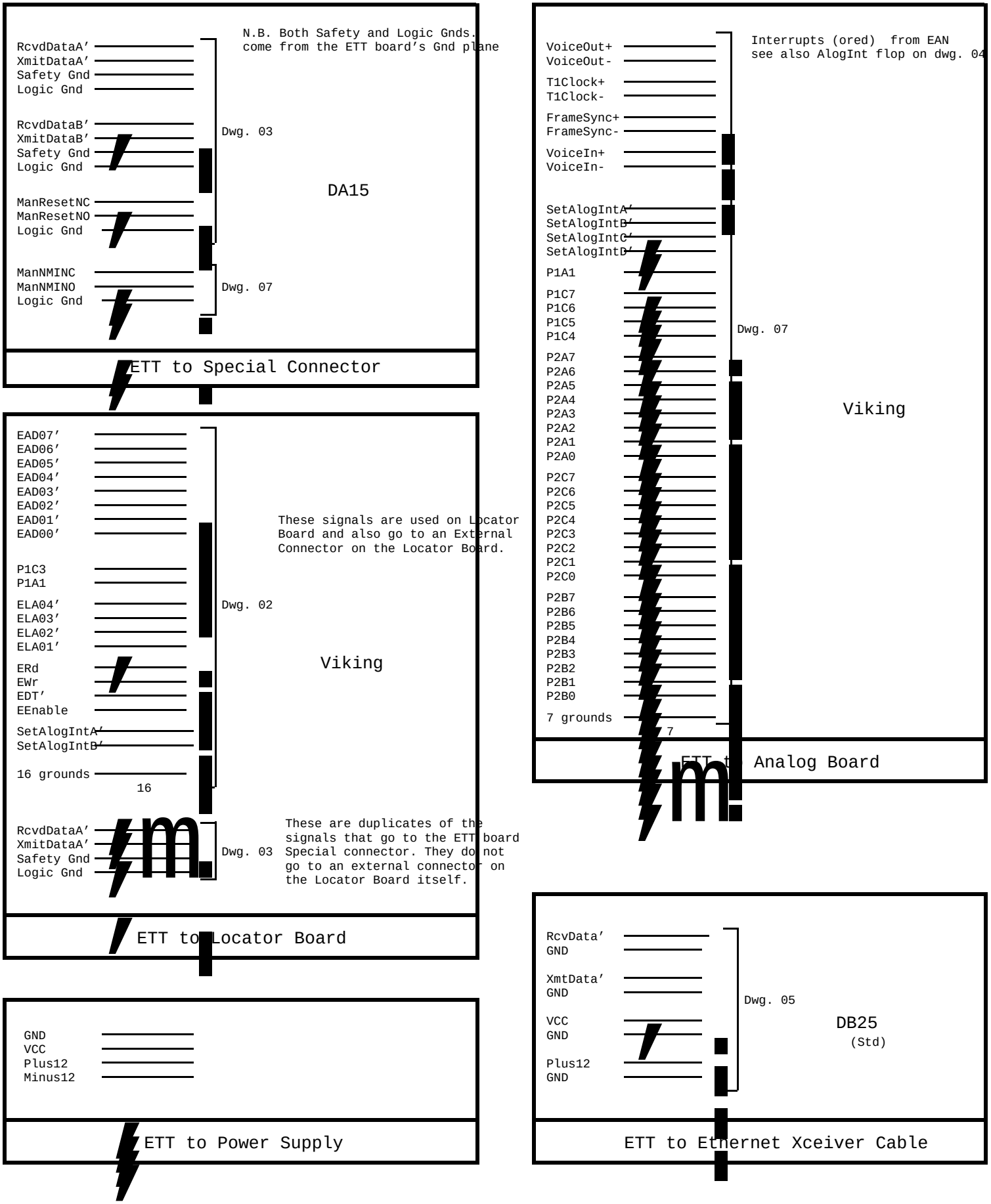
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	DRAM Memory Array	ETT08.sil	S. Ornstein L. Stewart	Ai	4/26/82	08



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	Slave 8088	ETT09.sil	S. Ornstein L. Stewart	Ai	10/01/82	09

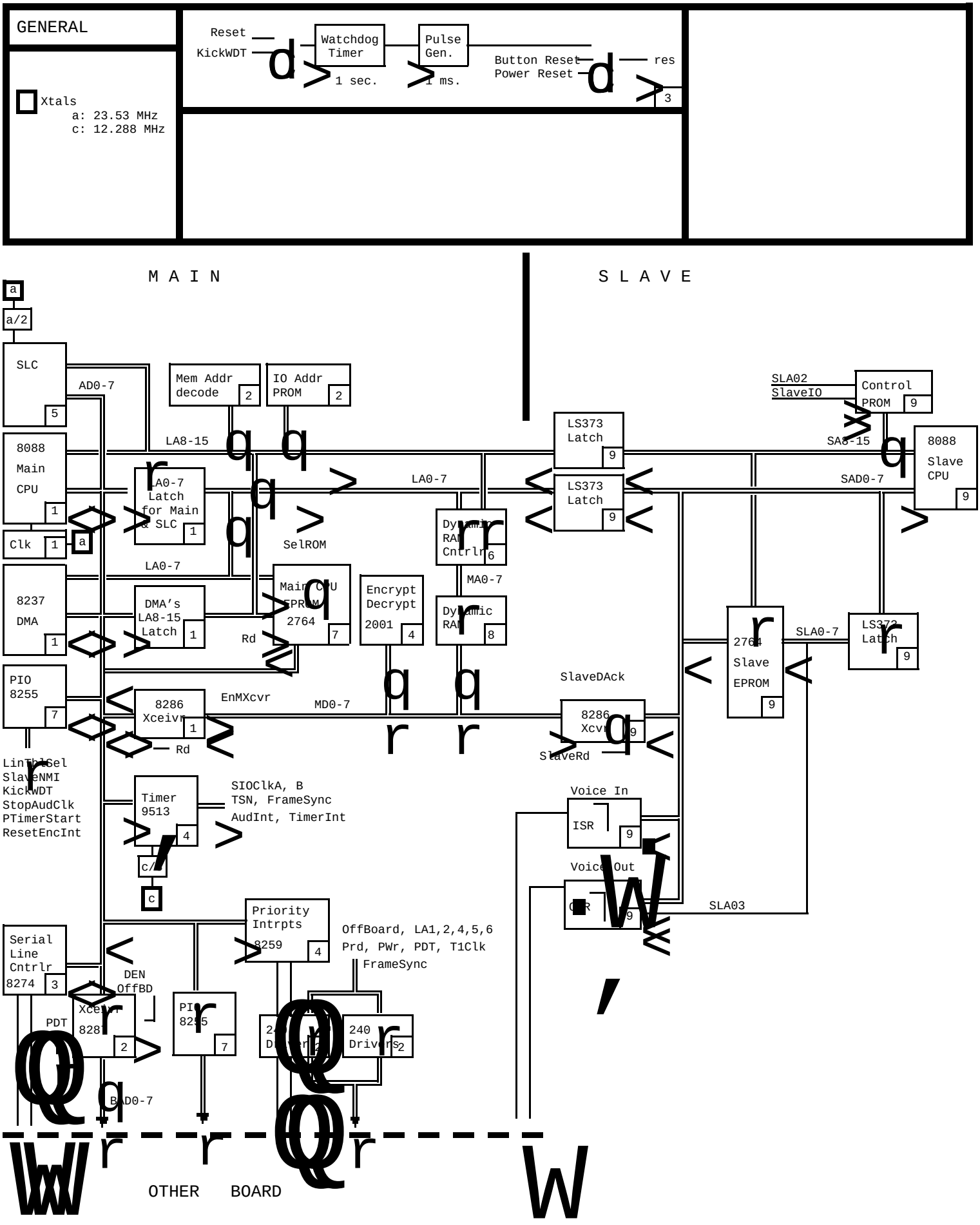


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Voice	Bypass Capacitors	ETT10.sil	S. Ornstein L. Stewart	Ai	3/17/82	10

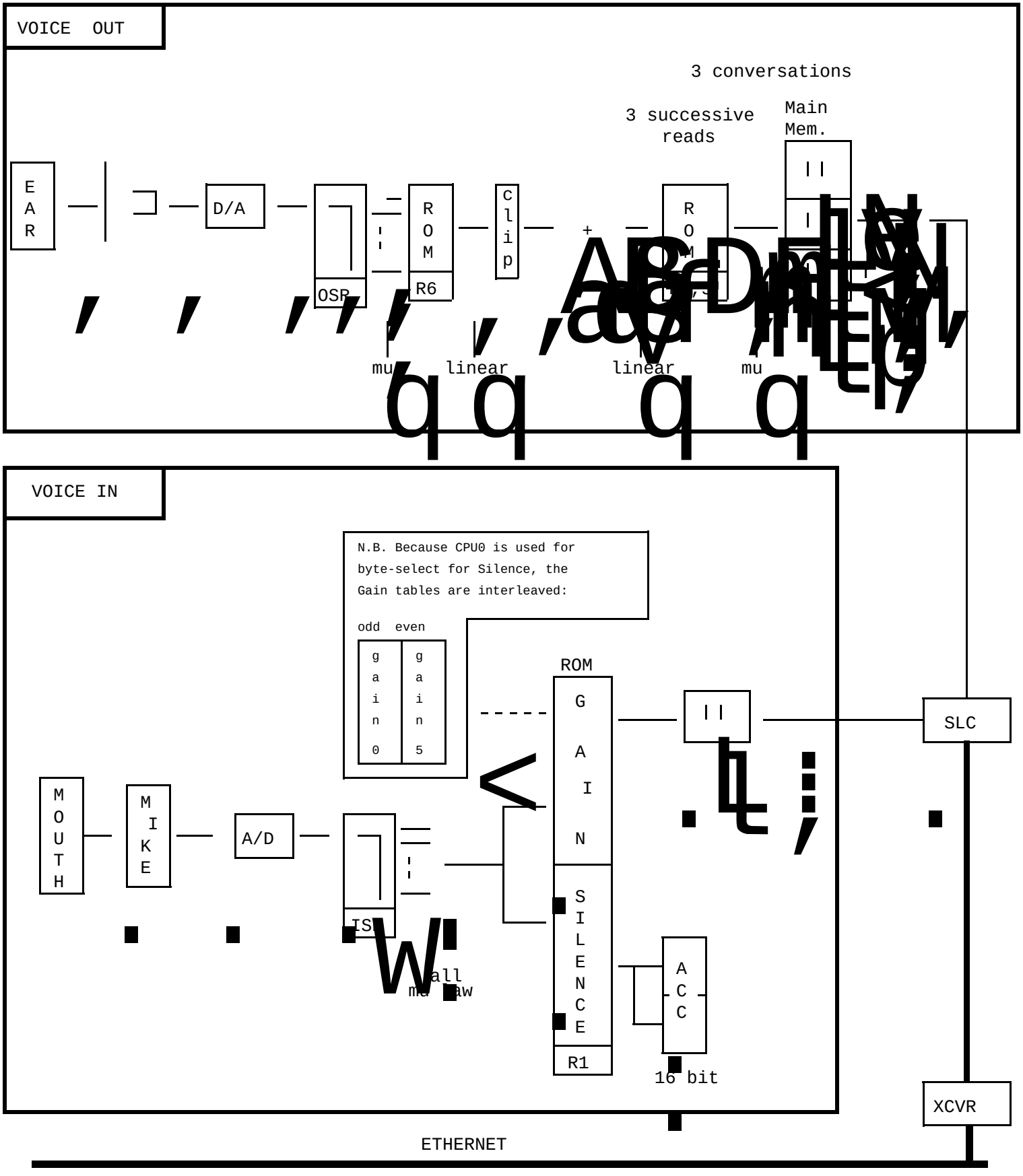


Arrows have ETT board on left

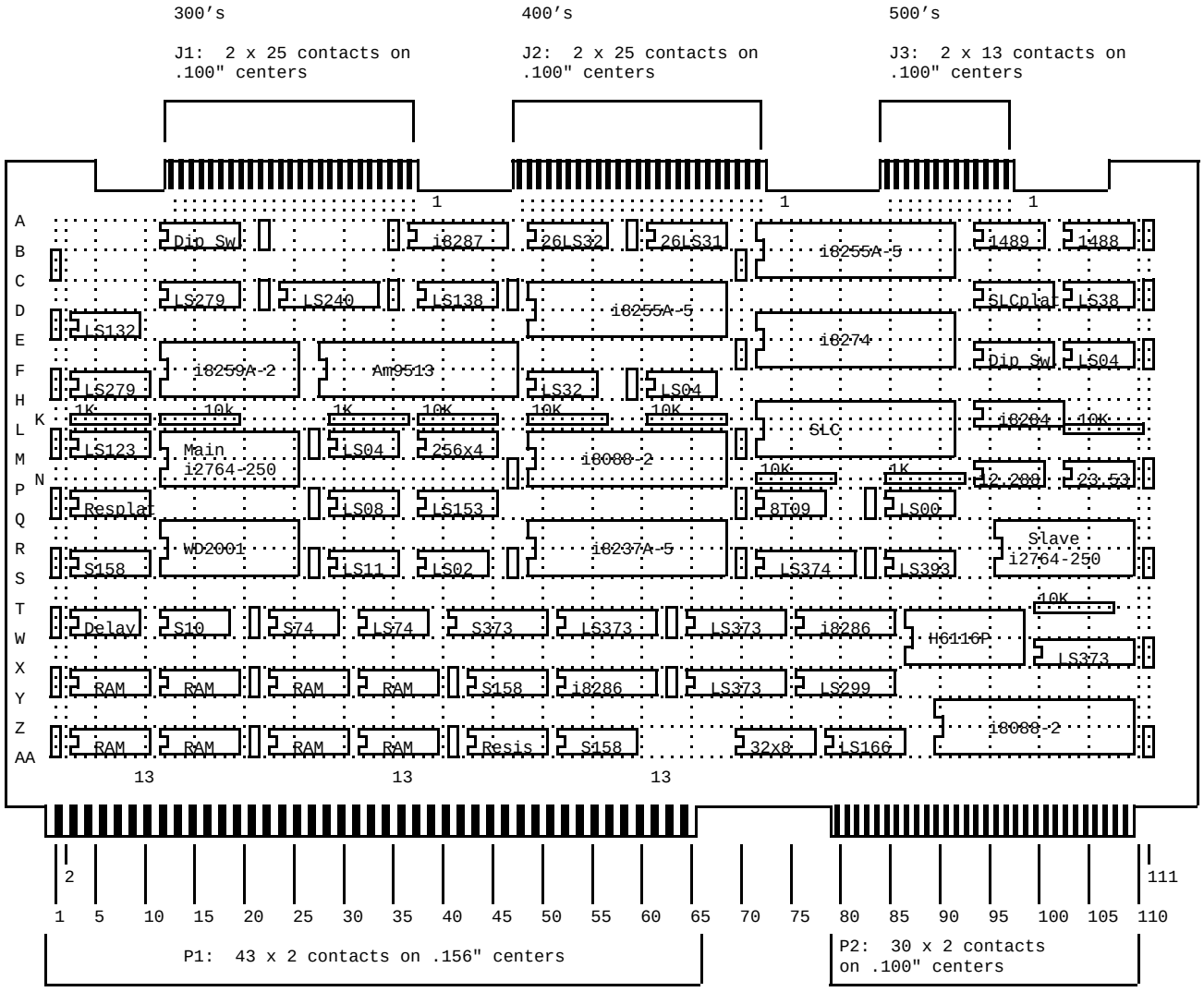
XEROX PARC	Project: Voice	Reference: ETT External Connections	File: ETT35.sil	Designer: S. Ornstein L. Stewart	Rev: Af	Date: 7/26/82	Page: 35



XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Voice	Lark Block Diagram	ETT40.sil	S. Ornstein L. Stewart		03/25/82	40



XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Voice	Etherphone General Picture	ETT41.sil	S. Ornstein L. Stewart		02/21/82	41



14 A
16 B
18 C
20 D
24 E
28 F
40 G

H 8 pin SIP

I Bypass cap

Component side shown

Plats:
ResPlat: (#Q3) Reset components, see page 3
SLC plat: #D94, Ethernet resistors, see page 5
Resis (#AA43) Memory address damping, see page 6

SIP values are marked above the SIP locations. Pin 1 is to the left

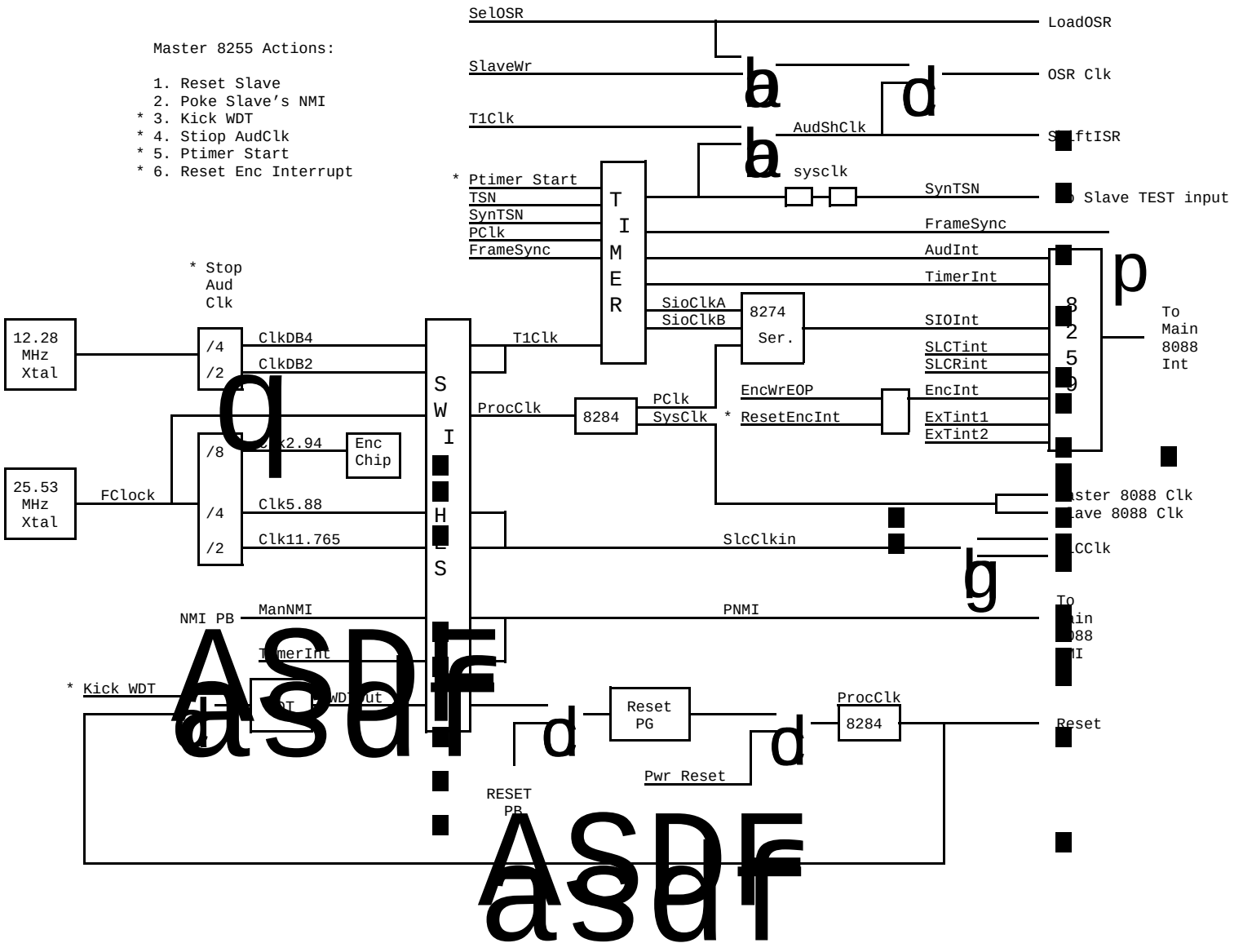
Switches are 8 switch (16 pin) dip switches (#B12 and #F94)
Crystals at #P94 and #P103 are marked with their frequencies

Delay: Belfuse 0447-0100-02 or 0447-0100-10

RAM are 150 ns 64K rams or 120 ns

32x8 prom at #AA70 is a TI TPB18S030
256x4 prom at #M38 is a F93427

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Voice	Layout	ETT42.sil	S. Ornstein L. Stewart		7/26/82	42



XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Voice	ETT Clocking	ETT43.sil	S. Ornstein L. Stewart		03/16/82	43

Cable for Voice

Multibus
Edge Connector

DA-15S

436		Ground	1
440		VoiceIn+	4
441		VoiceIn-	11
442		VoiceOut+	5
444		VoiceOut-	12
447		FrameSync+	6
448		FrameSync-	13
450		T1CLK+	8
449		T1CLK-	15

DB-25P

Cable to Ethernet

DB-25S

508	17	RcvData	16
501	4	Ground	3
506	16	XmtData	13
505	3	Ground	25
502	15	Plus5	11
503	2	Ground	23
507	14	Plus12	12
504	1	Ground	24

Cable to Console

DB-25S

510	18	RcvdDataA′	3
512	19	XmitDataA′	2
511	6	SafetyGround	4
509	5	LogicGround	7

Note: leave enough slack for possible swap of pins 2 and 3

Cable to LARK Display

DB-25S

514	20	RcvdDataB′	3
516	21	XmitDataB′	2
515	8	SafetyGround	4
513	7	LogicGround	7

Note: leave enough slack for possible swap of pins 2 and 3

Pushbuttons

522	24	ManNMINC	
520	23	ManNMIGround	
521	11	ManNMINO	
519	10	ManResetNC	
517	9	ManResetGround	
518	22	ManResetNO	

Momentary pushbuttons

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Voice	LARK Cables	ETT44.sil	S. Ornstein L. Stewart	Aa	6/10/82	44

A 8088
B DMA
C Clock
D Pri Int
E SLC
F Xceivr
G USART
H NOT IN DICT
I 26LS31
J Ser Contlr.
K 2Kx8 RAM H6116P
L Timer
M DES M = Multiplexed
N Latch, non inverting
O Inverting Xcvr
P Latch, inverting
Q LS240
R Direct control
S LS244, LS241 (low enable)
T PIO
U Timer
V 26LS31 26LS32
W 26LS32
X (ENC)
Y LS241, high enable
Z 2964B
a i2764
b 64 k ram
c delay line
d 8203
e bypass capacitor

1 74279, 1 S

2 74279 2 S'