

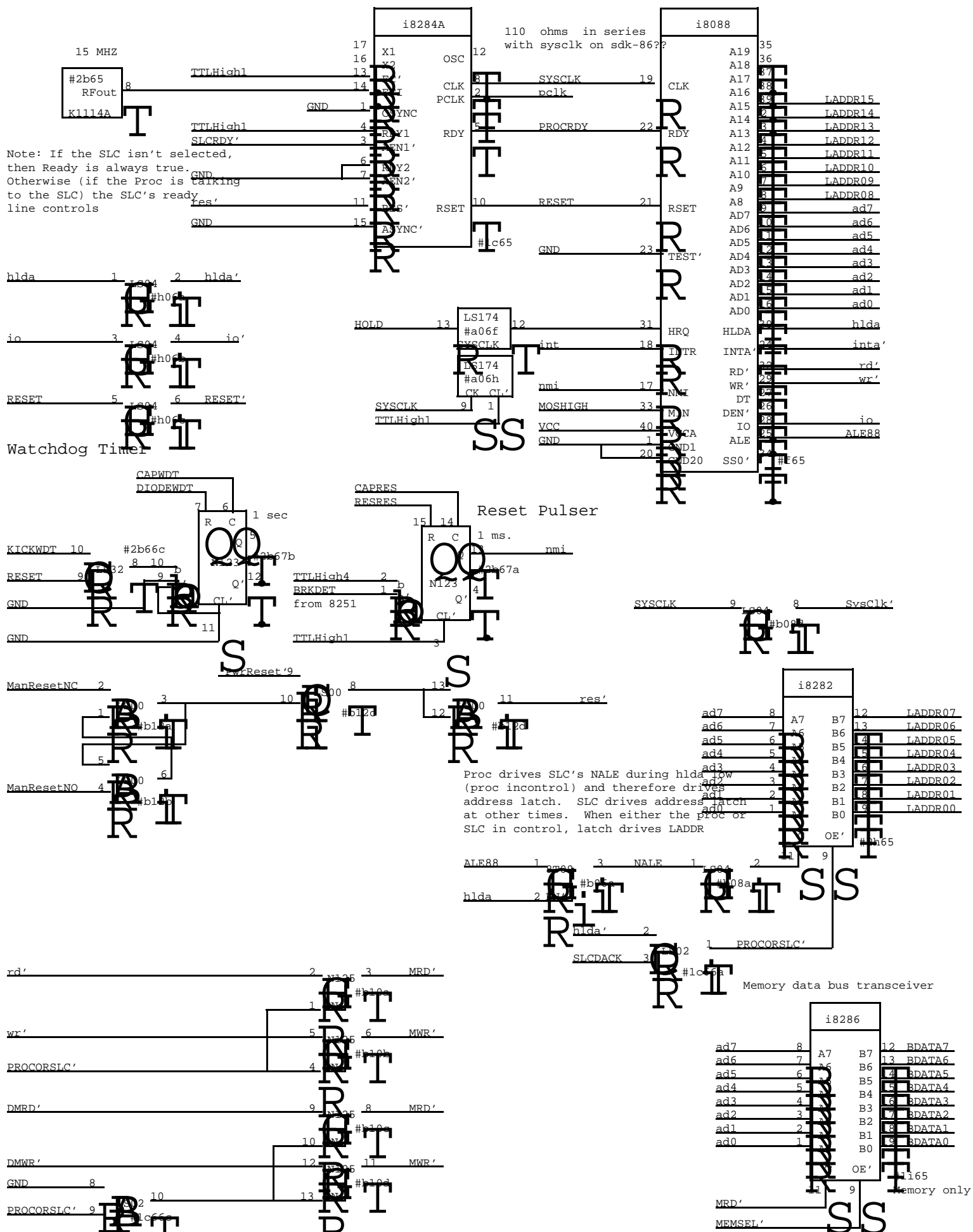
L A R K
E T H E R P H O N E S C H E M A T I C S

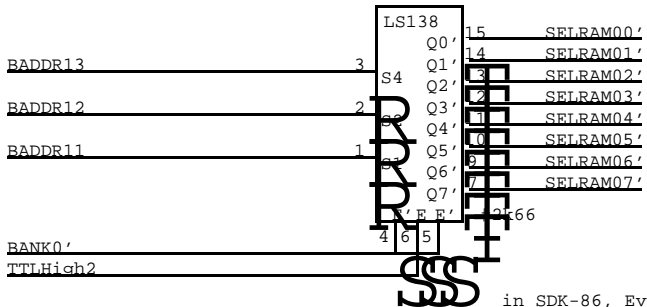
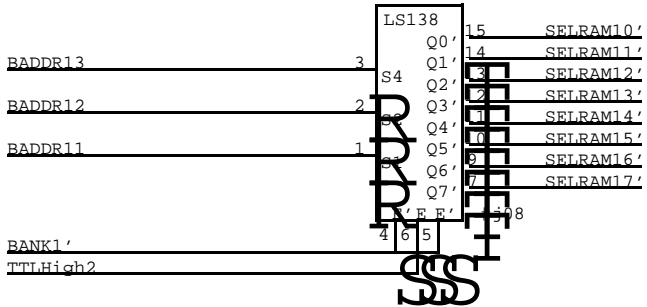
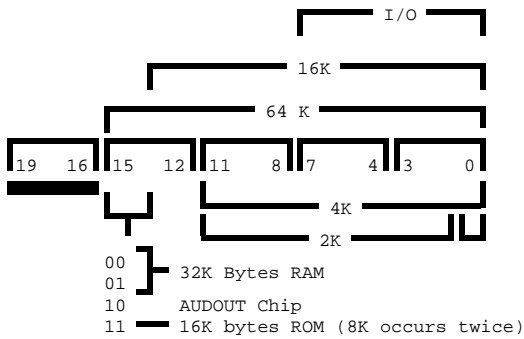
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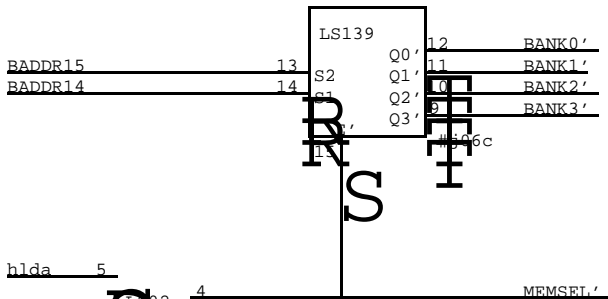
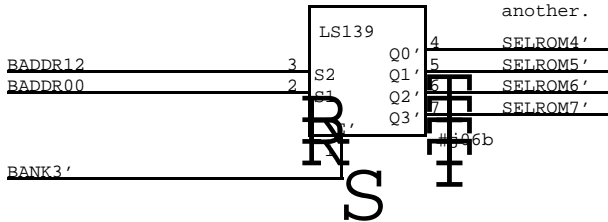
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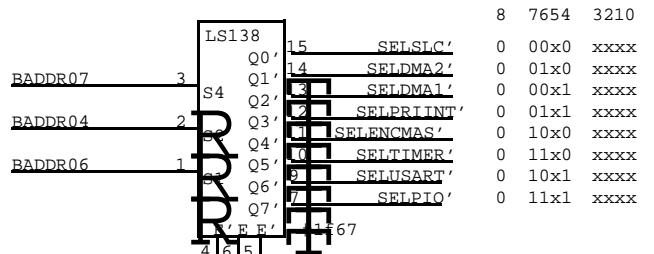
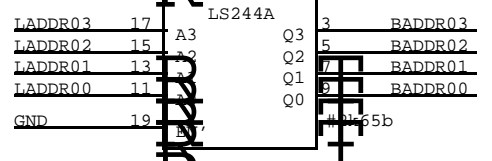
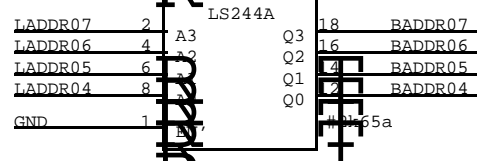
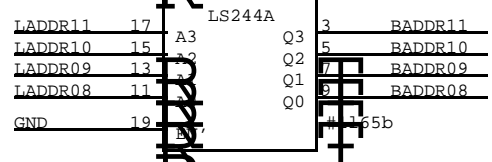
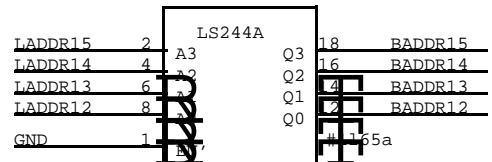
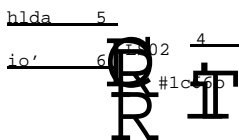




in SDK-86, Even addresses are in one chip, odd in another.

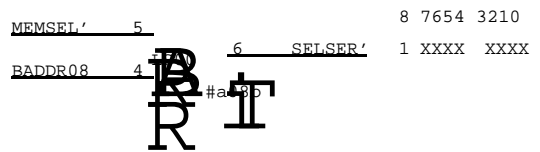


DMA access or Proc selecting memory

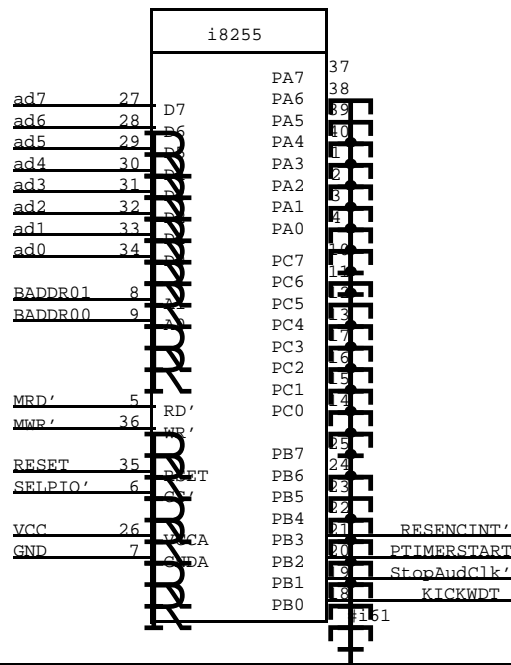


It is mandatory to address the SLC with addresses in the 20's

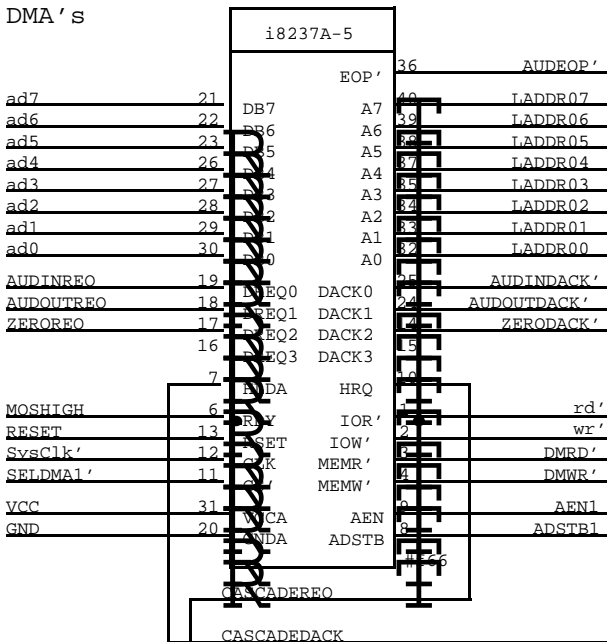
The SLC decodes the low 8 address bits



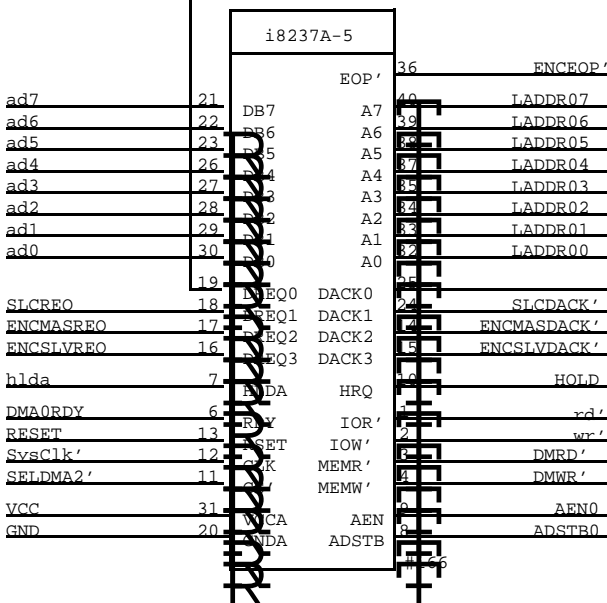
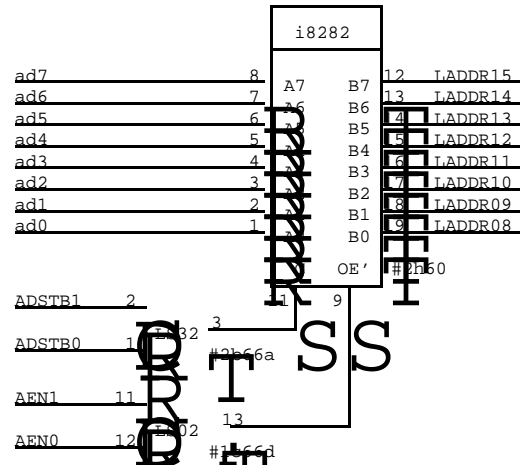
Parallel I/O

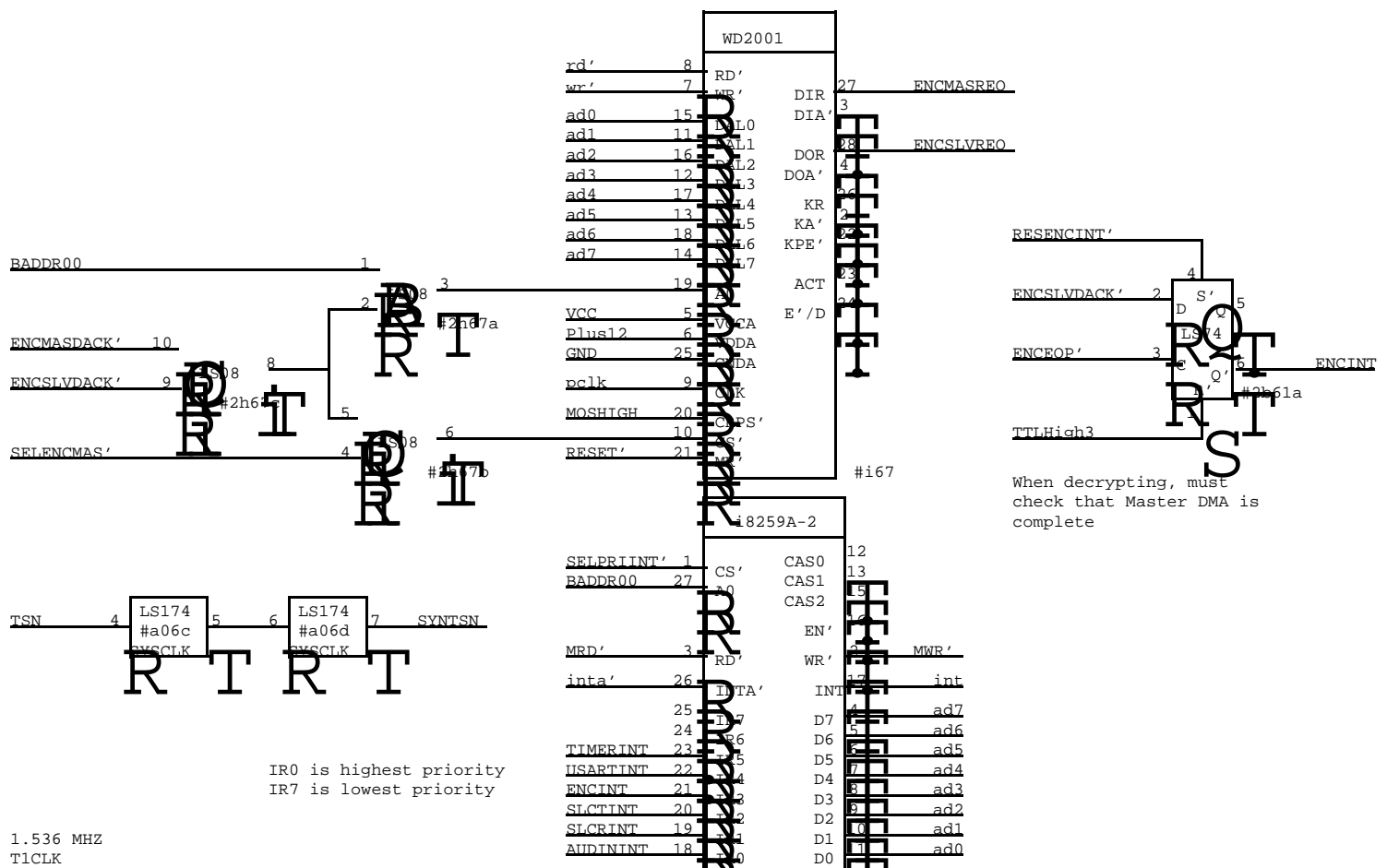


DMA's



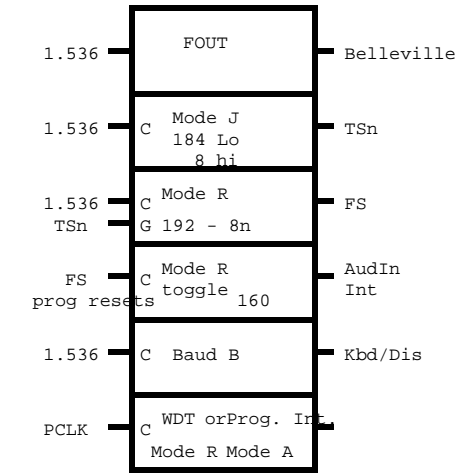
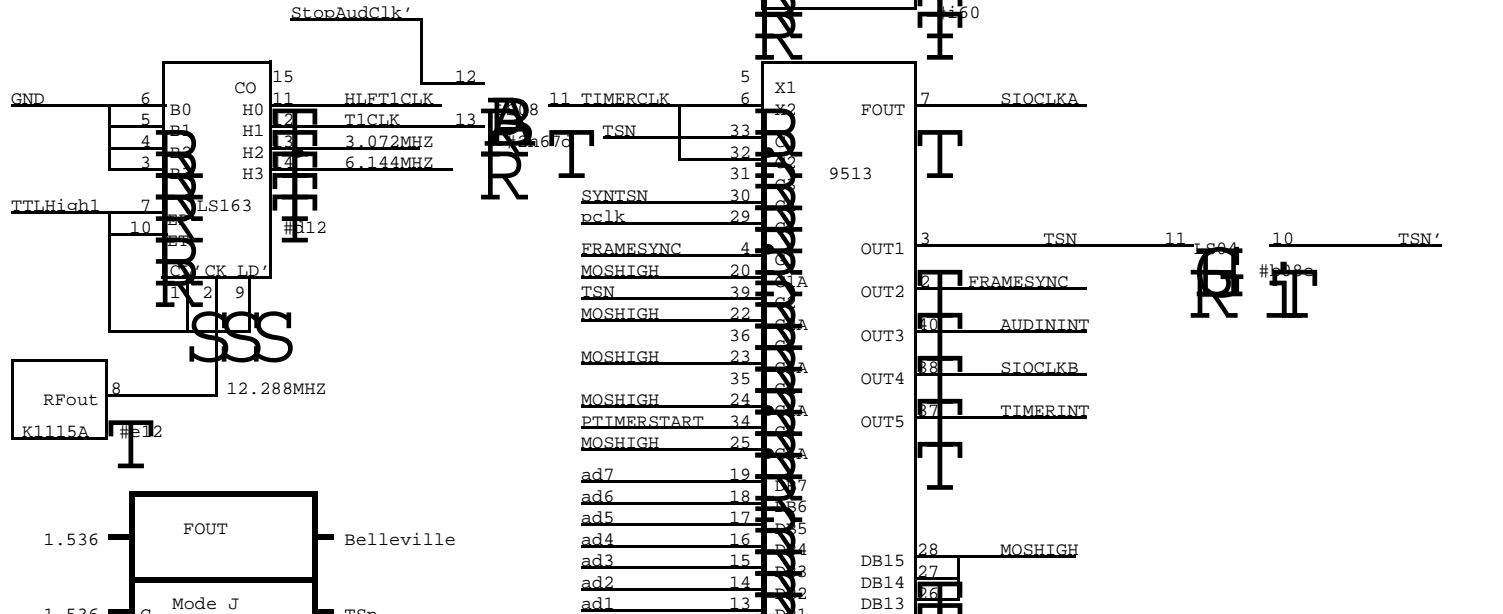
the DMA's are programmed for neg true DACK's - positive true REQ's





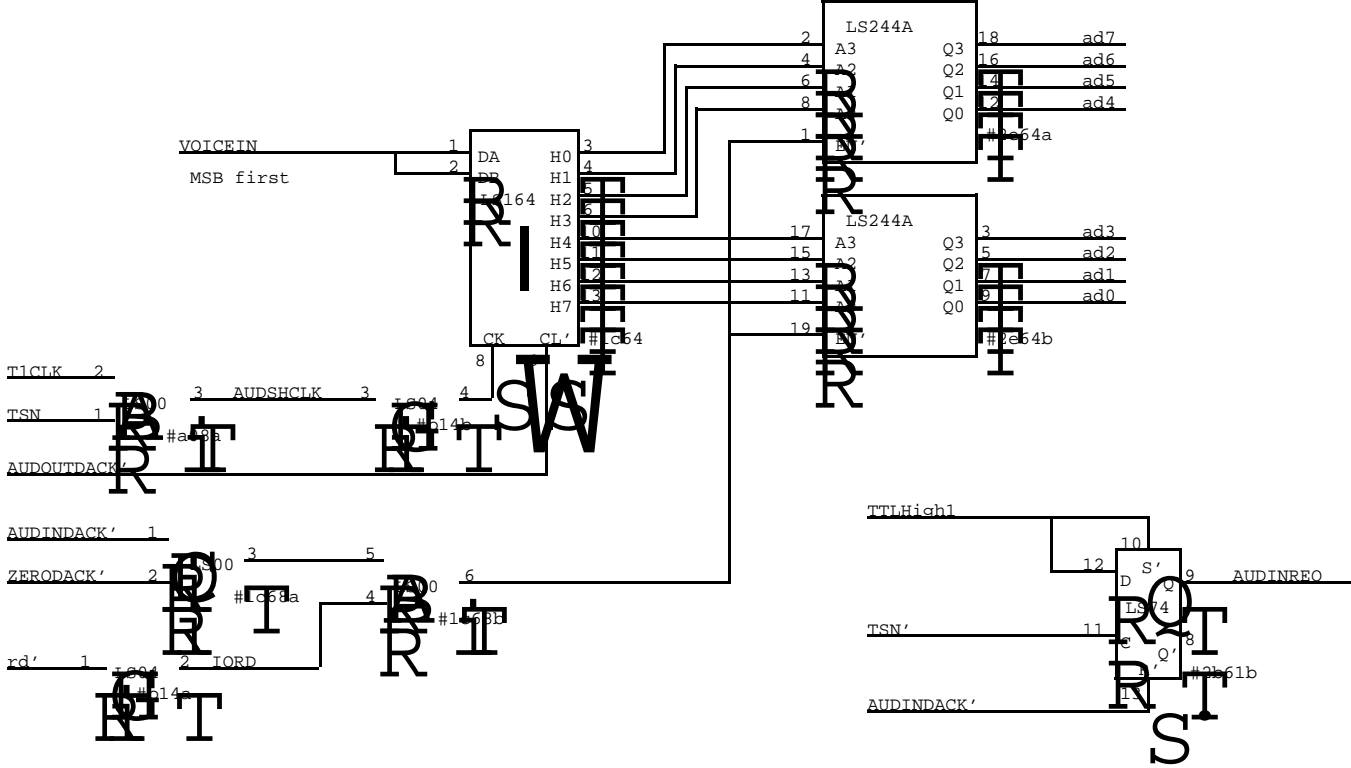
IR0 is highest priority
IR7 is lowest priority

1.536 MHZ
T1CLK



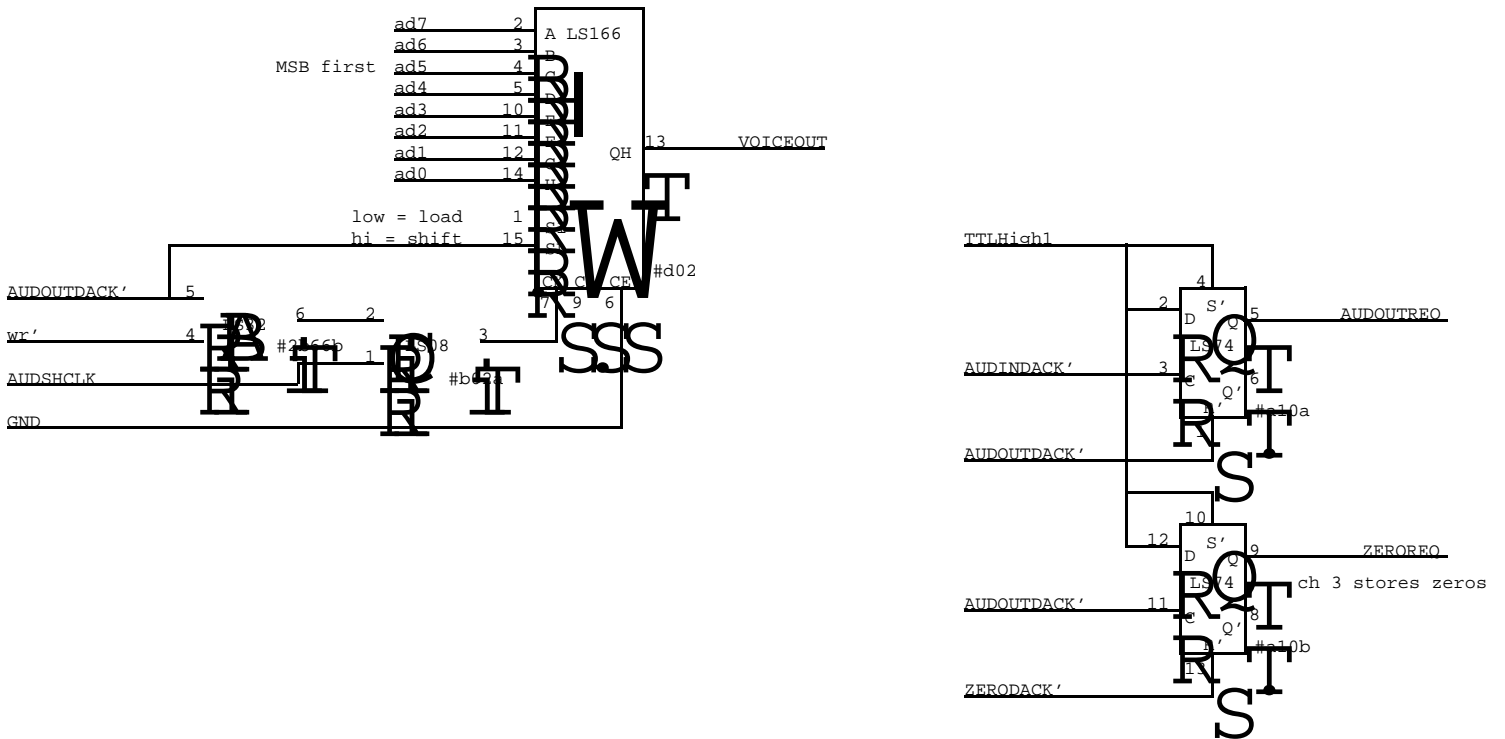
SIOCLKA POSSIBILITIES	
9513 DIVISIONS	8274 Divisions
1.536 / 80 (16 x 5) = 19,200	/ 16 = 1200
	/ 32 = 600
	/ 64 = 300
1.536 / 10 (1 x 10) = 153,600	/ 16 = 9600
	/ 32 = 4800
	/ 64 = 2400
1.536 / 5 (1 x 5) = 307,200	/ 16 = 19,200
	/ 32 = 9600
	/ 64 = 4800

INPUT



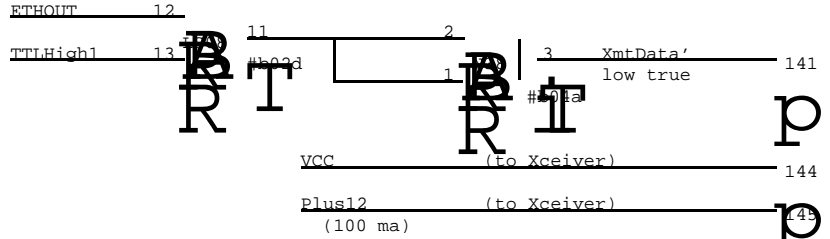
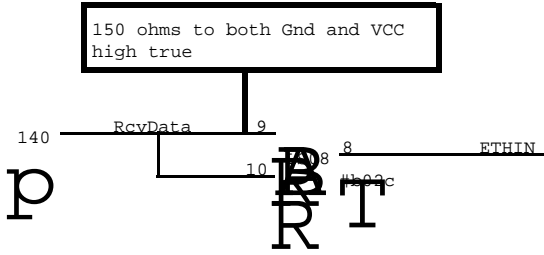
OUTPUT

Using 74165 shifter might save agate

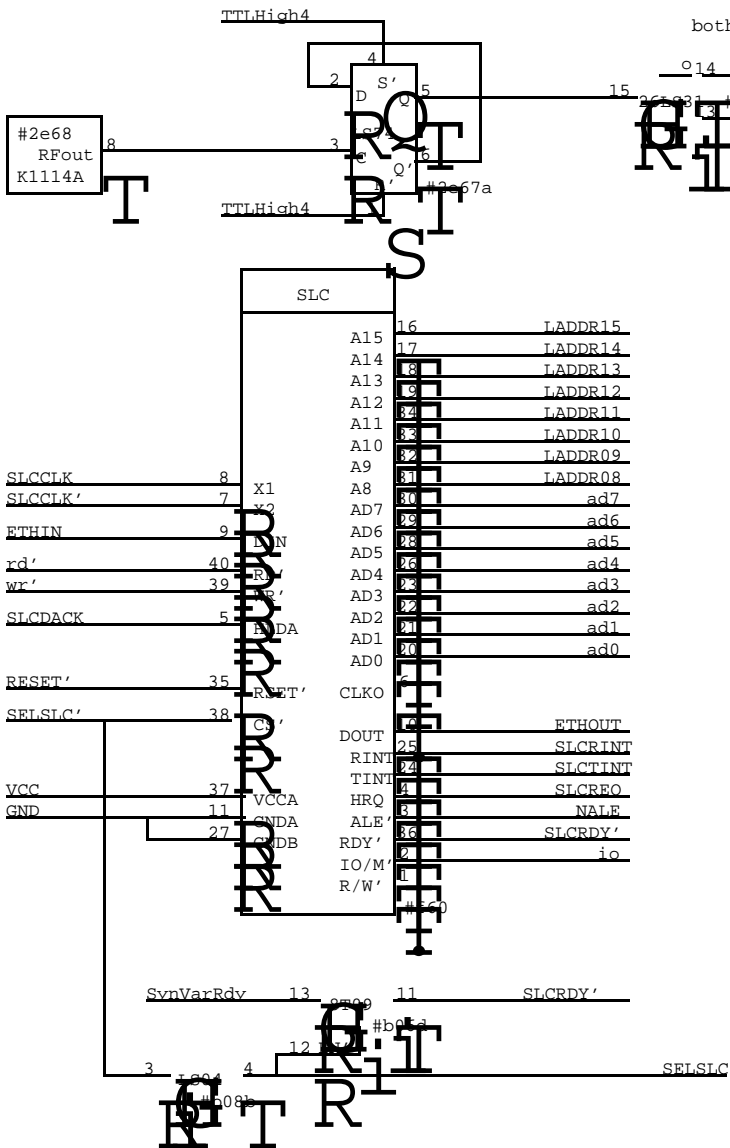


ETHERNET DRIVE/RECEIVE

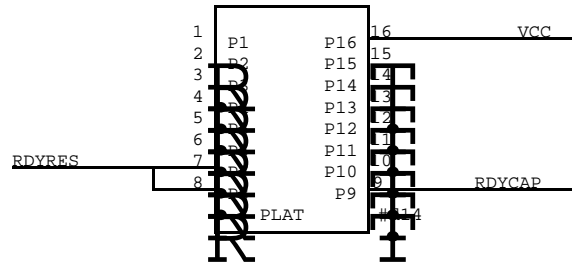
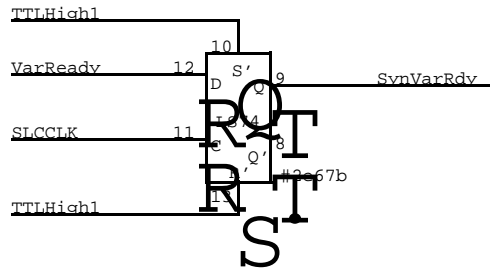
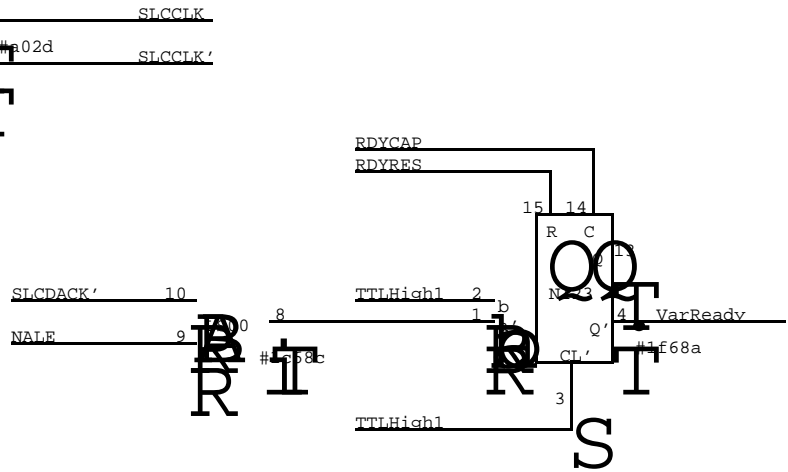
ALL lines are TP with gnd from edge



Must use Dorado transceiver in order to use +12 instead of +15.

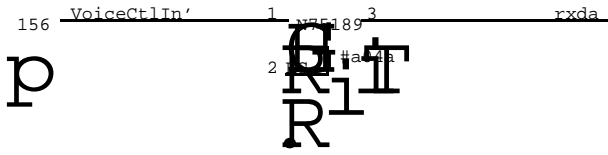


both sides have 2K ohm pullups to VCC

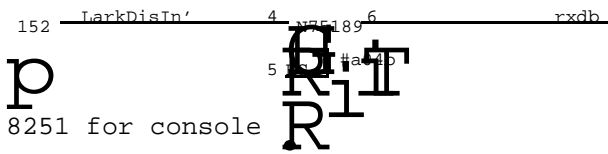


SLCRDY' is held low except when the SLC is selected - in which case, the SLC's own RDY controls the line

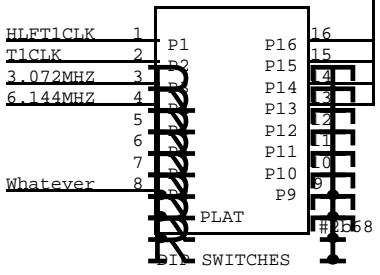
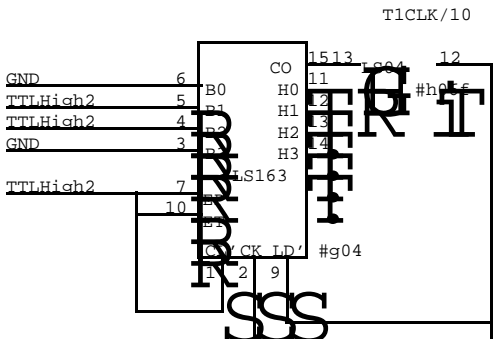
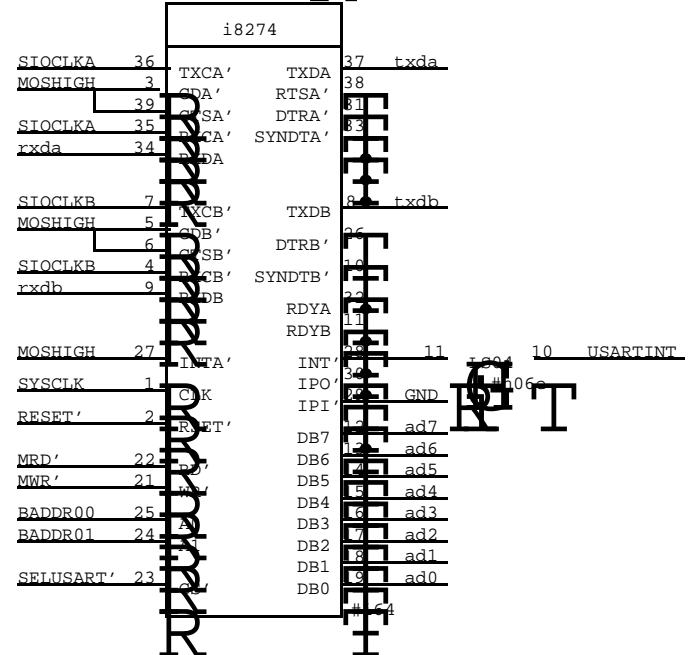
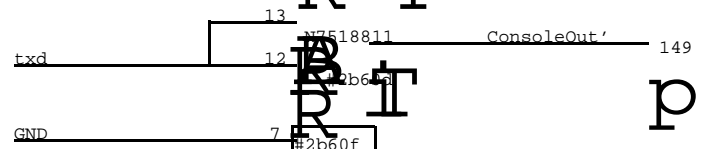
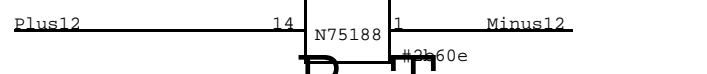
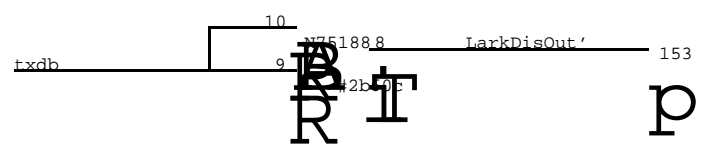
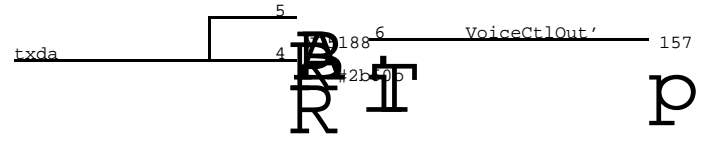
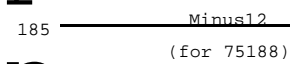
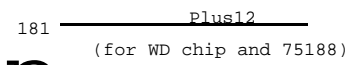
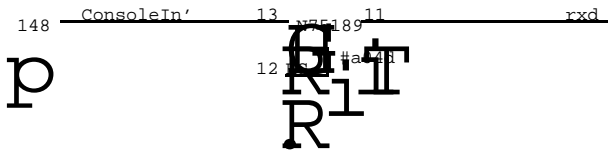
BELLEVILLE



LARK IIB Display

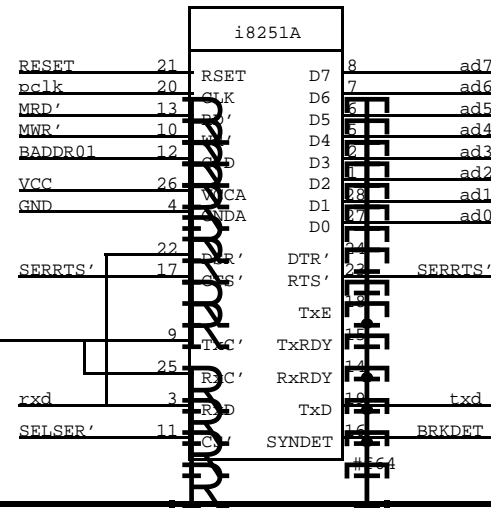


8251 for console

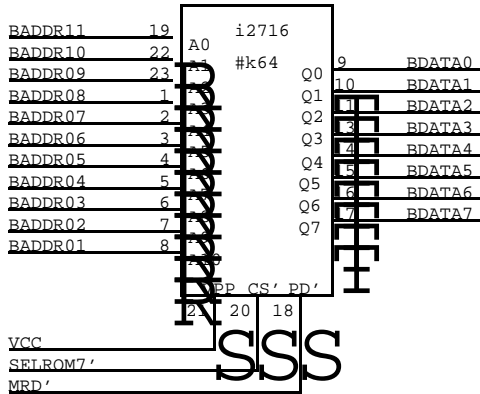


To enable WD Timer, switch 7 is closed and switch 8 open.
To disable, reverse them.

BRKDET goes high after two characters of spacing
returns low on master reset or when RxData returns to marking.

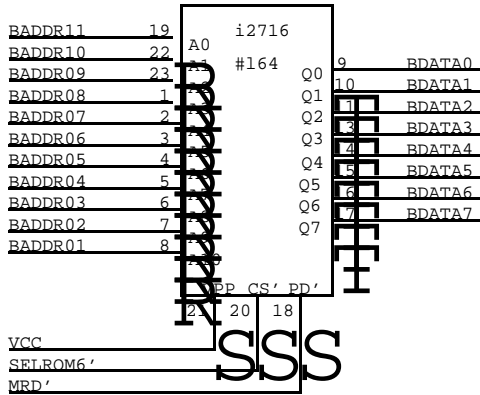


FF000 - FFFFF odd bytes only

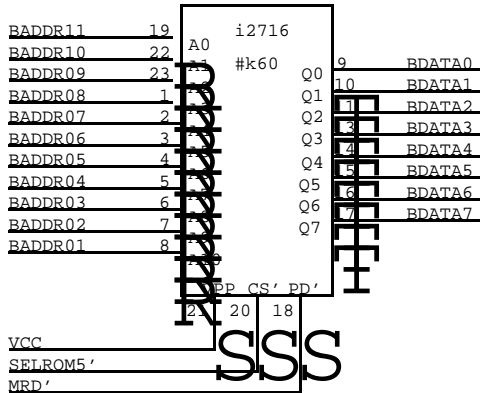


The two highest EPROMs hold the monitor. Because the monitor is from an 8086 system, the EPROMs were set up for a 16 bit bus. For an 8088 system, therefore, the two EPROMs hold the even and odd bytes...

FF000 - FFFFF even bytes only

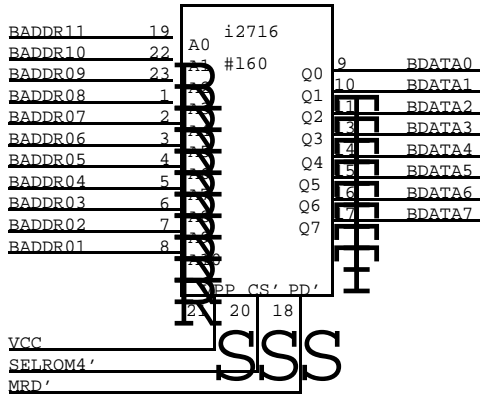


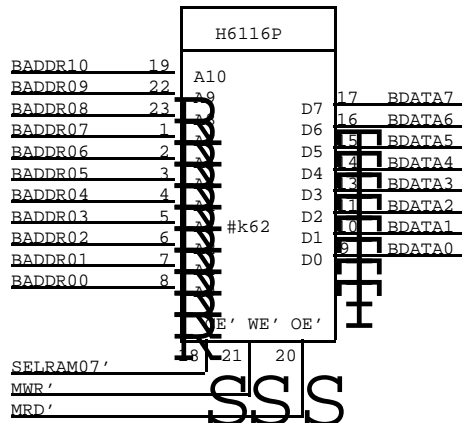
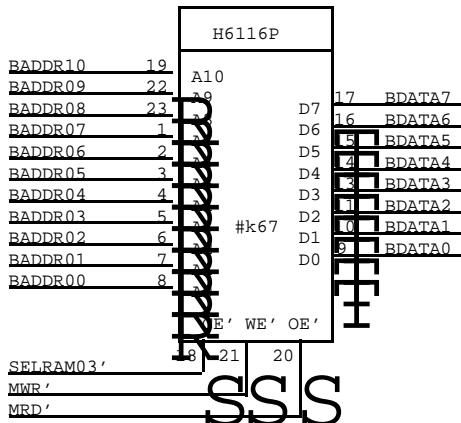
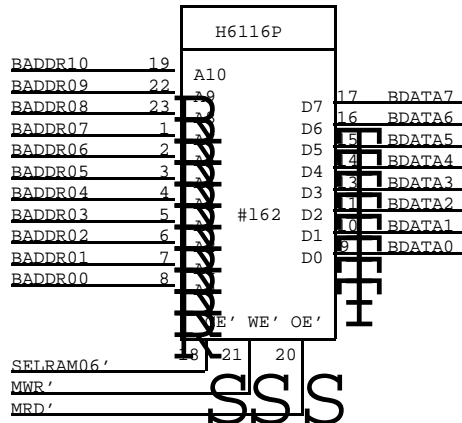
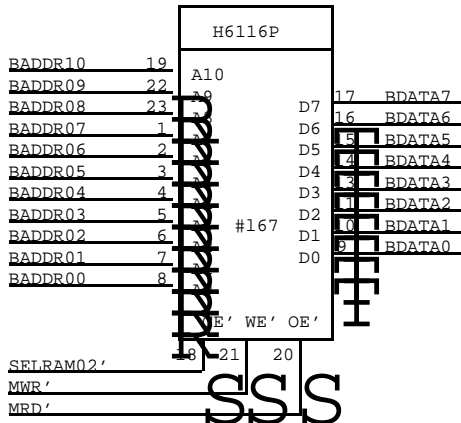
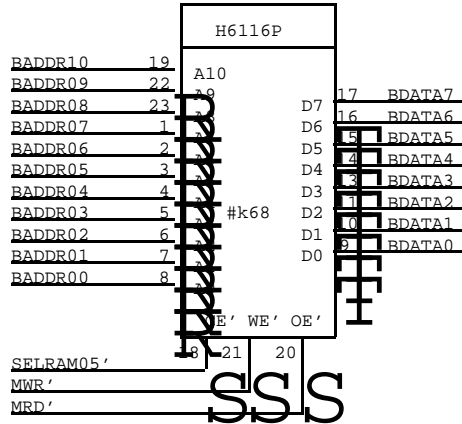
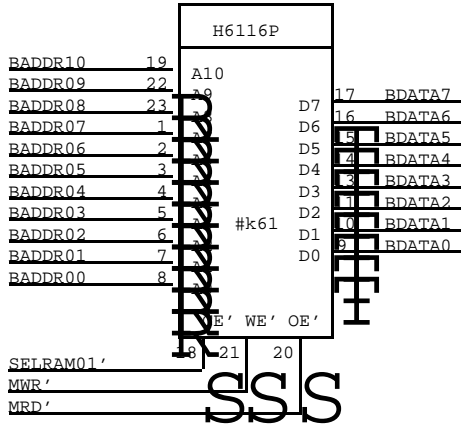
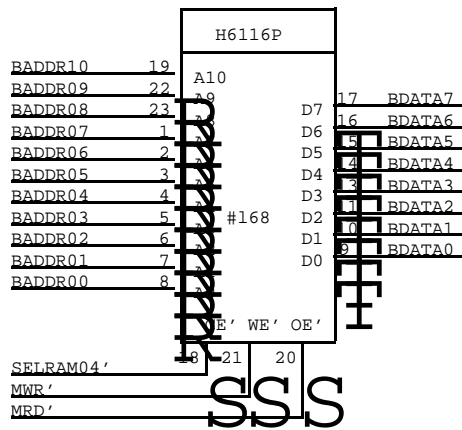
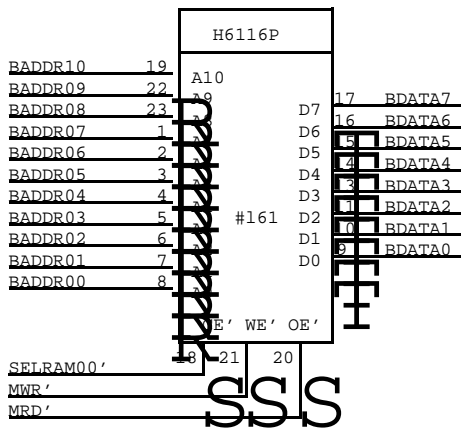
FE000 - FEFFF odd bytes only

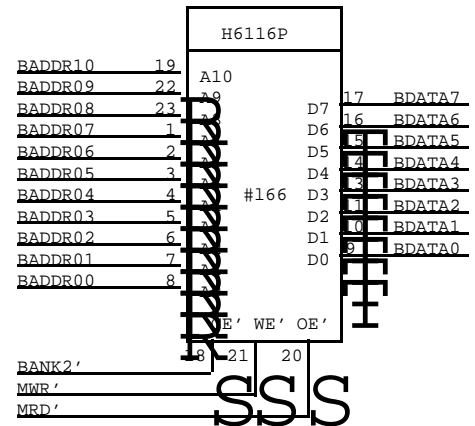
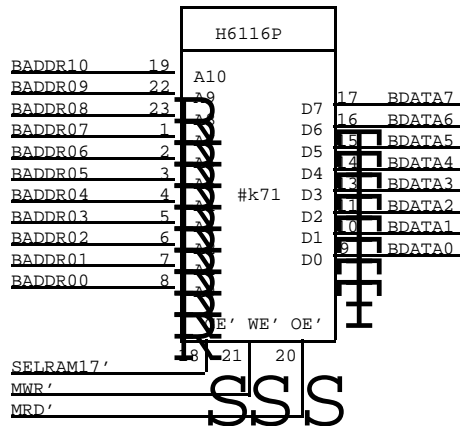
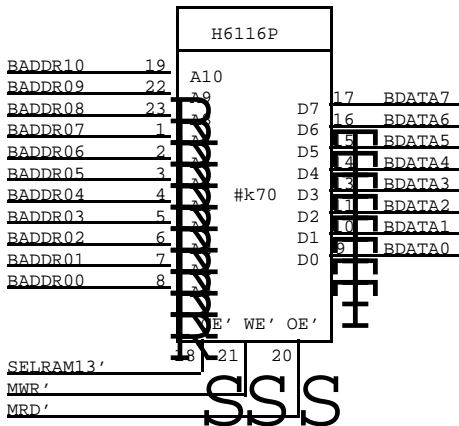
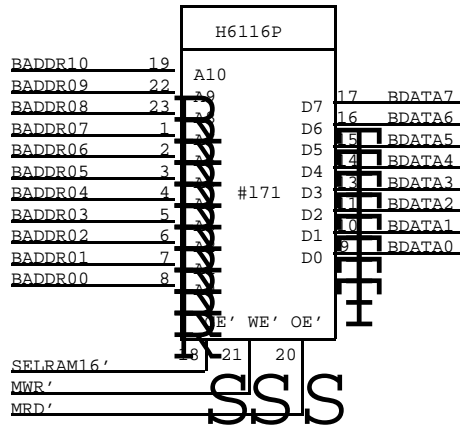
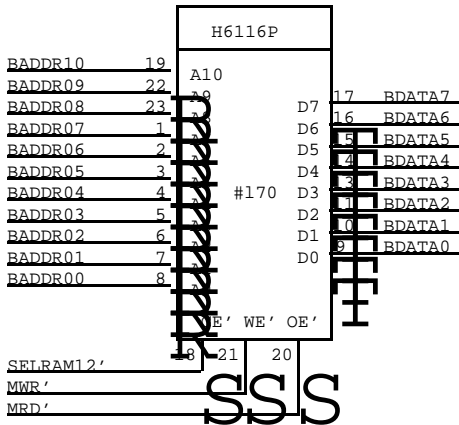
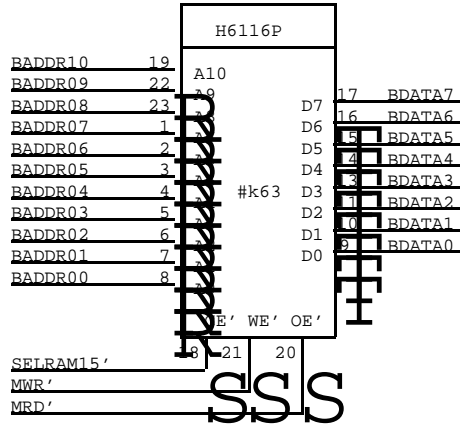
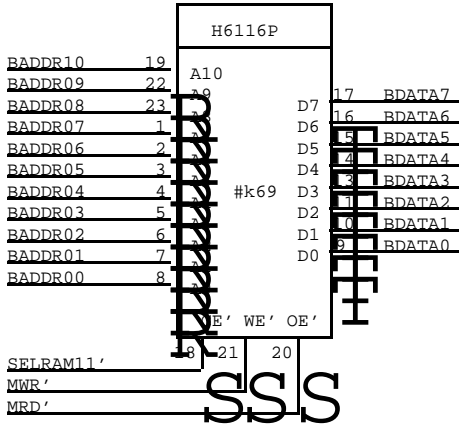
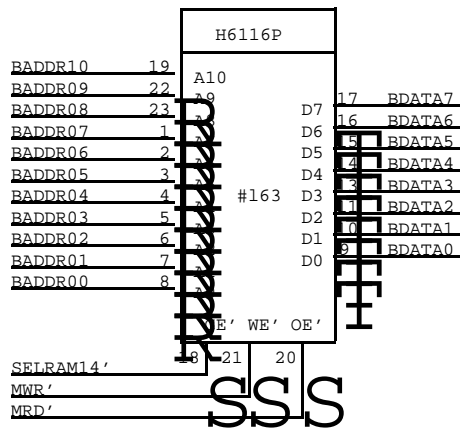
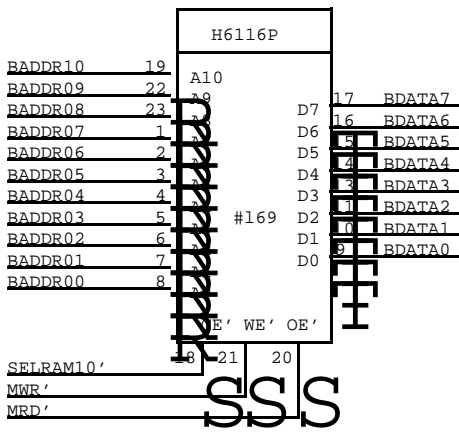


The other EPROMs will not immediately exist, but they are also set up for even and odd bytes. You must use both at once.

FE000 - FEFFF even bytes only

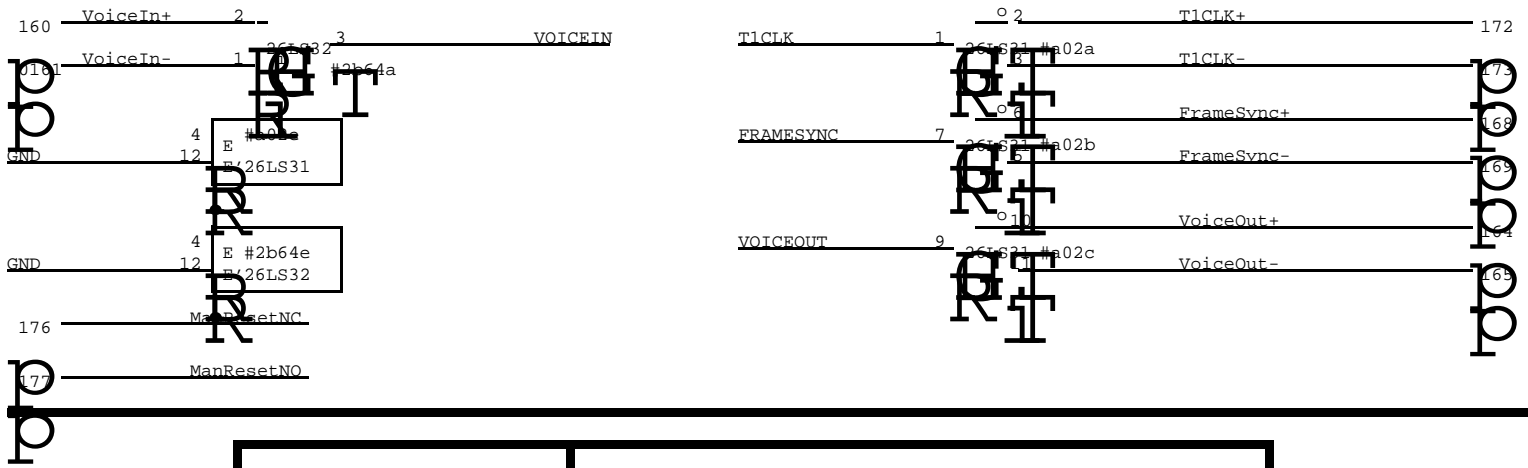




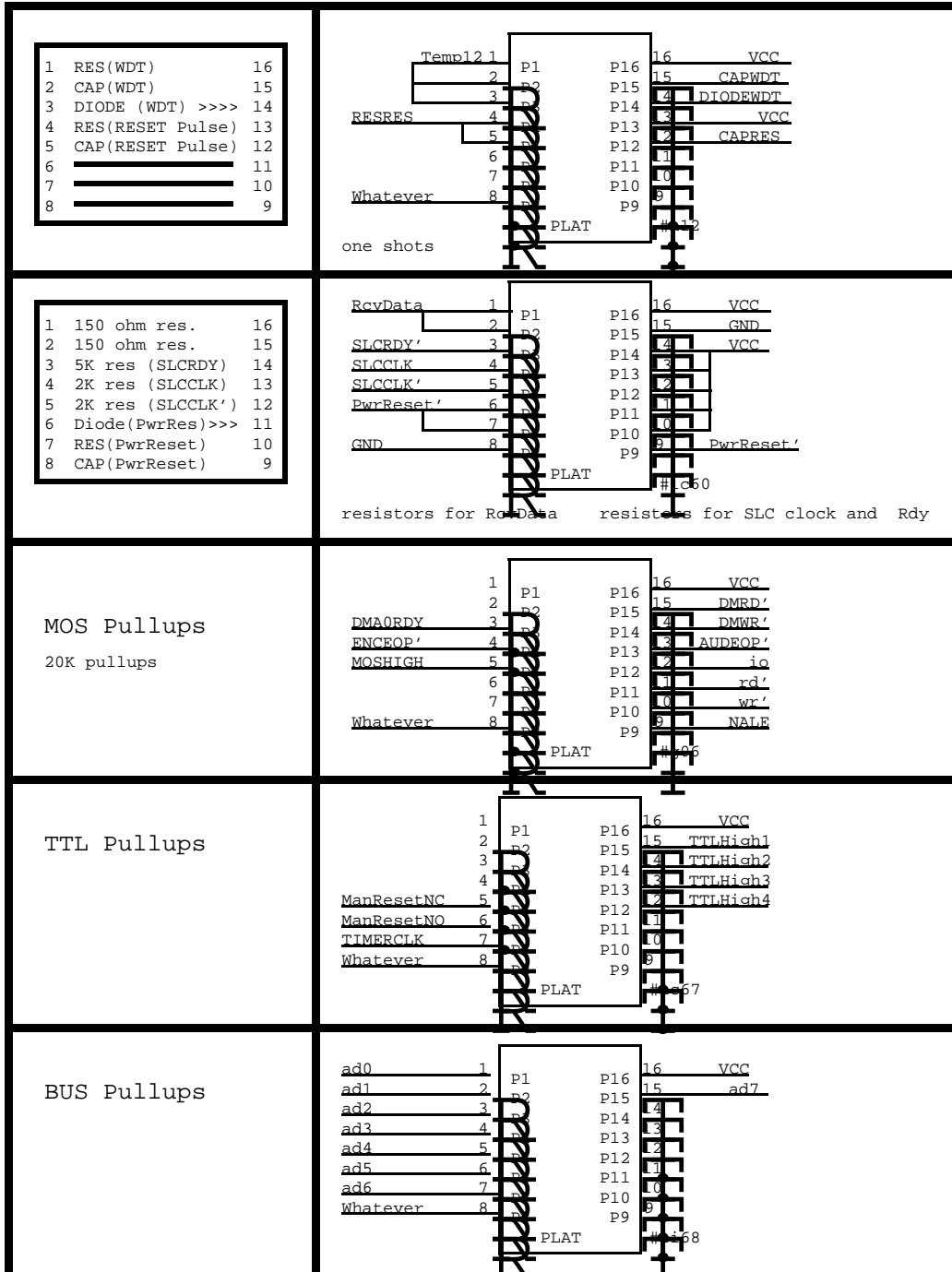


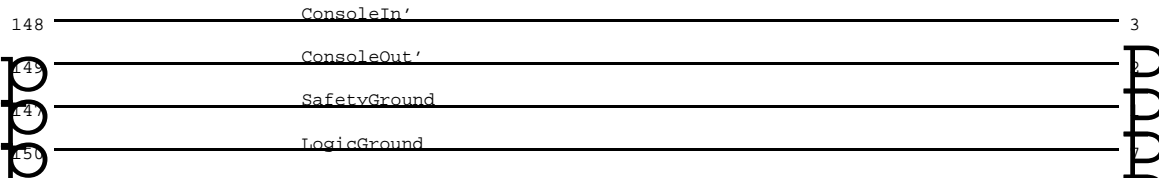
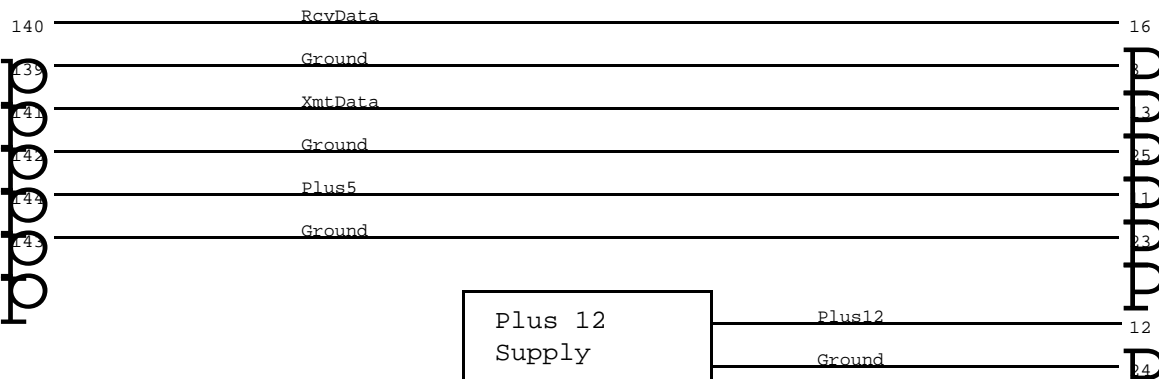
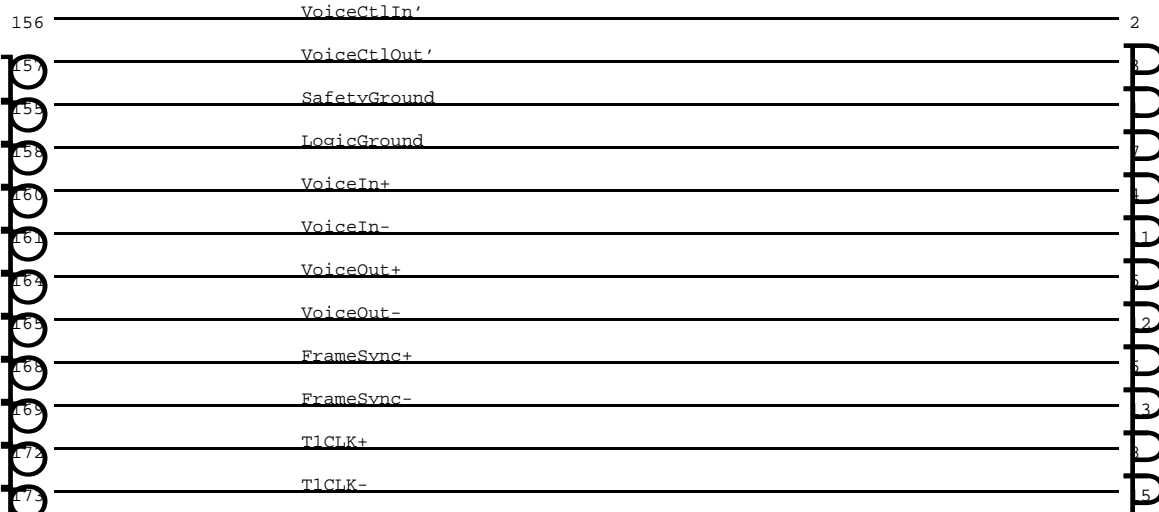
2K bytes of Audio Output
Repeats throughout the
third (10) 16K quadrant
of memory space

VOICE I/O

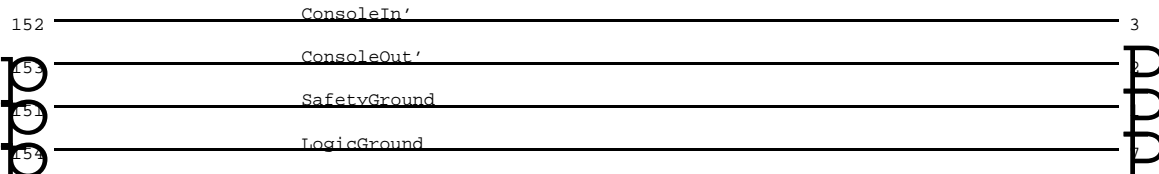


PLATFORMS



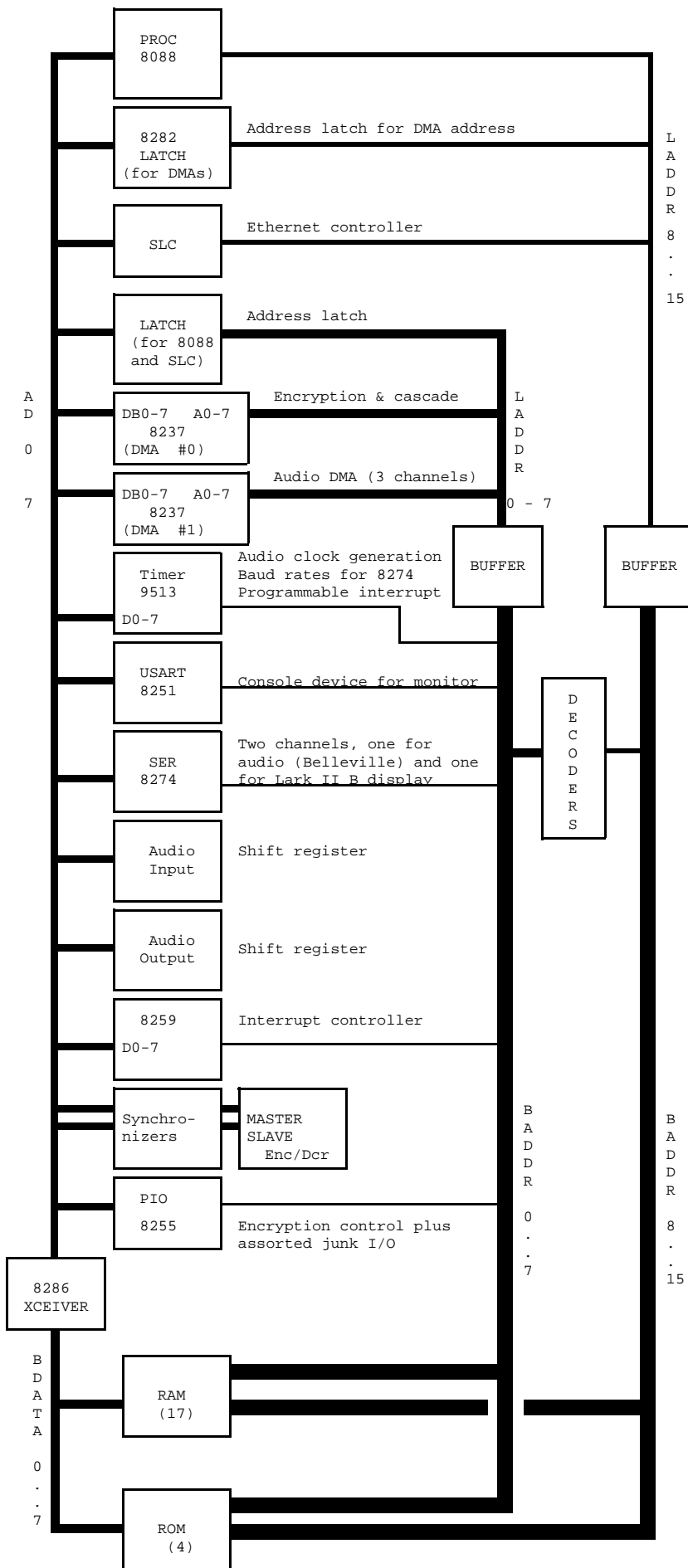


Note: leave enough slack for possible swap of pins 2 and 3



Note: leave enough slack for possible swap of pins 2 and 3





T1CLK
1.536MHZ



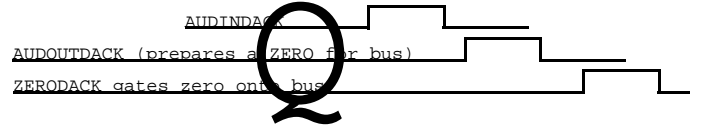
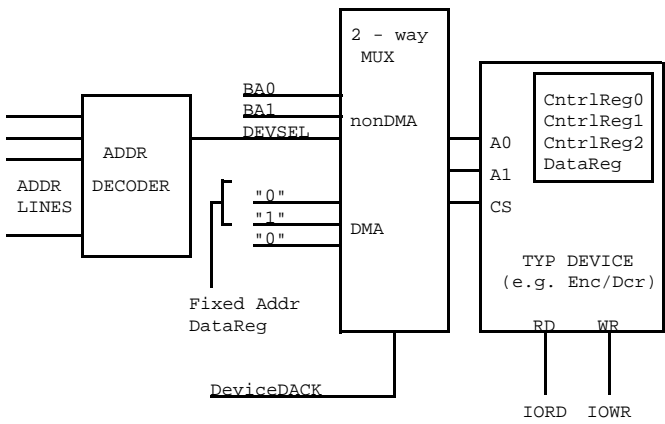
TSN (enable shifting)

FRAMESYNC

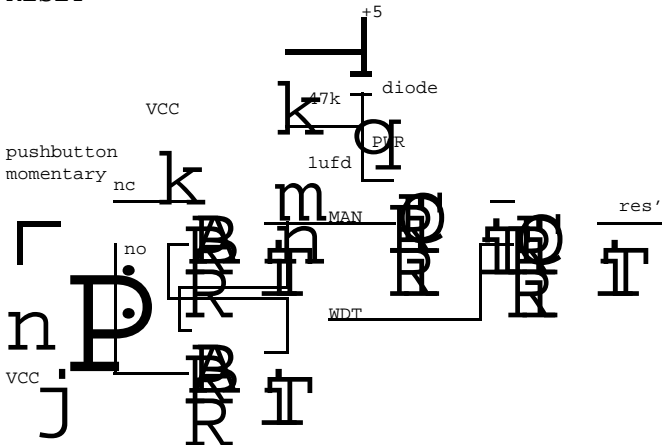
AUDIO TIMING

AUDININT - for 1 input and 2 output chs.

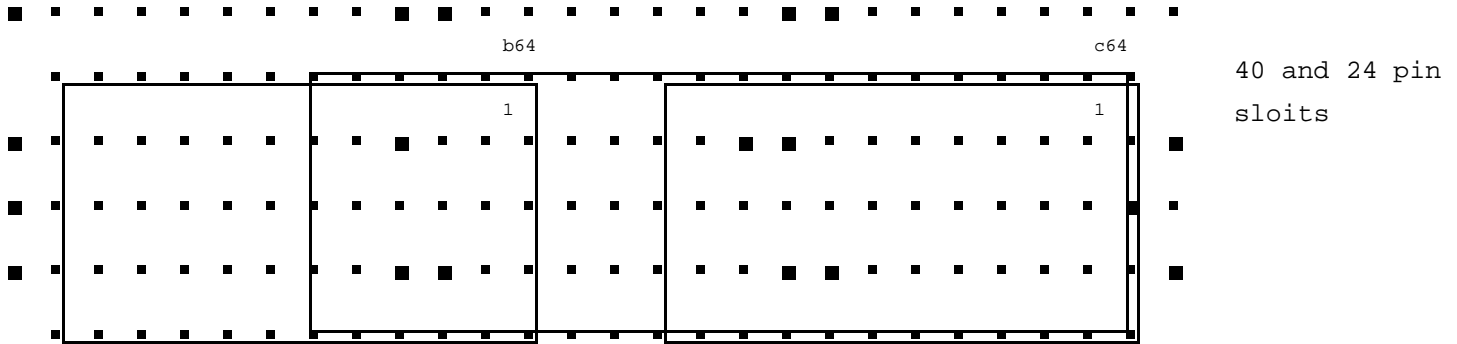
MUXING DMA/PROG ADDRESSING



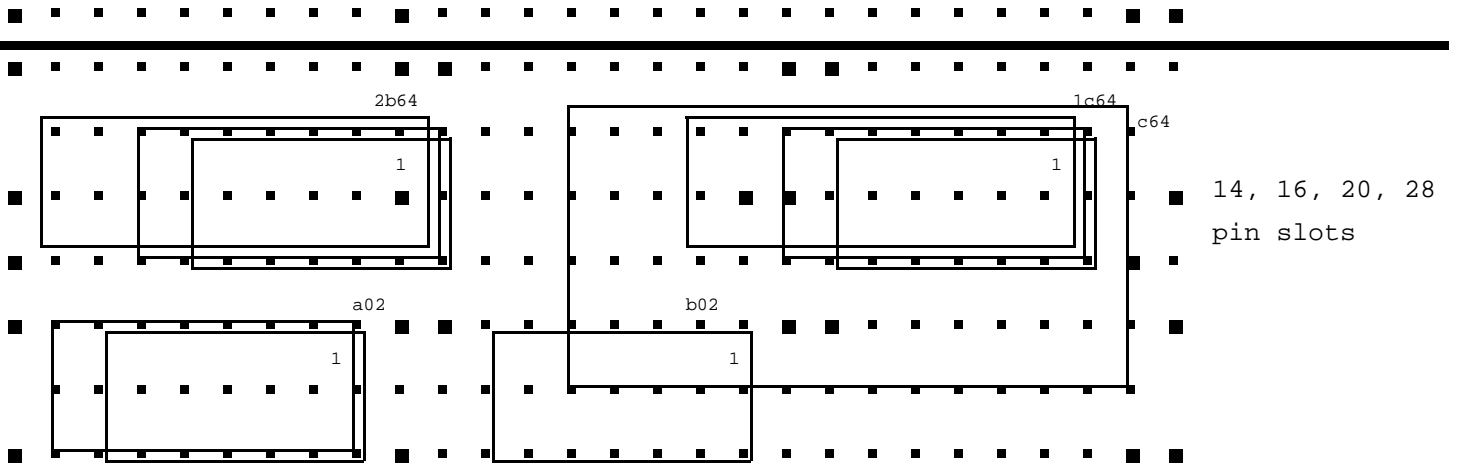
RESET



XEROX PARC	Project Voice	Reference Miscellaneous	File ETP37.sil	Designer S. Ornstein L. Stewart	Rev Ae	Date 2/07/82	Page 37
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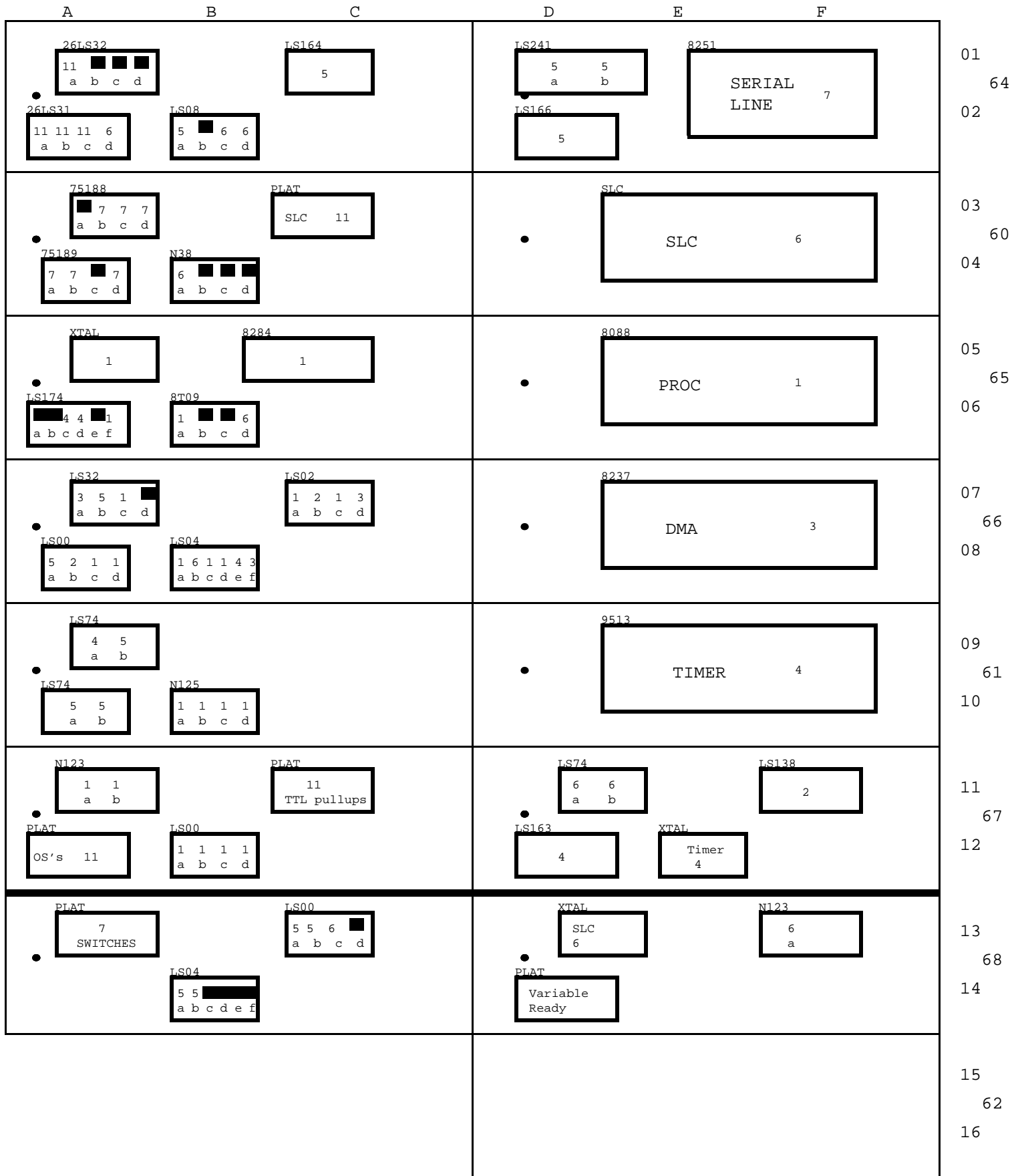
40 and 24 pin
slots

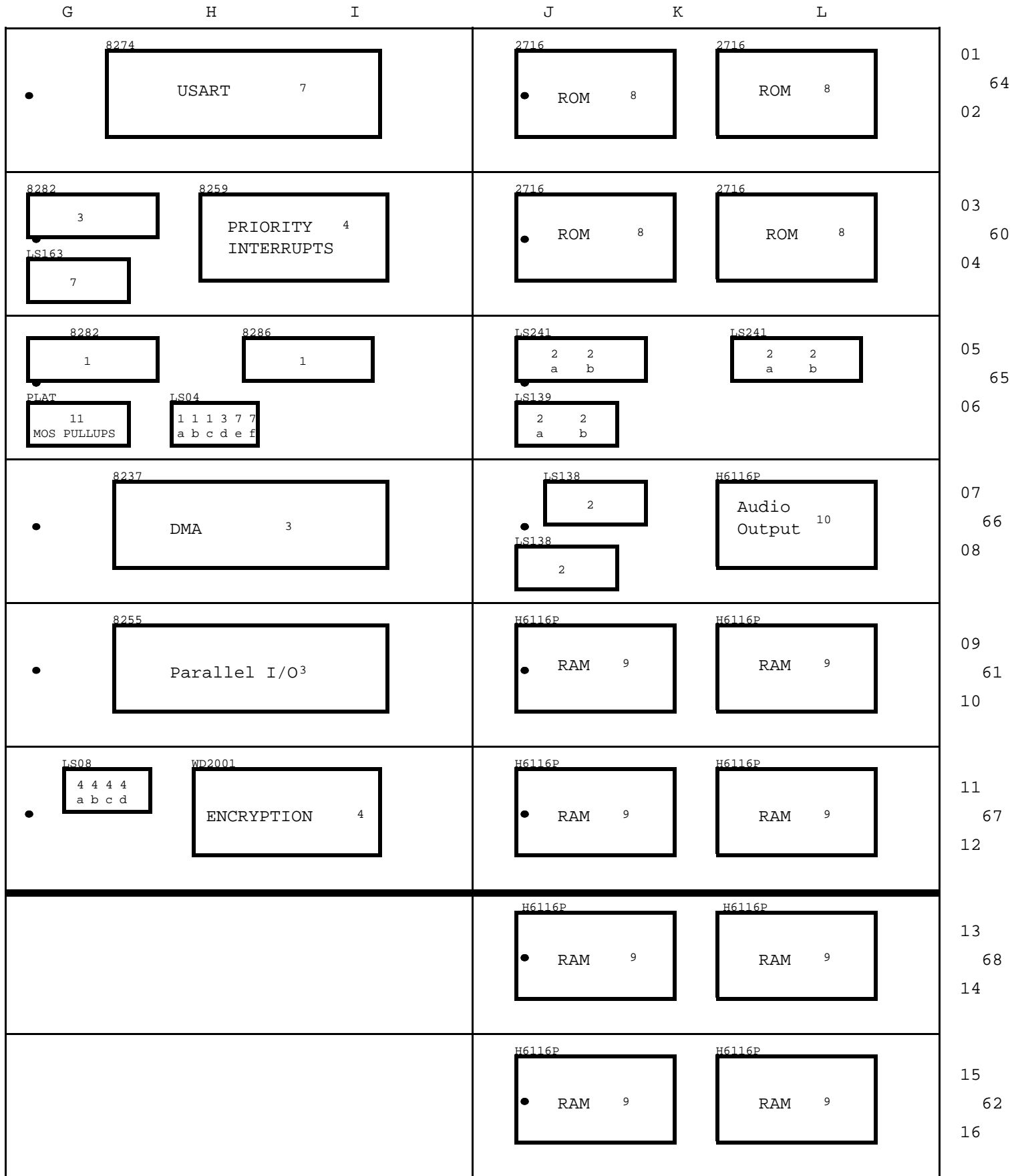


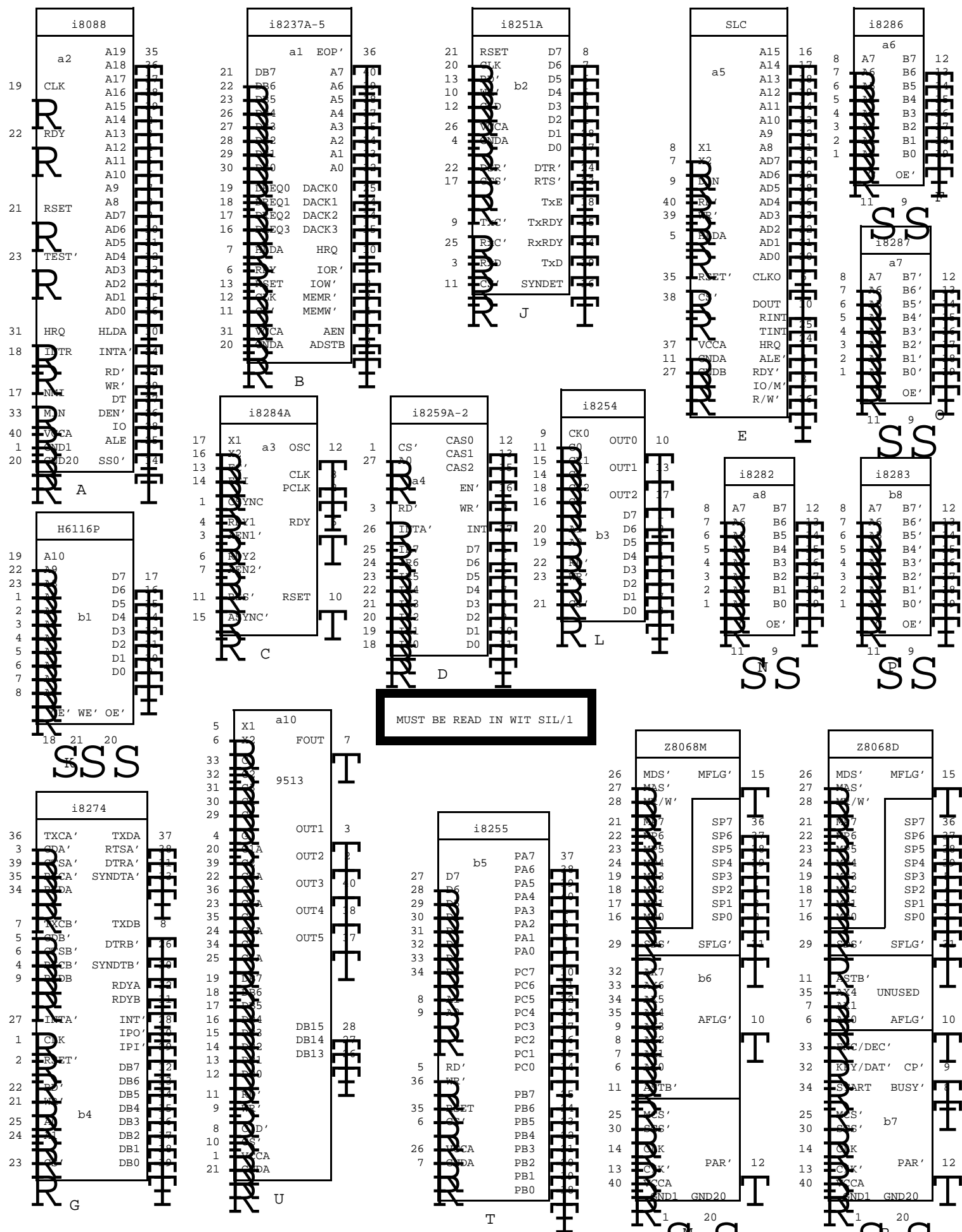
14, 16, 20, 28
pin slots

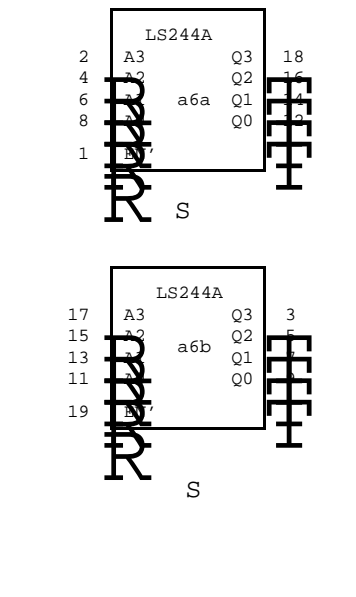
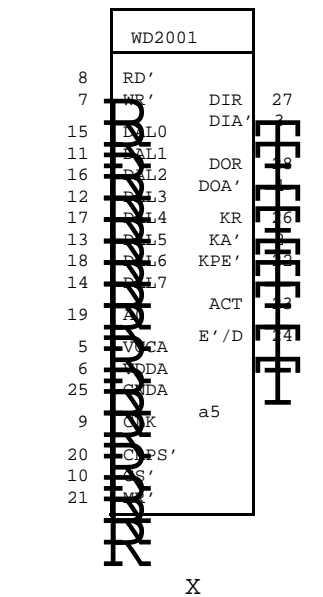
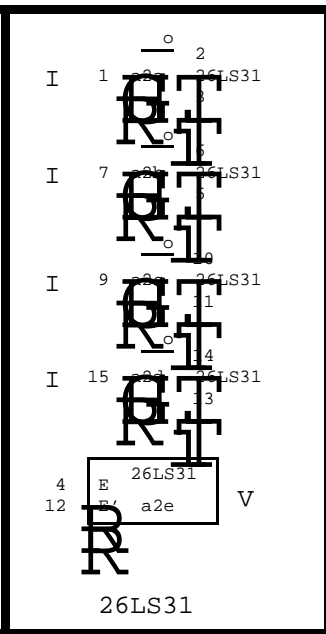
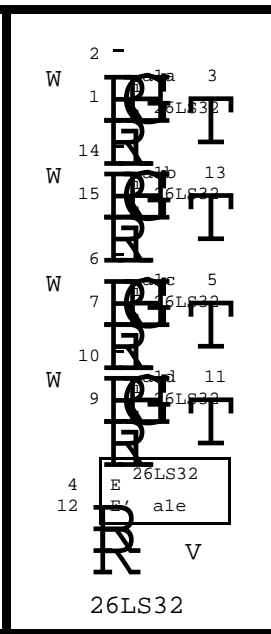
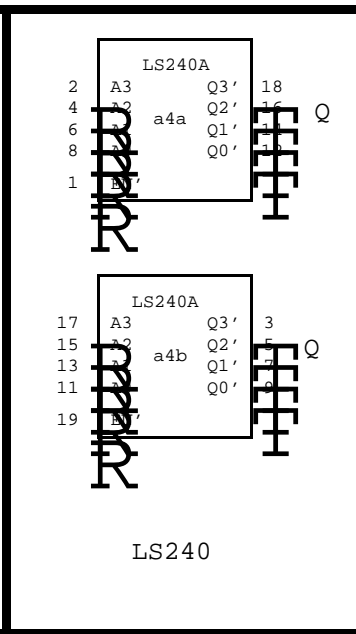
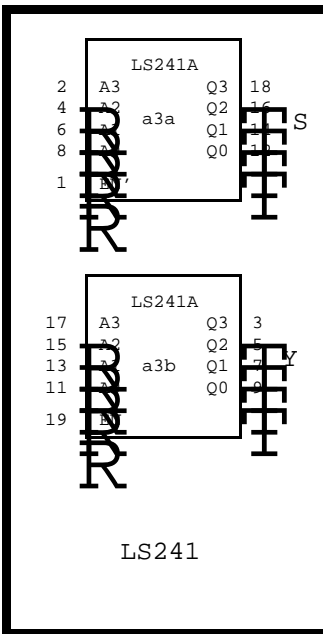
Possible chip locations, choose one

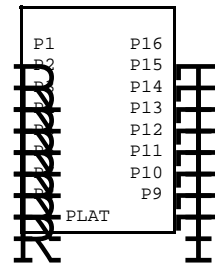
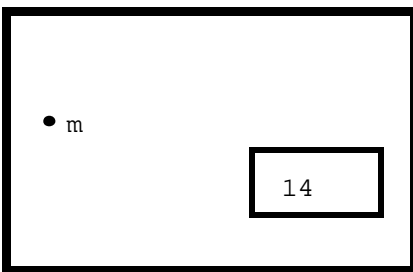
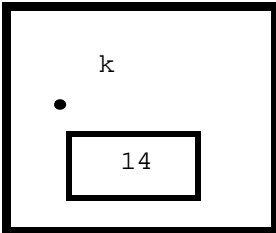
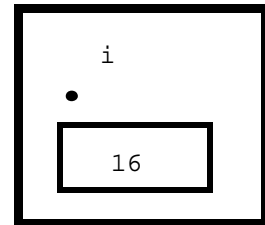
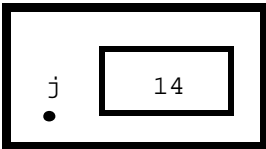
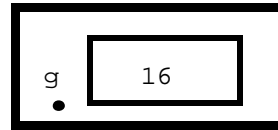
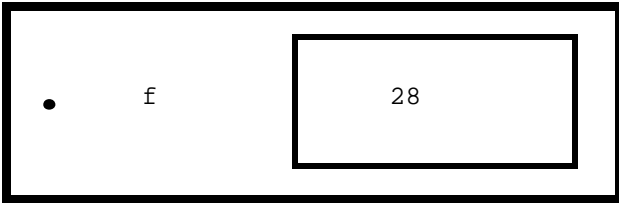
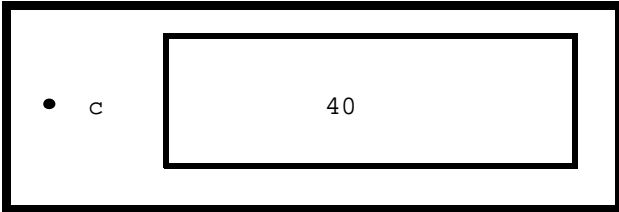
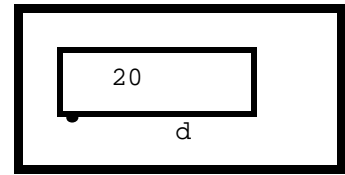
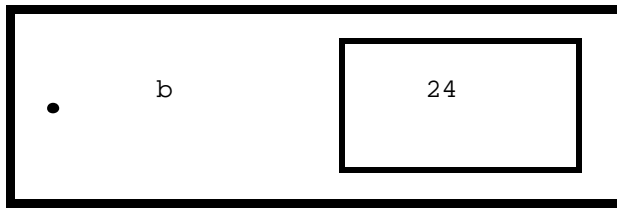
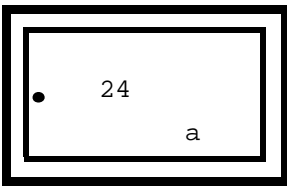
pins	columns		rows	
	left	right	top	bottom
40	c, f	k, l	64, 60, 65, 66, 61, 68	72, 69, 70, 63, 71
28	c, f	k, l	64, 60, 65, 66, 61, 68	72, 69, 70, 63, 71
24	b, c, e, f	h, i, k, l	64, 60, 65, 66, 61, 68	72, 69, 70, 63, 71
20	2b, 1c, 2e, 1f	2h, 1i, 2k, 1l	64, 60, 65, 66, 61, 68	72, 69, 70, 63, 71
16	2b, 1c, 2e, 1f	2h, 1i, 2k, 1l	64, 60, 65, 66, 61, 68	72, 69, 70, 63, 71
	a, d	g, j	02, 04, 06, 08, 10, 14	16, 18, 20, 22, 24
14	2b, 1c, 2e, 1f	2h, 1i, 2k, 1l	64, 60, 65, 66, 61, 68	72, 69, 70, 63, 71
	a, b, d, e	g, h, j, k	02, 04, 06, 08, 10, 14	16, 18, 20, 22, 24











L

