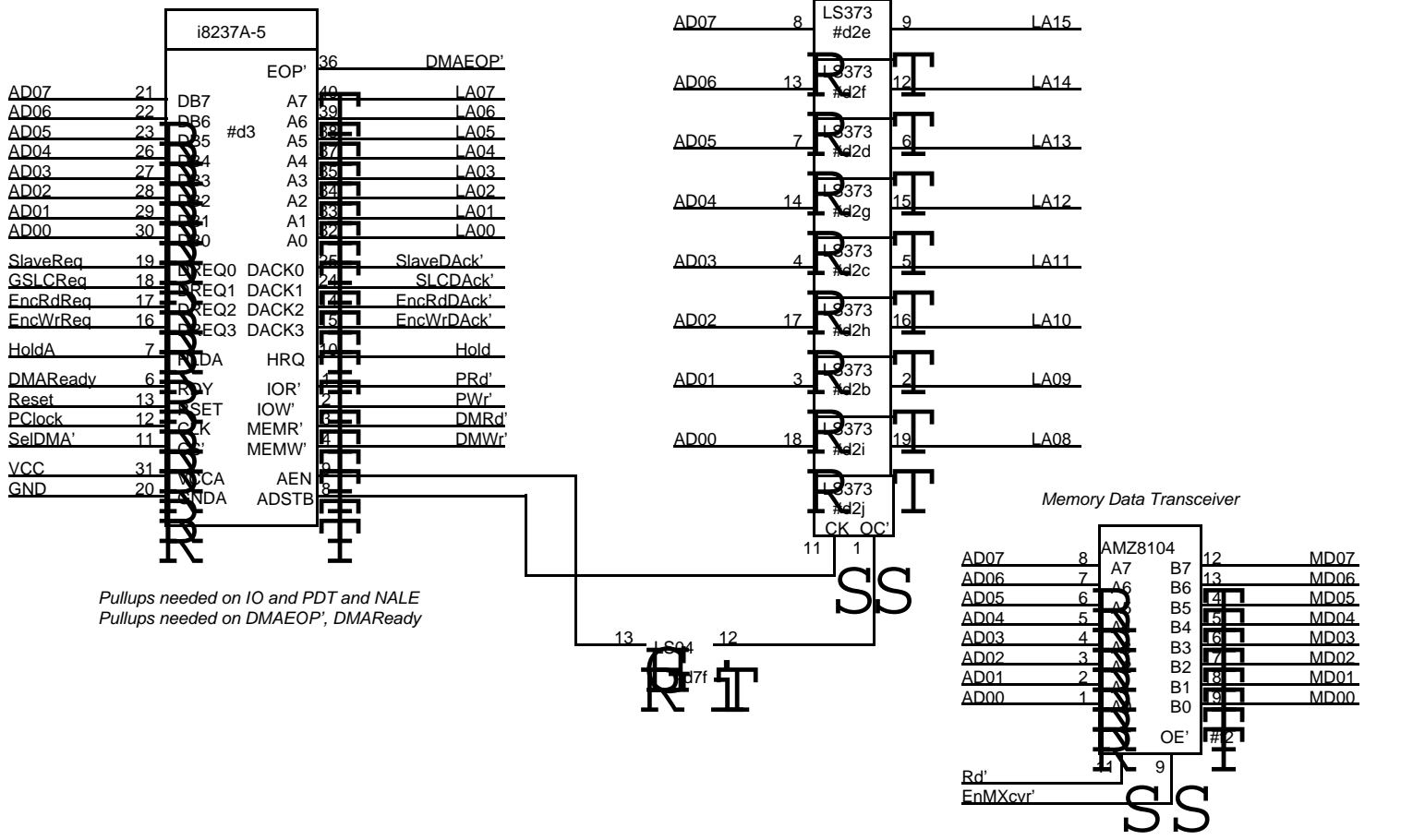
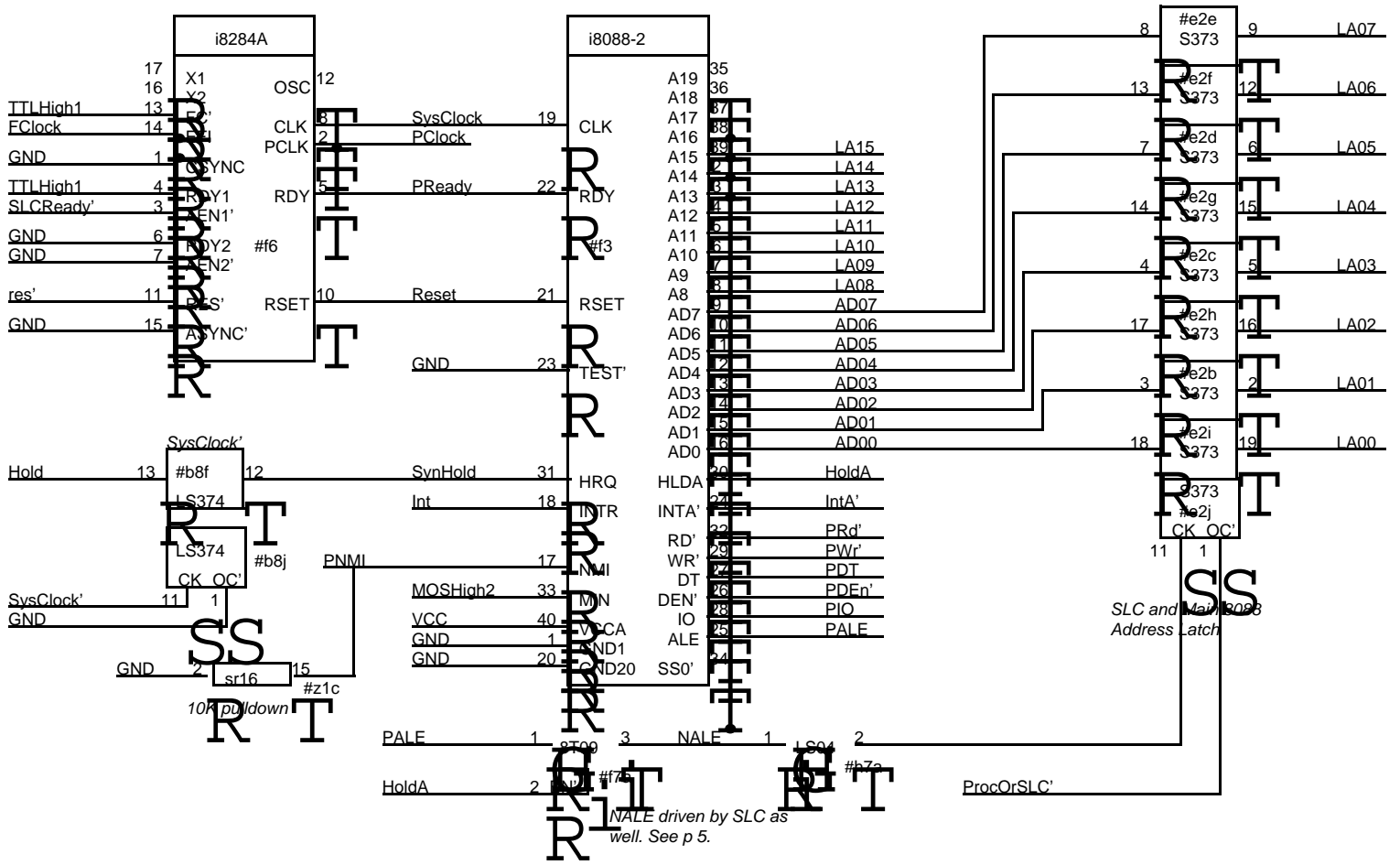


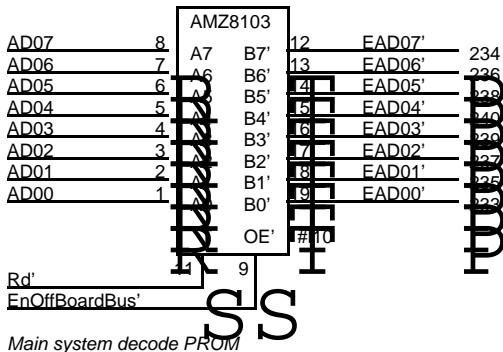
L A R K DIGITAL BOARD

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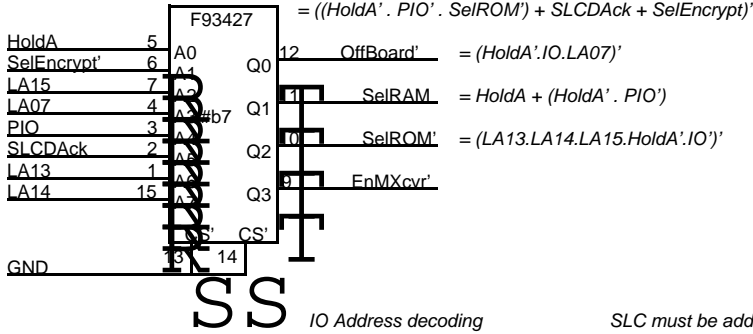
<u>TITLE</u>	<u>Page</u>
Main 8088 _____	01
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Off board data bus transceiver

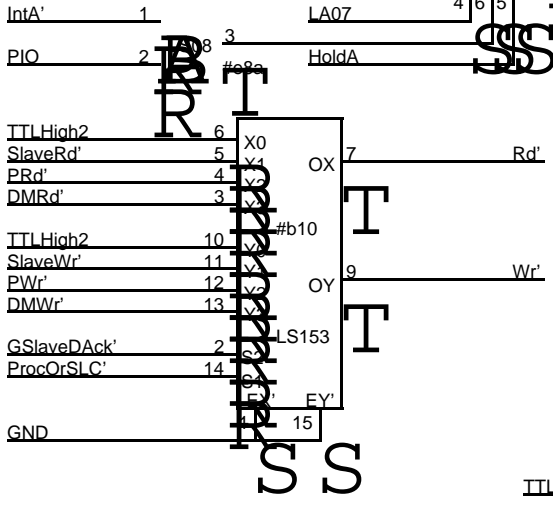
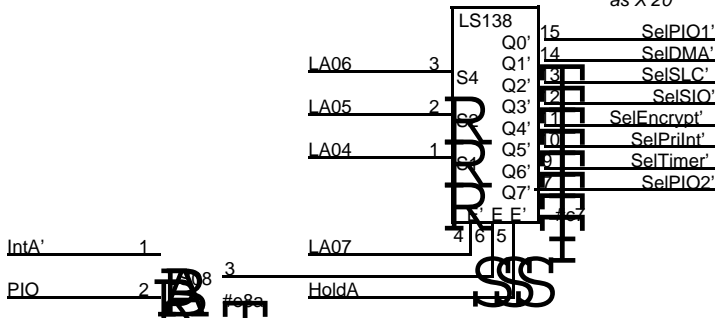


Main system decode PROM

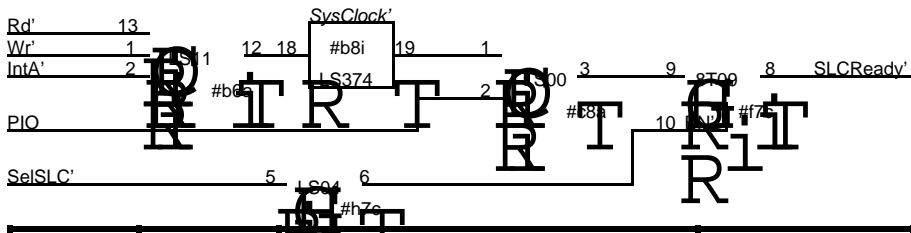


IO Address decoding

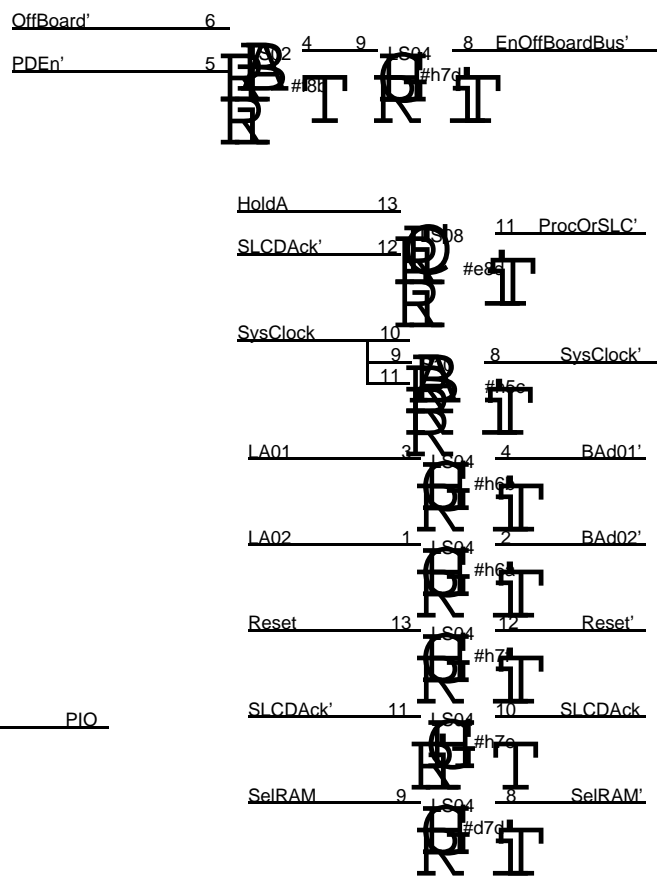
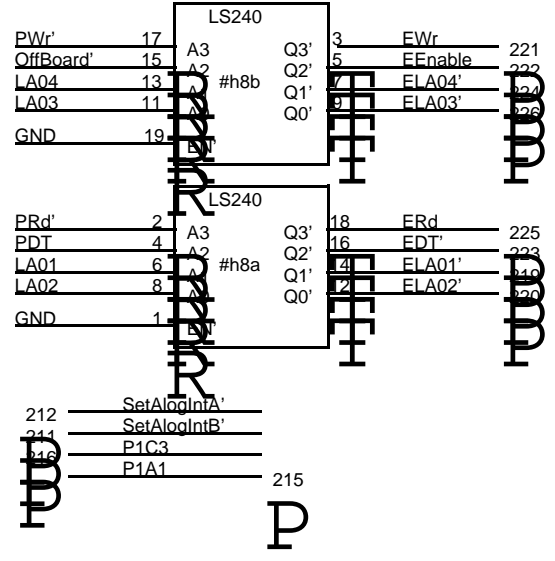
SLC must be addressed as X'20'



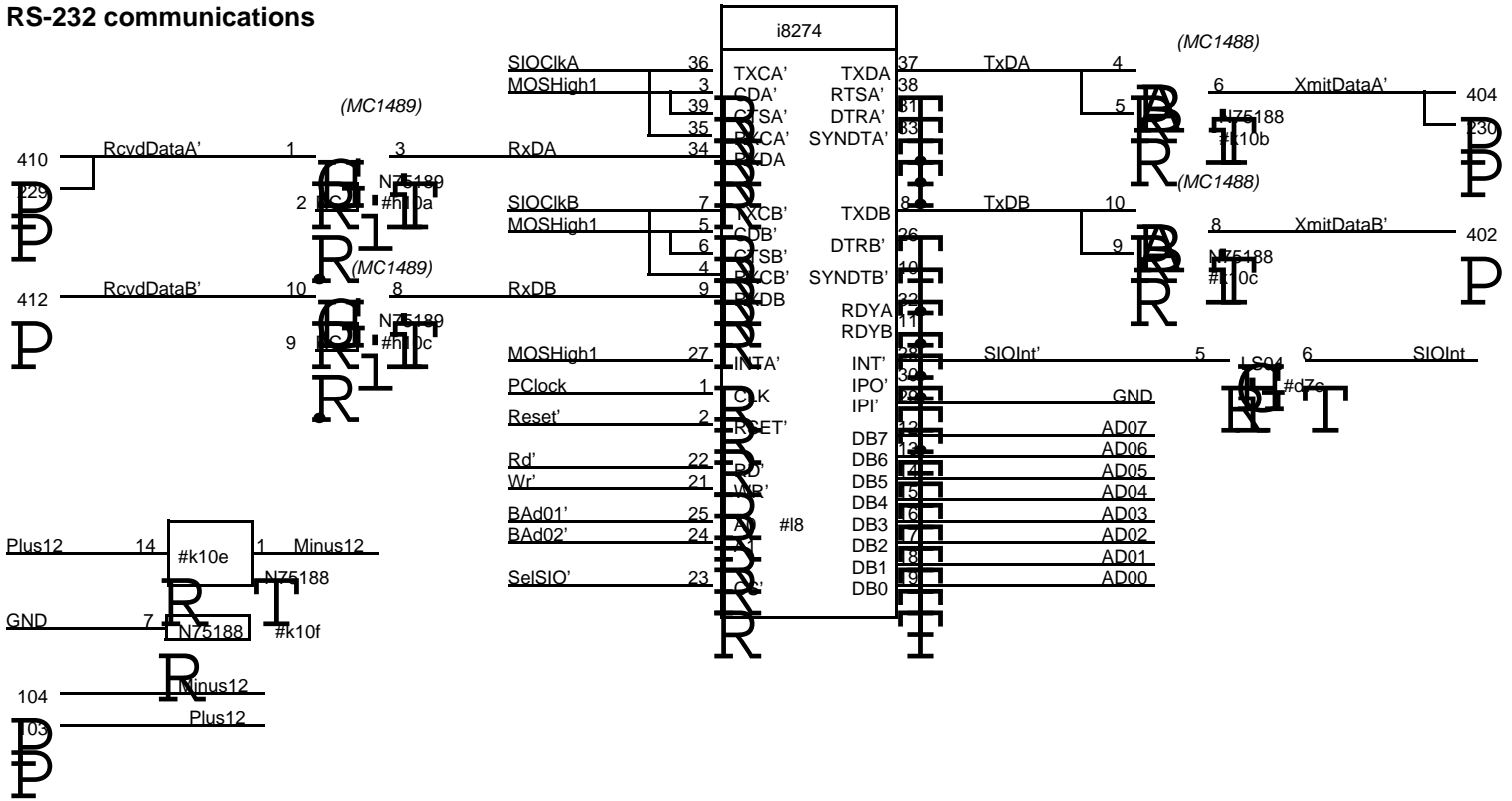
Wait state generator for Main CPU IO references



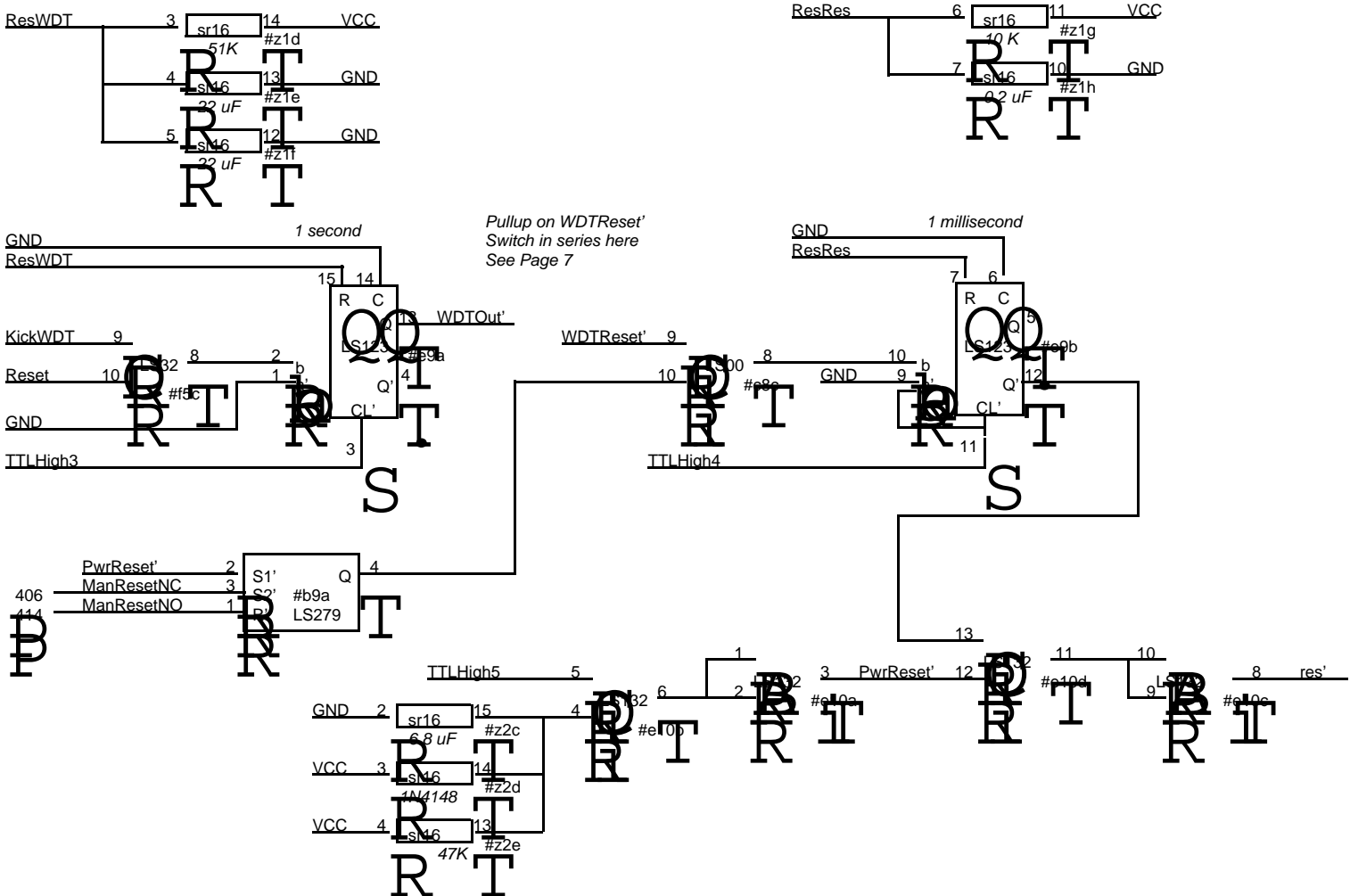
Off board control signal drivers



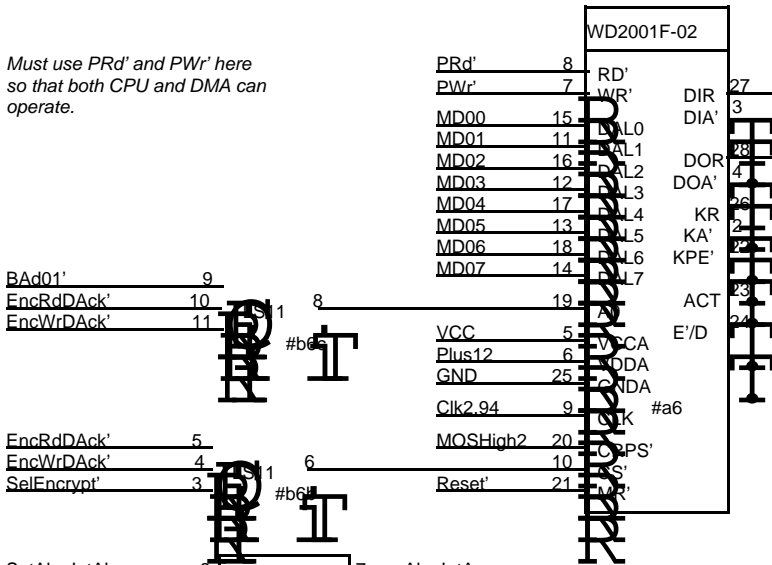
**RS-232 communications**



**Watchdog timer and Reset circuit**

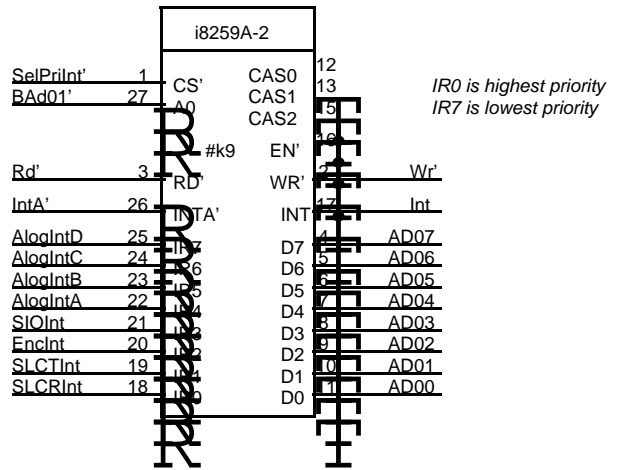
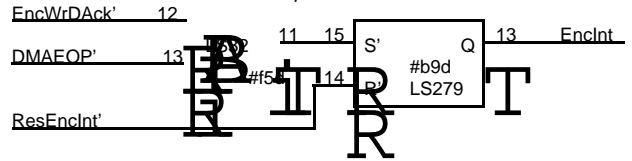
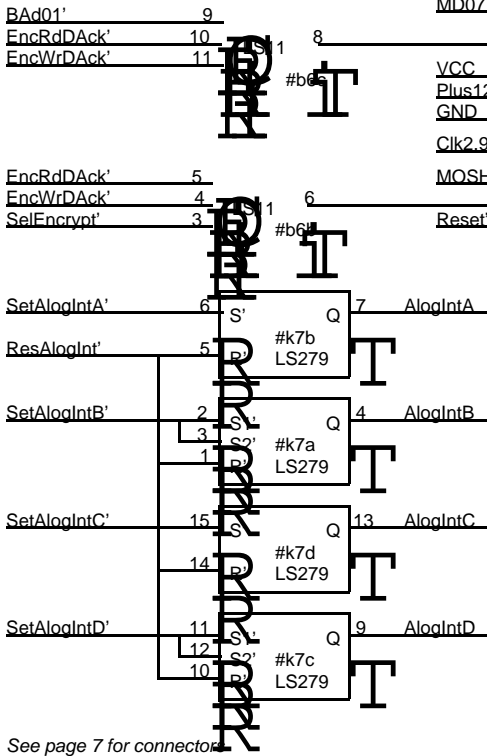


Must use PRd' and PWr' here so that both CPU and DMA can operate.

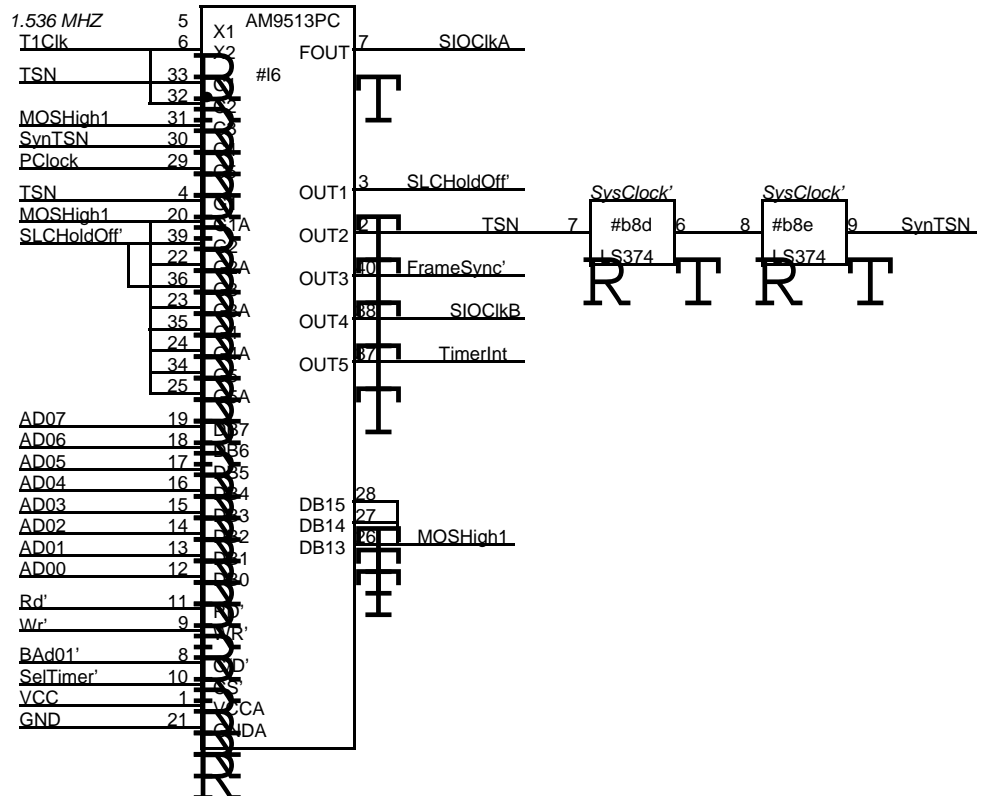


Encryption chip is on memory data bus in order to extend write hold time from CPU.

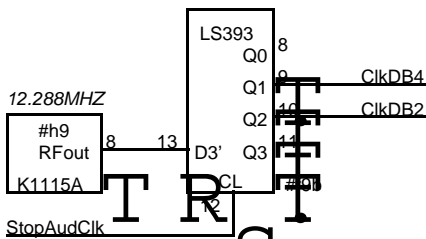
When decrypting, must check that Master DMA is complete



See page 7 for connector



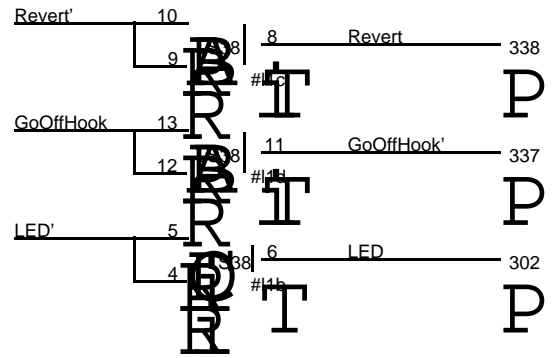
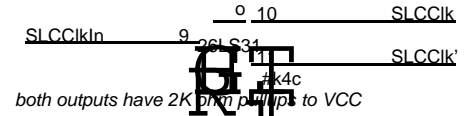
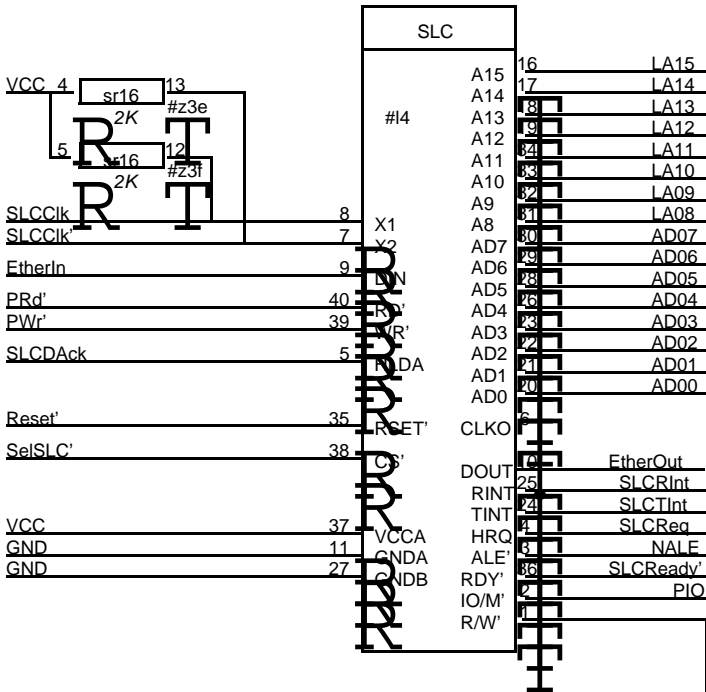
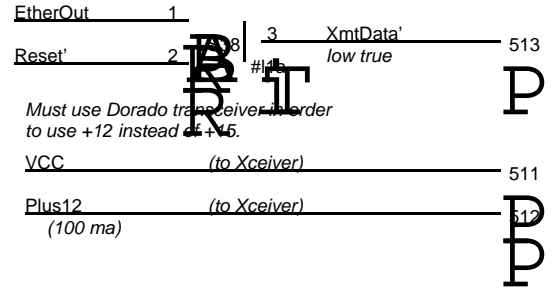
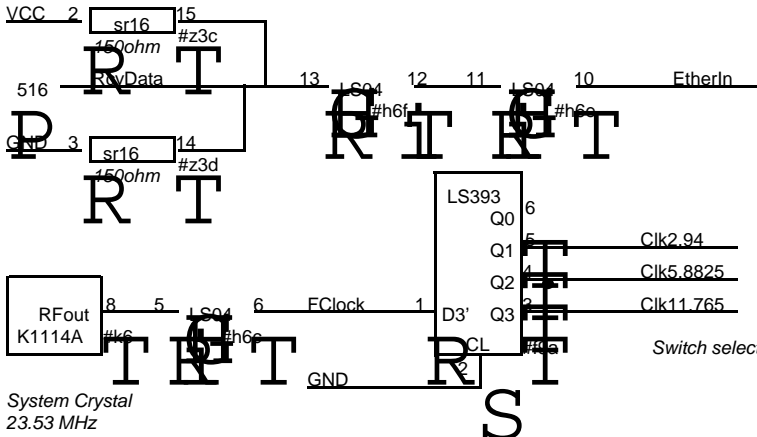
Need pullup on T1Clk



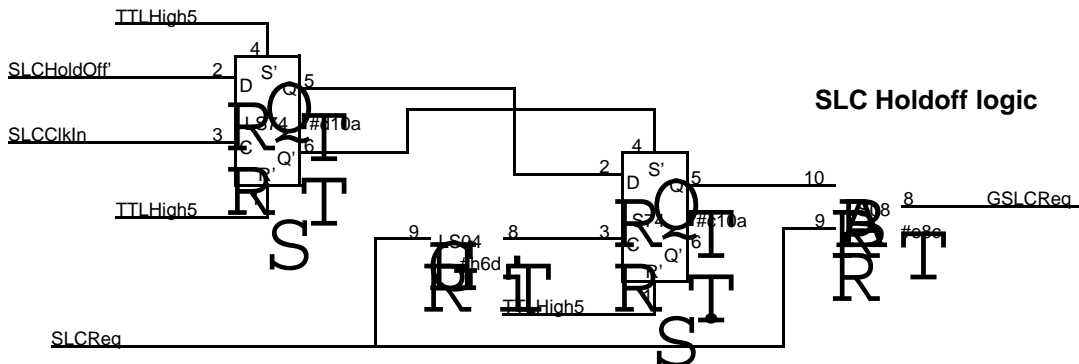
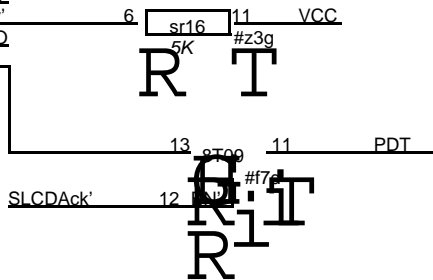
If StopAudClk' is low, refresh stops. Can program refresh to run from PClock!

**ETHERNET DRIVE/RECEIVE**

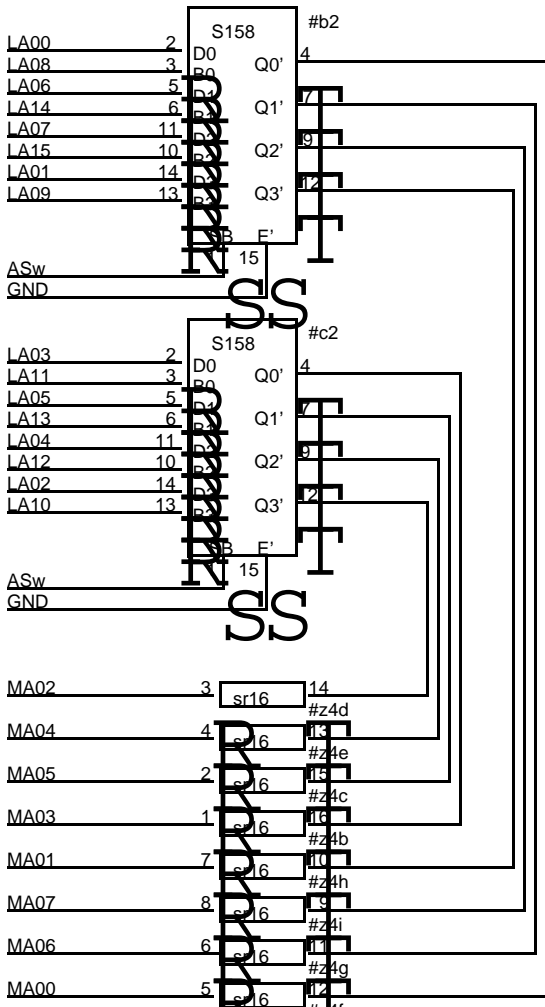
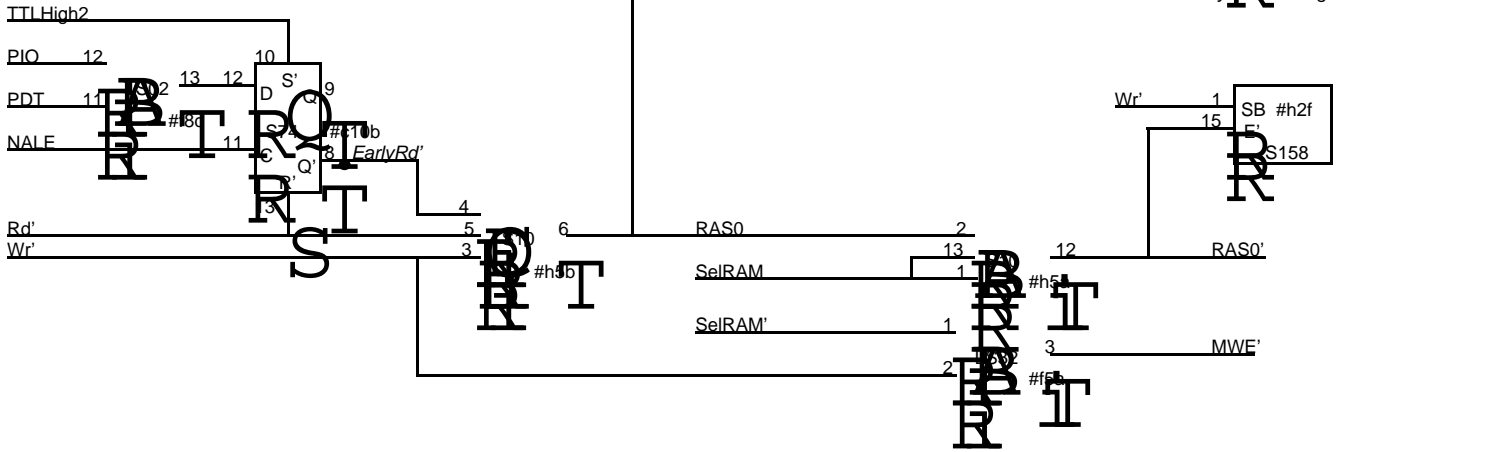
SLC floats EtherOut during and after Reset!



SLCReady' controlled on page 2.  
Also used on Page 1.

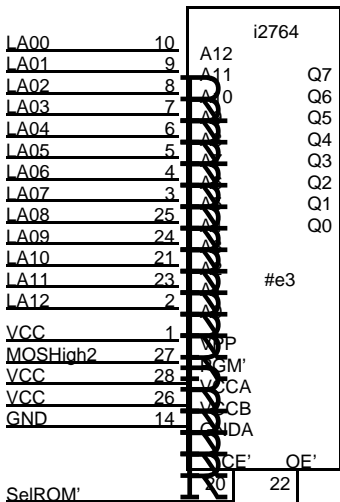


This circuit provides advance warning of Main processor and SLC memory reads

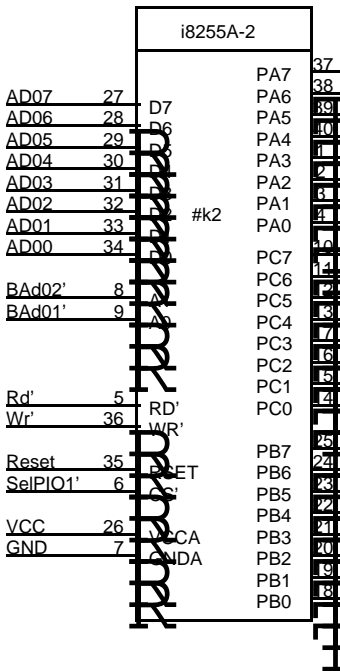


to memory  
27 ohm resistor DIP  
Damping resistors for  
the memory address lines.

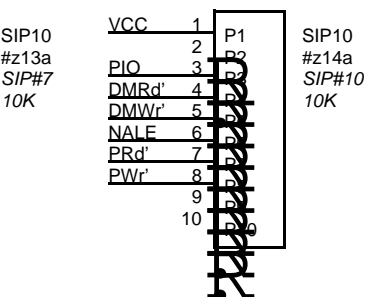
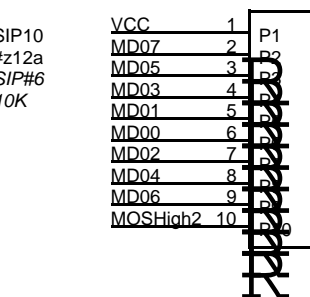
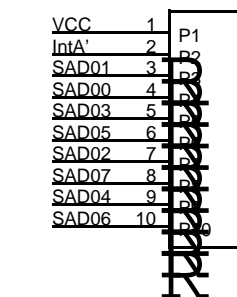
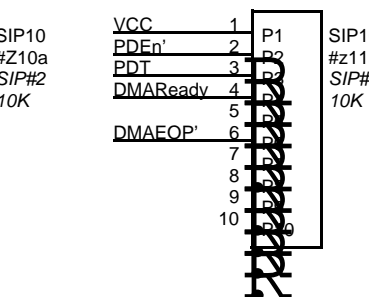
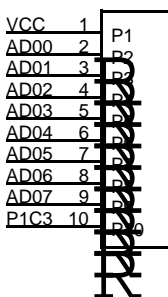
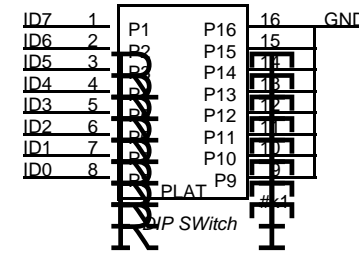
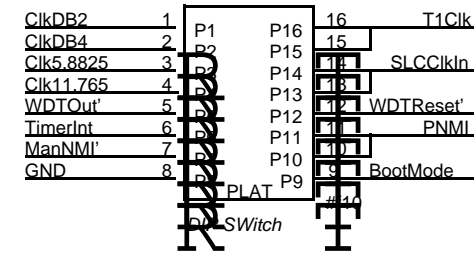
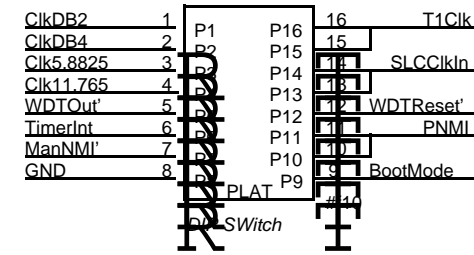
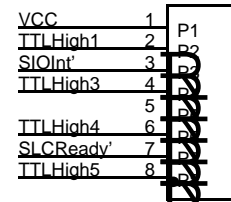
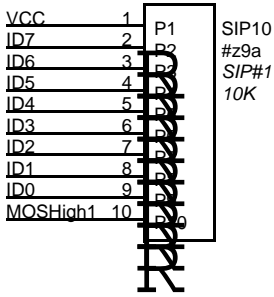
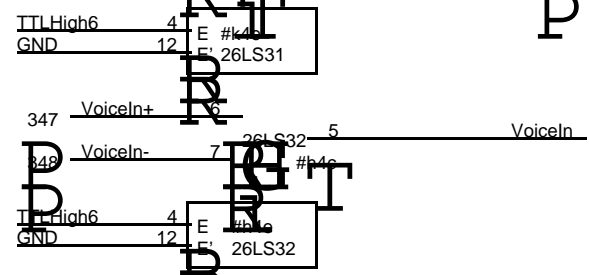
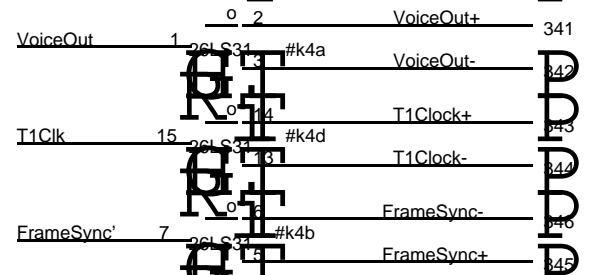
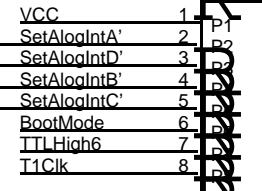
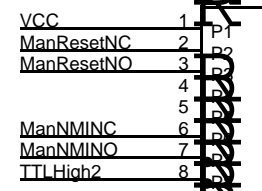
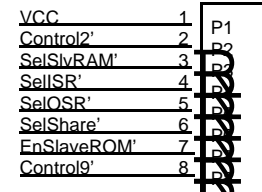
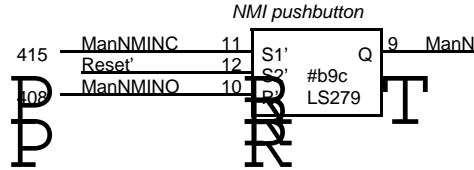
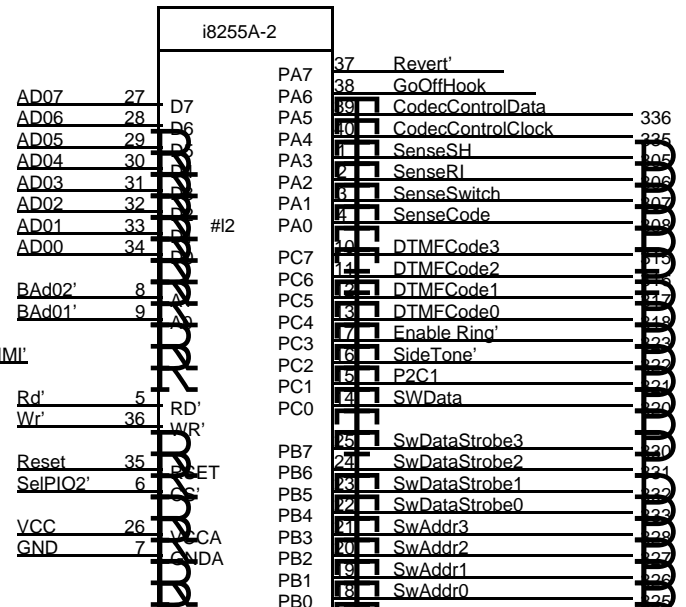
Main CPU EPROM



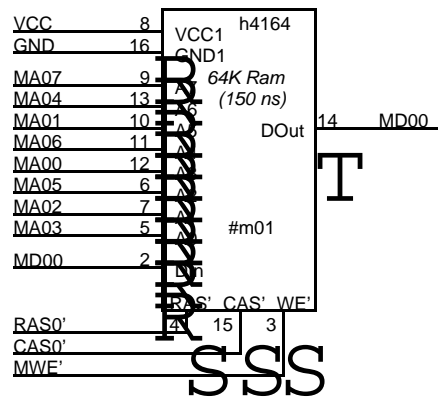
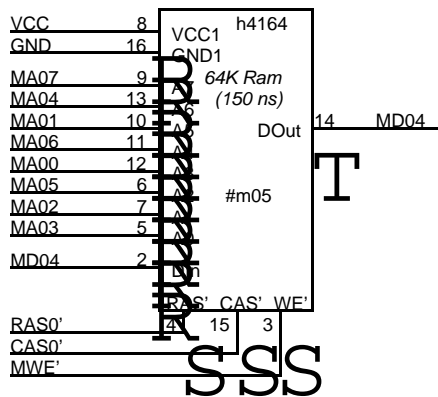
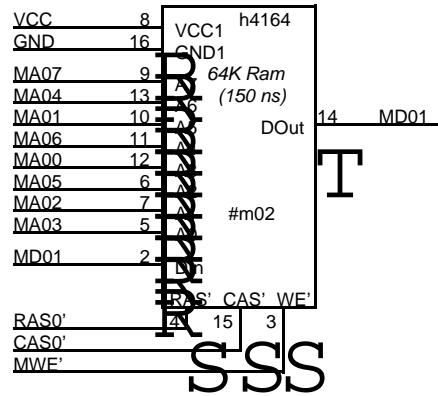
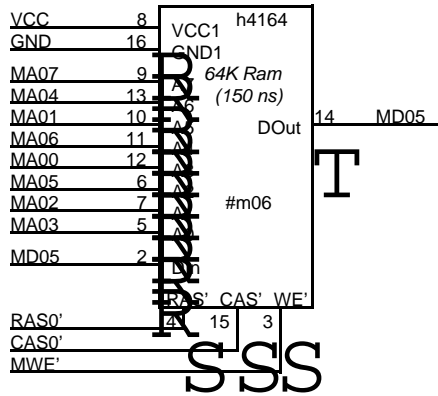
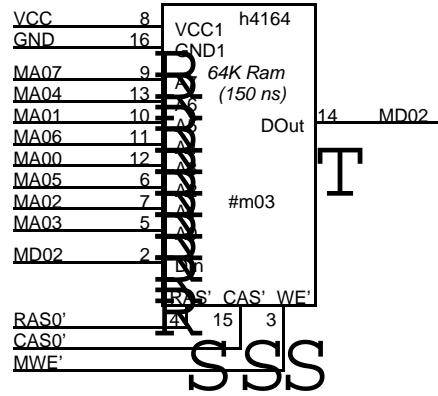
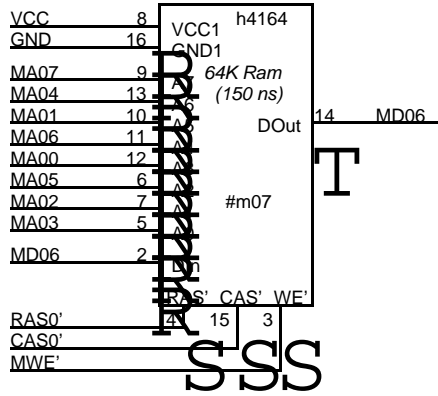
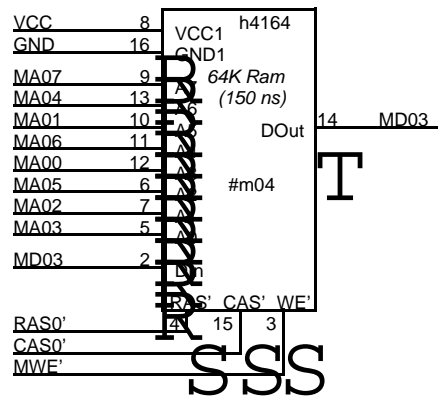
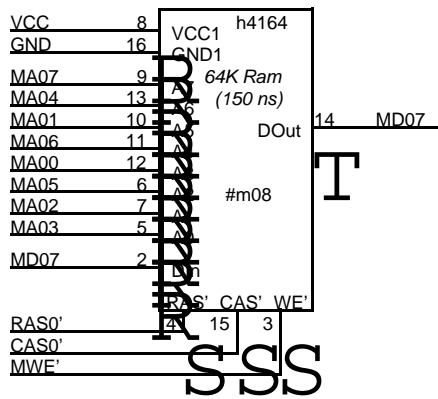
Main CPU Parallel port

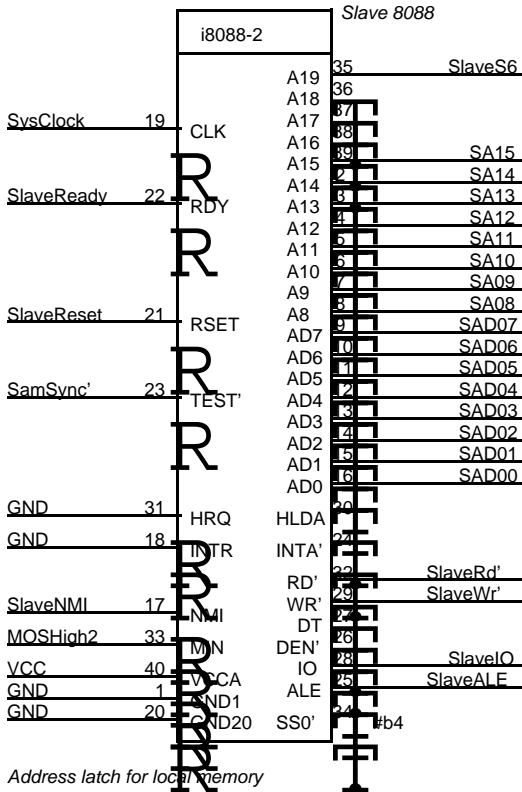


Extra IO PIO



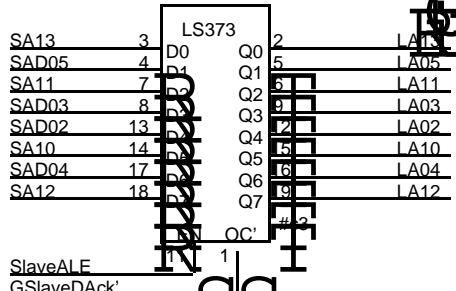
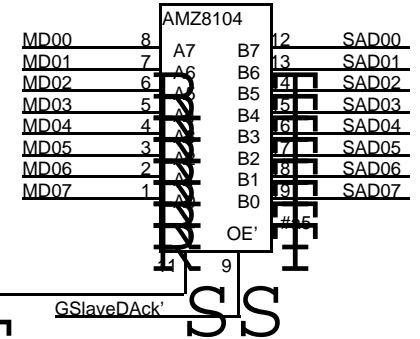
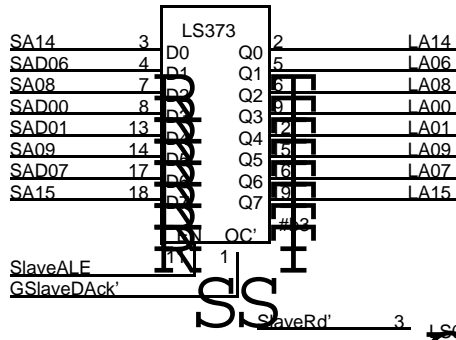




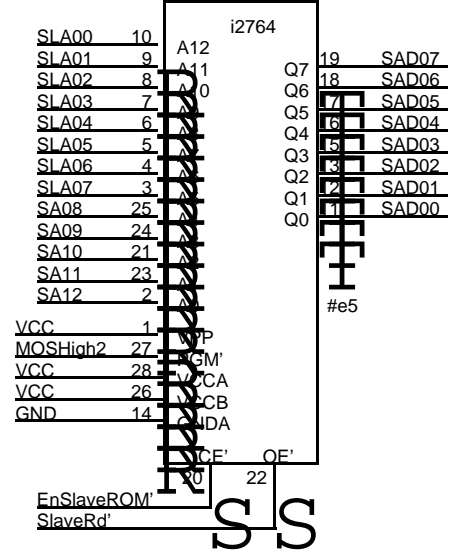


Address latches for shared memory

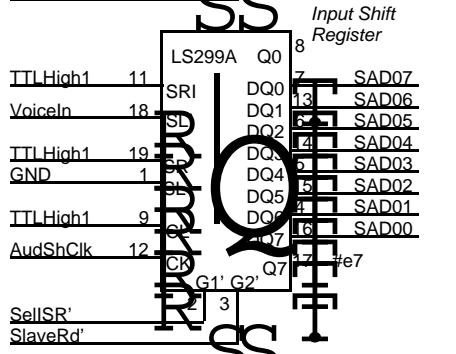
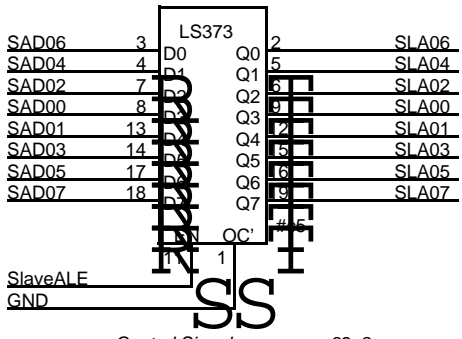
Bus transceiver to shared memory



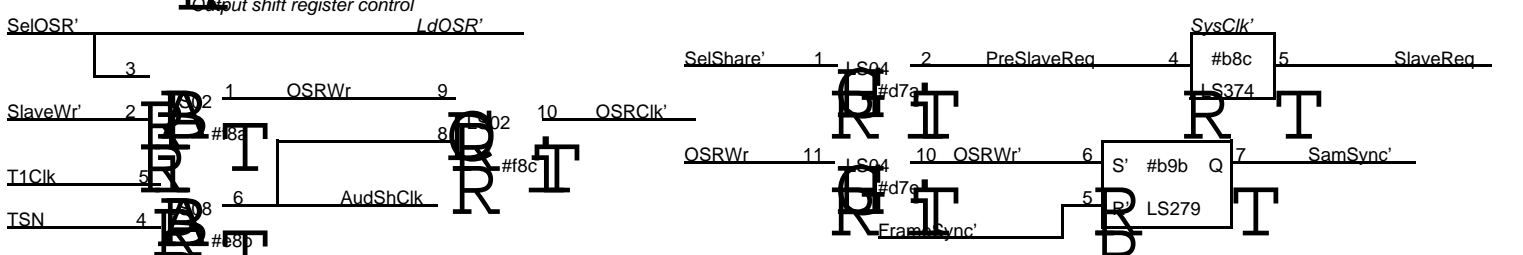
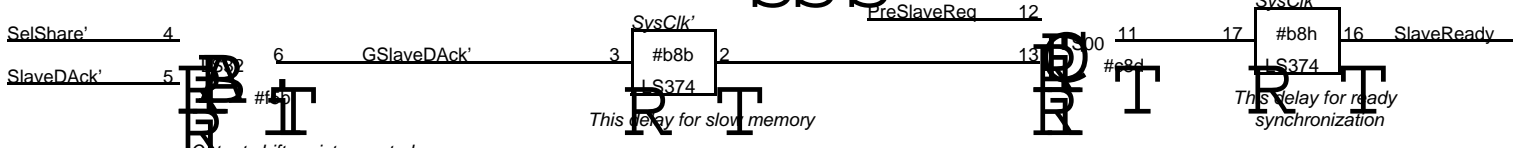
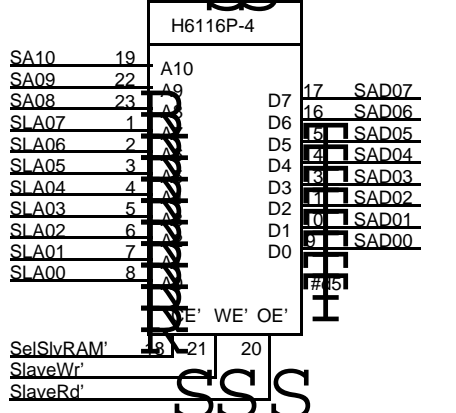
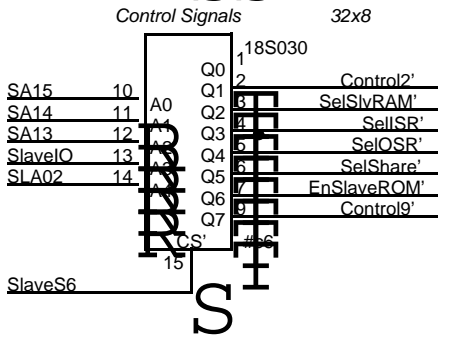
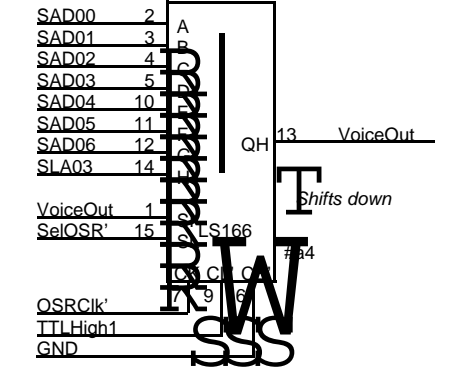
Slave system ROM



Address latch for local memory

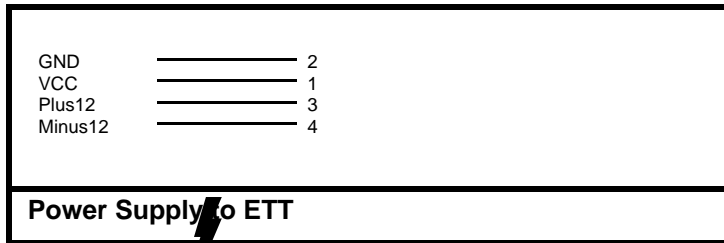


Output shift register

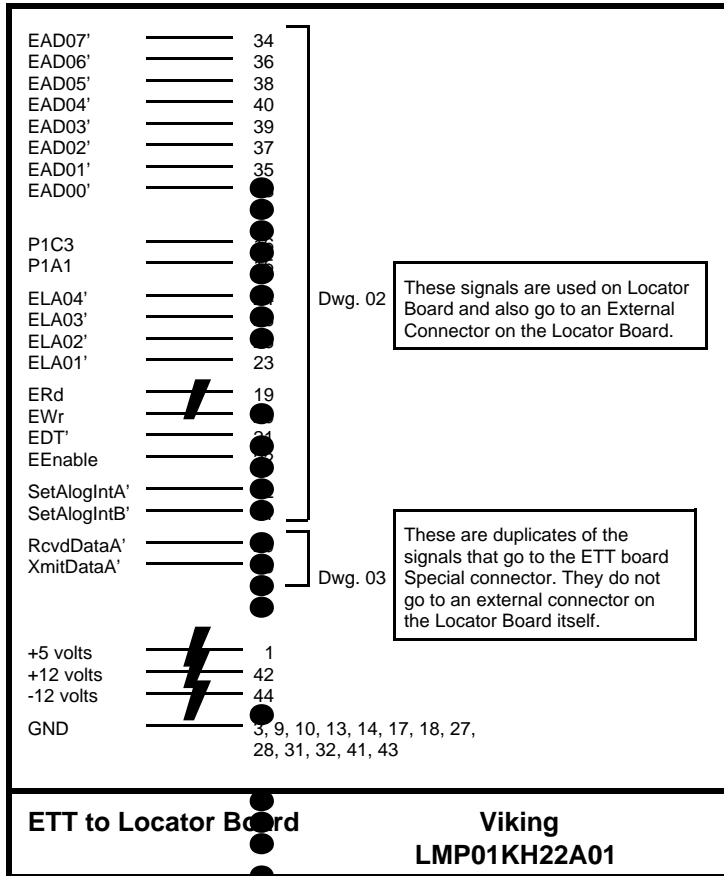


LOC	CONTENTS	DWG	LOC	CONTENTS	DWG
A1	_____		F1	_____	
A2	_____		F2	AMZ8104	1
A3	_____		F3	i8088-2	1
A4	LS166	9	F4	_____	
A5	AMZ8104	9	F5	LS32	3, 4, 6, 9
A6	WD2001F-02	4	F6	i8284A	1
A7	_____		F7	8T09	1, 2(2), 5
A8	_____		F8	LS02	2, 6, 9(2)
A9	_____		F9	LS393	4, 5
A10	_____		F10	Dip Sw	7
B1	27K Res. DIP	6	H1	_____	
B2	S158	6	H2	S158	6 ■ ■ ■
B3	LS373	9	H3	Delay Line	6
B4	i8088-2	9	H4	26LS32	7 ■ ■ ■
B5	_____		H5	S10	2, 6(2)
B6	LS11	2, 4(2)	H6	LS04	2(2), 5(4)
B7	F93427	2	H7	LS04	1, 2(5)
B8	LS374	1(2), 2,4(2),9(3)	H8	LS240	2(2)
B9	LS279	3, 4, 7, 9	H9	Xtal	4
B10	LS153	2	H10	SN75189	3(2) ■ ■
C1	_____		K1	Dip Sw	7
C2	S158	6	K2	i8255A-2	7
C3	LS373	9	K3	_____	
C4	_____		K4	26LS31	5, 7(3)
C5	LS373	9	K5	_____	
C6	18S030	9	K6	Xtal	5
C7	LS138	2	K7	LS279	4(4)
C8	LS00	2, 3, 9 ■	K8	_____	
C9	_____		K9	i8259A-2	4
C10	S74	5,6	K10	SN75188	3(2) ■ ■
D1	_____		L1	LS38	5(4)
D2	LS373	1	L2	i8255A-2	7
D3	i8237A-5	1	L3	_____	
D4	_____		L4	SLC	5
D5	H6116P-4	9	L5	_____	
D6	_____		L6	AM9513PC	4
D7	LS04	1, 2, 3, 9(3)	L7	_____	
D8	_____		L8	i8274	3
D9	_____		L9	_____	
D10	LS74	5 ■	L10	AMZ8103	2
E1	_____		MD00	64K RAM	8
E2	S373	1	MD01	64K RAM	8
E3	i2764	7	MD02	64K RAM	8
E4	_____		MD03	64K RAM	8
E5	i2764	9	MD04	64K RAM	8
E6	_____		MD05	64K RAM	8
E7	LS299	9	MD06	64K RAM	8
E8	LS08	2(2), 5, 9	MD07	64K RAM	8
E9	LS123	3(2)			
E10	LS132	3(4)			

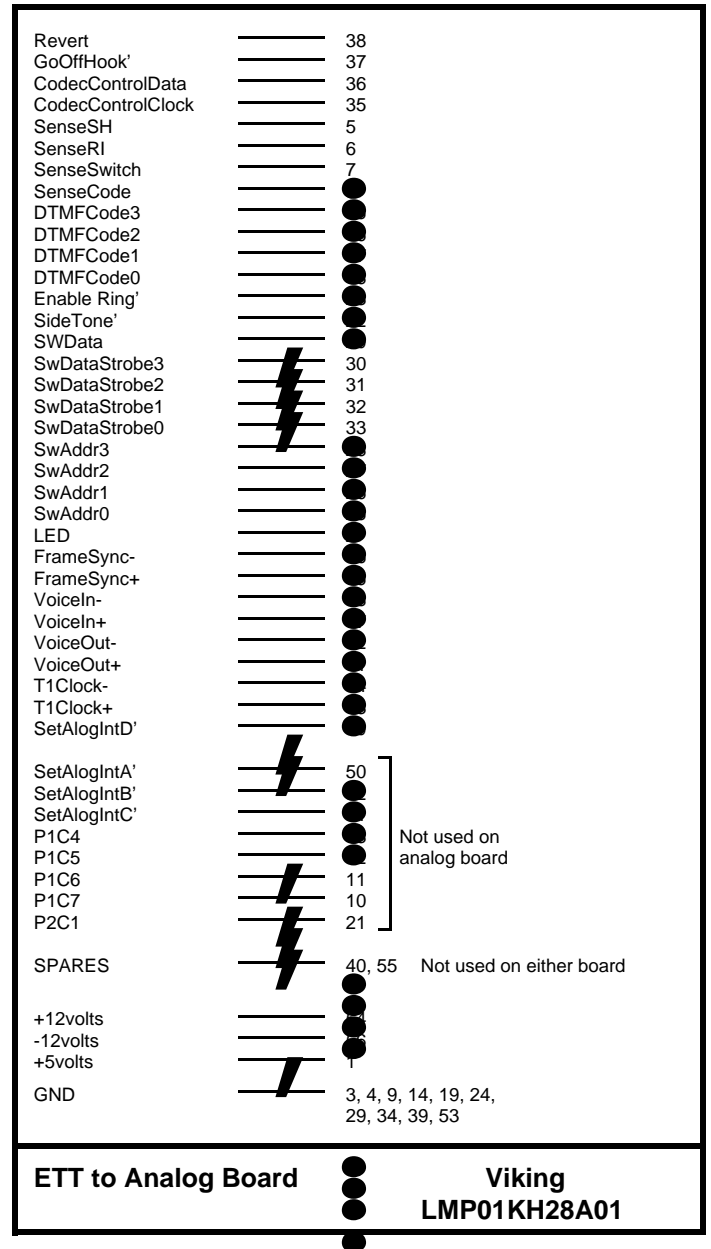
**P1**



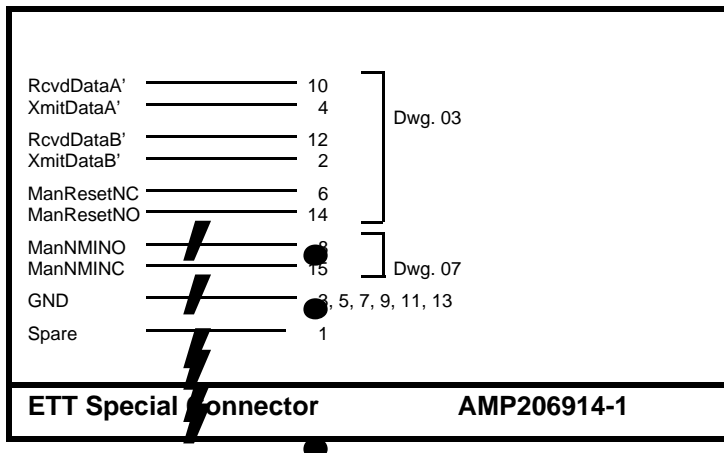
**P2**



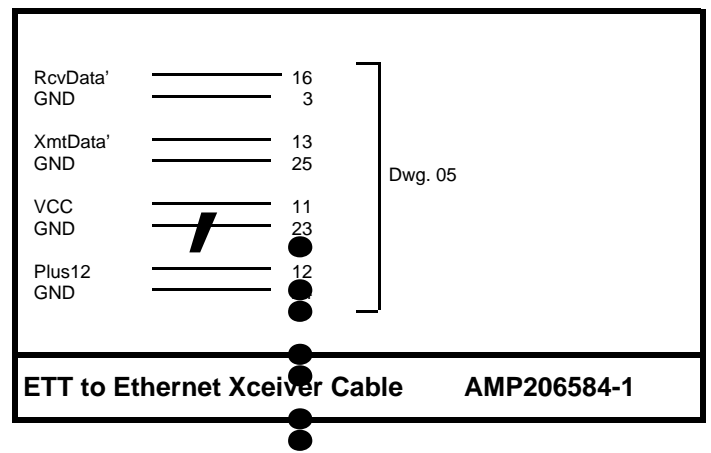
**P3**



**P4**



**P5**



Arrows have ETT board on left