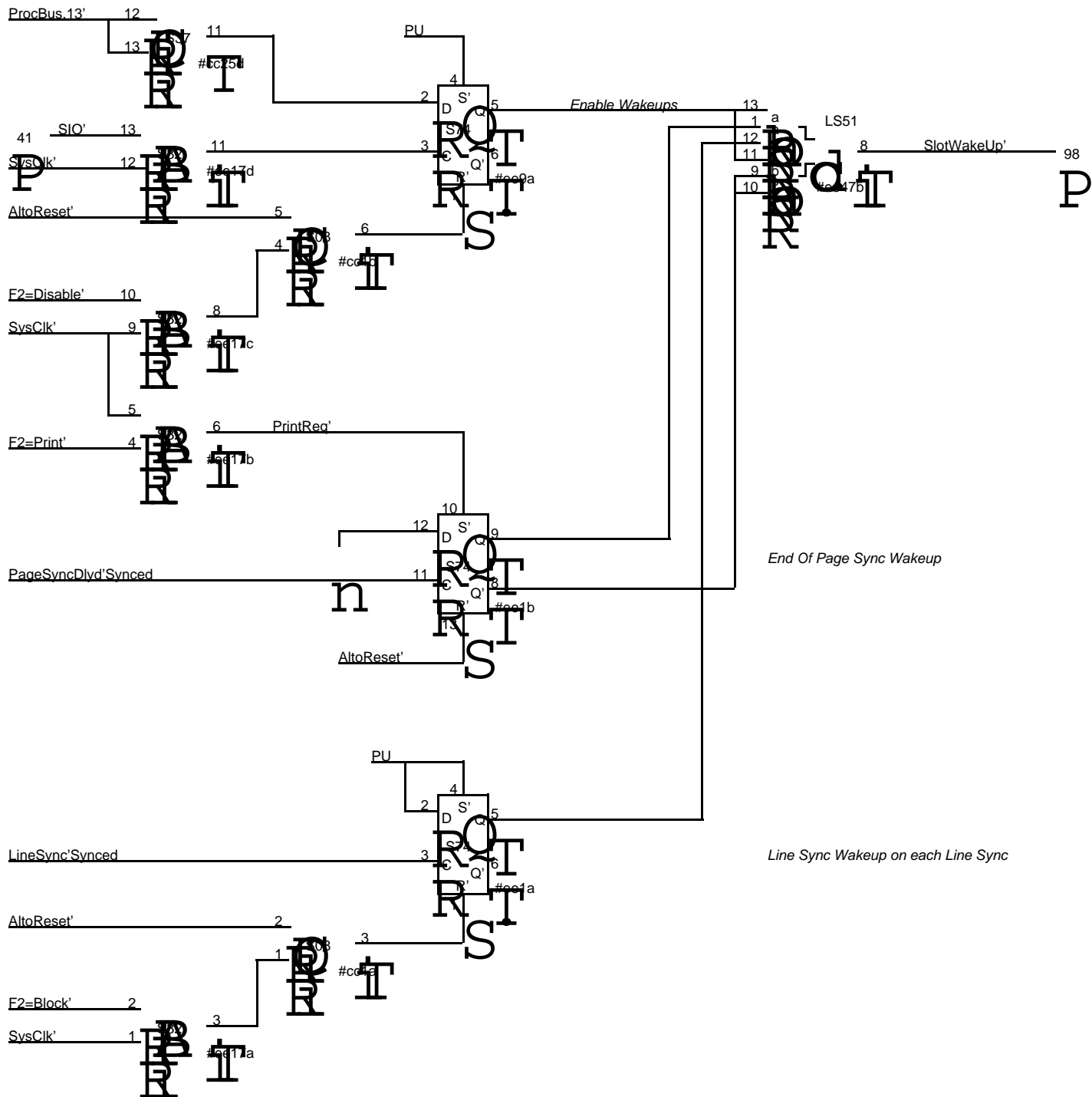
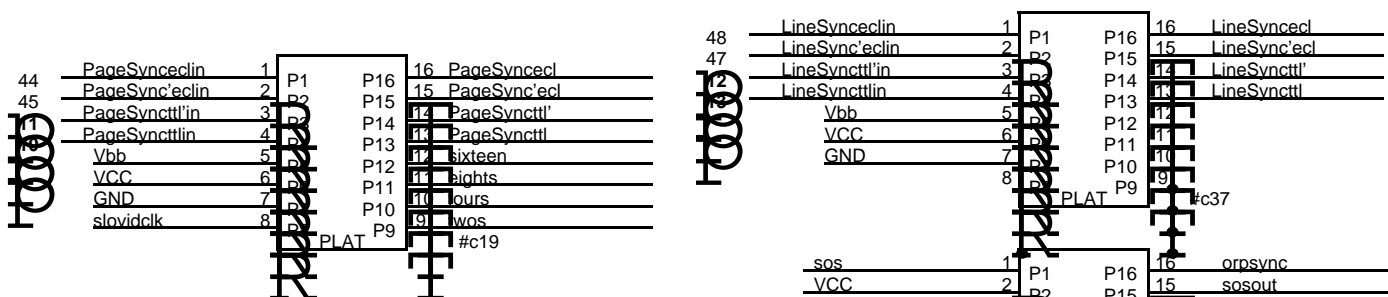
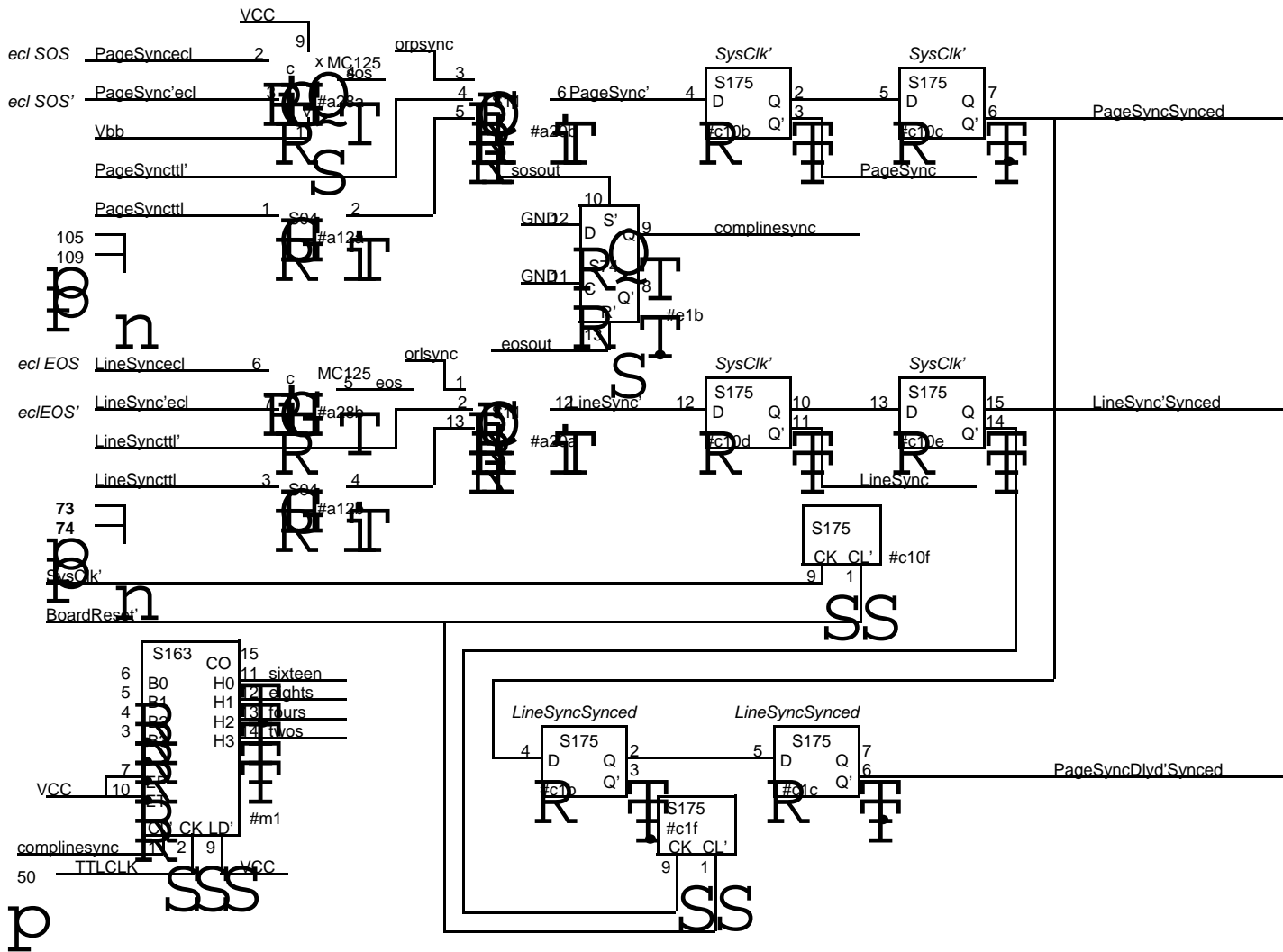


ALTO II 64k BIT  
SLOT INTERFAC E

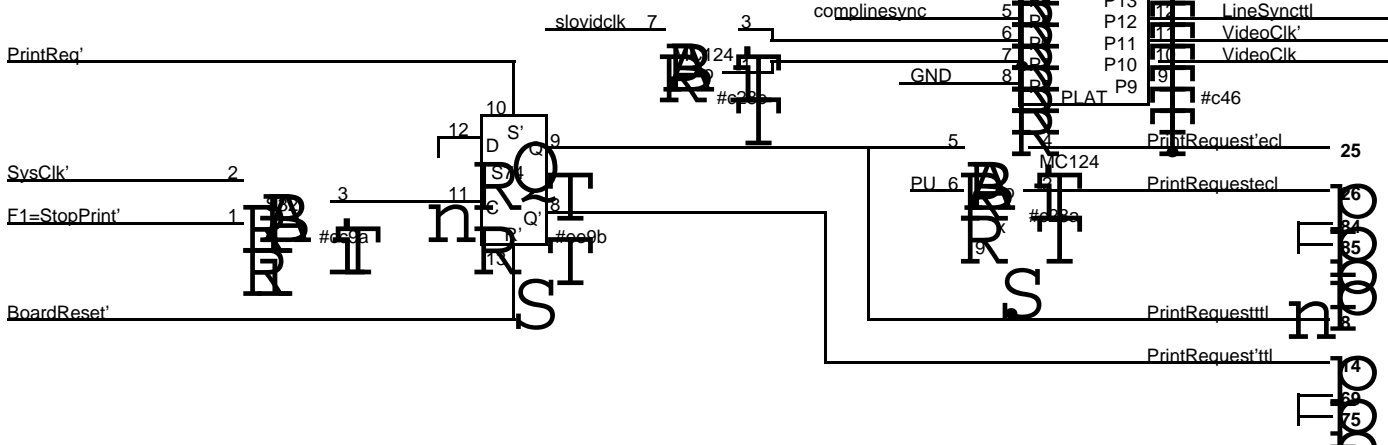
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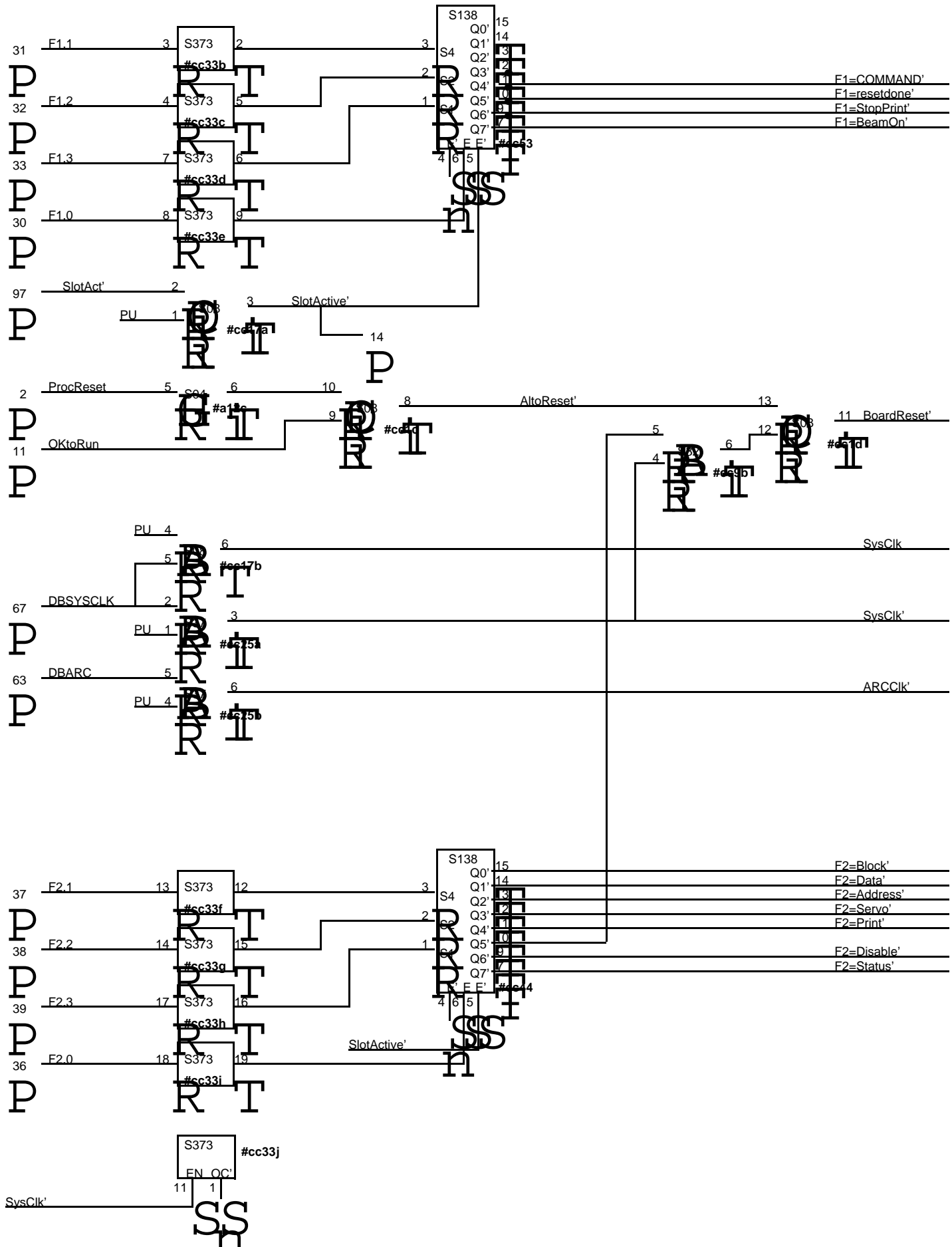
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Wake up logic	0 1
Printer interface	0 2
F Decodes	0 3
A Buffer Addressing	0 4
A Buffer Memory	0 5
B Buffer Addressing	0 7
B Buffer Memory	0 8
Shifter	1 0
Shifter Control	1 1
Buffer Conrtol	1 2
Alto Bus Interface	1 3
Route Information	1 4
Loading Chart	1 6

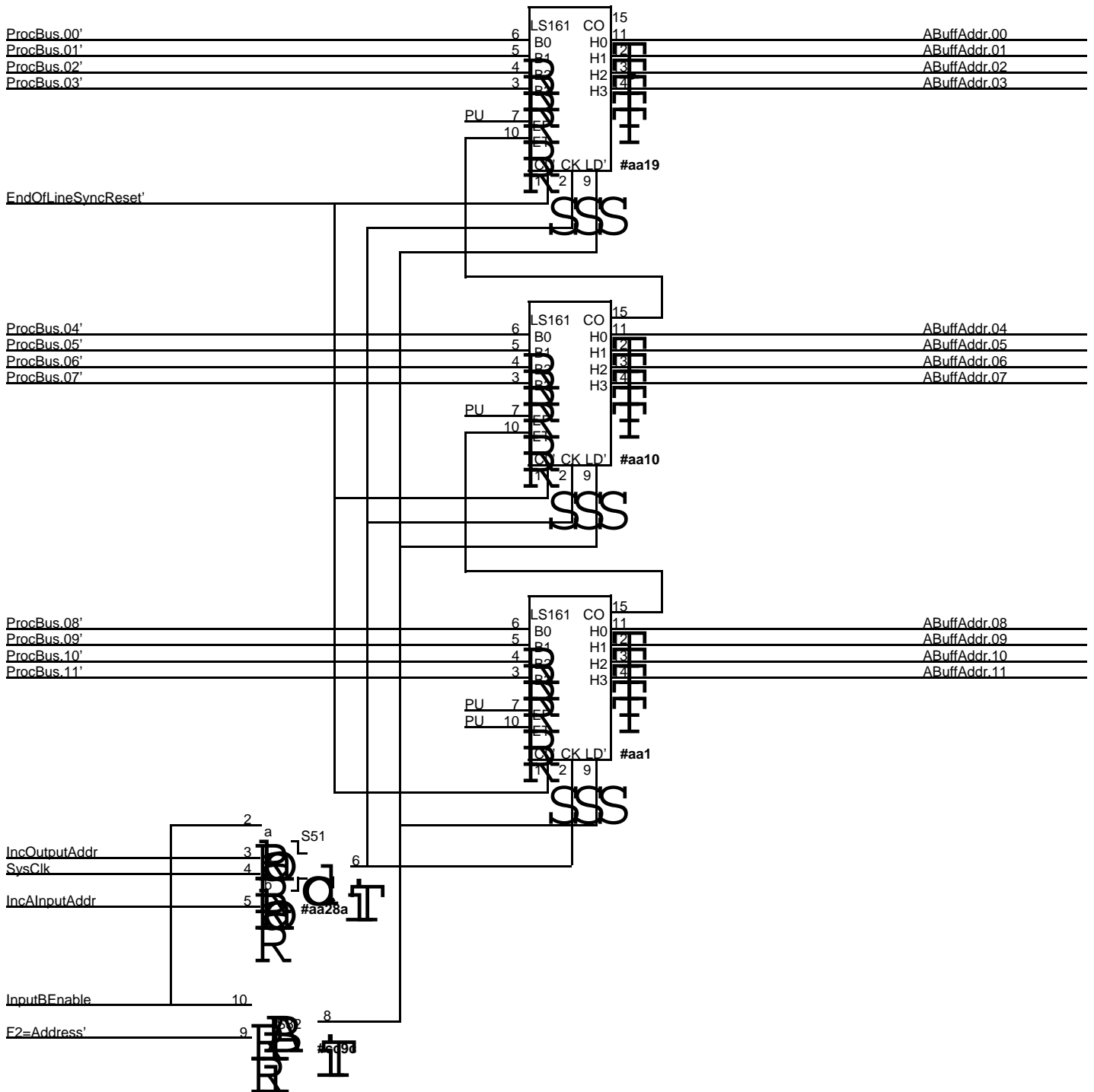


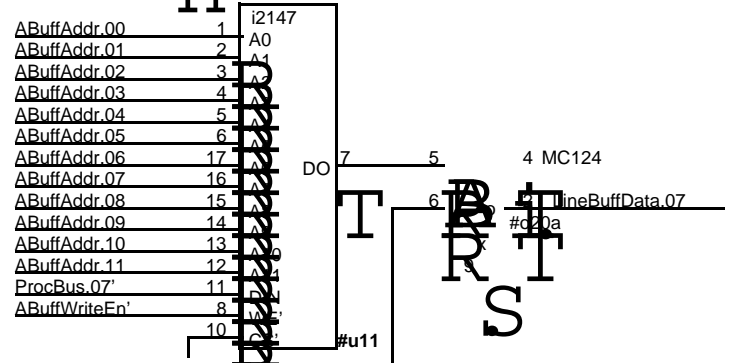
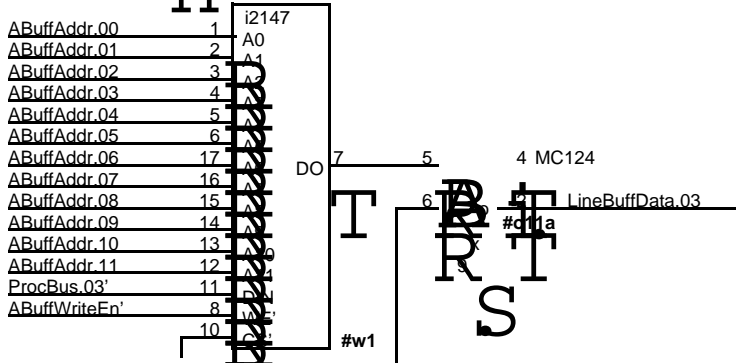
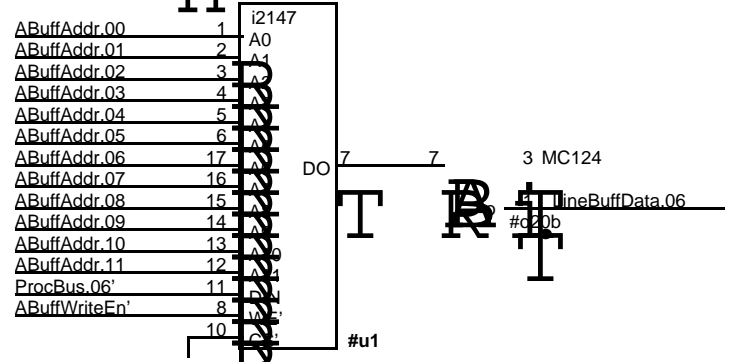
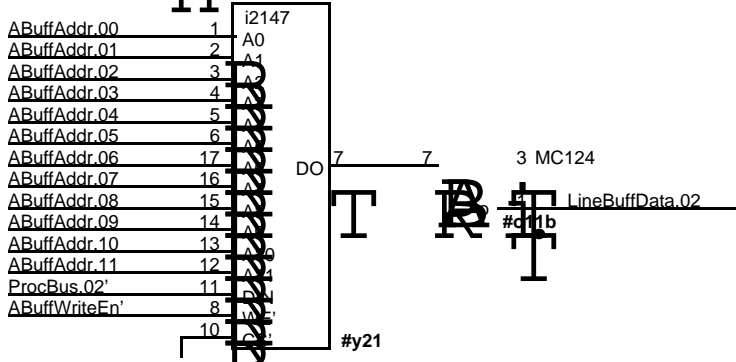
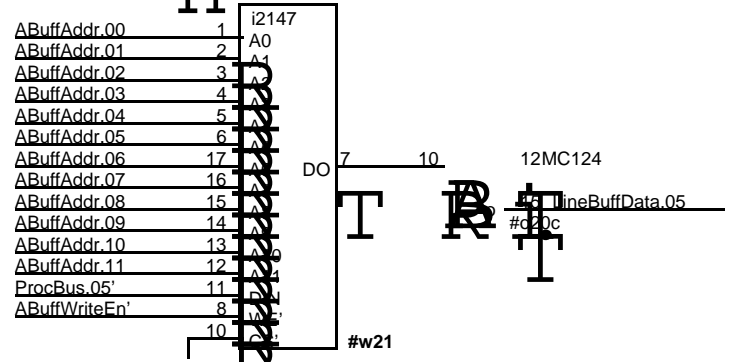
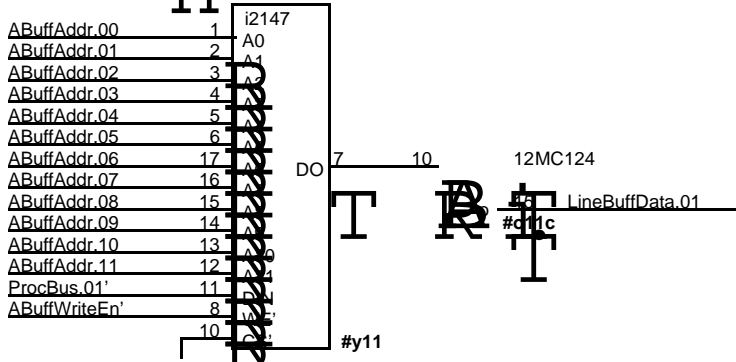
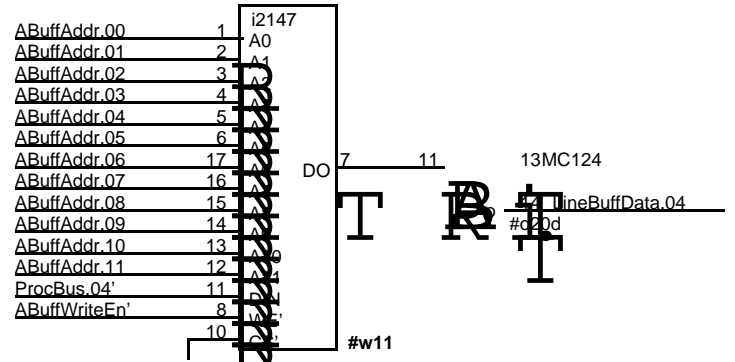
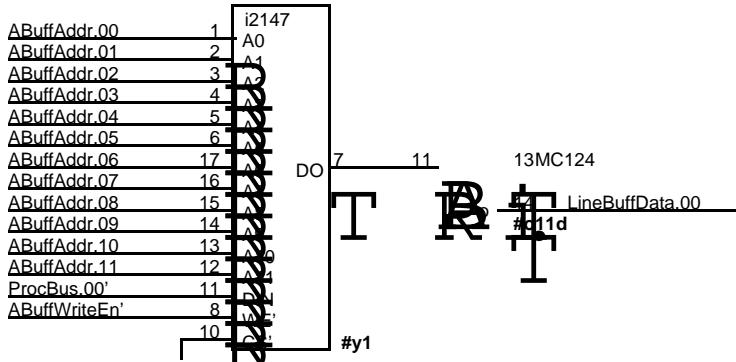


See Page 16 for configurations

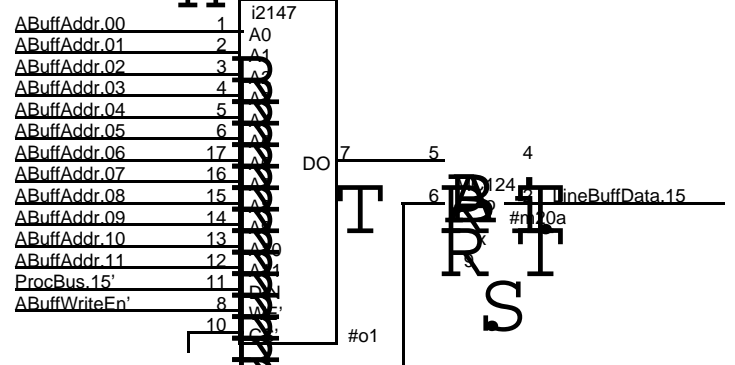
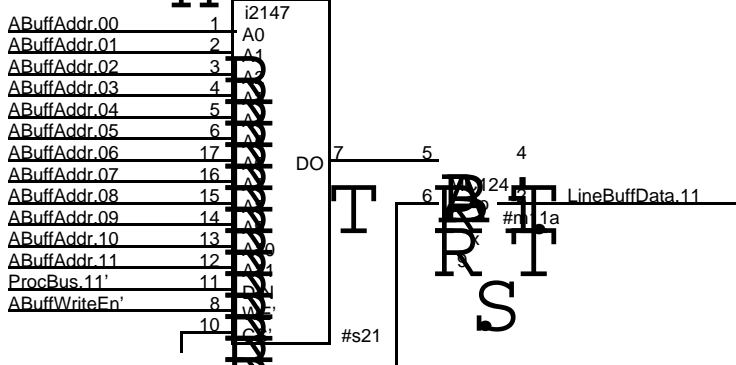
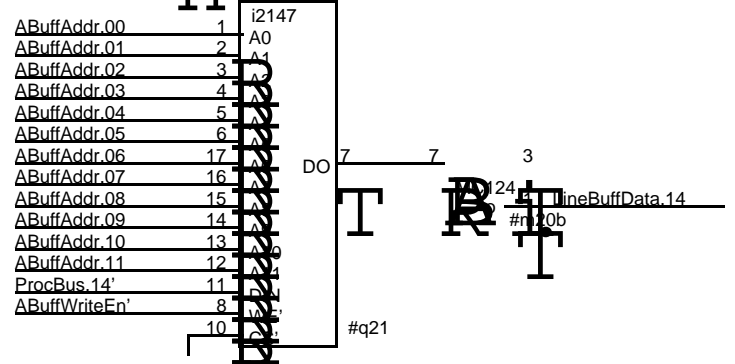
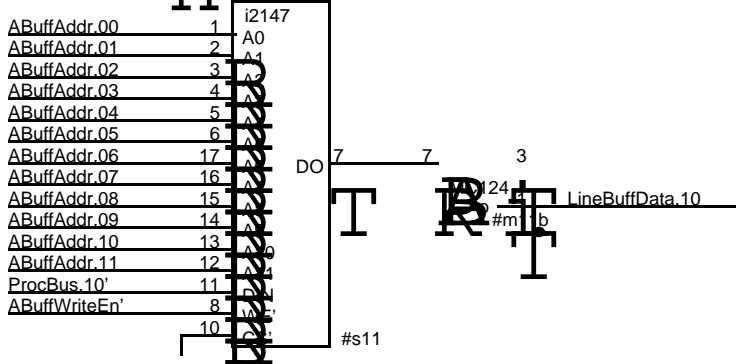
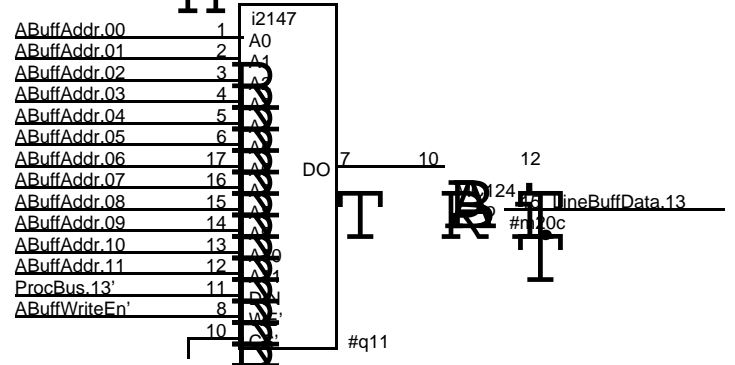
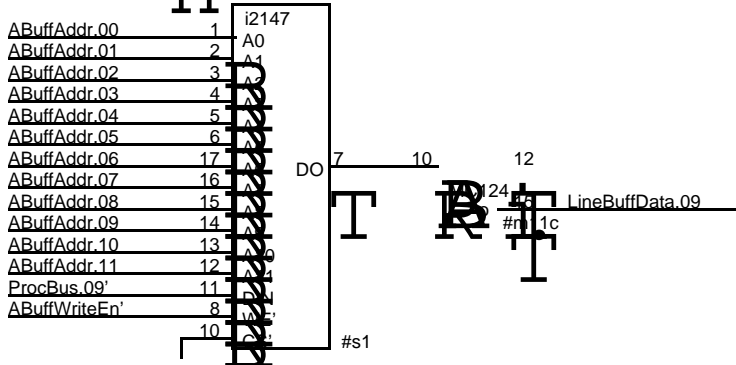
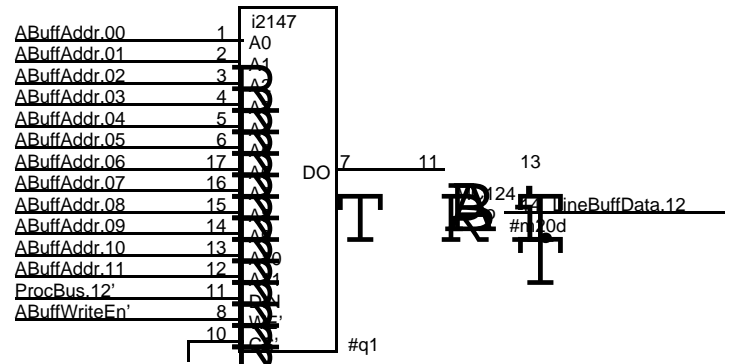
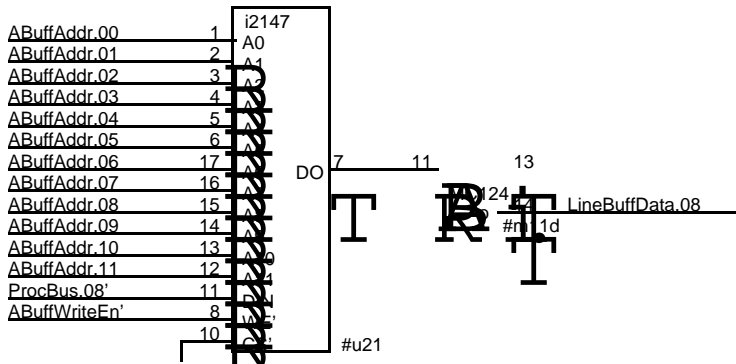




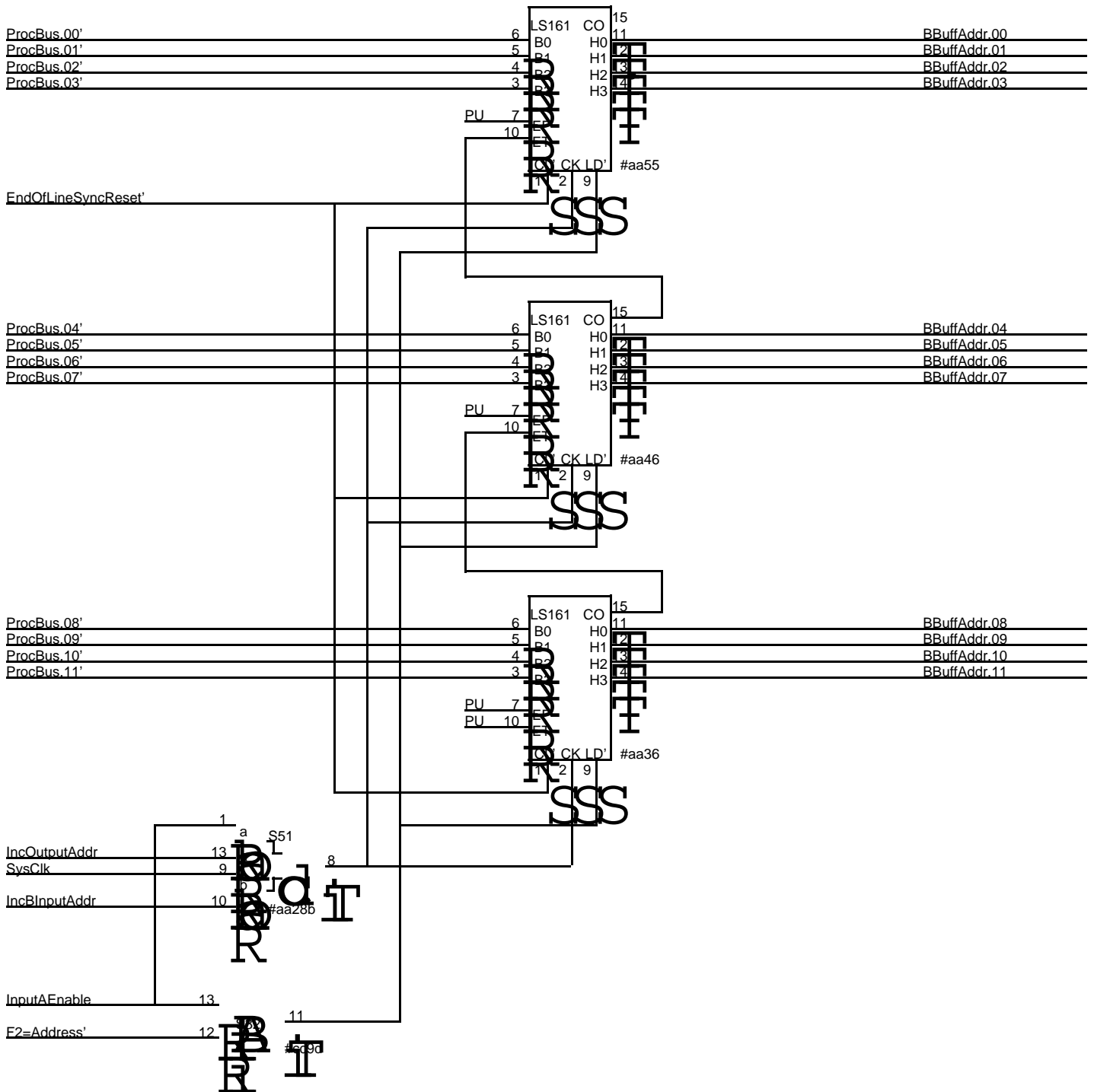




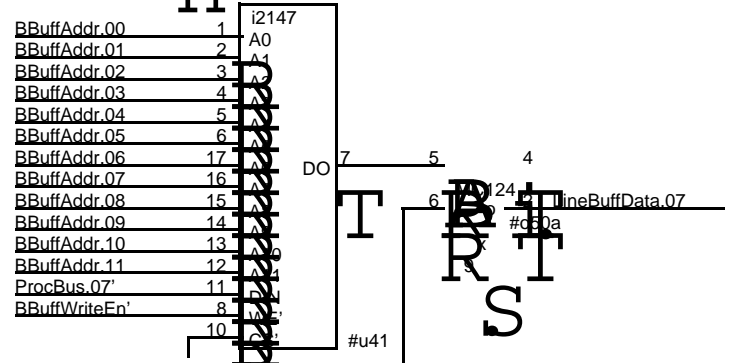
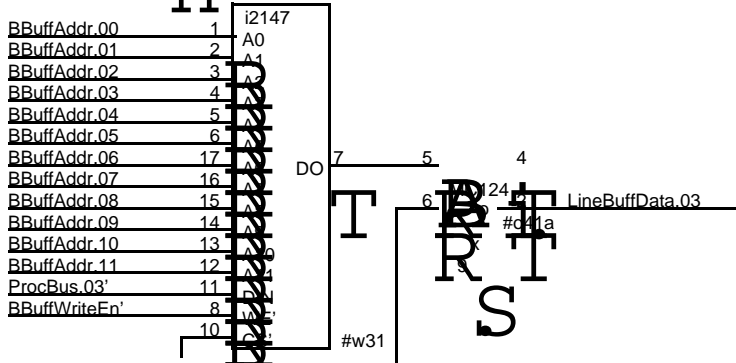
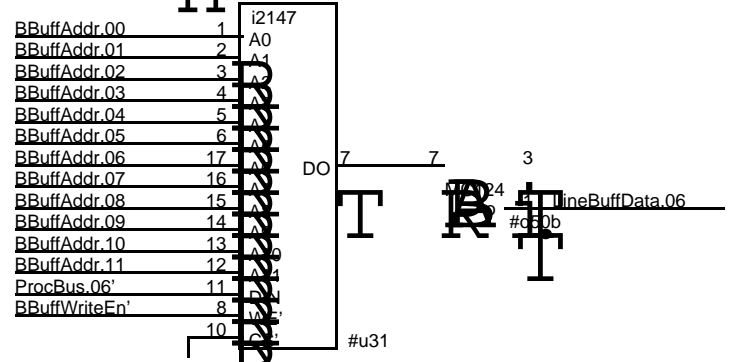
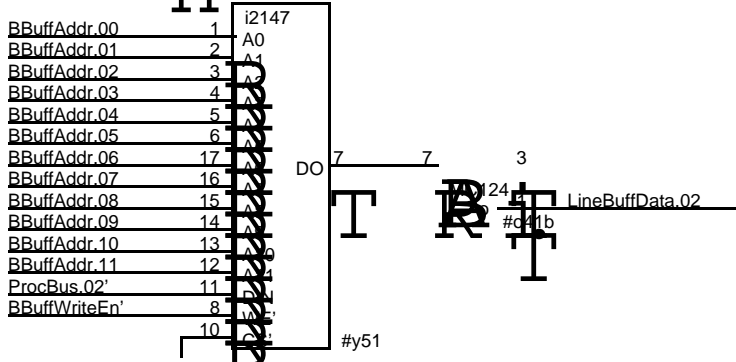
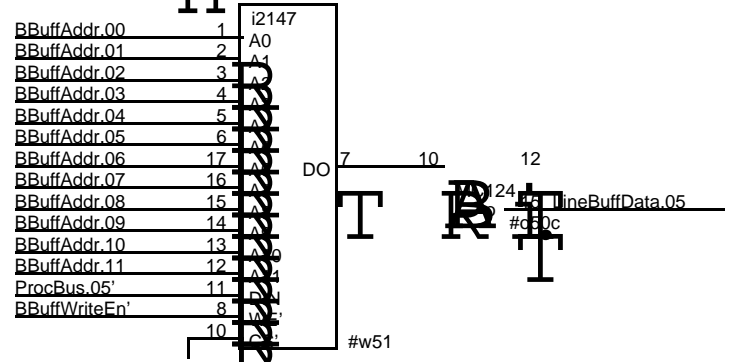
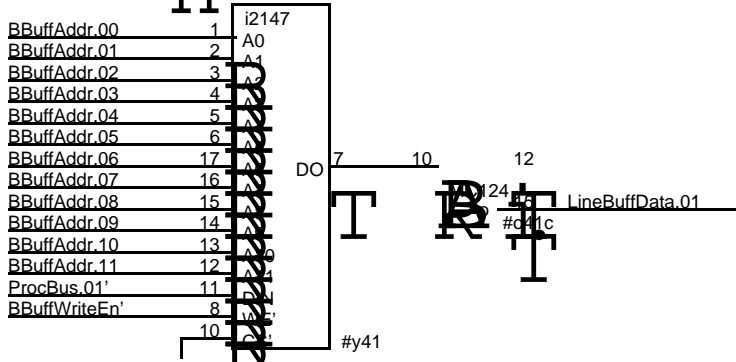
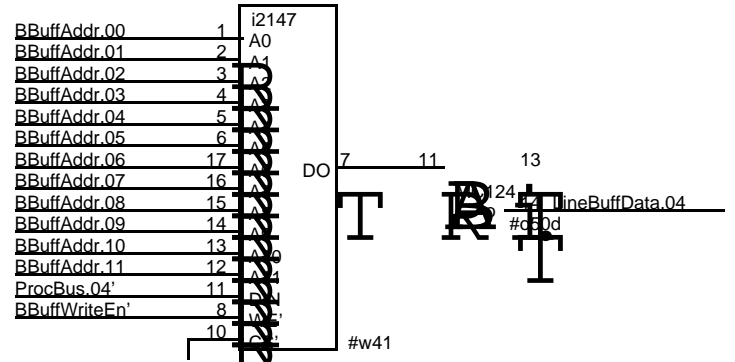
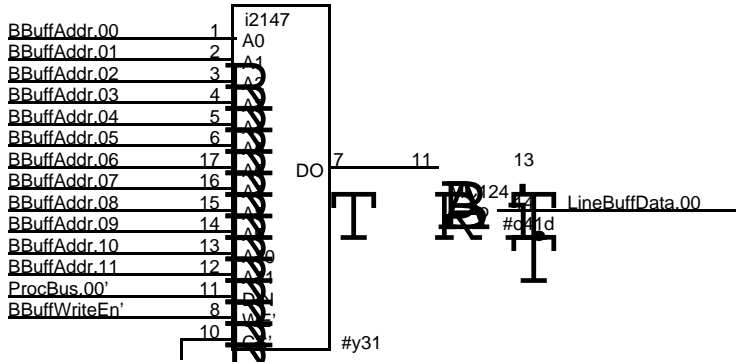
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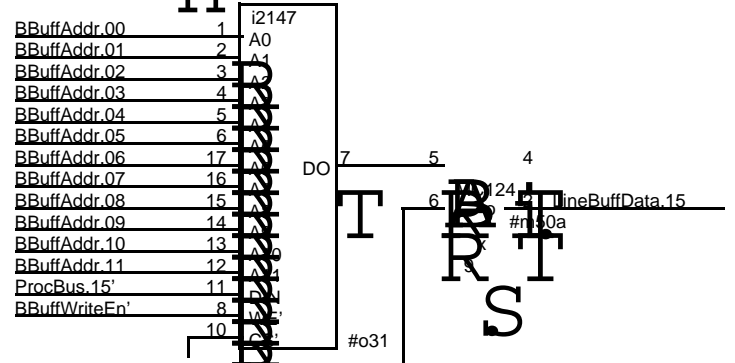
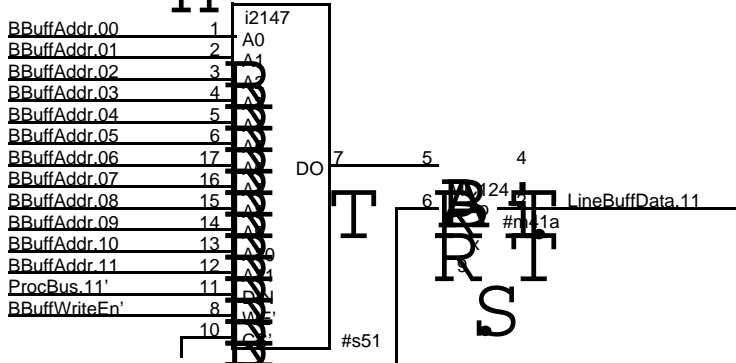
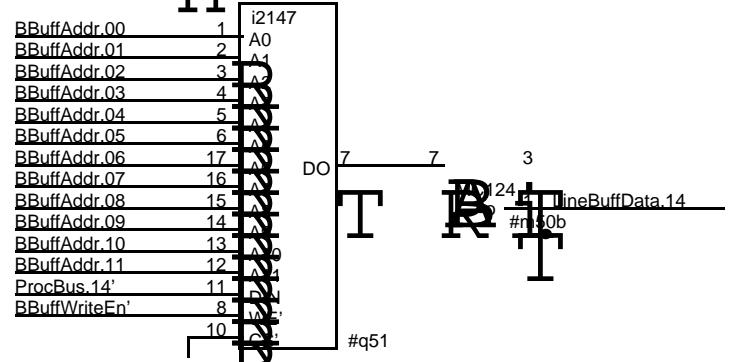
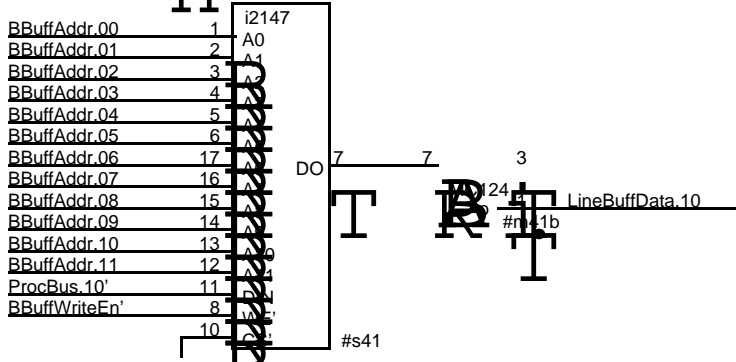
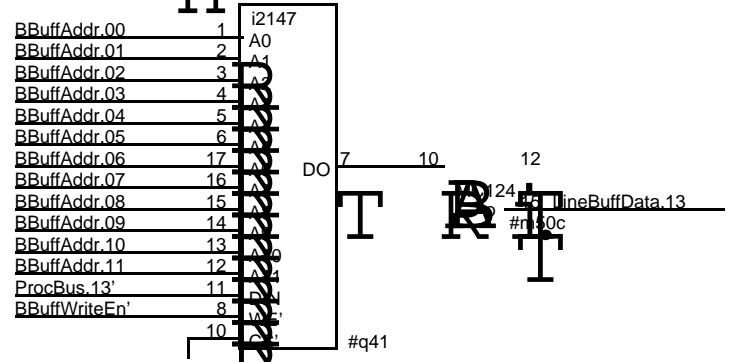
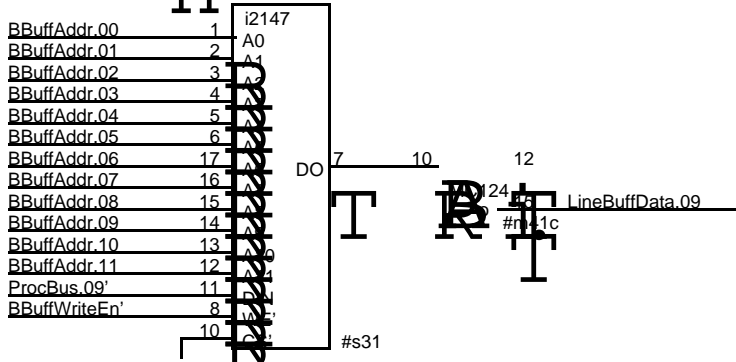
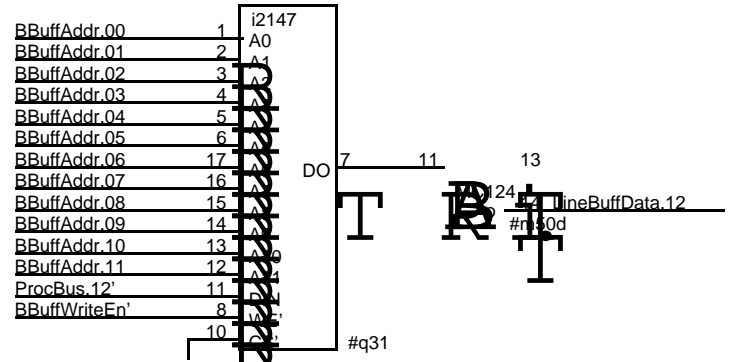
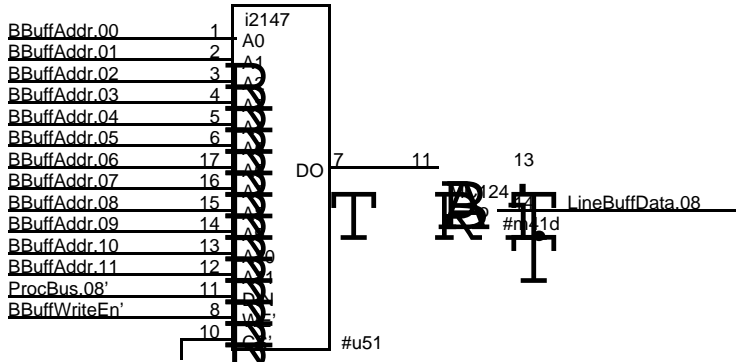
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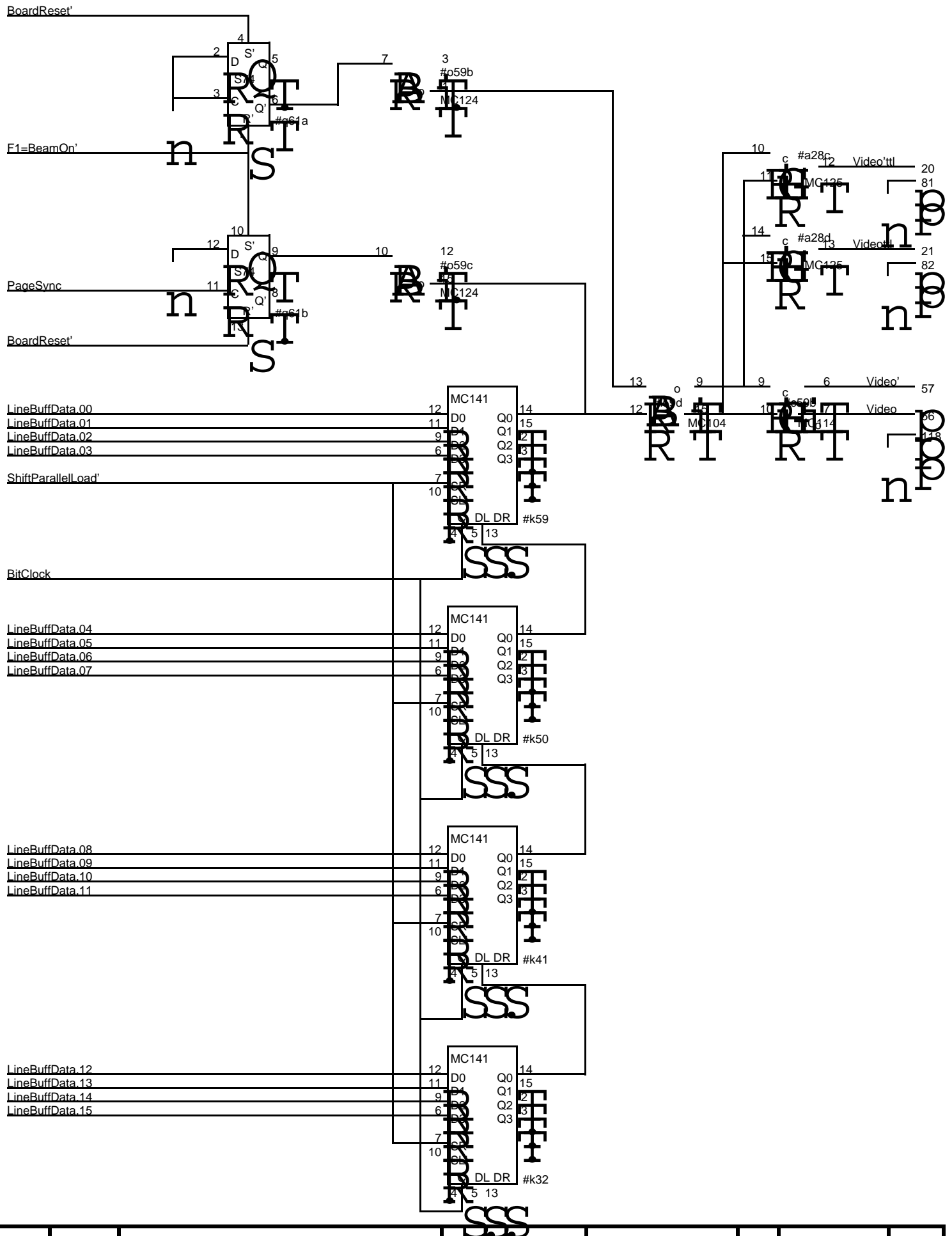


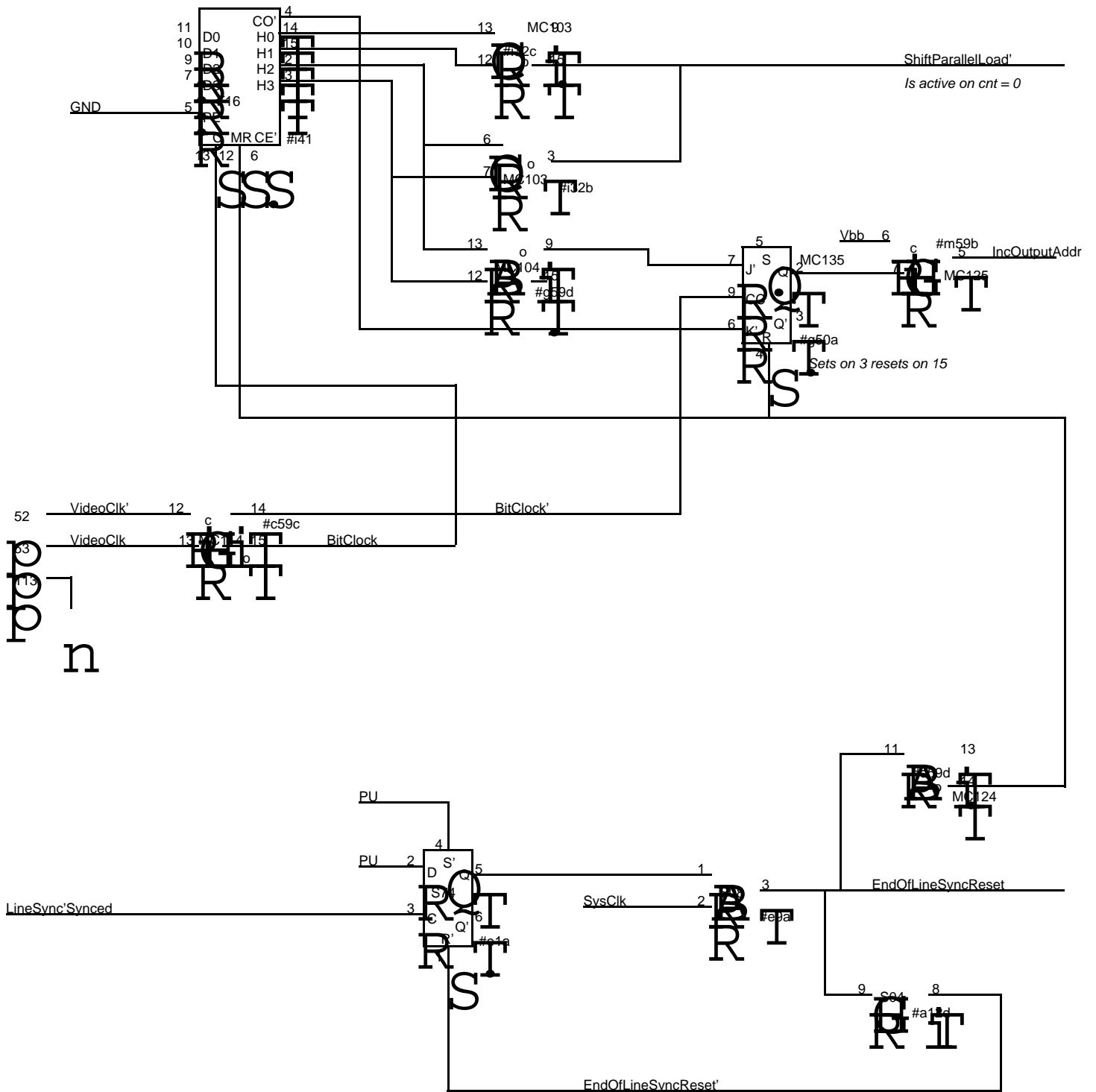


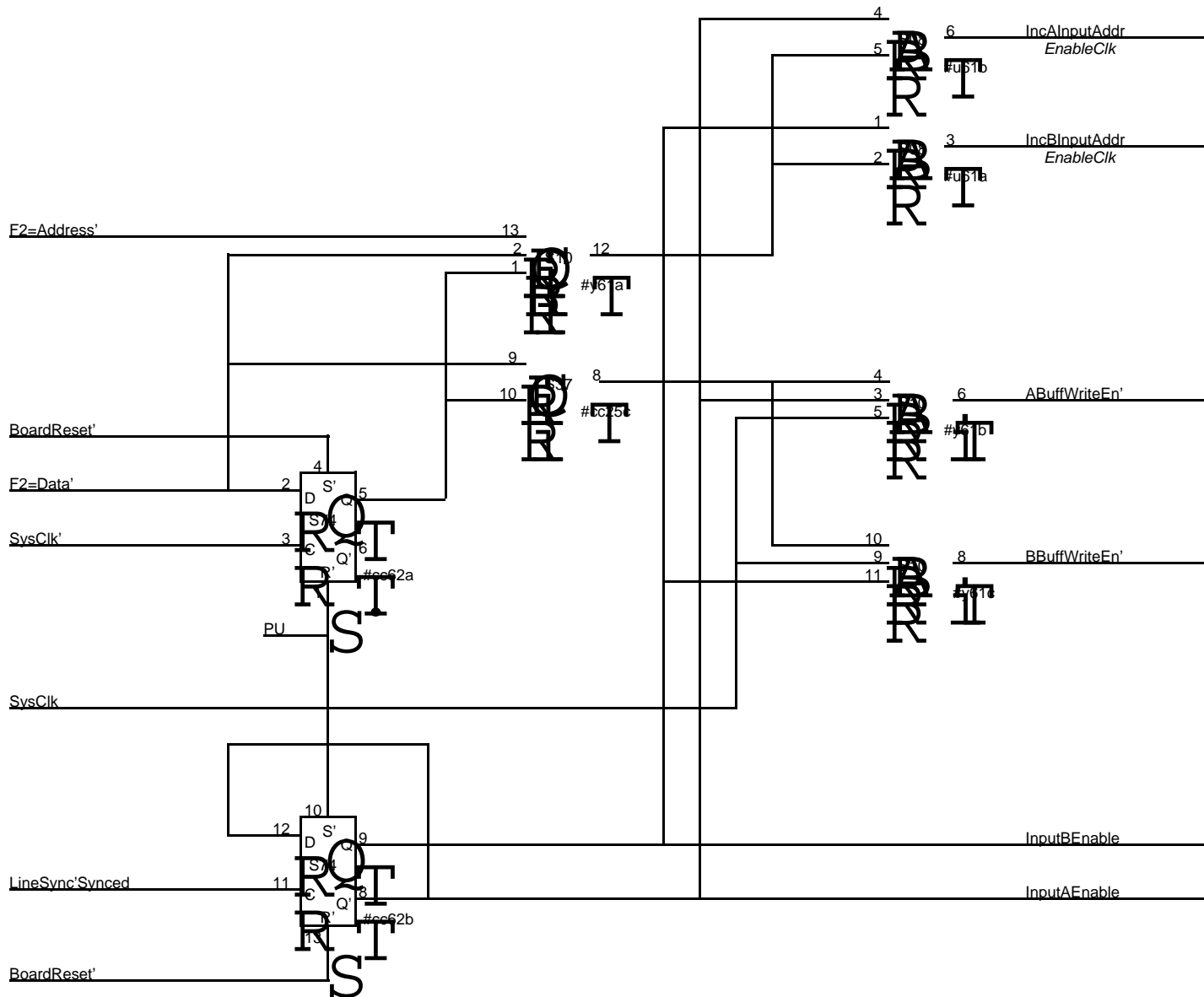
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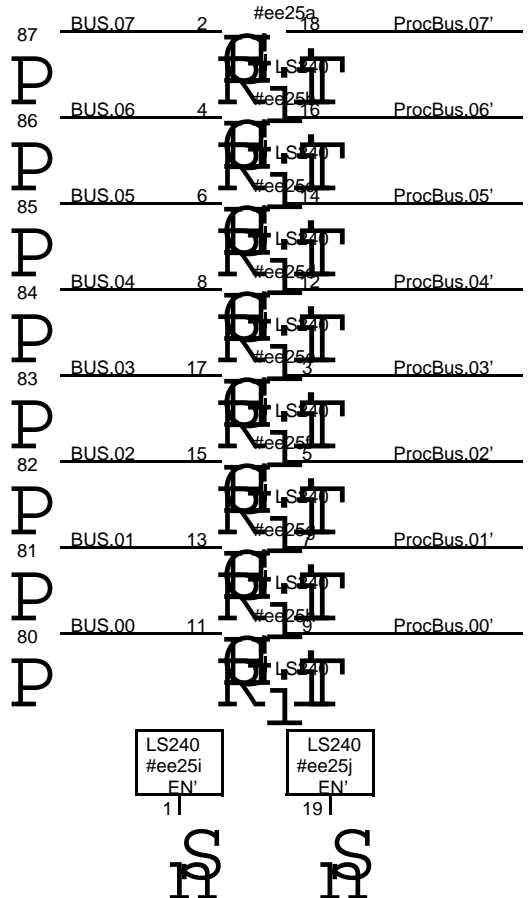
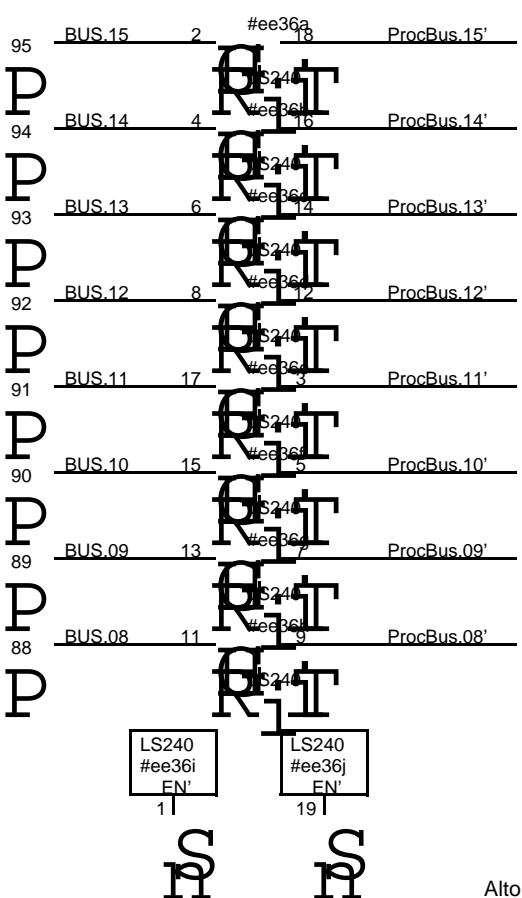
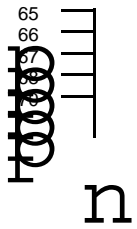
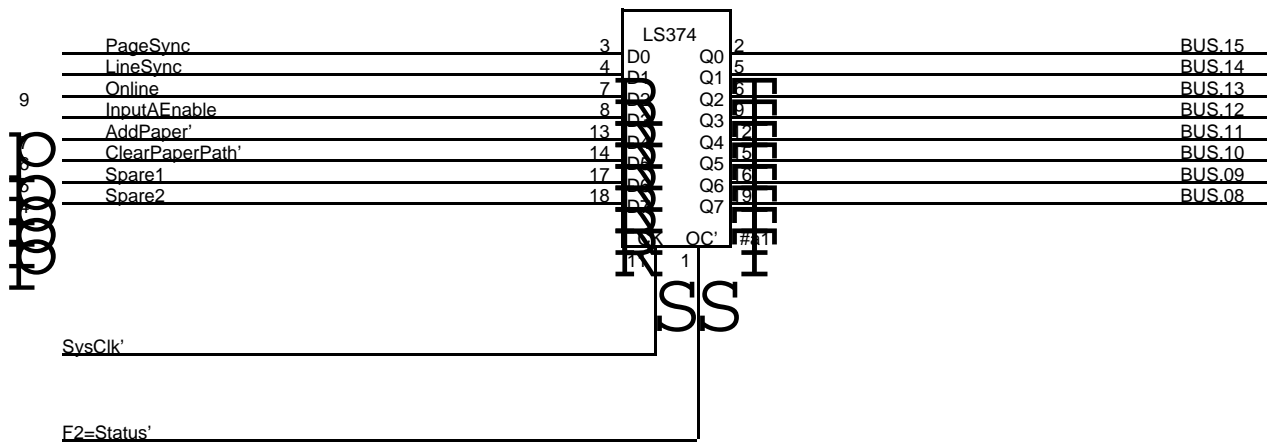


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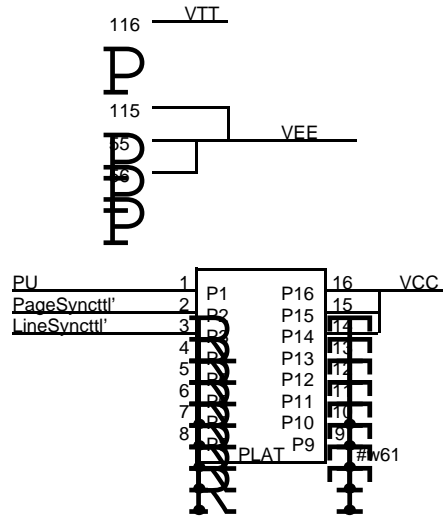
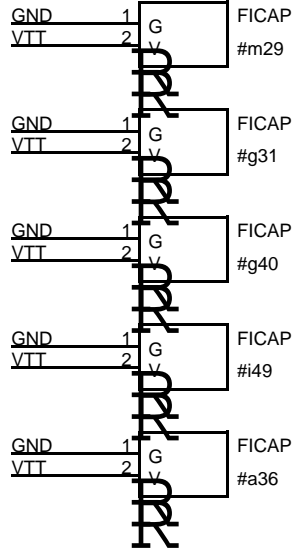
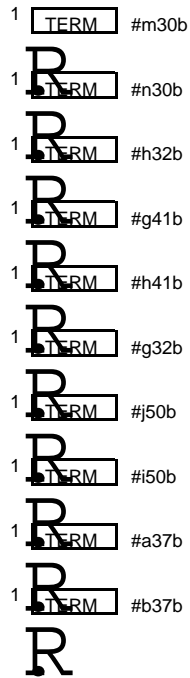




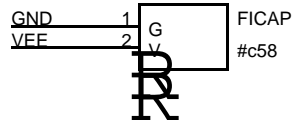
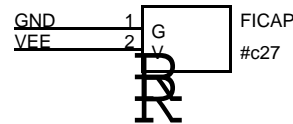
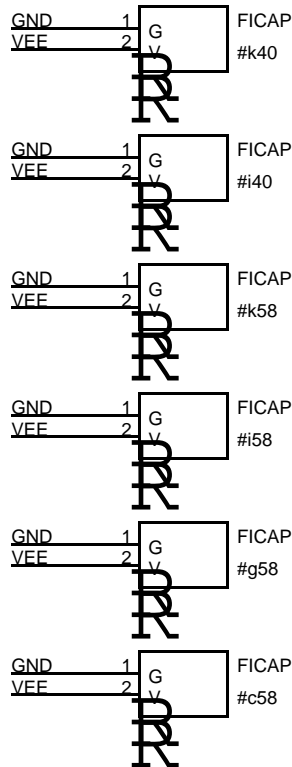
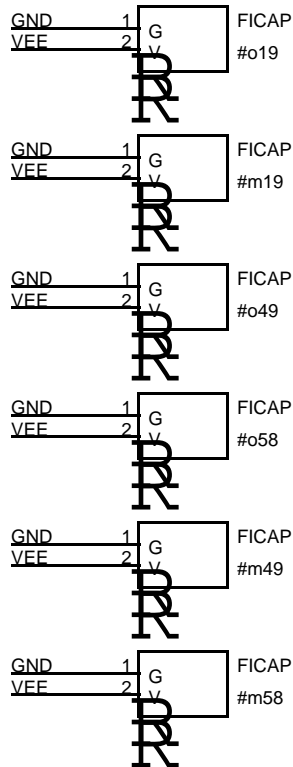


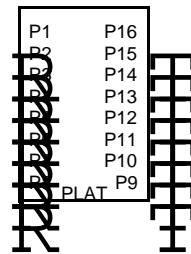
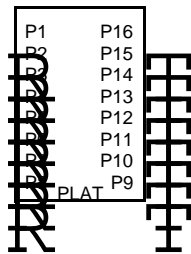
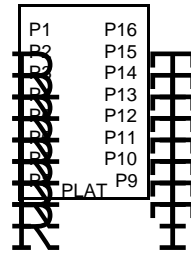
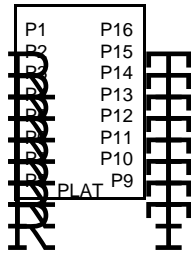
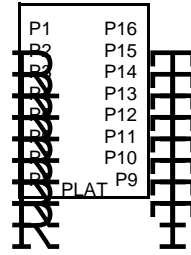
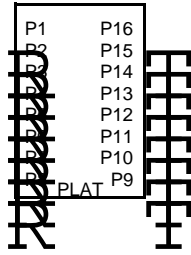


Alto Bus Interface



1k ohm resistor  
1k ohm resistor  
1k ohm resistor

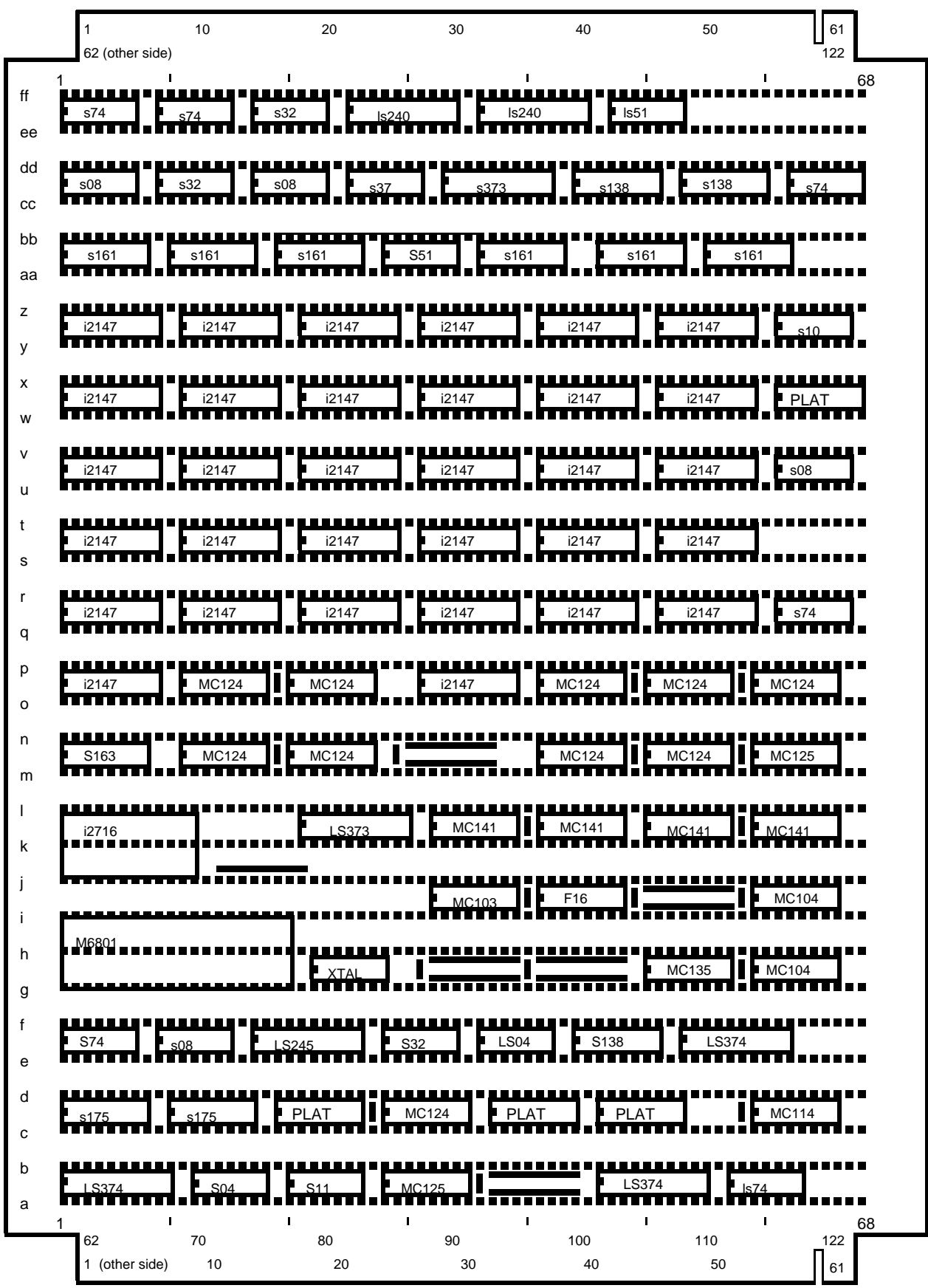




This needs to be done



EDGE CONNECTOR



CABLE CONNECTOR

As viewed from the component side

Load .01uf caps all available locations near chips  
Install heavy ground connections from edge to power plane

XEROX PARC/CSL	Project Slot 3	Reference Layout	File Slot16.sil	Designer Tim Diebert	Rev AE	Date 5/19/82	Page 18
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