13. INTERPRETING CHECKER FAILURES

The microcode Checker is normally run whenever Tenex is started or restarted, and may be run manually by issuing the Midas command "25;G". Checker failures are characterized by:

a) IMA=20

b) STK 0 = RETN (type "RETN=" to verify this)

c) a value in LM 10 between 0 and 77777.

To interpret a Checker failure, the following guidelines are offered:

a) If LM 10 contains 0, all SM, DM, DM1, DM2, and IM registers containing constants were verified to be correct, but some LM or RM constant or other processor operation failed. See the microinstruction at [STK 0]-1 in the Checker listing to determine what's wrong.

b) If LM 10 does not contain 0, it contains the logical "or" of all addresses containing incorrect values, where

00000-07777	Instruction memory (IM) bits 0-35
10000-17777	Instruction memory (IM) bits 36-71
20000-23777	Dispatch memory (DM) 0-3777
24000-24777	Scratch memory (SM) 0-777

Since these memories are composed of chips which span 400 or 2000 (octal) bits and since the normal failure mode is complete chip failure, it will seldom be true that the number in LM 10 is the address of a single failure. For total chip failures, the logical "or" of the addresses will wind up in LM 10. Note that on the old bipolar boards, chips are interleaved so that a chip hits every fourth address. The value in register LPGRT3 is the complement of the wrong bits in the word if there was only a single error.

c) On Maxc2, one can obtain additional information by invoking "LMPE-Scan" to find the bipolar memory locations containing parity errors, and by invoking "Compare"[1] to compare the current memory contents with the file from which the control memory was loaded. (Note that it is normal for "Compare" to find one error at location IODEND.)

d) Run the DGIMH and DGIML micro-diagnostics for further error information.

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[1] "Compare" (Ref. Section 2, par. C.3.) produces a list of errors on file Midas.Error. From the Alto executive issue the command "Type Midas.Errors". The number associated with each error is a 36 bit word numbered from left to right bit 0 through bit 35. These bit numbers correspond to the bit numbers identified in the bipolar memory card chip maps (Figures 1, 2 & 3).