10. OPERATING TENEX MICROCODE FROM MIDAS

A. Reset is accomplished by typing

21;G

to Midas. The effect of this is to put the machine in monitor mode, to clear the interrupt system, the APR, the processor flags and the disk system. However, Nova peripherals aren't affected, nor are the accumulators or PC affected. If AltIO is called after RESET the processor will start at its starting address (pointed to by absolute location 7).

B. Starting at an arbitrary PDP-10 location n is accomplished by changing the contents of PC (which is on the display) to n and then typing

REMAPPC: (Midas types out the value m of REMAPPC)
"AltIO", "Do-It"

C. The PDP-10 accumulators are LM 0, LM 1, ..., LM 17 and can be examined and changed in the usual way from Midas.

D. The PDP-10 flags are in the left-most 13 bits of the F-register on the display. If you change these from Midas, don't change the other 23 bits of F.

These and other interesting bits of F are as follows:

Bit	Definition
0	Overflow
1	Carry 0
2	Carry 1
3	Floating overflow
4	Byte increment suppress
5	User mode
6	PARC mode (replaces PDP-10 user I/O mode)
7	Call from monitor (see JSYS, UMOVE, and Pager addendums to PDP-10 System Reference Manual)
8-10	Machine mode (0=PDP-10, 1=Byte Lisp)
11	Floating underflow
12	No divide
13	Pushdown overflow
14	XCT0
15	XCT1
16	XCT2
17	XCT3
18	Incompatible
19	PI system is active
20	PI cycle in progress
21	MONALT - Temporary flag used by map loading microcode
22	THIRDPT - Temporary flag used by map loading microcode

23	Unused
24	TTYBSY - console teletype output busy
25	LOGF - enables main loop "LOGI", "BRKI", or "TRACEI" path
26	PICYCLE
27	CUM
28	MICRO
29	IENABLE
30	Unused
31	NOVA - Nova/Alto has left an interrupt request
32	K
33	J
34	H
35	G

E. The interrupt system state is given by the following:

PISTAT[29,35] have 1's when interrupts are in progress on the corresponding PI levels[1,7]. PISTAT[22,28] have 1's when interrupts are disabled on the corresponding PI levels.

SM 600 to SM 643 contain in bits 12-35 the interrupt locations corresponding to devices 0 through 35. The device assignments are in Maxc document 11.

SM 644 to SM 652 are the interrupt-enabled bit tables for priority interrupt levels 1 through 7. 1's in each word indicate that the corresponding device (bit 0=device 35, bit 35=device 0) is enabled for interrupts at that level.

MICINTS contains 1's for each device which has requested an interrupt. (However, OVF, FOVF, and PDOVF are recomputed from F for each instruction, so their state in MICINTS isn't important.)

F. The microcode consistency "Checker" uses four variables CSUMD, CSUM0, CSUM1, and CSUM2 which contain checksums for all constants in the microprocessor's IM, DM, DM1, DM2, and SM memories. CSUMD is an overall checksum (for detection of errors) while CSUM0-CSUM2 contain 18 6-bit bytes each of which is a checksum in a Hamming code. The checker computes the address which is clobbered assuming only a single word is wrong.

When newly assembled microcode is loaded for the first time on Maxc2, these checksums are computed and dumped automatically by "Midas Init". Subsequent runnings of the TENLOAD, MEXECGO, and TENGO command files check the newly loaded system against these constants, and crash on errors. Also the CHECK JMC does this (executed during Tenex initialization).