

x: { null => memory, IO}  
y: { null => no hold, Hold}

A processor: {PCmdA \_xFetchy; PData \_address} cache: {PRejectB \_FALSE; PFaultB \_None}  
B cache: {PRejectB \_FALSE; PFaultB \_None; PData \_data; PParityB \_parity}

Figure 2a. Fetch Timing, No Reject, No Fault

w cycles (w>=0) | A processor: {PCmdA \_xFetchy; PData \_address} cache: {PRejectB \_FALSE; PFaultB \_None}  
| B cache: {PRejectB \_TRUE; PFaultB \_None}  
| A cache: {PRejectB \_FALSE; PFaultB \_None}  
| B cache: {PRejectB \_TRUE; PFaultB \_None}  
| A cache: {PRejectB \_FALSE; PFaultB \_None}  
| B cache: {PRejectB \_FALSE; PFaultB \_None; PData \_data; PParityB \_parity}

Figure 2b. Fetch Timing, Reject, No Fault

w cycles (w>=0) | A processor: {PCmdA \_xFetchy; PData \_address} cache: {PRejectB \_FALSE; PFaultB \_None}  
| B cache: {PRejectB \_TRUE; PFaultB \_None}  
| A cache: {PRejectB \_FALSE; PFaultB \_None}  
| B cache: {PRejectB \_TRUE; PFaultB \_None}  
| A cache: {PRejectB \_FALSE; PFaultB \_None}  
| B cache: {PRejectB \_TRUE; PFaultB \_fault}

Figure 2c. Fetch Timing, Reject, Fault

Figure 2. Fetch Timing