| Cycle | Phase | |
|---|---|---|
| 0 | A | |
| | B | requestor: Mrq _ TRUE; |
| 1 | A | |
| | B | |
| 2 | A | arbiter: MGnt _ TRUE; |
| | B | |
| 3 | A | master: {MCmdAB _ ReadQuad; MDataAB _ RQAddress; nMShared _ TRUE; nMAbort _ TRUE} |
| | B | |
| 4 | A | slave: {MCmdAB _ NoOp; match => nMShared _ FALSE; owner => nMAbort _ FALSE} |
| | B | |
| w cycles (w>=0) | A | slave: MCmdAB _ NoOp; |
| | B | |
| 5+w | A | slave: {MCmdAB _ DataTransport; MDataAB _ RQData0; MParity _ parity} |
| | B | |
| 6+w | A | slave: {MCmdAB _ DataTransport; MDataAB _ RQData1; MParity _ parity} |
| | B | master: MRq _ FALSE; |
| 7+w | A | slave: {MCmdAB _ DataTransport; MDataAB _ RQData2; MParity _ parity} |
| | B | |
| 8+w | A | slave: {MCmdAB _ DataTransport; MDataAB _ RQData3; MParity _ parity} arbiter: MGnt _ FALSE; |
| | B | |
| | | |

Figure 3. Timing for ReadQuad