

Cycle	Phase	
0	A	
	B	requestor: Mrq _ TRUE;
1	A	
	B	
2	A	arbiter: MGnt _ TRUE;
	B	
3	A	master: {MCmdAB _ IOWrite; MDataAB _ IOAddress}
	B	
4	A	master: MDataAB _ IOData; slave: MCmdAB _ NoOp or IODone;
	B	
w cycles (w>=0)	A	slave: {MCmdAB _ anything but IODone; M bus lines other than MCmdAB _ anything}
	B	
5+w	A	slave: {MCmdAB _ IODone; MDataAB _ undefined}
	B	
6+w	A	master: MCmdAB _ NoOp;
	B	master: MRq _ FALSE;
7+w	A	master: MCmdAB _ NoOp;
	B	
8+w	A	master: MCmdAB _ NoOp; arbiter MGnt _ FALSE;
	B	

Figure 7. Timing for IOWrite