x: {null => memory, IO}
y: { null=> no hold, Hold}

A processor: {PCmdA _ xFetchy; PData _ address} cache: {PRejectB _ FALSE; PFaultB _ None}

B cache: {PRejectB _ FALSE; PFaultB _ None; PData _ data; PParityB _ parity}

Figure 2a. Fetch Timing, No Reject, No Fault

A processor: {PCmdA _ xFetchy; PData _ address} cache: {PRejectB _ FALSE; PFaultB _ None}

B cache: {PRejectB _ TRUE; PFaultB _ None}

w cycles (w>=0)

A cache: {PRejectB _ FALSE; PFaultB _ None}

B cache: {PRejectB _ TRUE; PFaultB _ None}

A cache: {PRejectB _ FALSE; PFaultB _ None}

B cache: {PRejectB _ FALSE; PFaultB _ None; PData _ data; PParityB _ parity}

Figure 2b. Fetch Timing, Reject, No Fault

A processor: {PCmdA _ xFetchy; PData _ address} cache: {PRejectB _ FALSE; PFaultB _ None}

B cache: {PRejectB _ TRUE; PFaultB _ None}

w cycles (w>=0)

A cache: {PRejectB _ FALSE; PFaultB _ None}

B cache: {PRejectB _ TRUE; PFaultB _ None}

A cache: {PRejectB _ FALSE; PFaultB _ None}

B cache: {PRejectB _ TRUE; PFaultB _ fault}

Figure 2c. Fetch Timing, Reject, Fault

Figure 2. Fetch Timing