Cycle	Phase	
0	A	
	B	requestor: Mrq _ TRUE;
1	A	
	B	
2	A	arbiter: MGnt _ TRUE;
	B	master: MRq _ FALSE;
3	A	master: {MCmdAB _ WriteSingle; MDataAB _ WSAddress; nMShared _ TRUE}
	B	
4	A	master: {MCmdAB _ DataTransport; MDataAB _ WSData; MParity _ parity} slave: match => nMShared _ FALSE;
	B	

Figure 5. Timing for WriteSingle