Cycle	Phase	
0	A	
	B	requestor: Mrq _ TRUE;
1	A	
	B	
2	A	arbiter: MGnt _ TRUE;
	B	
3	A	master: {MCmdAB _ WriteQuad; MDataAb _ WQAddress; nMShared _ TRUE}
	B	
w cycles (w>=0)	A	master: MDataAB _ WQData0; memory: MCmdAB _ NoOp;
	B	
4+w	A	master: MDataAB _ WQData0; memory: MCmdAB _ DataTransport; slave: match => nMShared _ FALSE;
	B	
5+w	A	master: MDataAB _ WQData1; memory: MCmdAB _ DataTransport;
	B	master: MRq _ FALSE;
6+w	A	master: MDataAB _ WQData2; memory: MCmdAB _ DataTransport;
	B	
7+w	A	master: MDataAB _ WQData3; memory: MCmdAB _ DataTransport; arbiter MGnt _ FALSE;
	B	

Figure 4. Timing for WriteQuad