| Cycle | Phase | |
|---|---|---|
| 0 | A | |
| | B | requestor: Mrq _ TRUE; |
| 1 | A | |
| | B | |
| 2 | A | arbiter: MGnt _ TRUE; |
| | B | |
| 3 | A | master: {MCmdAB _ IORead; MDataAB _ IOAddress} |
| | B | |
| w cycles (w>=0) | A | slave: {MCmdAB _ anything but IODone; M bus lines other than MCmdAB _ anything} |
| | B | |
| 4+w | A | slave: {MCmdAB _ IODone; MDataAB _ IOData} |
| | B | |
| 5+w | A | master: MCmdAB _ NoOp; |
| | B | master: MRq _ FALSE; |
| 6+w | A | master: MCmdAB _ NoOp; |
| | B | |
| 7+w | A | master: MCmdAB _ NoOp; arbiter MGnt _ FALSE; |
| | B | |
| | | |

Figure 6. Timing for IORead