| Cycle | Phase | |
|---|---|---|
| 0 | A | |
| | B | requestor: Mrq _ TRUE; |
| 1 | A | arbiter: latch request; |
| | B | |
| w cycles (w>=0) | A | |
| | B | |
| 2+w | A | arbiter: MGnt _ TRUE; |
| | B | conditionally retain bus => master: MNewRq _ TRUE; <<earliest master: MRq _ FALSE>> |
| 3+w | A | <<first transaction cycle>> |
| | B | |
| 4+w | A | <<earliest arbiter: MGnt _ FALSE>> |
| | B | |
| 5+w | A | <<earliest next master>> |
| | B | |
| | | |

Figure 2. Timing for Bus Arbitration