1 processor: DHoldAB _ TRUE

2 All components continue execution normally during this cycle; processor: DHoldAB _ FALSE

3 All components do not update their state during this cycle.

4 All components continue execution normally during this cycle

Figure 2a. Hold Timing

1 processor: {DExecuteAB _ TRUE; DHoldAB must be true by the end of this cycle}

2 The selected component prepares itself for execution during this cycle; processor: DExecuteAB _ FALSE

3 The content of the shift register is replaced. First cycle that DHold may fall.

4 All components prepare to resume execution.

5 First cycle that execution may resume.

Figure 2b. Execute Timing

1 processor: DShiftAB _ TRUE; selected component: sample DDataIn

2 processor: DShiftAB _ FALSE; selected component: insert bit into shift register, extract bit that falls out the end

3 selected component: DDataOutAB changes

Figure 2c. Shift Timing

Figure 2. D Bus Timing