

<p>DRAGON SCHEMATICS</p> <p>CrossRam Test Board</p>

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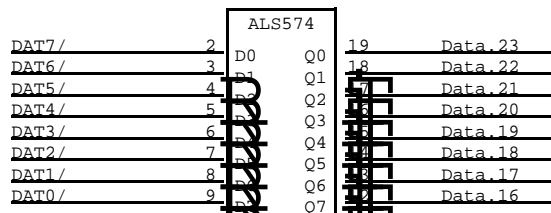
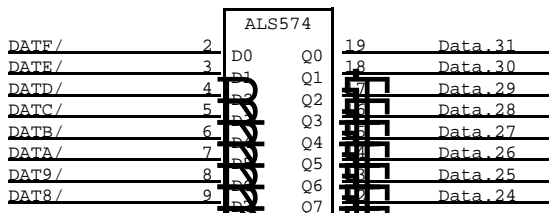
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These drawings use the following [SIL] user.cm parameters:

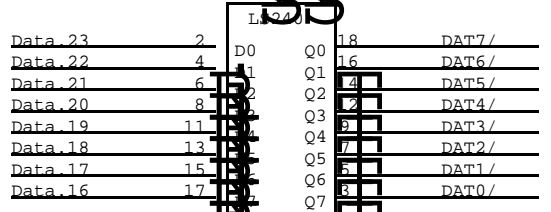
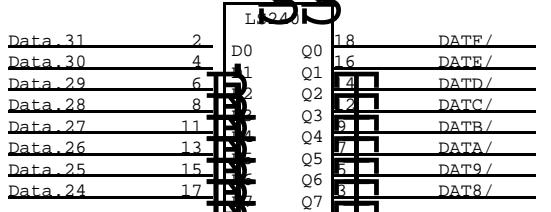
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- 3: Gates32
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- 6: Dicentra.lb6
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- A: Dicentra.Analyze
- Y: 712

All files are kept on [Indigo]<Dragon>

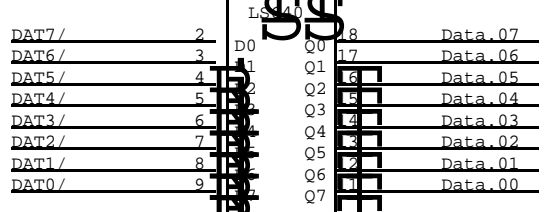
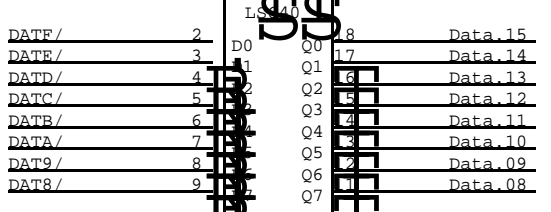
XEROX PARC	Project Dragon	Reference Title Page	File CRTest-Rev-A.sil	Designer Jim Gasbarro	Rev A	Date 7/26/85	Page 00
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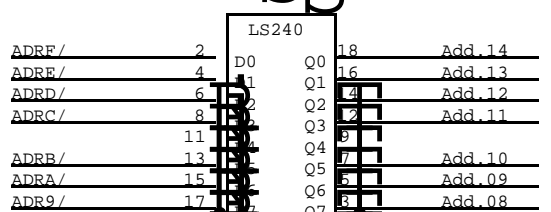
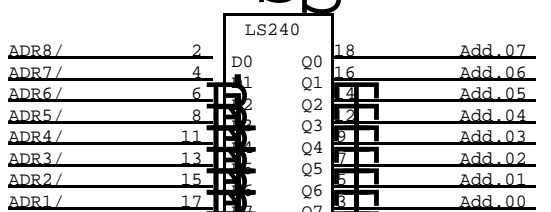
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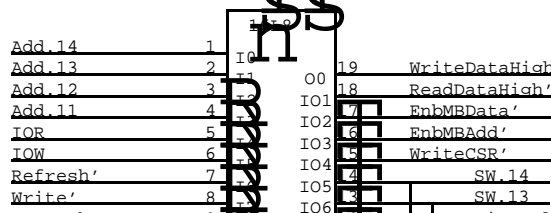
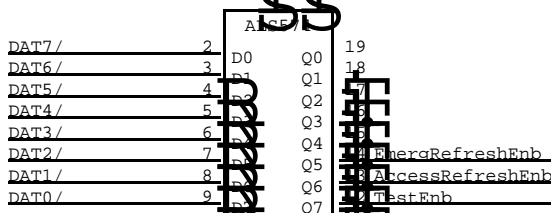
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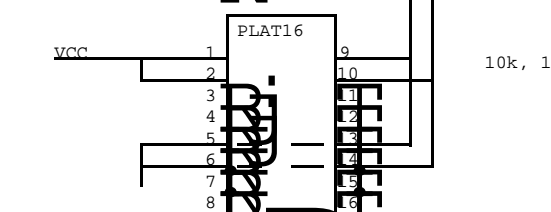
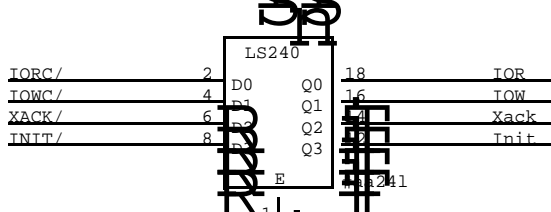
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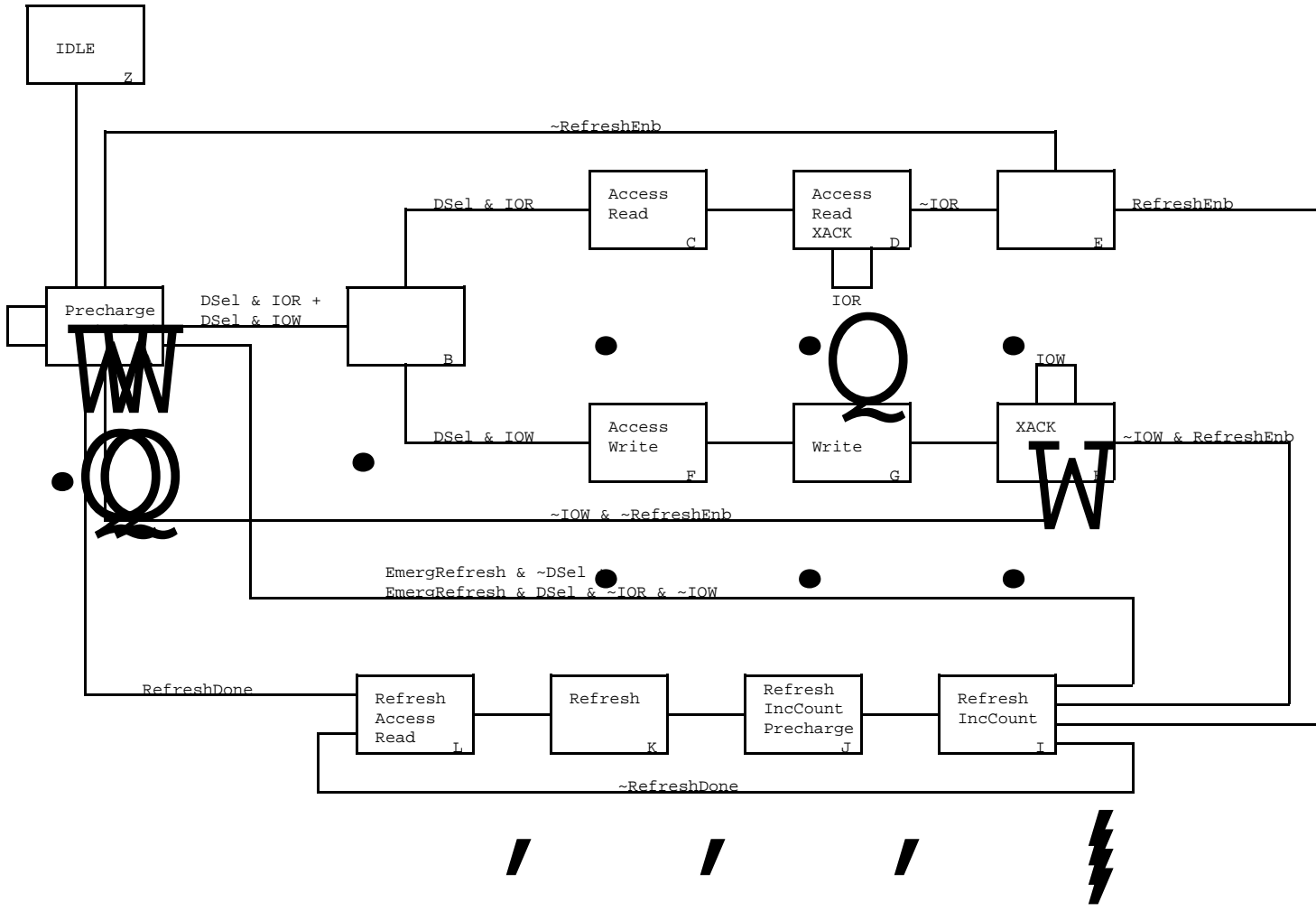
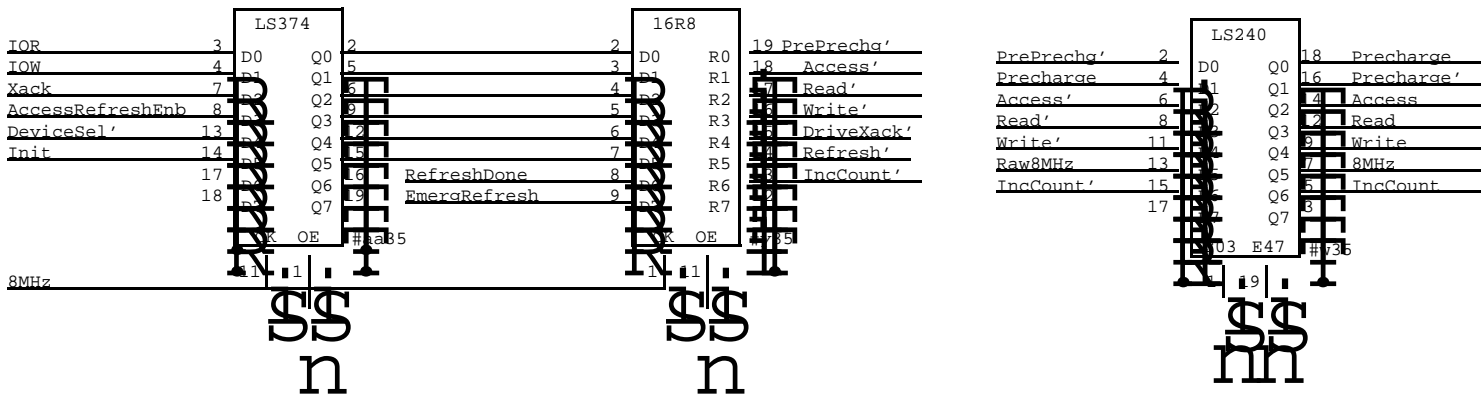
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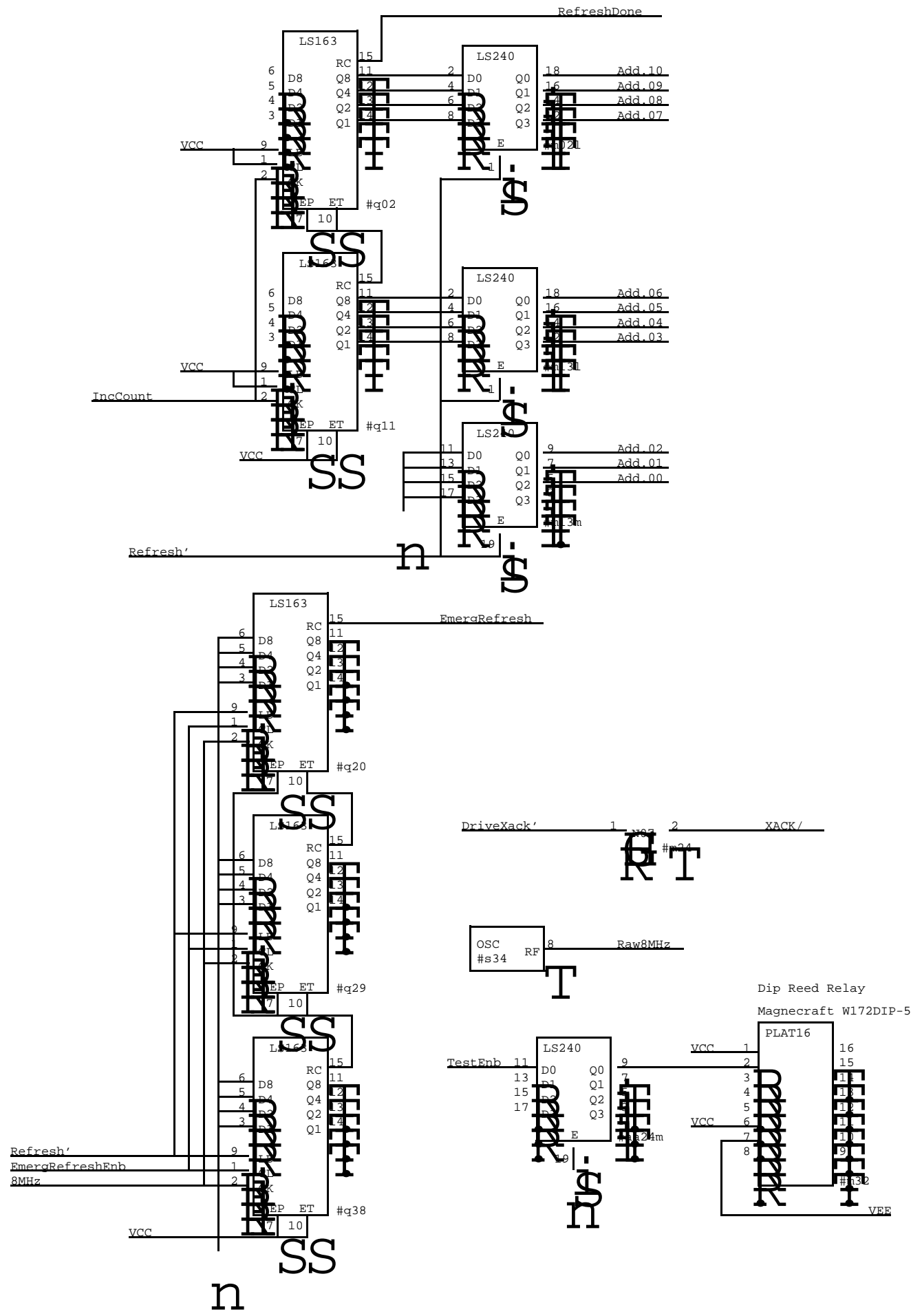


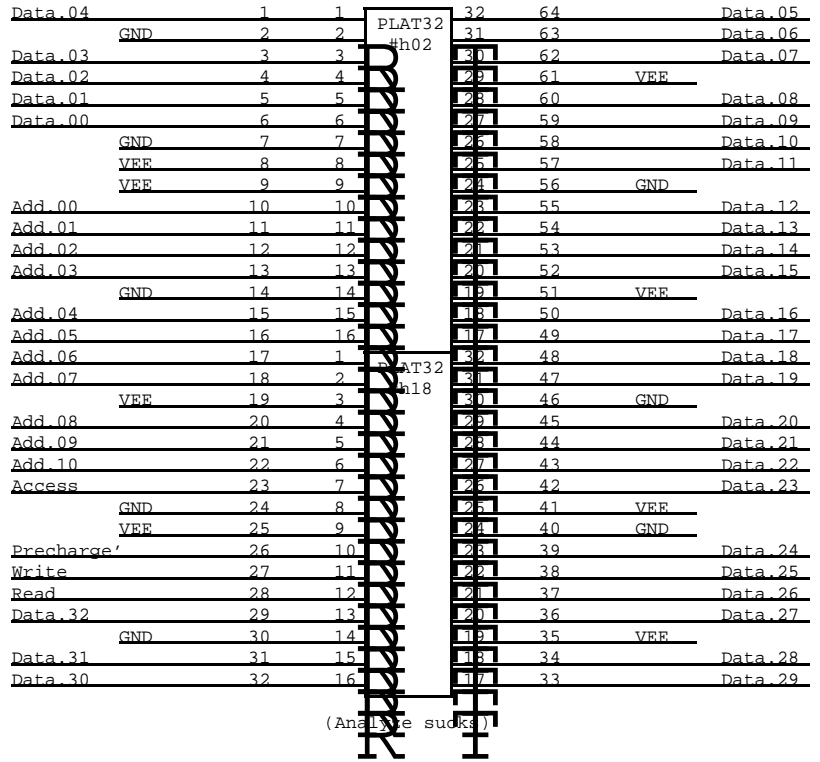
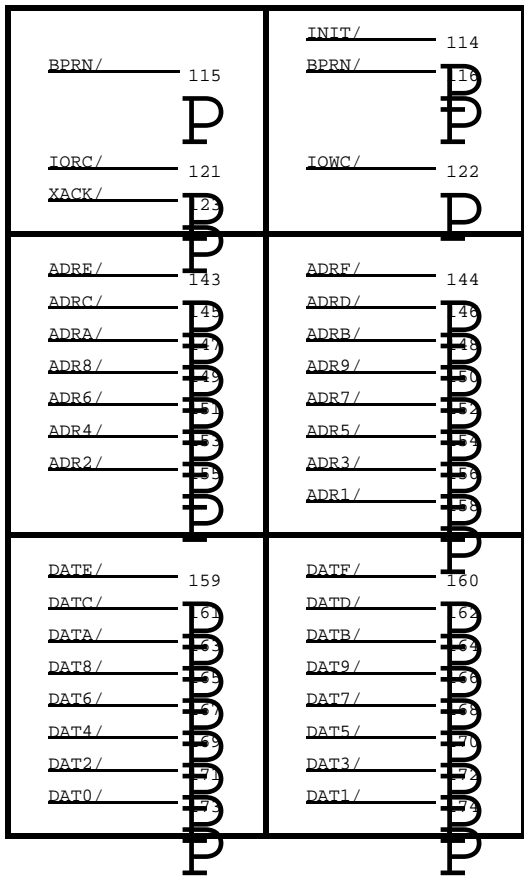
WriteCSR'



10k, 1/4 watt

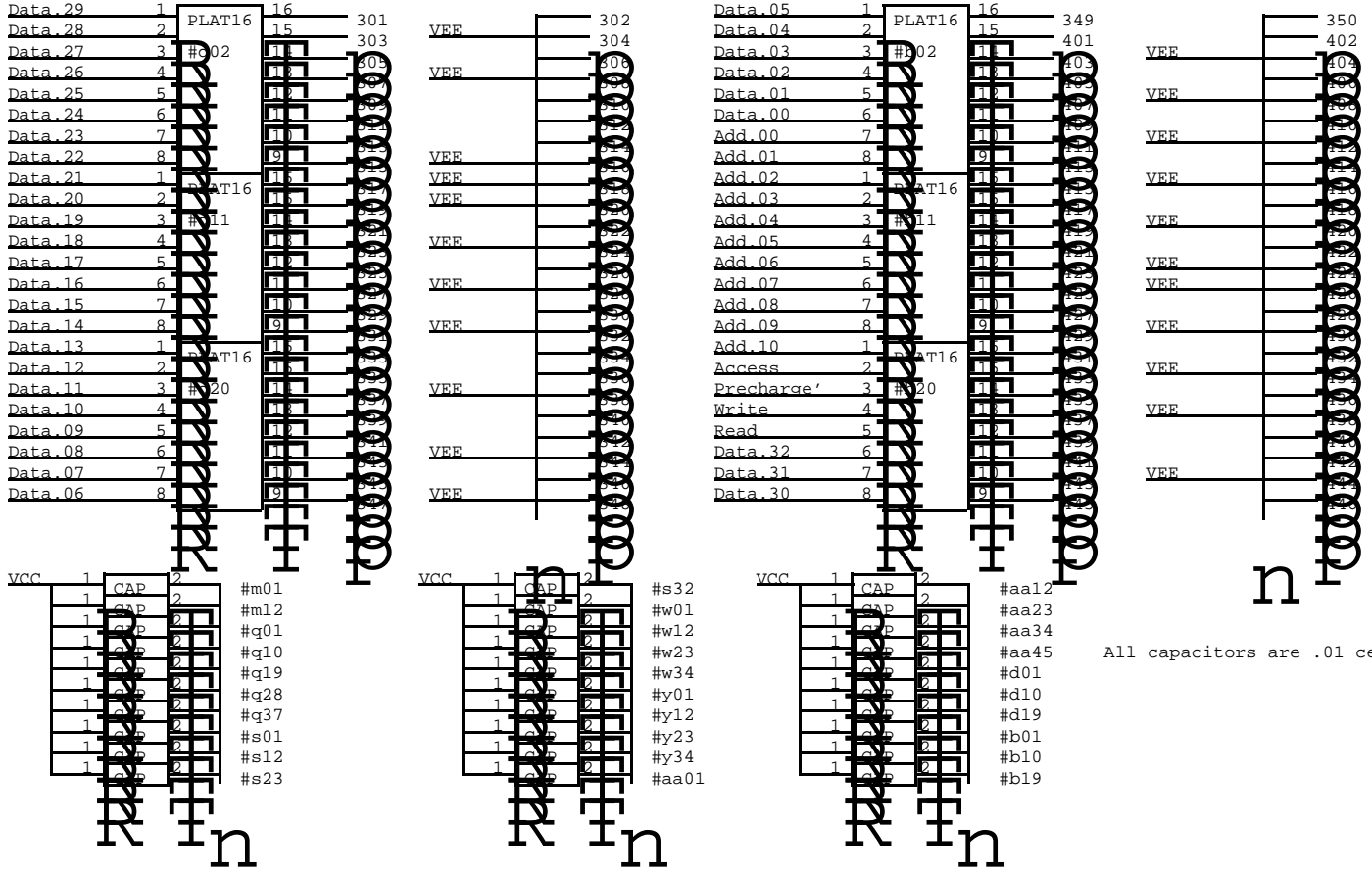




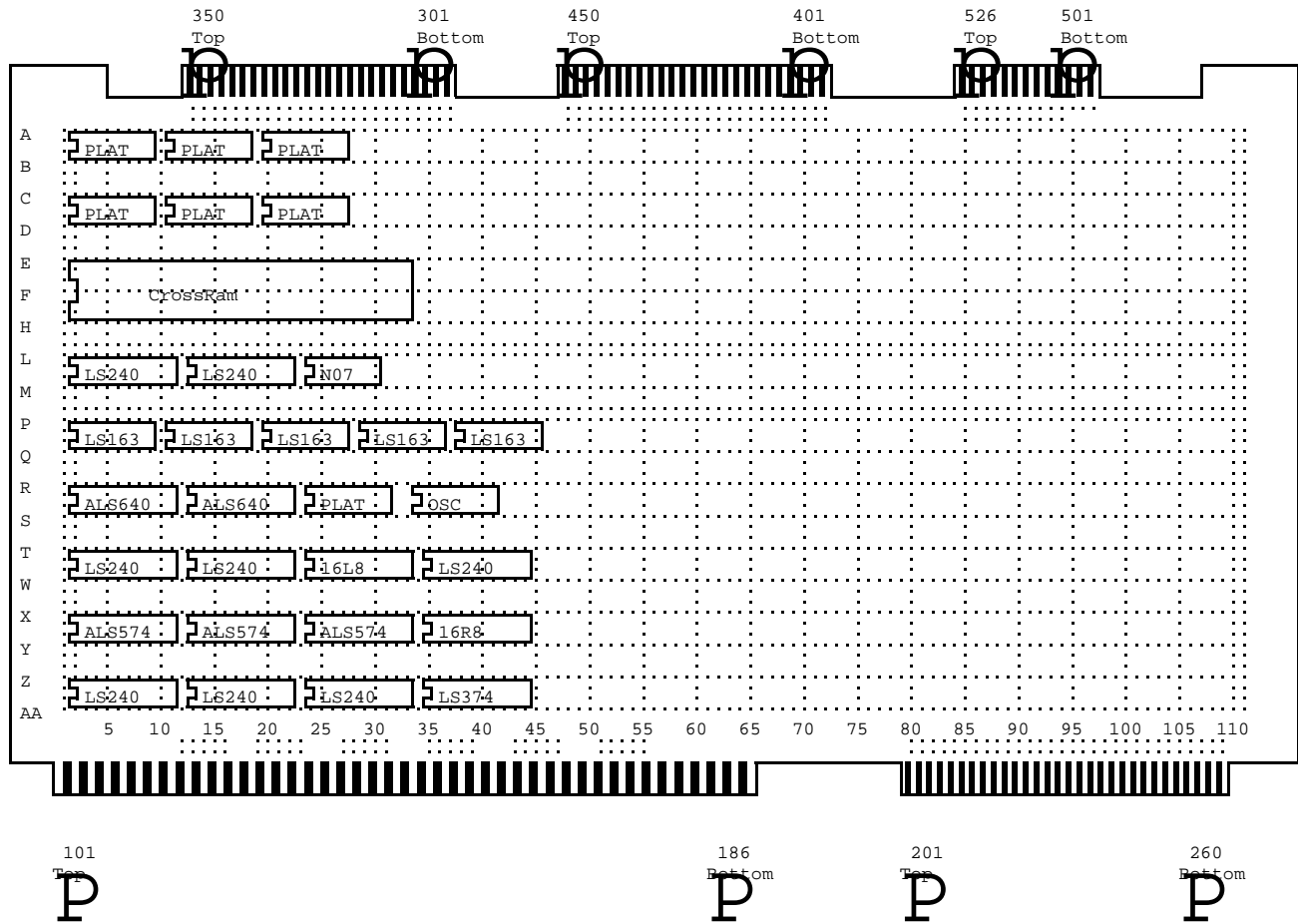


(Analogue sucks)

Termination resistors should be around 30 to 50 ohms.
(To be experimentally determined)



All capacitors are .01 ceramic



Multibus Address	15	14	13	12	_____	01			
Chip Address	14	13	12	11	_____	00	IOW	IOR	Ram access
	S	S	1	_____	X _____	1	Write Data High		NO
	S	S	1	_____	X _____	0	WriteCSR		NO
	S	S	0	1 _____	Address _____			Read Data High	YES
	S	S	0	0 _____	Address _____			Read Data Low	YES
	S	S	0	X / _____	Address _____		Write Data Low		YES

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Cable 0

Signal Name	Probe Pin#	Connector Pin#	Cable Wire#	Signal Name	Probe Pin#	Connector Pin#	Cable Wire#
		A1		25		A33	61
		B1		26		B33	62
		A2				A34	63
		B2		27		B34	64
1		A3	1			A35	65
2		B3	2			B35	66
		A4	3	28		A36	67
3		B4	4			B36	68
		A5	5			A37	69
		B5	6	29		B37	70
4		A6	7	30		A38	71
		B6	8			B38	72
		A7	9	31		A39	73
5		B7	10	32		B39	74
6		A8	11			A40	75
		B8	12	33		B40	76
7		A9	13	34		A41	77
8		B9	14			B41	78
		A10	15	35		A42	79
9		B10	16			B42	80
10		A11	17			A43	81
		B11	18	36		B43	82
11		A12	19			A44	83
		B12	20			B44	84
		A13	21			A45	85
12		B13	22			B45	86
		A14	23			A46	87
		B14	24			B46	88
		A15	25			A47	89
		B15	26			B47	90
		A16	27			A48	91
		B16	28			B48	92
		A17	29			A49	93
		B17	30			B49	94
		A18	31			A50	95
		B18	32			B50	96
		A19	33	37		A51	97
		B19	34	38		B51	98
		A20	35			A52	99
		B20	36	39		B52	100
		A21	37	40		A53	101
		B21	38			B53	102
13		A22	39	41		A54	103
14		B22	40	42		B54	104
		A23	41			A55	105
		B23	42	43		B55	106
15		A24	43			A56	107
16		B24	44			B56	108
		A25	45	44		A57	109
17		B25	46			B57	110
18		A26	47			A58	111
		B26	48	45		B58	112
19		A27	49	46		A59	113
20		B27	50			B59	114
21		A28	51	47		A60	115
22		B28	52	48		B60	116
		A29	53			A61	117
		B29	54	49		B61	118
		A30	55	50		A62	119
		B30	56			B62	120
		A31	57			A63	
23		B31	58			B63	
24		A32	59			A64	
		B32	60			B64	

VCC and GND should be bussed and bypassed on each end of probe card.

Cable 1

Signal Name	Probe Pin#	Connector Pin#	Cable Wire#	Signal Name	Probe Pin#	Connector Pin#	Cable Wire#
		A1		23		A33	181
		B1		24		B33	182
		A2				A34	183
		B2		25		B34	184
1		A3	121			A35	185
		B3	122			B35	186
		A4	123	26		A36	187
2		B4	124			B36	188
		A5	125			A37	189
		B5	126	27		B37	190
		A6	127			A38	191
3		B6	128	28		B38	192
4		A7	129			A39	193
		B7	130	29		B39	194
5		A8	131			A40	195
6		B8	132	31		B40	196
		A9	133			A41	197
7		B9	134	32		B41	198
8		A10	135			A42	199
		B10	136	33		B42	200
		A11	137			A43	201
10		B11	138			B43	202
		A12	139			A44	203
		B12	140			B44	204
		A13	141			A45	205
		B13	142			B45	206
		A14	143			A46	207
		B14	144			B46	208
		A15	145			A47	209
		B15	146			B47	210
		A16	147			A48	211
		B16	148			B48	212
		A17	149			A49	213
		B17	150			B49	214
		A18	151			A50	215
		B18	152			B50	216
		A19	153	34		A51	217
		B19	154			B51	218
		A20	155			A52	219
		B20	156	35		B52	220
		A21	157			A53	221
		B21	158	36		B53	222
		A22	159			A54	223
11		B22	160	37		B54	224
12		A23	161			A55	225
		B23	162	39		B55	226
13		A24	163			A56	227
14		B24	164	40		B56	228
		A25	165			A57	229
15		B25	166	41		B57	230
		A26	167			A58	231
16		B26	168			B58	232
17		A27	169	42		A59	233
		B27	170			B59	234
		A28	171			A60	235
18		B28	172	43		B60	236
		A29	173			A61	237
		B29	174	44		B61	238
19		A30	175			A62	239
20		B30	176	46		B62	240
		A31	177			A63	
21		B31	178	47		B63	
22		A32	179			A64	
		B32	180	50		B64	

VCC and GND should be bussed and bypassed on each end of probe card.