Cycle	Phase	
0	A	requestor: MnRq _ FALSE;
	B	
1	A	arbiter: MnGnt _ FALSE;
	B	
2	A	master: {MnRq _ TRUE; MCmd _ WriteSingle; MAddr _ WSAddress; MnAdCycle _ FALSE}
	B	
3	A	master: {MData _ WSData; MnAdCycle _ TRUE}; arbiter: MnGnt _ TRUE;
	B	
4	A	master: MParity _ WSDataParity; slave: match => MnShared _ FALSE;
	B	
5	A	slave: match => MnShared _ TRUE;
	B	

Figure 5. Timing for WriteSingle