Cycle	Phase	
0	A	requestor: MnRq _ FALSE;
	B	
1	A	arbiter: MnGnt _ FALSE;
	B	
2	A	master: {MCmd _ WriteQuad; MAddr _ WQAddress; MnAdCycle _ FALSE}
	B	
3	A	master: {MData _ WQData0; MnAdCycle _ TRUE}
	B	
4	A	master: {MData _ WQData1; MParity _ WQData0Parity} w=0 => memory: MnDV _ FALSE;
	B	
5	A	master: {MData _ WQData2; MParity _ WQData1Parity; w=0 => MnRq _ TRUE} w=0 => memory: MnDV _ TRUE; w=1 => memory: MnDV _ FALSE;
	B	
6	A	master: {MData _ WQData3; MParity _ WQData2Parity; w=1 => MnRQ _ TRUE} w=0 => arbiter: MnGnt _ TRUE; w=1 => memory: MnDV _ TRUE; w=2 => memory: MnDV _ FALSE;
	B	
7	A	master: {MParity _ WQData3Parity; w=2 => MnRq _ TRUE}; waitCycle _ 1; w=1 => arbiter: MnGnt _ TRUE; w=2 => memory: MnDV _ TRUE; w=3 => memory: MnDV _ FALSE;
	B	
w-1 cycles (w>0)	A	waitCycle _ waitCycle + 1; waitCycle=w-3 => {master: MnRq _ TRUE; memory: MnDV _ TRUE} waitCycle=w-2 => arbiter: MnGnt _ TRUE; waitCycle=w-4 => memory: MnDV _ FALSE;
	B	

Figure 4. Timing for WriteQuad