Cycle	Phase	
0	A	requestor: MnRq _ FALSE;
	B	
1	A	arbiter: MnGnt _ FALSE;
	B	
2	A	master: {MCmd _ ReadQuad; MAddr _ RQAddress; MnAdCycle _ FALSE}
	B	
3	A	master: MnAdCycle _ TRUE;
	B	
4	A	any cache: {match => MnShared _ FALSE; owner => MnAbort _ FALSE}; waitCycle _ 0;
	B	
w cycles (w>=0)	A	(waitCycle _ waitCycle+1)=1 => {some cache: owner => MnAbort _ TRUE; memory: MnShared _ TRUE}
	B	
5+w	A	slave: {MData _ RQData0; MnDV _ FALSE}; w=0 => {some cache: owner => MnAbort _ TRUE; memory: MnShared _ TRUE}
	B	
6+w	A	slave: {MData _ RQData1; MParity _ RQData0Parity; MnDV _ TRUE}
	B	
7+w	A	slave: {MData _ RQData2; MParity _ RQData1Parity} master: MnRq _ TRUE;
	B	
8+w	A	slave: {MData _ RQData3; MParity _ RQData2Parity} arbiter: MnGnt _ TRUE;
	B	
9+w	A	slave: MParity _ RQData3Parity
	B	

Figure 3. Timing for ReadQuad