Cycle	Phase	
0	A	requestor: MnRq _ FALSE;
	B	
1	A	arbiter: MnGnt _ FALSE;
	B	
2	A	master: {MCmd _ IOWriteFlow; MAddr _ IOAddress; MnAdCycle _ FALSE}
	B	
3	A	master: {MnAdCycle _ TRUE; MData _ IOData}
	B	
w cycles (w>=0)	A	slave: MnAdCycle=FALSE => MCmd#Done;
	B	
4+w	A	slave: {MCmd _ Done; MAddr _ mumble; MnAdCycle _ FALSE}
	B	
5+w	A	master: {MData _ IOData; MnRq _ TRUE} slave: MnAdCycle _ TRUE;
	B	
6+w	A	arbiter: MnGnt _ TRUE;
	B	

Figure 9. Timing for IOWriteFlow