Cycle	Phase	
0	A	requestor: MnRq _ FALSE;
	B	
1	A	arbiter: MnGnt _ FALSE;
	B	
2	A	master: {MCmd _ IORead; MAddr _ IOAddress; MnAdCycle _ FALSE; MnRq _ TRUE}
	B	
3	A	master: MnAdCycle _ TRUE; slave: MData _ IOData; arbiter: MnGnt _ TRUE;
	B	

Figure 6. Timing for IORead