Cycle	Phase	
0	A	requestor: MnRq _ FALSE
	B	arbiter: latch request;
w cycles (w>=0)	A	
	B	
1+w	A	arbiter: MnGnt _ FALSE;
	B	
2+w	A	<<first transaction cycle>> <<earliest master: MnRq _ TRUE; or MnNewRq _ FALSE>>
	B	
3+w	A	<<earliest arbiter: MnGnt _ TRUE>>; MnNewRq _ TRUE;
	B	
4+w	A	<<earliest next master>>
	B	

Figure 2. Timing for Bus Arbitration