

Figure 1a: Dorado chassis

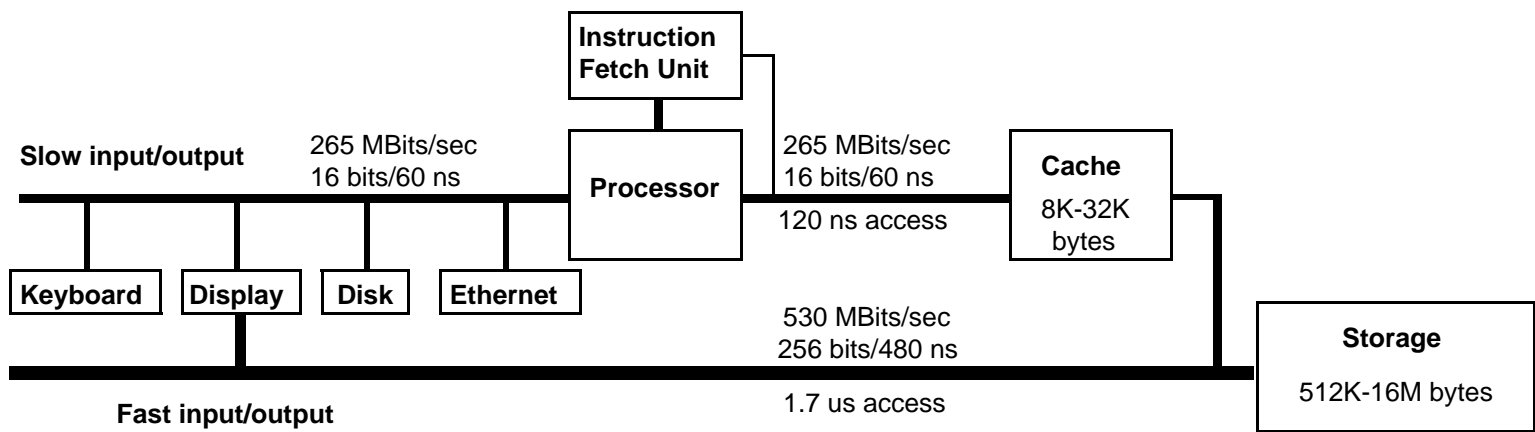


Figure 1b: Dorado block diagram

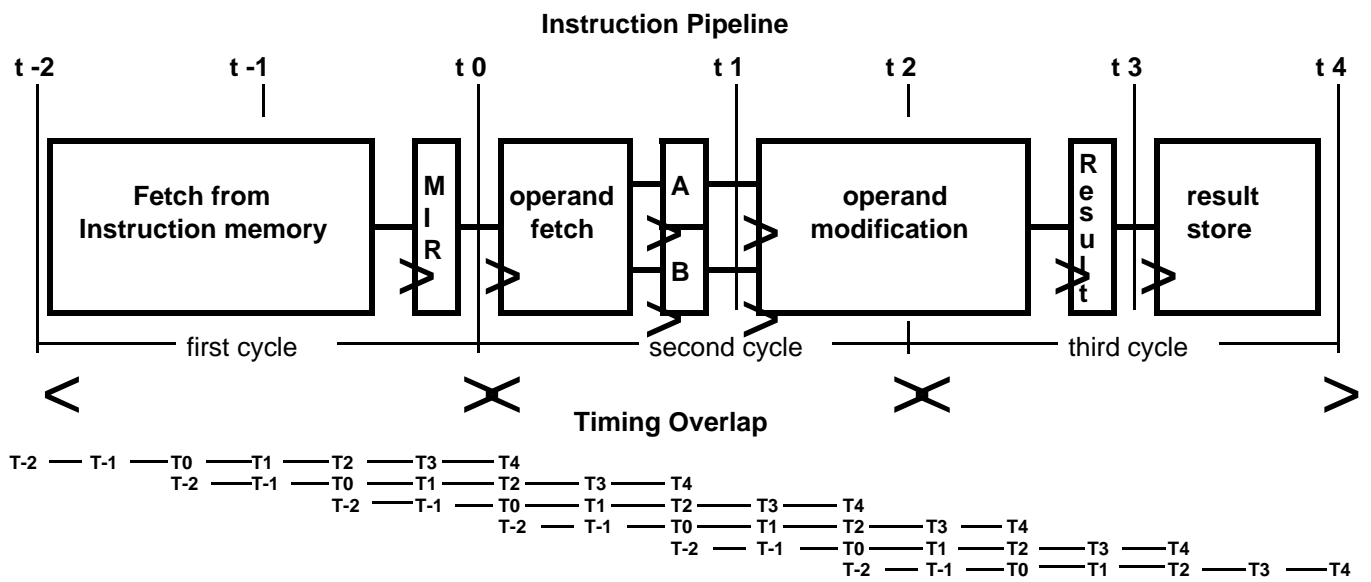


Figure 2: Instruction pipeline and timing overlap
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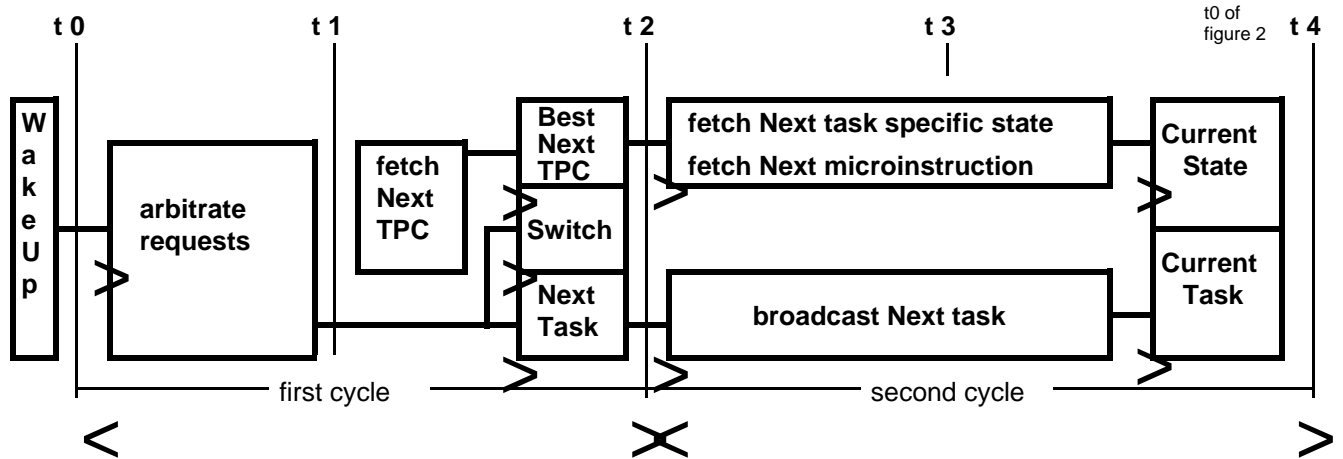


Figure 3: Task arbitration pipeline

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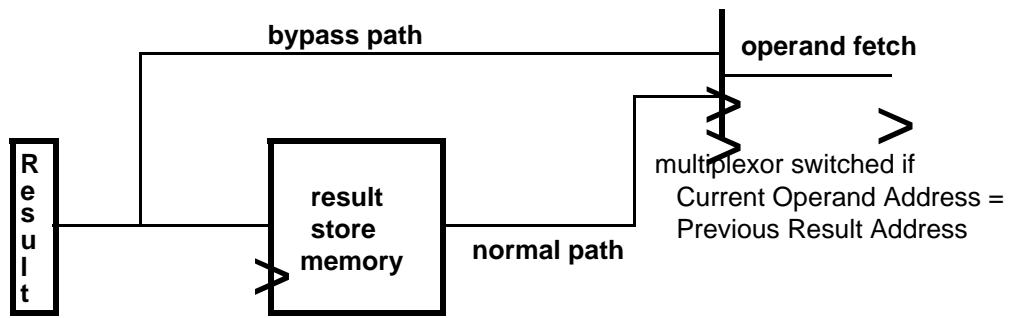


Figure 4: Bypassing example

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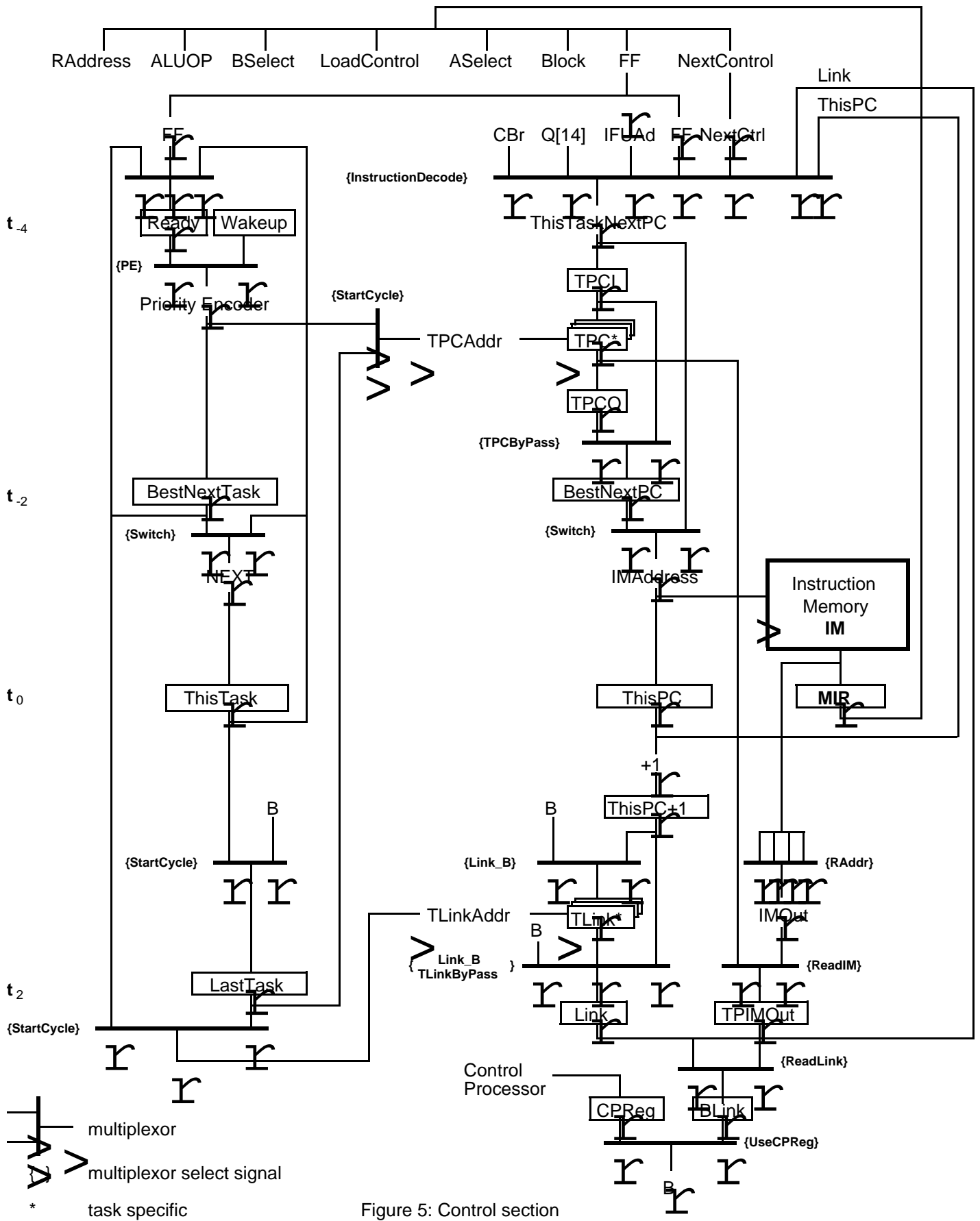
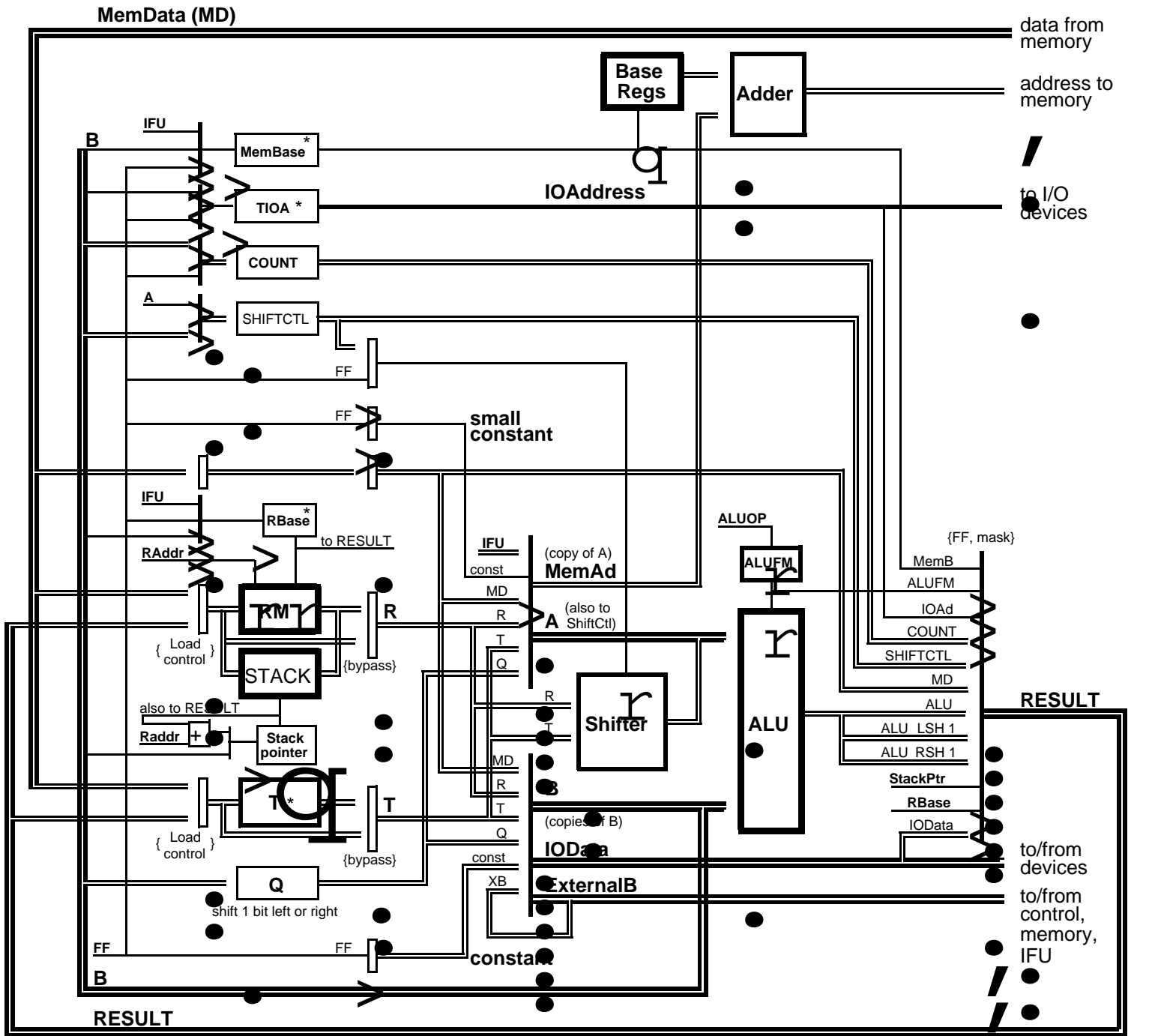


Figure 5: Control section
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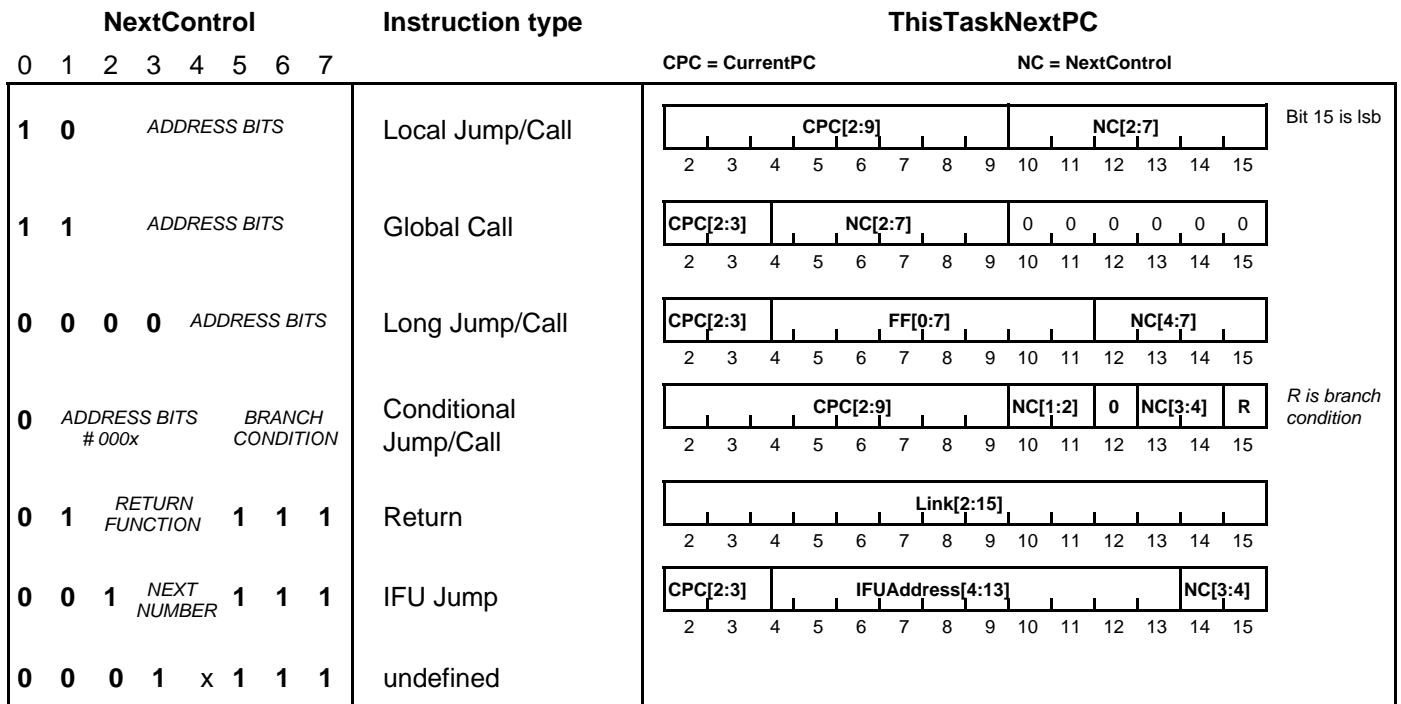


Latches follow from t2 to t3 Registers load at t3 Latches follow from t1 to t2 Data ready shortly after t1 Data ready shortly before t3

RAMs read at t1, load at t4

- register or memory
- latch
- multiplexor latch (control)
- multiplexor (control)
- main bus (A, B, RESULT, MemData, IOData)
- other 16 bit path
- narrower data path
- * task specific

Figure 6: Data section
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Conditional Branch

NC[5:7]	-or-	FF	Branch condition
0		60	ALU = 0
1		61	ALU < 0
2		62	Carry'
3		63	Count=0 (& Count_Count-1)
4		64	R < 0
5		65	R odd
6		66	IOAtten' (non-emulator)
--		67	Overflow'

A long, local or conditional branch is a CALL if, before any modification by branch conditions or dispatches, ThisTaskNextPC[12:15]=0; otherwise it is a jump.

Loaded into Link by Call, Return, or IFUJump

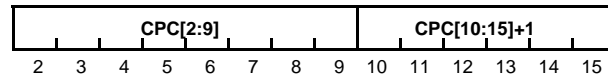


Figure 7: Next address formation

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