

Figure 1: Dorado block diagram

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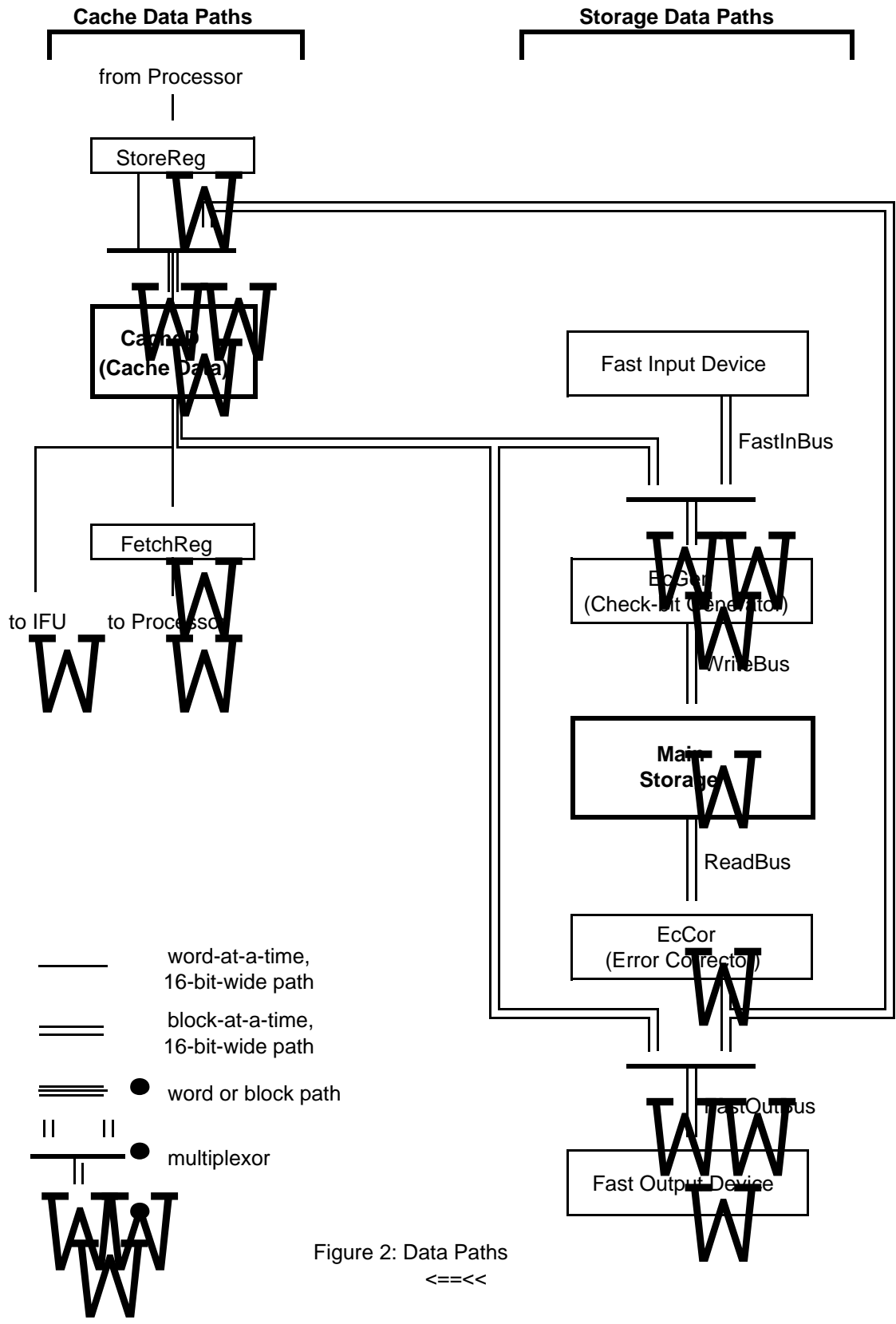


Figure 2: Data Paths
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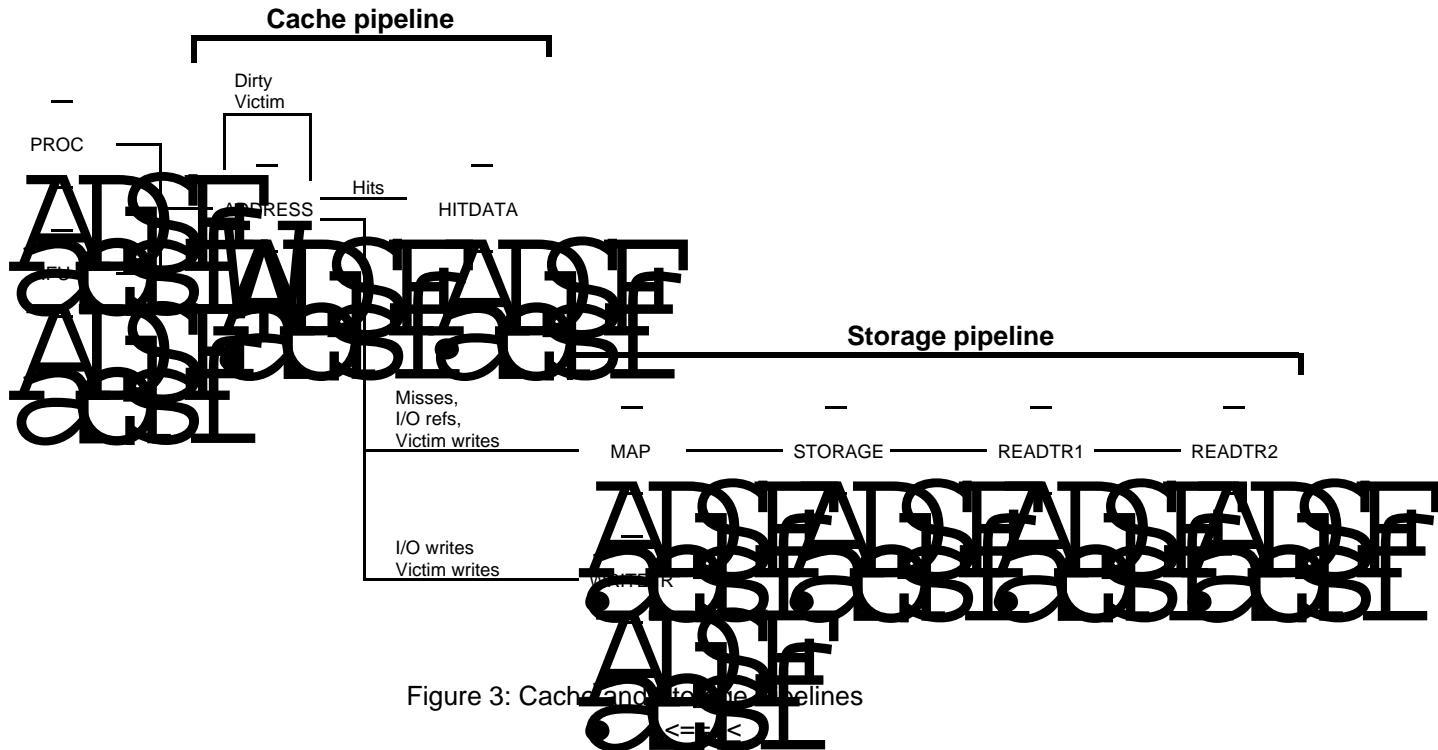
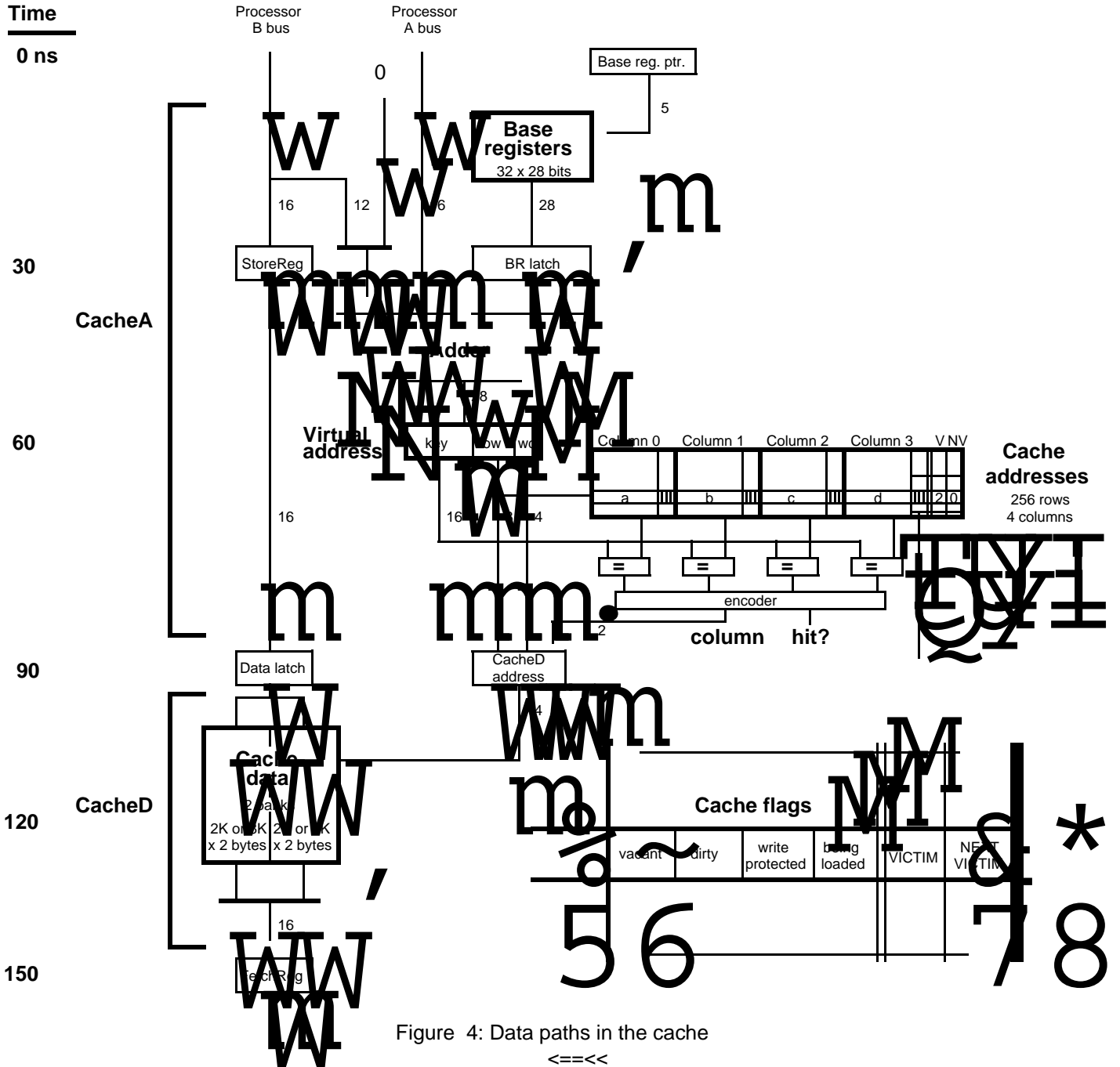
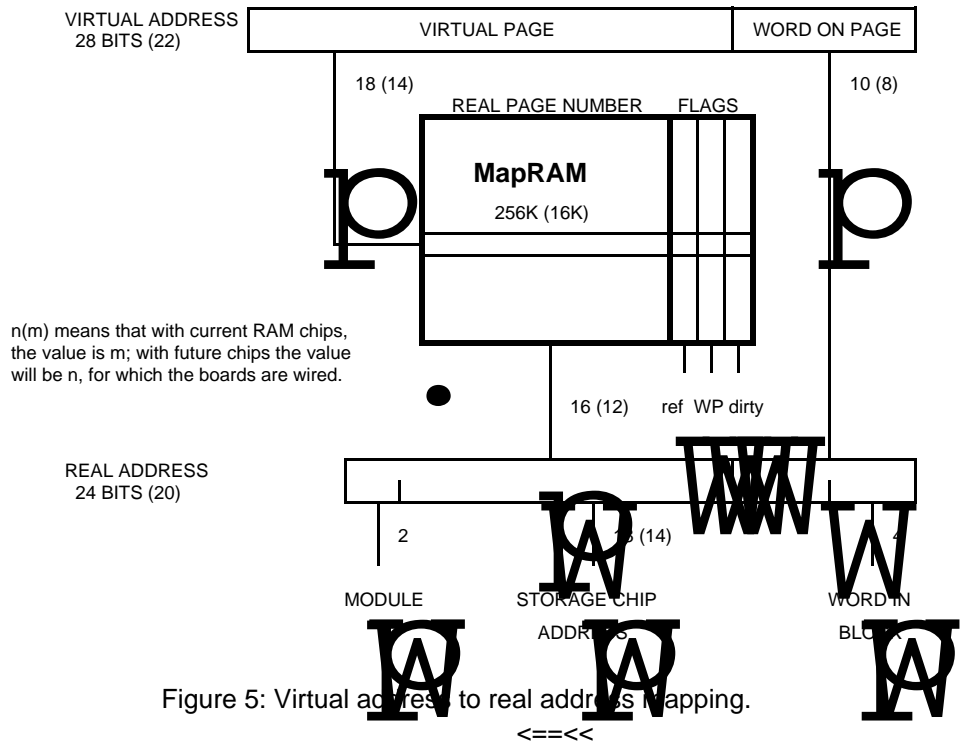


Figure 3: Cache and storage pipelines





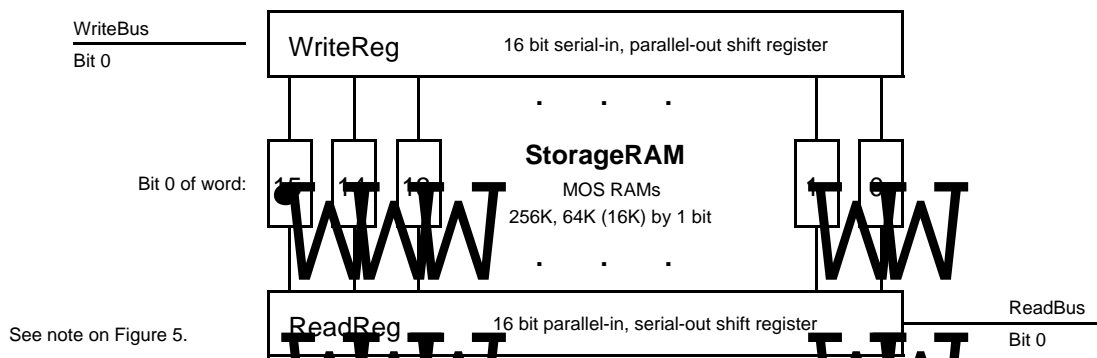


Figure 6: One bit-slice of StorageRAM and its data registers.

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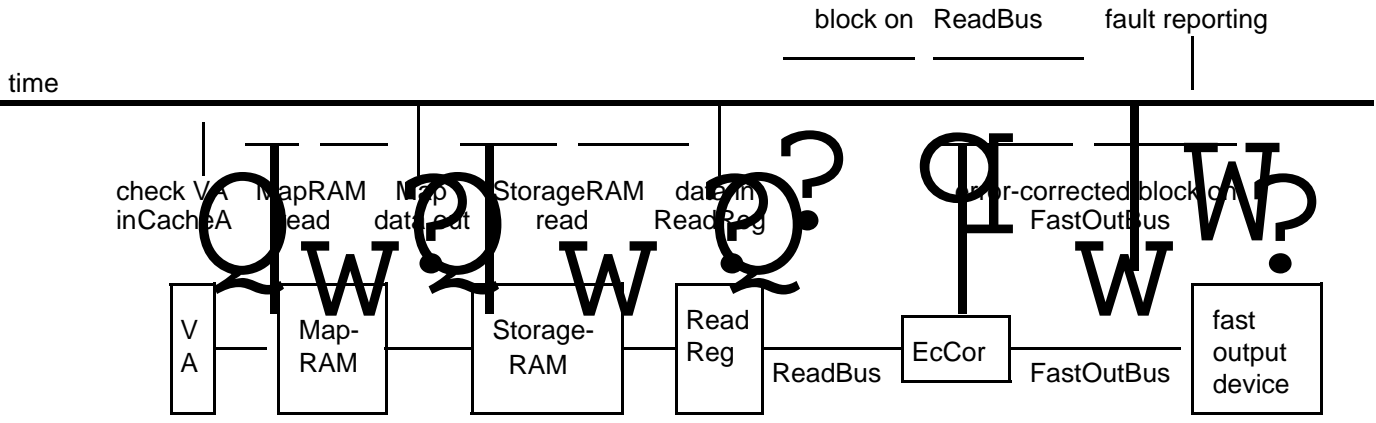
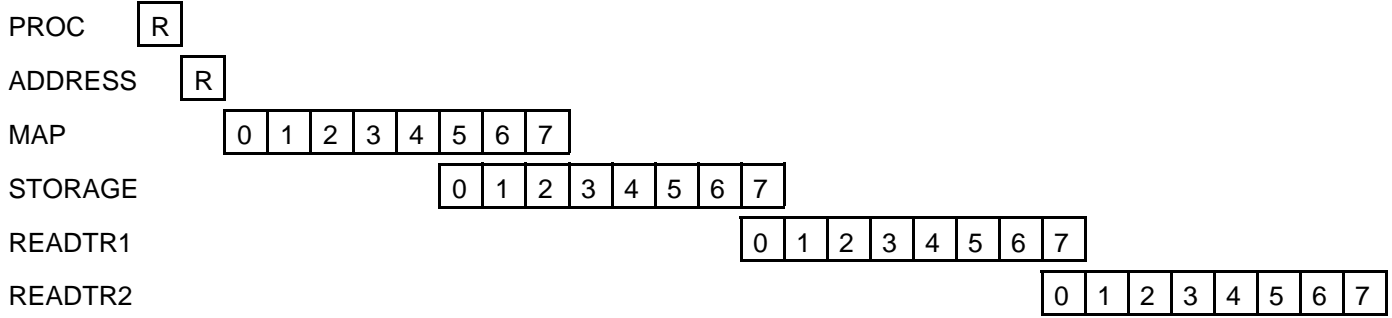


Figure 7: An I/ORead reference <====<

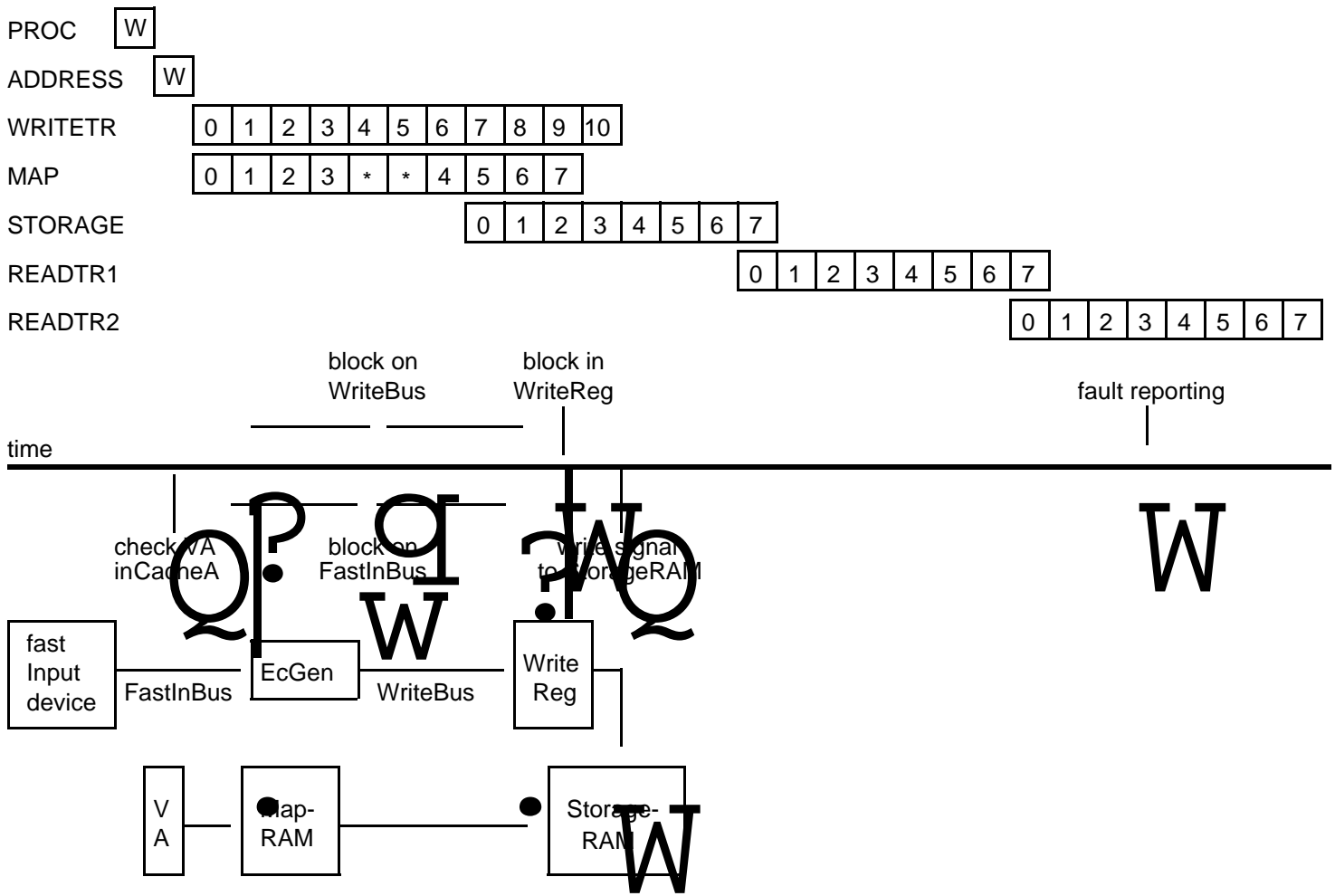


Figure 8: An I/O write reference

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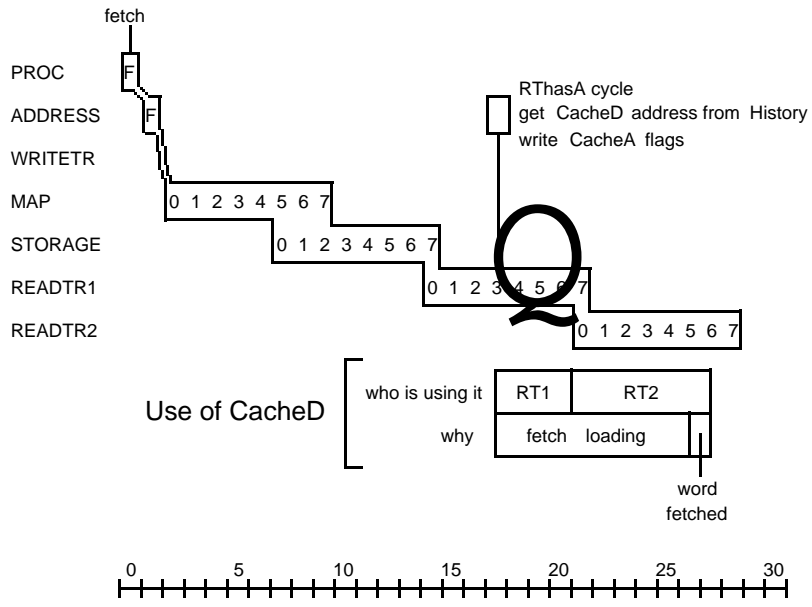


Figure 9: A clean miss

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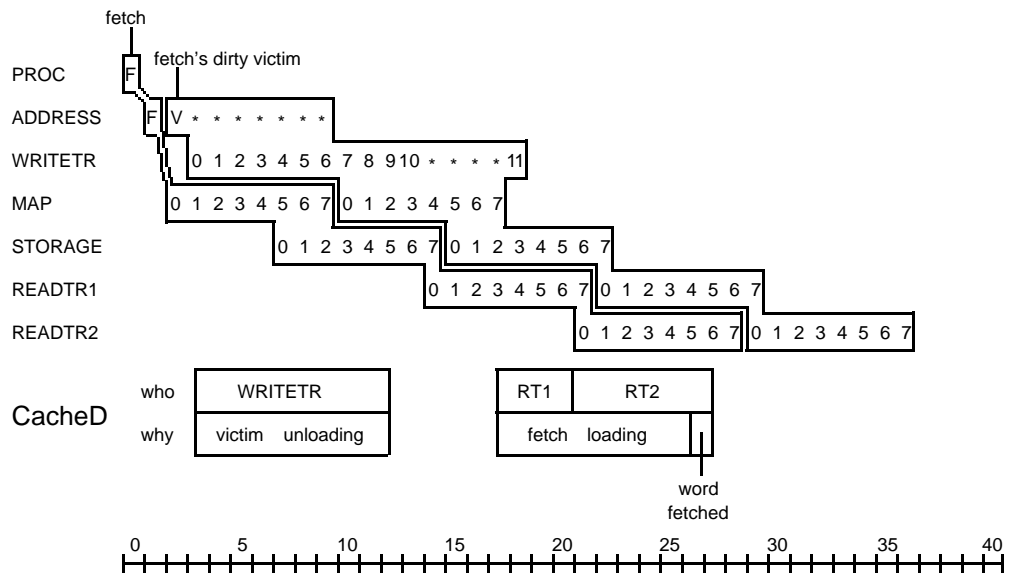


Figure 10: A dirty miss

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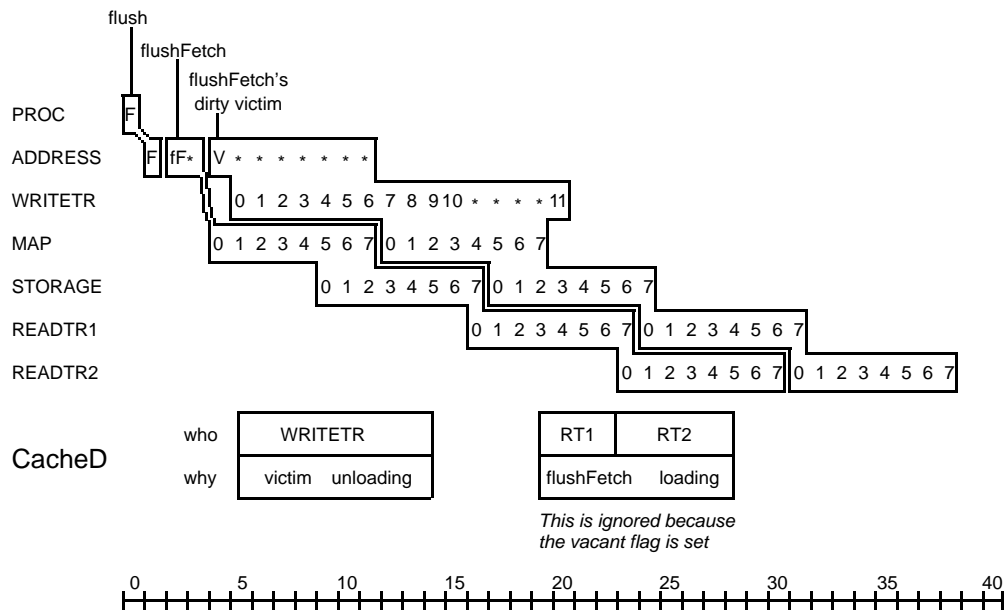


Figure 11: A dirty flush

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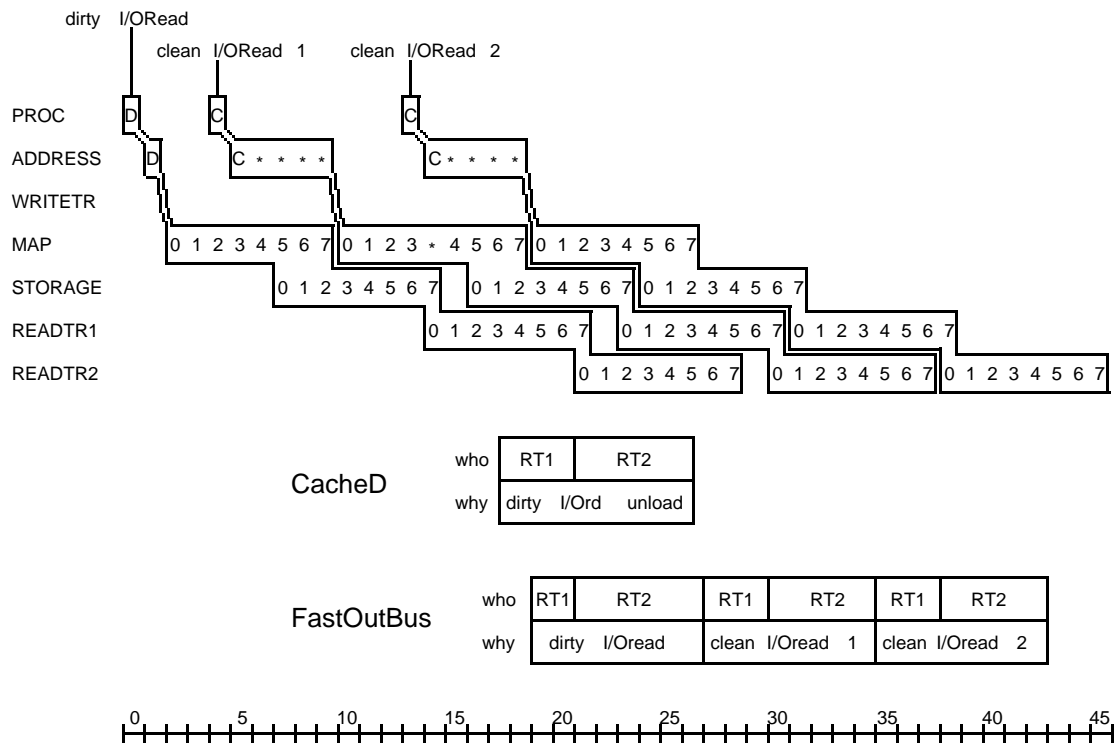


Figure 12: A dirty I/O read and two clean ones

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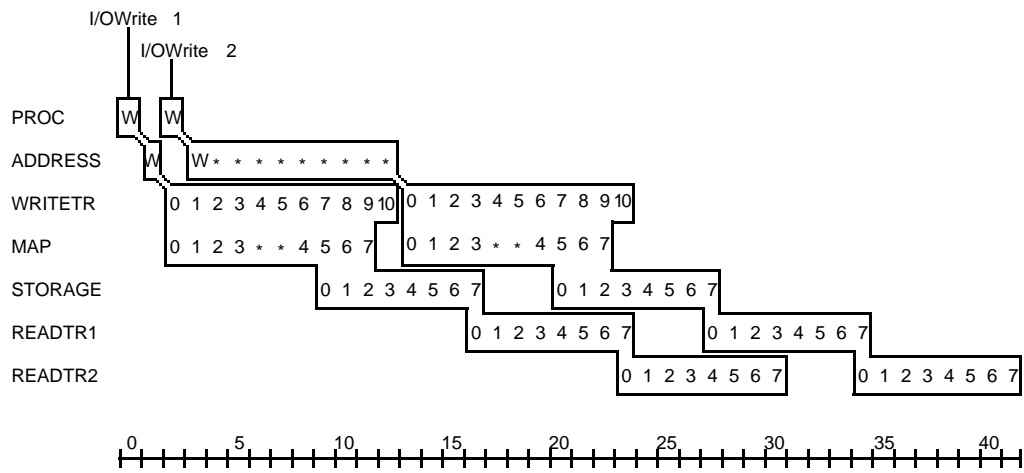


Figure 13: Two I/Owrites

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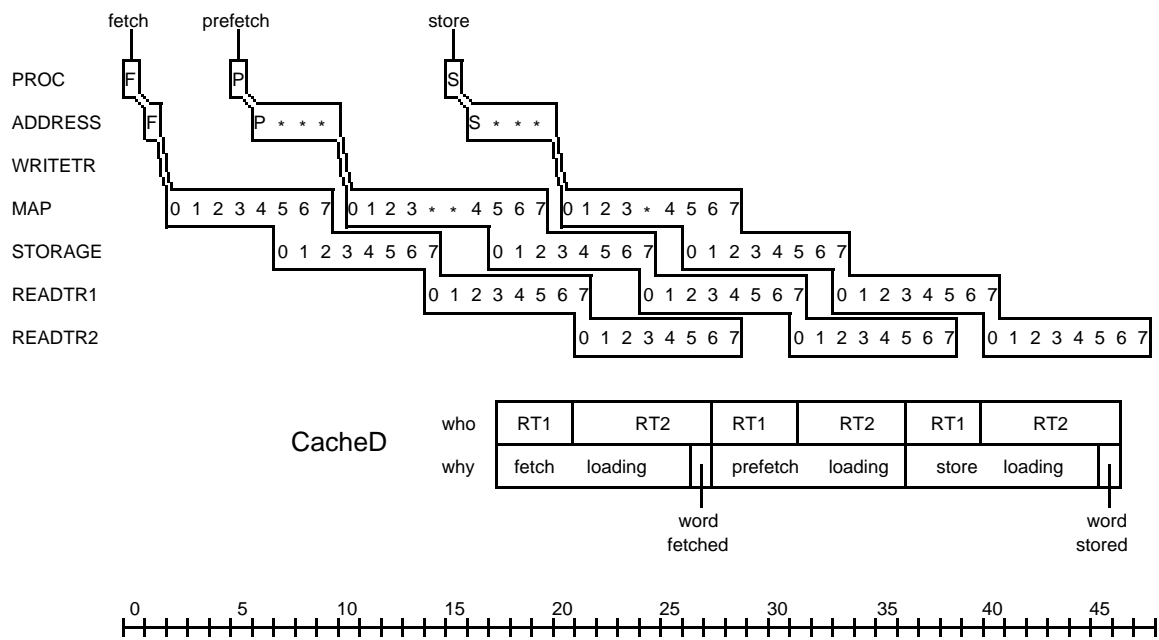


Figure 14: Cache load conflict for CacheD
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